

Subpixel Rendering

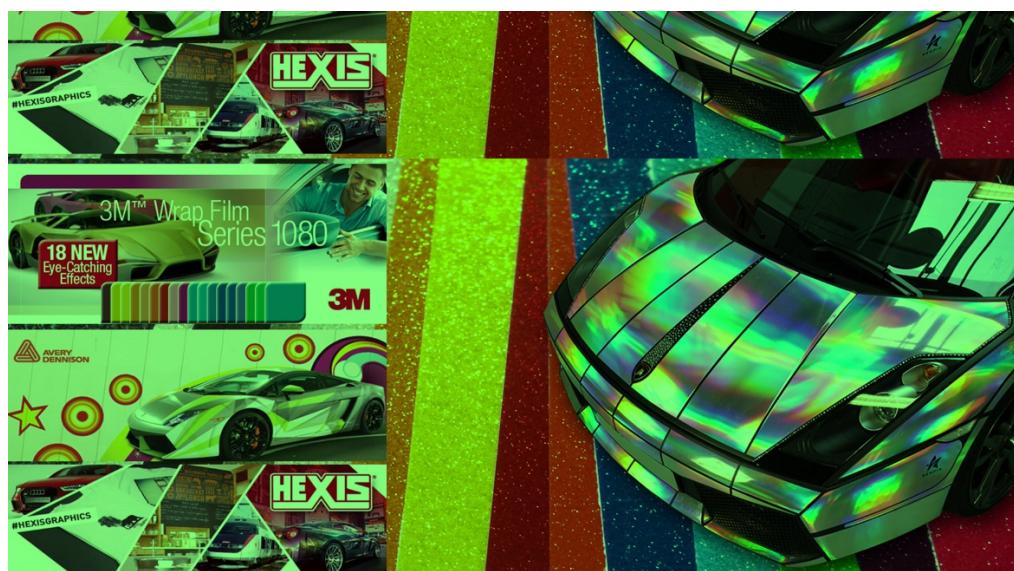
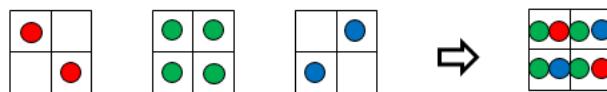
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• Chapter 1 Overview

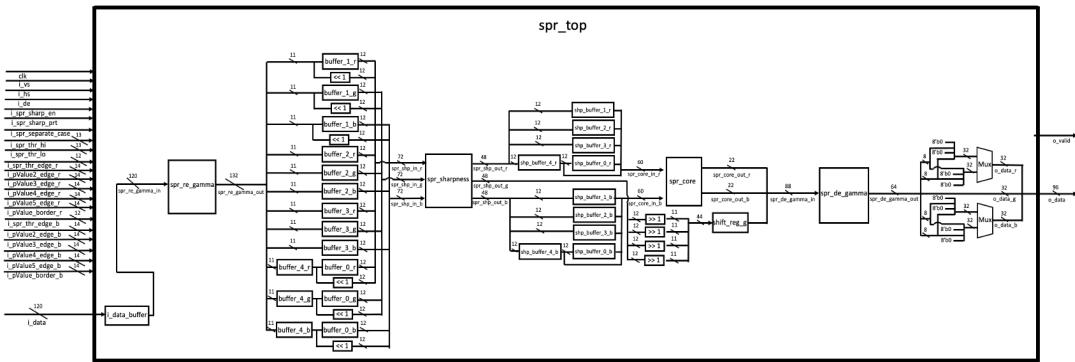
• Key feature

1. 利用人眼本身具有 Low Pass 的特性來減少 subpixels，並且使人眼不易察覺。
2. 透過減少 subpixels 使面板的設計更加容易
3. 經過 subpixel rendering 之後的資料量降低
4. 利用人眼視網膜上對綠色光敏感的 M 錐細胞比紅藍光的多的特性，減少紅藍色子像素，保留綠色子像素

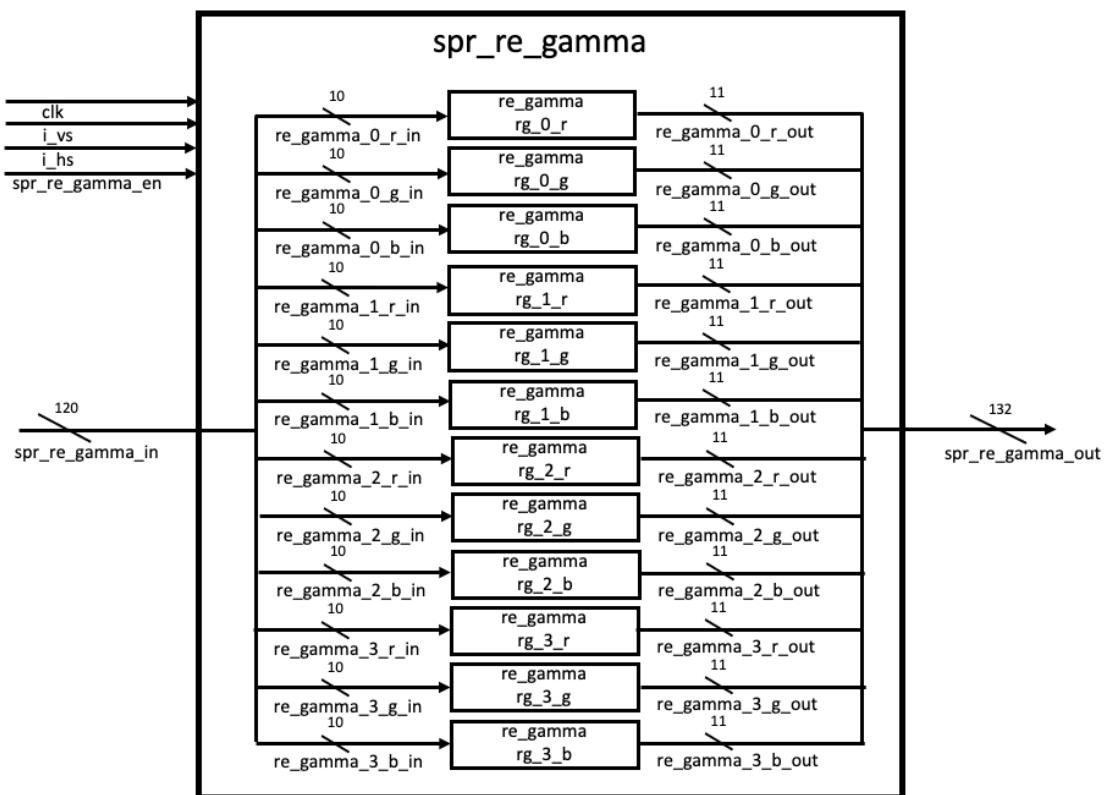


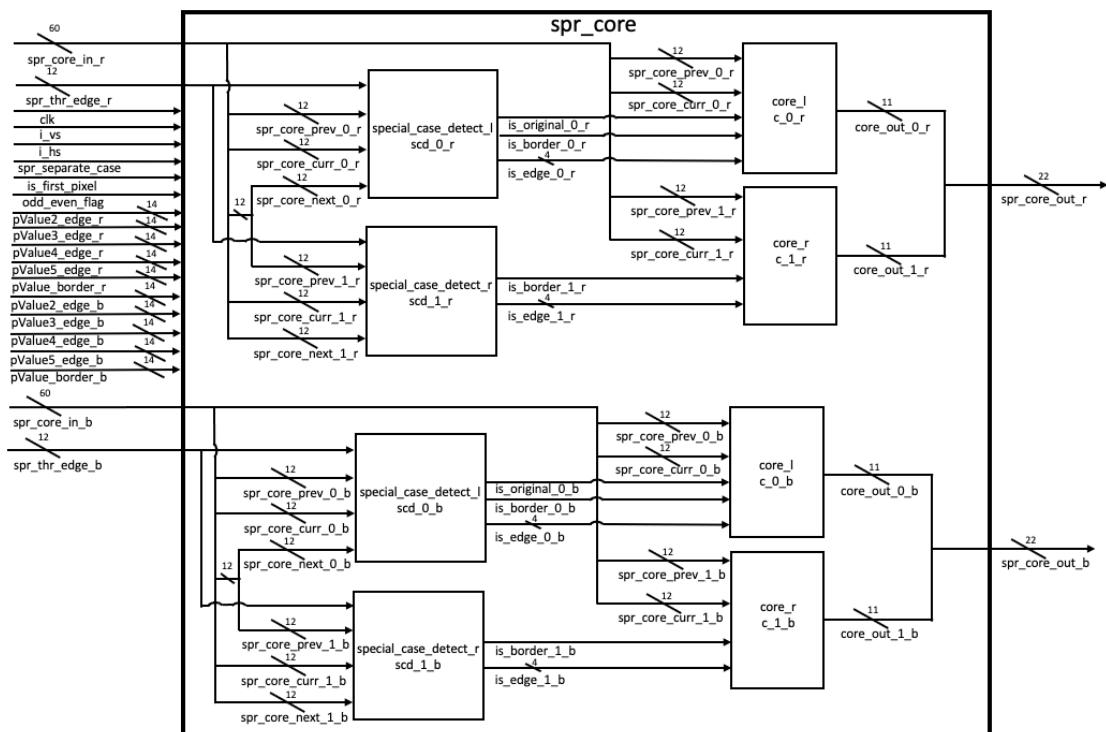
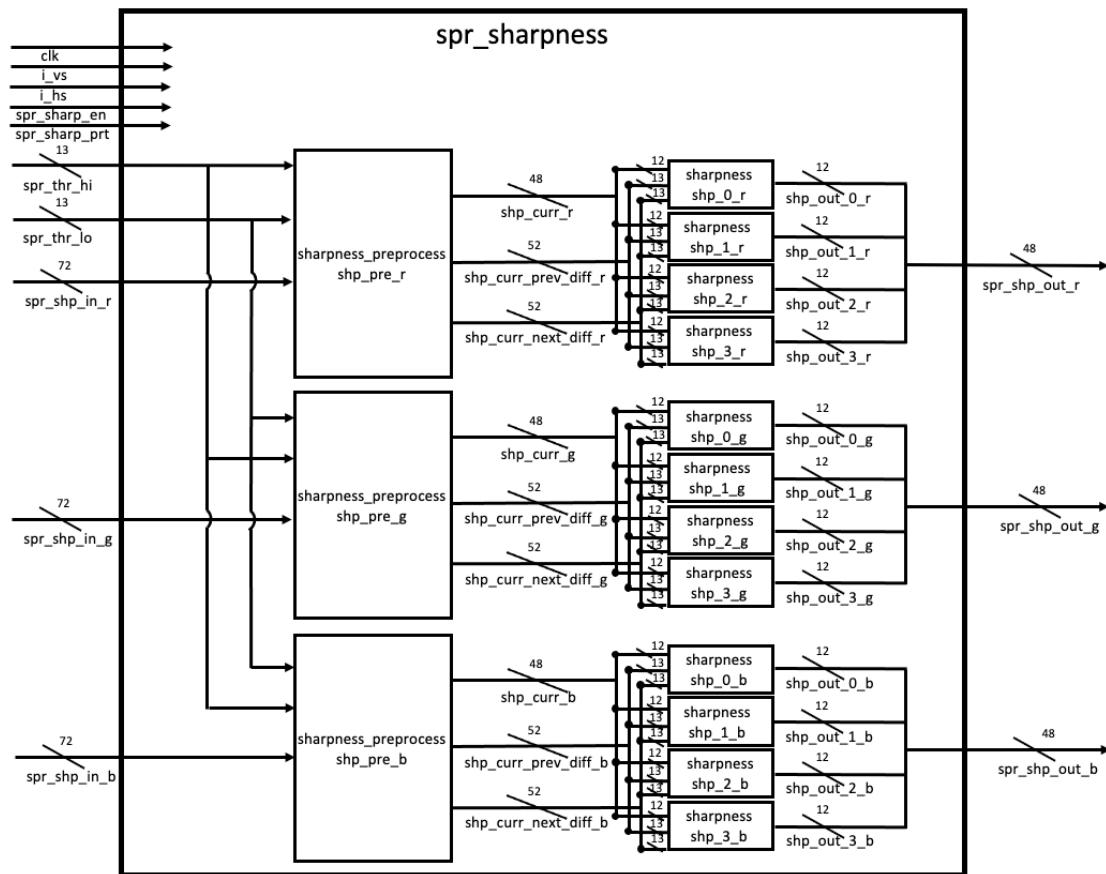
• Block diagram

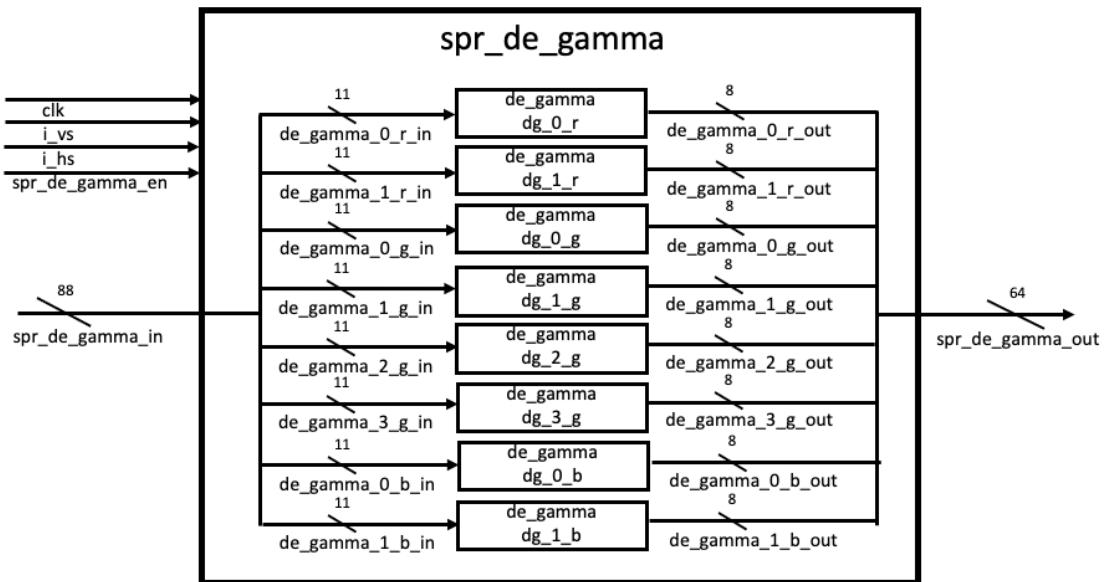
• Top module



• Sub module





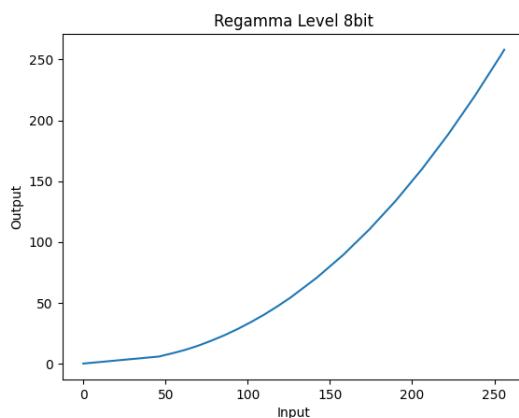


• Chapter 2 Design block

• spr_re_gamma

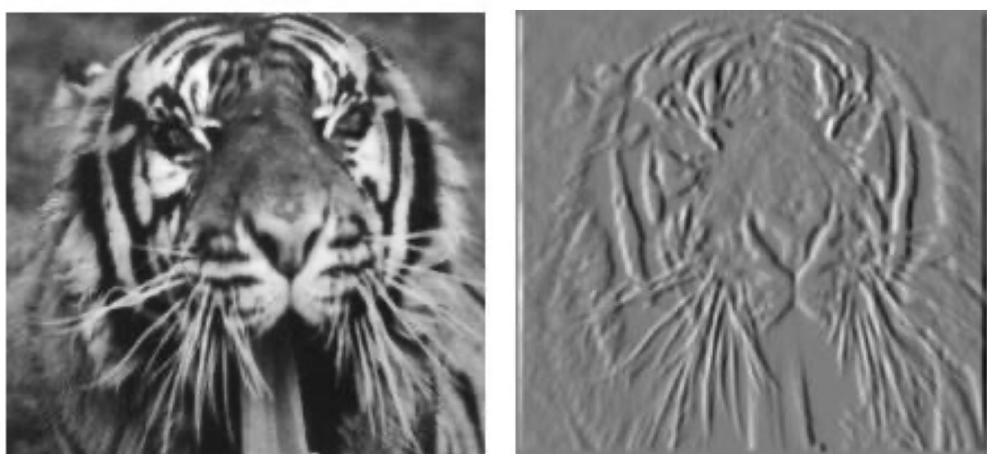
- 由於人眼感知到的亮度變化與實際物理亮度變化之間的關係是非線性的，伽馬校正可以確保在顯示器上看到的影像更接近真實世界所看到的影像。
- 設定標準顯示伽馬值為 2.2，將像素分成 32 個 Level，利用事先計算好的數值建立 LUT，對每個像素值進行伽馬校正。

```
re_gamma_x = np.array([0,4,8,12,16,20,24,28,32,36,40,44,46,50,54,62,70,78,86,94,102,110,118,126,142,158,174,190,206,222,238,254,256])  
re_gamma_y = np.array([0,4,8,12,16,20,24,28,32,36,40,44,46,57,67,90,118,151,187,228,273,322,376,434,565,714,883,1071,1280,1509,1759,2029,2065])
```



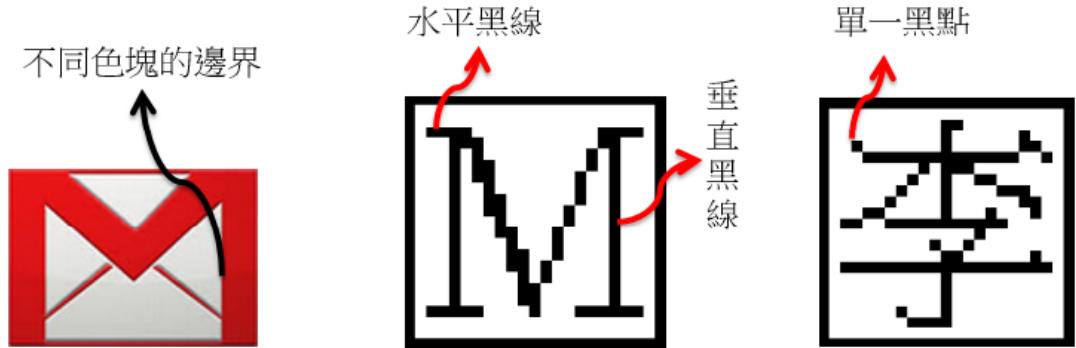
• spr_sharpness

- 偵測圖像中的高頻成分並疊加在原始圖像上，增加圖像中的對比度。



• spr_core

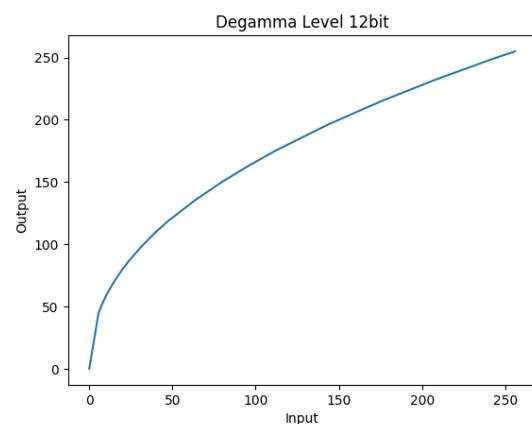
- 進行 RGBG 子像素渲染運算。
- 由於在邊緣處資料變化劇烈，容易造成模糊或色偏等現象，因此需偵測邊緣並對邊緣進行特殊處理。



- **spr_de_gamma**

- a. 設定伽馬值為 $1/2.2$ ，將像素分成 32 個 Level，利用事先計算好的數值建立 LUT，對每個像素值進行逆伽馬校正。

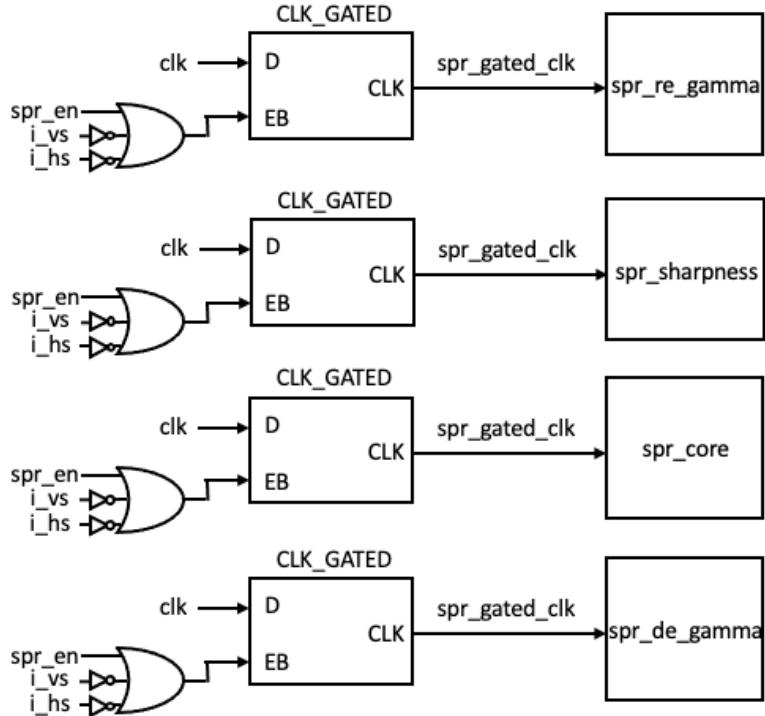
```
de_gamma_x = np.array([0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 46, 62, 78, 94, 126, 158, 190, 254, 318, 382, 510, 638, 766, 894, 1150, 1406, 1662, 1918, 1982, 2046, 2047])
de_gamma_y = np.array([0, 32, 64, 96, 128, 160, 192, 224, 256, 288, 320, 352, 364, 416, 462, 502, 574, 636, 692, 790, 876, 952, 1084, 1200, 1304, 1400, 1570, 1720, 1856, 1980, 2010, 2038, 2040])
```



• Chapter 3 Clock and reset

• Clock

- clock diagram



除了 spr_top 中的 hd_cnt, dly_cnt, odd_even_flag, i_de_r 以及 spr_core 中的 is_original_r, is_border_r, is_edge_r 之外，其餘皆使用 clock gated。

Clock Gating Summary	
Number of Clock gating elements	119
Number of Gated registers	6061 (99.07%)
Number of Ungated registers	57 (0.93%)
Total number of registers	6118

• Reset

只有 hd_cnt, dly_cnt, odd_even_flag 及 i_de_r 等與控制訊號相關的 register 有進行 reset。

• Chapter 4 interface waveform

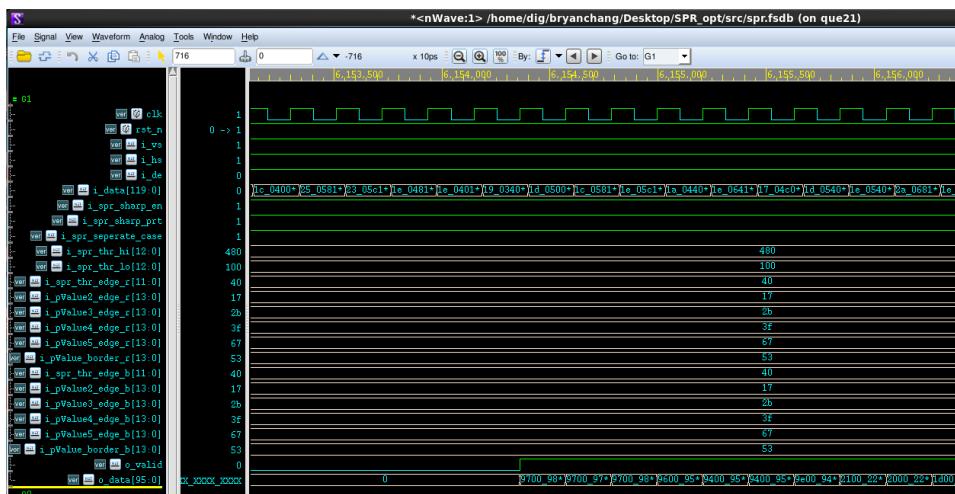
• Input:

- i_hs/i_vs: Active low, 在 rst_n 後開始運作
- i_de:
- i_spr_sharp_en/i_spr_sharp_prt/i_spr_special_case: 在 Vsync 前賦值
- i_spr_thr_hi/i_spr_thr_lo: 在 Vsync 前賦值
- i_spr_thr_edge_r/i_spr_thr_edge_b: 在 Vsync 前賦值
- i_pValue2_edge_r/i_pValue3_edge_r/i_pValue4_edge_r/i_pValue5_edge_r/i_pValue2_edge_b/i_pValue3_edge_b/i_pValue4_edge_b/i_pValue5_edge_b: 在 Vsync 前賦值
- i_pValue_border_r / i_pValue_border_b: 在 Vsync 前賦值



• Output

- o_valid: 在 i_de 後第 20T 拉起，持續 HD 個 T
- o_data: 在 i_data 後第 20T 變化



• Chapter 5 Parameter definition

name	default	Description
SHP_64	64*16	If cur_dot < SHP_64, shift_factor = (SHP_64 - cur_dot)*0 + cur_dot*0.75
SHP_128	128*16	If SHP_64 <= cur_dot < SHP_128, shift_factor = (SHP_128 - cur_dot)*0.75 + cur_dot*0.5
SHP_192	192*16	If SHP_128 <= cur_dot < SHP_192, shift_factor = (SHP_192 - cur_dot)*0.5 + cur_dot*0.25
SHP_256	256*16	If SHP_192 <= cur_dot, shift_factor = (SHP_256 - cur_dot)*0.25 + cur_dot*0.125
SPR_SHARP_amout	4*16	Default amout_r

• Chapter 6 IO Definition

name	I/O	width	Description
clk	IN	1	System clock signal
rst_n	IN	1	Active low. Asynchronous system reset signal
i_hs	IN	1	Active low. Line synchronous signal
i_vs	IN	1	Active low. Frame synchronous signal
i_de	IN	1	Input data enable signal
i_spr_sharp_en	IN	1	If i_spr_sharp_en == 0, sharpness operation is not applied. If i_spr_sharp_en == 1, sharpness operation is applied.
i_spr_sharp_prt	IN	1	If i_spr_seperate_case == 0, amout_r = amout. If i_spr_seperate_case == 1, amout_r = amout * sharp_factor.
i_spr_seperate_case	IN	1	If i_spr_sharp_prt == 0, only considers original case. If i_spr_sharp_prt == 1, also considers border and edge cases.
i_spr_thr_hi	IN	13	If abs(max - cur_dot) >= i_spr_thr_hi, amout_r = 0.
i_spr_thr_lo	IN	13	If abs(min - cur_dot) <= i_spr_thr_lo, amout_r = 0.
i_spr_thr_edge_r	IN	12	If the difference of two red adjacent dots is larger than i_spr_thr_edge_r, it is considered as an edge.
i_pValue2_edge_r	IN	14	pValue of special_case_red2_edge
i_pValue3_edge_r	IN	14	pValue of special_case_red3_edge
i_pValue4_edge_r	IN	14	pValue of special_case_red4_edge
i_pValue5_edge_r	IN	14	pValue of special_case_red5_edge
i_pValue_border_r	IN	14	pValue of red_border
i_spr_thr_edge_b	IN	12	If the difference of two blue adjacent dots is larger than i_spr_thr_edge_r, it is considered as an edge.
i_pValue2_edge_b	IN	14	pValue of special_case_blue2_edge
i_pValue3_edge_b	IN	14	pValue of special_case_blue3_edge
i_pValue4_edge_b	IN	14	pValue of special_case_blue4_edge
i_pValue5_edge_b	IN	14	pValue of special_case_blue5_edge
i_pValue_border_b	IN	14	pValue of blue_border
i_data	IN	120	RGB subpixel color values of 4 pixels. Consists of {B ₃ , G ₃ , R ₃ , B ₂ , G ₂ , R ₂ , B ₁ , G ₁ , R ₁ , B ₀ , G ₀ , R ₀ } .
o_valid	OUT	1	Indicates that the output data is valid.
o_data	OUT	96	RGB subpixel color values of 4 pixels after SPR. Consists of {B ₃ , G ₃ , R ₃ , B ₂ , G ₂ , R ₂ , B ₁ , G ₁ , R ₁ , B ₀ , G ₀ , R ₀ } .

• Chapter 7 Register Definition

name	module	width	Default value	Program rule	Description
i_data_r	spr_top	120	0	i_de = 1	Input data buffer
i_de_r	spr_top	20	0	None	Shift Register of enable signal
hd_cnt	spr_top	9	0	i_de_r[0] = 1	Line counter
dly_cnt	spr_top	5	0	(!i_de_r[0] && valid) = 1	Latency counter
odd_even_flag	spr_top	1	0	dly_cnt = 18	Flag of odd / even line
spr_sharp_en	spr_top	1	0	None	Register of i_spr_sharp_en
spr_sharp_prt	spr_top	1	0	None	Register of i_spr_sharp_prt
spr_seperate_case	spr_top	1	0	None	Register of i_spr_seperate_case
spr_thr_hi	spr_top	13	0	None	Register of i_spr_thr_hi
spr_thr_lo	spr_top	13	0	None	Register of i_spr_thr_lo
spr_thr_edge_r	spr_top	12	0	None	Register of i_spr_thr_edge_r
pValue2_edge_r	spr_top	14	0	None	Register of i_pValue2_edge_r
pValue3_edge_r	spr_top	14	0	None	Register of i_pValue3_edge_r
pValue4_edge_r	spr_top	14	0	None	Register of i_pValue4_edge_r
pValue5_edge_r	spr_top	14	0	None	Register of i_pValue5_edge_r
pValue_border_r	spr_top	14	0	None	Register of i_pValue_border_r
spr_thr_edge_b	spr_top	12	0	None	Register of i_spr_thr_edge_b
pValue2_edge_b	spr_top	14	0	None	Register of i_pValue2_edge_b
pValue3_edge_b	spr_top	14	0	None	Register of i_pValue3_edge_b
pValue4_edge_b	spr_top	14	0	None	Register of i_pValue4_edge_b
pValue5_edge_b	spr_top	14	0	None	Register of i_pValue5_edge_b
pValue_border_b	spr_top	14	0	None	Register of i_pValue_border_b
buffer_0_r	spr_top	11	0	i_de_r[4] = 1	Buffer of buffer_4_r
buffer_1_r	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[10:0]
buffer_2_r	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[43:33]
buffer_3_r	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[76:66]
buffer_4_r	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[109:99]
buffer_0_g	spr_top	11	0	i_de_r[4] = 1	Buffer of buffer_4_g
buffer_1_g	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[21:11]
buffer_2_g	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[54:44]
buffer_3_g	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[87:77]
buffer_4_g	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[120:110]

buffer_0_b	spr_top	11	0	i_de_r[4] = 1	Buffer of buffer_4_b
buffer_1_b	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[32:22]
buffer_2_b	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[65:55]
buffer_3_b	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[76:66]
buffer_4_b	spr_top	11	0	i_de_r[4] = 1	Buffer of spr_re_gamma_out[109:99]
shp_buffer_0_r	spr_top	12	0	i_de_r[12] = 1	Buffer of shp_buffer_4_r
shp_buffer_1_r	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_r[11:0]
shp_buffer_2_r	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_r[23:12]
shp_buffer_3_r	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_r[35:24]
shp_buffer_4_r	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_r[47:36]
shp_buffer_0_b	spr_top	12	0	i_de_r[12] = 1	Buffer of shp_buffer_4_b
shp_buffer_1_b	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_b[11:0]
shp_buffer_2_b	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_b[23:12]
shp_buffer_3_b	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_b[35:24]
shp_buffer_4_b	spr_top	12	0	i_de_r[12] = 1	Buffer of spr_shp_out_b[47:36]
shift_reg_g	spr_top	44*3	0	(i_de_r[0] i_de_r[19]) = 1	Shift Register of spr_shp_out_g
lobound_r	re_gamma	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of lobound in re_gamma
lobound_r_dly	re_gamma	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of lobound_r in re_gamma
re_gamma_out_r	re_gamma	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of re_gamma_out
idx_r	search_idx_10bit	5	0	(i_de_r[0] i_de_r[19]) = 1	Register of idx of re_gamma_lut
lowLevel_r	search_idx_10bit	8	0	(i_de_r[0] i_de_r[19]) = 1	Register of lowLevel of re_gamma_lut
highLevel_r	search_idx_10bit	9	0	(i_de_r[0] i_de_r[19]) = 1	Register of highLevel of re_gamma_lut
pixel_in_r	search_idx_10bit	10	0	(i_de_r[0] i_de_r[19]) = 1	Register of re_gamma_in
bound_diff_r	interpolator_10bit	9	0	(i_de_r[0] i_de_r[19]) = 1	Result of upbound - lobound in re_gamma
alpha_r	interpolator_10bit	10	0	(i_de_r[0] i_de_r[19]) = 1	Register of alpha in re_gamma
interval_r	interpolator_10bit	4	0	(i_de_r[0] i_de_r[19]) = 1	Result of highLevel - lowLevel in re_gamma

delta_bound_r	interpolator_10bit	17	0	(i_de_r[0] i_de_r[19]) = 1	Result of bound_diff_r *alpha_r in re_gamma
shift_bit_r	log2_4bit	3	0	(i_de_r[0] i_de_r[19]) = 1	Register of shift_bit in re_gamma
shp_1_0_diff_r	sharpness_preprocess	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of pre_shp_in[23:12] - pre_shp_in[11:0]
shp_1_2_diff_r	sharpness_preprocess	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of pre_shp_in[23:12] - pre_shp_in[35:24]
shp_2_3_diff_r	sharpness_preprocess	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of pre_shp_in[35:24] - pre_shp_in[47:36]
shp_3_4_diff_r	sharpness_preprocess	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of pre_shp_in[47:36] - pre_shp_in[59:48]
shp_4_5_diff_r	sharpness_preprocess	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of pre_shp_in[59:48] - pre_shp_in[71:60]
shp_curr_0_r	sharpness_preprocess	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of pre_shp_in[23:12]
shp_curr_1_r	sharpness_preprocess	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of pre_shp_in[35:24]
shp_curr_2_r	sharpness_preprocess	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of pre_shp_in[47:36]
shp_curr_3_r	sharpness_preprocess	12	0	(i_de_r[0] i_de_r[19]) = 1	Register of pre_shp_in[59:48]
shp_sel_0_r	sharpness_preprocess	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of shp_sel_0
shp_sel_1_r	sharpness_preprocess	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of shp_sel_1
shp_sel_2_r	sharpness_preprocess	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of shp_sel_2
shp_sel_3_r	sharpness_preprocess	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of shp_sel_3
shp_curr_prev_diff_r	sharpness_preprocess	52	0	(i_de_r[0] i_de_r[19]) = 1	Consist of {~shp_3_4_diff_r+1, ~shp_2_3_diff_r+1, ~shp_1_2_diff_r+1, shp_1_0_diff_r}
shp_curr_next_diff_r	sharpness_preprocess	52	0	(i_de_r[0] i_de_r[19]) = 1	Consist of {shp_4_5_diff_r, shp_3_4_diff_r, shp_2_3_diff_r, shp_1_2_diff_r}
dot_add_r	sharpness	10	0	(i_de_r[0] i_de_r[19]) = 1	Result of curr_prev_diff - curr_next_diff
dot_add_dly	sharpness	10*2	0	(i_de_r[0] i_de_r[19]) = 1	Shift Register of dot_add_r

				$i_de_r[19] = 1$	
shift_reg	sharpness	12*5	0	$(i_de_r[0] i_de_r[19]) = 1$	Shift Register of shp_curr
mult_r	sharpness	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of dot_add_dly[2] * amout_r
shp_out_r	sharpness	13	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of mult_r + shift_reg[4]
sub_left_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of SHP_{256, 192, 128, 64} - shp_curr
sub_right_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of shp_curr - SHP_{192, 128, 64, 0}
fac_sel_dly	shift_factor	3	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of fac_sel
add_left_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of sub_left_r * {1, 0.75, 0.5, 0.25, 0.125}
add_right_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of sub_right_r * {1, 0.75, 0.5, 0.25, 0.125}
sharp_fac_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of add_left_r + add_right_r
mult_r	shift_factor	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of SPR_SHARP_amout * sharp_fac_r
is_original_r	special_case_detect_l	1	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_original
is_border_r	special_case_detect_l	1	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_border
is_edge_r	special_case_detect_l	4	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_edge
is_original_r	special_case_detect_r	1	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_original
is_border_r	special_case_detect_r	1	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_border
is_edge_r	special_case_detect_r	4	0	$(i_de_r[0] i_de_r[19]) = 1$	Register of is_edge
add_r	core_l	13	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of prev + curr
mult_r	core_l	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of add_r * {pValue{2, 3, 4, 5}_edge, pValue_border}
add_shift_r	core_l	12	0	$(i_de_r[0] i_de_r[19]) = 1$	Result of add_r >> 1

				i_de_r[19]) = 1	
is_special_case_r	core_l	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of is_special_case
add_r	core_r	13	0	(i_de_r[0] i_de_r[19]) = 1	Result of prev + curr
mult_r	core_r	12	0	(i_de_r[0] i_de_r[19]) = 1	Result of add_r * {pValue{2, 3, 4, 5}_edge, pValue_border}
add_shift_r	core_r	12	0	(i_de_r[0] i_de_r[19]) = 1	Result of add_r >> 1
is_special_case_r	core_r	1	0	(i_de_r[0] i_de_r[19]) = 1	Register of is_special_case
lobound_r	de_gamma	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of lobound in de_gamma
lobound_r_dly	de_gamma	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of lobound_r in de_gamma
de_gamma_out_r	de_gamma	8	0	(i_de_r[0] i_de_r[19]) = 1	Register of de_gamma_out
idx_r	search_idx_11bit	5	0	(i_de_r[0] i_de_r[19]) = 1	Register of idx of de_gamma_lut
lowLevel_r	search_idx_11bit	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of lowLevel of de_gamma_lut
highLevel_r	search_idx_11bit	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of highLevel of de_gamma_lut
pixel_in_r	search_idx_11bit	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of de_gamma_in
bound_diff_r	interpolator_11bit	8	0	(i_de_r[0] i_de_r[19]) = 1	Result of upbound - lobound in de_gamma
alpha_r	interpolator_11bit	11	0	(i_de_r[0] i_de_r[19]) = 1	Register of alpha in de_gamma
interval_r	interpolator_11bit	8	0	(i_de_r[0] i_de_r[19]) = 1	Result of highLevel - lowLevel in de_gamma
delta_bound_r	interpolator_11bit	19	0	(i_de_r[0] i_de_r[19]) = 1	Result of bound_diff_r * alpha_r in de_gamma
shift_bit_r	log2_8bit	8	0	(i_de_r[0] i_de_r[19]) = 1	Register of shift_bit in de_gamma

• Chapter 8 nLint Report

• Before

```
File Edit View Search Terminal Help
1 ..../src/core_l.v(31): Error 25005: signal "mult_w[26:20]" has never been referenced. (Design Style)
2 ..../src/core_l.v(31): Error 25005: signal "mult_w[7:0]" has never been referenced. (Design Style)
3 ..../src/core_l.v(37): Error 25005: signal "add_shift_r[0]" has never been referenced. (Design Style)
4 ..../src/core_r.v(29): Error 25005: signal "mult_w[26:20]" has never been referenced. (Design Style)
5 ..../src/core_r.v(29): Error 25005: signal "mult_w[7:0]" has never been referenced. (Design Style)
6 ..../src/core_r.v(35): Error 25005: signal "add_shift_r[0]" has never been referenced. (Design Style)
7 ..../src/de_gamma.v(25): Error 25005: signal "de_gamma_out w[2:0]" has never been referenced. (Design Style)
8 ..../src/de_gamma.v(27): Error 25005: signal "delta bound sh w[18:11]" has never been referenced. (Design Style)
9 ..../src/interpolator_10bit.v(13): Error 25005: signal "bound_diff w[11:9]" has never been referenced. (Design Style)
10 ..../src/interpolator_10bit.v(17): Error 25005: signal "interval_w[8:4]" has never been referenced. (Design Style)
11 ..../src/interpolator_11bit.v(13): Error 25005: signal "bound_diff w[10:8]" has never been referenced. (Design Style)
12 ..../src/interpolator_11bit.v(16): Error 25005: signal "interval_w[10:8]" has never been referenced. (Design Style)
13 ..../src/re_gamma.v(25): Error 25005: signal "re_gamma_out shift_w[11]" has never been referenced. (Design Style)
14 ..../src/re_gamma.v(27): Error 25005: signal "delta bound sh w[16:12]" has never been referenced. (Design Style)
15 ..../src/sharpness.v(21): Error 25005: signal "dot_add w[2:0]" has never been referenced. (Design Style)
16 ..../src/sharpness.v(34): Error 25005: signal "mult_w[3:0]" has never been referenced. (Design Style)
17 ..../src/shift_factor.v(29): Error 25005: signal "sharp_fac w[0]" has never been referenced. (Design Style)
18 ..../src/shift_factor.v(34): Error 25005: signal "mult_w[23:16]" has never been referenced. (Design Style)
19 ..../src/shift_factor.v(34): Error 25005: signal "mult_w[3:0]" has never been referenced. (Design Style)
20 ..../src/shift_factor.v(50): Error 22003: bit width of left-hand-side variable "sub2"(12) does not match that of right-hand-side variable "(256 * 16)"(13) in the assignment. (Language Construct)
21 ..../src/shift_factor.v(50): Error 22005: significant bit of operand "(256 * 16)" lost due to mismatched width assignment or shift operation. (Simulation, Language Construct)
22 ..../src/shift_factor.v(85): Error 22265: bit width of left-hand-side operand "sub_left_r"(12) does not match the right-hand-side operand "{sub_le...}"(13) in addition or subtraction operation. (Language Construct)
23 ..../src/shift_factor.v(91): Error 22265: bit width of left-hand-side operand "sub_right_r"(12) does not match the right-hand-side operand "{sub ri...}"(13) in addition or subtraction operation. (Language Construct)
24 ..../src/special_case_detect_l.v(24): Error 25005: signal "abs_curr_next_diff_w[3:0]" has never been referenced. (Design Style)
25 ..../src/special_case_detect_l.v(24): Error 25005: signal "abs_curr_prev_diff_w[3:0]" has never been referenced. (Design Style)
26 ..../src/special_case_detect_r.v(18): Error 25005: signal "abs_curr_next_diff_w[3:0]" has never been referenced. (Design Style)
27 ..../src/special_case_detect_r.v(18): Error 25005: signal "abs_curr_prev_diff_w[3:0]" has never been referenced. (Design Style)
28 ..../src/spr_top.v(43): Error 25005: signal "spr_shp_out_g[0]" has never been referenced. (Design Style)
29 ..../src/spr_top.v(43): Error 25005: signal "spr_shp_out_g[12]" has never been referenced. (Design Style)
30 ..../src/spr_top.v(43): Error 25005: signal "spr_shp_out_g[24]" has never been referenced. (Design Style)
31 ..../src/spr_top.v(43): Error 25005: signal "spr_shp_out_g[36]" has never been referenced. (Design Style)
32 ..../src/spr_top.v(4): Error 25005: signal "i_hs" has never been referenced. (Design Style)
33 ..../src/spr_top.v(5): Error 25005: signal "i_vs" has never been referenced. (Design Style)
```

• After adjustment

Check RTL with all.rs

```
=====
# Compile Result:
# Total Error(s) : 0
=====
```

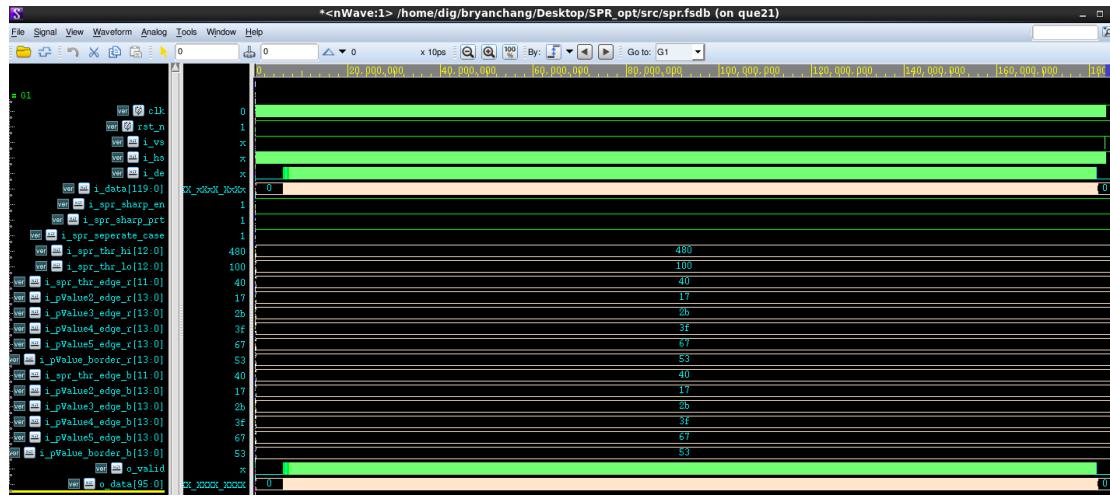
```
# COMPILE OK !!!
```

```
=====
# Linting Result:
#     Warning(s) : 5551
=====
```

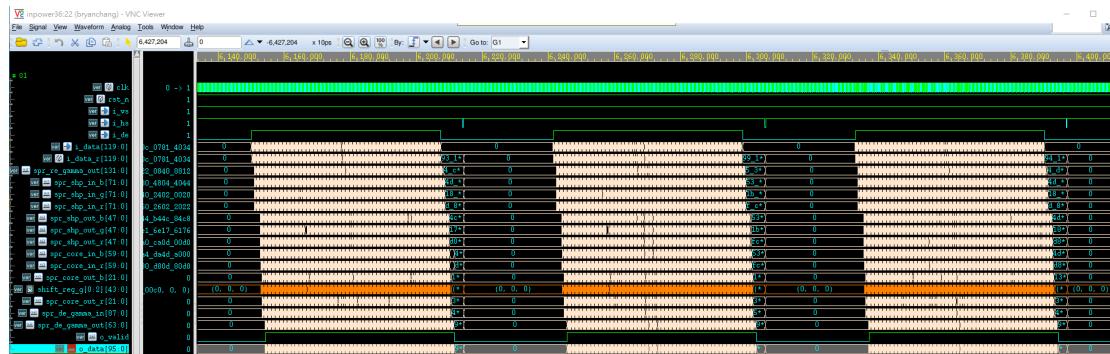
```
# Please Review All Linting Warning(s) !!!
```

• Chapter 9 Simulation

- Frame

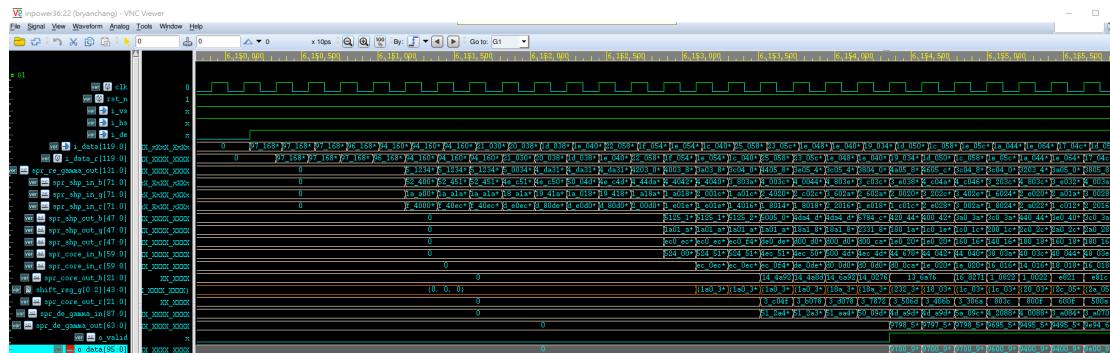


- Line



- Latency: 20T

Input buffer(1T) + spr_re_gamma(4T) +spr_sharpness(8T) +spr_core(3T)+ spr_de_gamma(4T)



• Chapter 10 VCS Coverage

```

1 vcs \
2 +v2k \
3 +neg_tchk \
4 +define+CASE5 \
5 -debug_access+all \
6 -full64 \
7 -R \
8 -f "spr.vc" \
9 -cm line+tgl+fsm+cond+branch+assert \
0 -cm_name CASE5_PIC1

```

```

1 verdi \
2 -cov \
3 -covdir simv.vdb \
4 -workMode coverageAnalysis \
5 -line nocasedef

```

• Before

Name	Score	Line	Toggle	FSM	Condition	Branch
spr_top_tb	89.83%	90.44%	84.32%		91.62%	92.94%
spr_top_0	89.71%	90.38%	84.23%		91.32%	92.92%
spr_core_0	88.64%	98.44%	72.74%		85.23%	98.15%
spr_de_gamma_0	92.75%	89.42%	86.85%		100.00%	94.74%
spr_re_gamma_0	89.05%	89.19%	82.20%		91.67%	93.15%
spr_sharpness_0	90.01%	93.52%	84.92%		92.19%	89.41%

• After adjustment

Name	Score	Line	Toggle	FSM	Condition	Branch
spr_top_tb	94.55%	99.90%	84.45%		98.47%	95.38%
spr_top_0	94.54%	100.00%	84.36%		98.41%	95.40%
spr_core_0	93.58%	100.00%	74.32%		100.00%	100.00%
spr_de_gamma_0	95.71%	100.00%	86.85%		100.00%	96.00%
spr_re_gamma_0	92.08%	100.00%	82.20%		91.67%	94.44%
spr_sharpness_0	94.99%	100.00%	84.92%		100.00%	95.06%

• Chapter 11 Synthesis

Library	tcbn40hvbwp_c150630ss0p99v125c_ccs.db tcbn40hvbwp_lvt_c150630ss0p99v125c_ccs.db tcbn40hvbwpulvt_c150630ss0p99v125c_ccs.db
Clock Constraint	create clock -name "clk" -period 2.12 set_clock_uncertainty -setup 0.4 [all_clocks] set_clock_uncertainty -hold 0.4 [all_clocks]
False Path	set_input_delay 0.4 -clock clk [remove_from_collection [all_inputs] [get_ports clk]] set_output_delay 0.4 -clock clk [all_outputs]
Don't touch	set_dont_touch_network [get_ports clk]
Compile Constraint	compile_ultra -congestion -scan -no_autoungroup - no_seq_output_inversion -no_boundary_optimization -spg - gate_clock
Area Result	spr_top = 80780.616708 μm^2 = 114.485K gate count 2 input NAND area 0.7056 μm^2 (ND2D1BWP)
Leakage Result	LVT cell = 18047/44825 = 40.26% Ungated registers = 57 / 6061 = 0.93%

• Chapter 12 LEC Report

• run_r2g_hier_ip

```
####-- data settings:  
setenv TOP_MODULE "spr_top"  
setenv TOP_MODULE_G "spr_top"  
setenv LIB_DOFILE "LIB.do"  
#setenv RTL_DOFILE "lec_rdrtl.do"  
  
#setenv VSDC "ILI0838E_CORE.vsd"  
#setenv RES_FILE "ILI0838E_CORE_resource.lec"  
setenv VSDC ""  
setenv RES_FILE ""  
setenv RTL_VC "spr.f"  
setenv NETLIST "../syn/Netlist/spr_top_gate.v"  
  
setenv PIN_CONS_DO "pin_constraints.do"  
  
####-- bring settings to lec dofle:  
setenv LOG_NAME "lec.log"
```

• Result

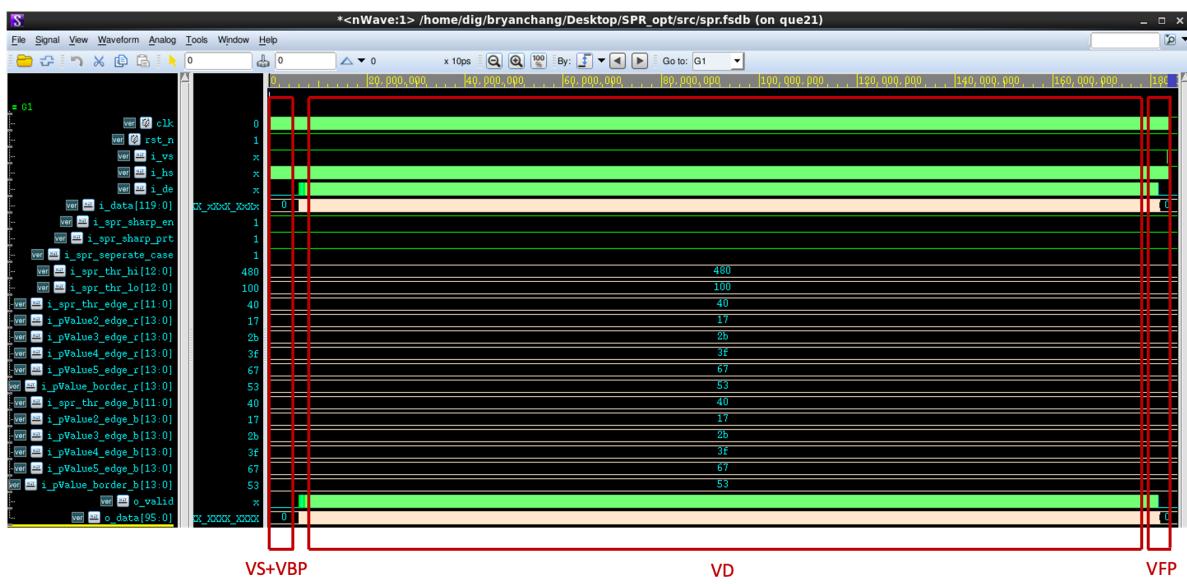
Compared points	P0	DFF	BBOX	Total
Equivalent	97	765	4	866

0 Inverted-equivalent point(s) reported
0 Non-equivalent point(s) reported
0 Abort point(s) reported
0 Not-compared point(s) reported
0 compared point(s) reported

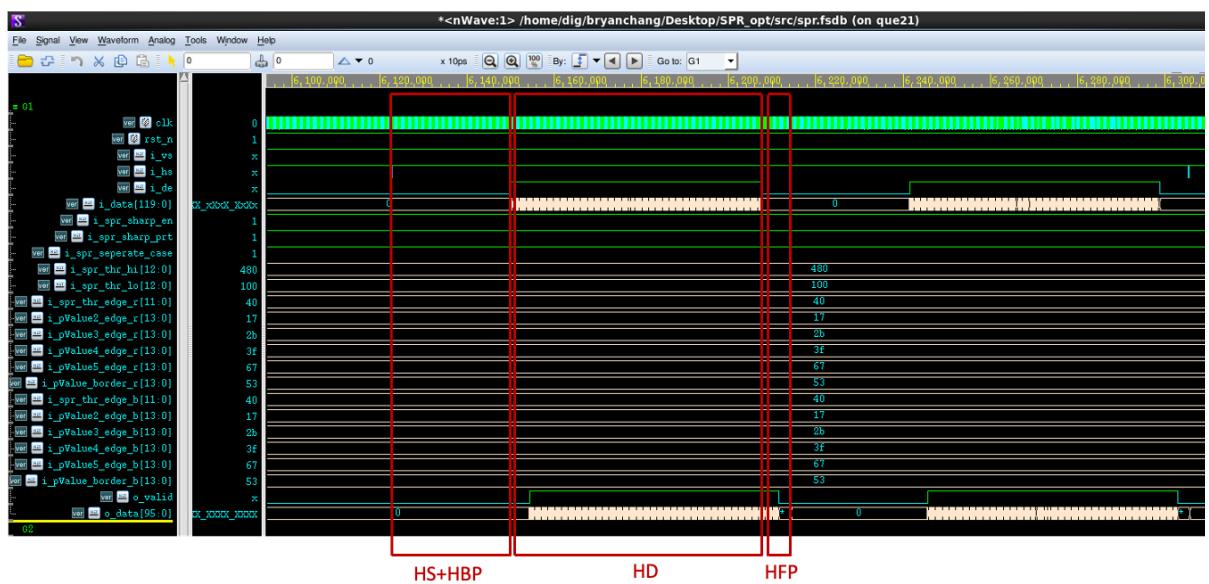
Compared points	P0	DFF	BBOX	Total
Equivalent	97	765	4	866

Total Equivalent modules = 132
Hierarchical compare : Equivalent

- Chapter 13 Pre-Routed Power
- PowerPro analysis
- 分成 VS+VBP、VD、VFP、HS+HBP、HD、HFP
- Frame



- Line



- VS+VBP 區間

- Non clock gating

- Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	10.913	2.27242	0.854423	14.0399	0.1%
combinational	35092	17.5081	2.28918	6.17478	25.9721	0.19%
sequential	0	0	0	0	0	0%
clock_network	267	0.199781	11951.7	1583.56	13535.5	99.71%
total	41505	28.6209	11956.3	1590.59	13575.5	100%

- Hierarchical

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.6209	11956.3	1590.59	13575.5	100%
spr_de_gamma_0	5.99697	1977.82	264.075	2247.89	16.56%
spr_core_0	2.29275	350.709	40.0759	393.077	2.9%
spr_sharpness_0	10.8156	5915.34	757.538	6683.7	49.23%
spr_re_gamma_0	8.13519	2765.23	364.599	3137.96	23.11%

- Clock gating(Efficiency: 98.86%)

- Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.2413	0.854078	0.0794032	12.1747	2.26%
combinational	35219	17.3646	1.81048	4.62698	23.802	4.41%
sequential	0	0	0	0	0	0%
clock_network	408	0.286443	419.438	83.6916	503.416	93.33%
total	41773	28.8923	422.103	88.398	539.393	100%

- Hierarchical

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.8923	422.103	88.398	539.393	100%
spr_de_gamma_0	6.02413	79.8341	19.2139	105.072	19.48%
spr_core_0	2.2988	50.2987	1.73871	54.3363	10.07%
spr_sharpness_0	10.5545	68.0412	13.7617	92.3574	17.12%
spr_re_gamma_0	8.74324	118.014	26.8789	153.637	28.48%

- VD 區間

- Non clock gating

- Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.5	1853.08	277.354	2141.93	11.29%
combinational	35092	17.4563	2732.43	1714.7	4464.59	23.53%
sequential	0	0	0	0	0	0%
clock_network	267	0.199554	10893.3	1474.2	12367.7	65.18%
total	41505	29.1558	15478.8	3466.26	18974.2	100%

- Hierarchical

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.1558	15478.8	3466.26	18974.2	100%
spr_de_gamma_0	6.21075	2286.98	526.538	2819.73	14.86%
spr_core_0	2.28192	850.726	196.583	1049.59	5.53%
spr_sharpness_0	11.0107	7739.37	1434.24	9184.62	48.41%
spr_re_gamma_0	8.223	3163.39	731.868	3903.48	20.57%

- **Clock gating(Efficiency: 40.20%)**

- **Total**

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.8723	1874.97	265.169	2152.02	13.92%
combinational	35219	17.1896	2669.97	1721.46	4408.62	28.51%
sequential	0	0	0	0	0	0%
clock_network	408	0.287368	7872.5	1028.88	8901.66	57.57%
total	41773	29.3493	12417.4	3015.51	15462.3	100%

- **Hierarchical**

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.3493	12417.4	3015.51	15462.3	100%
spr_de_gamma_0	6.23063	1884.17	465.639	2356.04	15.24%
spr_core_0	2.28028	767.973	179.154	949.407	6.14%
spr_sharpness_0	10.5893	5943.28	1210.57	7164.45	46.33%
spr_re_gamma_0	8.92655	2665.99	665.485	3340.4	21.6%

- **VFP 區間**

- **Non clock gating**

- **Total**

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	10.9132	2.61529	0.874999	14.4035	0.11%
combinational	35092	17.5078	4.06864	7.39001	28.9664	0.21%
sequential	0	0	0	0	0	0%
clock_network	267	0.19978	11949.2	1583.25	13532.7	99.68%
total	41505	28.6207	11955.9	1591.51	13576	100%

- **Hierarchy**

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.6207	11955.9	1591.51	13576	100%
spr_de_gamma_0	5.99701	1977.12	264.15	2247.26	16.55%
spr_core_0	2.29274	350.863	40.1095	393.265	2.9%
spr_sharpness_0	10.8154	5916.43	758.152	6685.4	49.24%
spr_re_gamma_0	8.13516	2764.27	364.69	3137.09	23.11%

- **Clock gating(Efficiency: 98.87%)**

- **Total**

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.2414	1.23914	0.113547	12.5941	2.32%
combinational	35219	17.3641	3.54111	5.90754	26.8128	4.94%
sequential	0	0	0	0	0	0%
clock_network	408	0.286443	419.011	83.6392	502.937	92.73%
total	41773	28.892	423.791	89.6602	542.344	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.892	423.791	89.6602	542.344	100%
spr_de_gamma_0	6.02415	80.1077	19.4357	105.568	19.47%
spr_core_0	2.29879	50.4447	1.77127	54.5148	10.05%
spr_sharpness_0	10.5542	68.9585	14.3766	93.8893	17.31%
spr_re_gamma_0	8.74321	118.335	27.1586	154.237	28.44%

- HS+HBP 區間

- Non clock gating

■ Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	10.9139	5.71946	2.59213	19.2255	0.14%
combinational	35092	17.5	5.25863	13.0529	35.8116	0.26%
sequential	0	0	0	0	0	0%
clock_network	267	0.199781	11952.6	1583.73	13536.6	99.6%
total	41505	28.6137	11963.6	1599.38	13591.6	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.6137	11963.6	1599.38	13591.6	100%
spr_de_gamma_0	5.99576	1979.87	266.213	2252.08	16.57%
spr_core_0	2.29232	350.666	40.123	393.081	2.89%
spr_sharpness_0	10.813	5916.09	760.81	6687.71	49.2%
spr_re_gamma_0	8.1324	2768	367.314	3143.45	23.13%

- Clock gating(Efficiency: 98.35%)

■ Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.2408	0.978763	0	12.2196	1.98%
combinational	35219	17.3567	2.74809	7.38388	27.4887	4.44%
sequential	0	0	0	0	0	0%
clock_network	408	0.286452	486.413	92.1058	578.805	93.58%
total	41773	28.884	490.14	99.4897	618.514	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	28.884	490.14	99.4897	618.514	100%
spr_de_gamma_0	6.02233	90.9367	21.0443	118.003	19.08%
spr_core_0	2.29838	52.0306	2.00244	56.3314	9.11%
spr_sharpness_0	10.5508	100.656	19.0226	130.229	21.06%
spr_re_gamma_0	8.74107	134.175	29.5564	172.473	27.89%

- **HD 區間**
- **Non clock gating**
 - **Total**

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.47	2584.61	395.816	2991.89	14.24%
combinational	35692	17.5006	3282.24	2236.31	5536.05	26.35%
sequential	0	0	0	0	0	0%
clock_network	267	0.199559	10994.6	1486.76	12481.5	59.41%
total	41505	29.1701	16861.4	4118.88	21009.5	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.1701	16861.4	4118.88	21009.5	100%
spr_de_gamma_0	6.19495	2381.76	600.388	2988.34	14.22%
spr_core_0	2.28678	975.572	239.602	1217.46	5.79%
spr_sharpness_0	11.0543	8425.6	1660	10096.7	48.06%
spr_re_gamma_0	8.19746	3442.97	892.65	4343.81	20.68%

- **Clock gating(Efficiency: 11.32%)**

■ Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.8381	2615.41	382.181	3009.42	13.92%
combinational	35219	17.1953	3266.19	2257.24	5540.62	25.64%
sequential	0	0	0	0	0	0%
clock_network	408	0.28782	11567.5	1494.12	13061.9	60.44%
total	41773	29.3212	17449.1	4133.54	21612	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.3212	17449.1	4133.54	21612	100%
spr_de_gamma_0	6.2056	2512.7	606.879	3125.79	14.46%
spr_core_0	2.28339	997.355	233.342	1232.98	5.71%
spr_sharpness_0	10.5958	8570.3	1692.23	10273.1	47.53%
spr_re_gamma_0	8.90733	3733.78	936.942	4679.63	21.65%

- **HFP 區間**
- **Non clock gating**
 - **Total**

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.2916	738.094	96.7939	846.18	5.09%
combinational	35092	18.0782	1491.69	828.731	2338.5	14.05%
sequential	0	0	0	0	0	0%
clock_network	267	0.199781	11870.8	1583.48	13454.5	80.86%
total	41505	29.5696	14100.6	2509	16639.2	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.5696	14100.6	2509	16639.2	100%
spr_de_gamma_0	6.35097	2644.56	470.163	3121.08	18.76%
spr_core_0	2.30576	731.551	160.988	894.844	5.38%
spr_sharpness_0	11.035	6752	1097.63	7860.66	47.24%
spr_re_gamma_0	8.45702	2873.32	394.968	3276.75	19.69%

- Clock gating (Efficiency: 42.59%)

■ Total

Power Summary for Initial Design						
Power Group	Count	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
io_pad	0	0	0	0	0	0%
memory	0	0	0	0	0	0%
black_box	0	0	0	0	0	0%
register	6146	11.6517	774.364	89.4957	875.511	7.4%
combinational	35222	17.7706	1467.57	816.341	2301.68	19.45%
sequential	0	0	0	0	0	0%
clock_network	408	0.287427	7663.8	995.172	8659.26	73.16%
total	41776	29.7097	9905.73	1901.01	11836.5	100%

■ Hierarchy

Hierarchy	Leakage Power(uW)	Internal Power(uW)	Switching Power(uW)	Total Power(uW)	Percentage(%)
_Top_Node_	29.7097	9905.73	1901.01	11836.5	100%
spr_de_gamma_0	6.36016	1999.3	376.175	2381.84	20.12%
spr_core_0	2.30065	627.554	140.769	770.624	6.51%
spr_sharpness_0	10.5896	4654.82	824.104	5489.51	46.38%
spr_re_gamma_0	9.13943	2043.29	283.725	2336.16	19.74%