Solution for Analog and Digital Electronics (15CS32) - DEC 2016/ JAN 2017

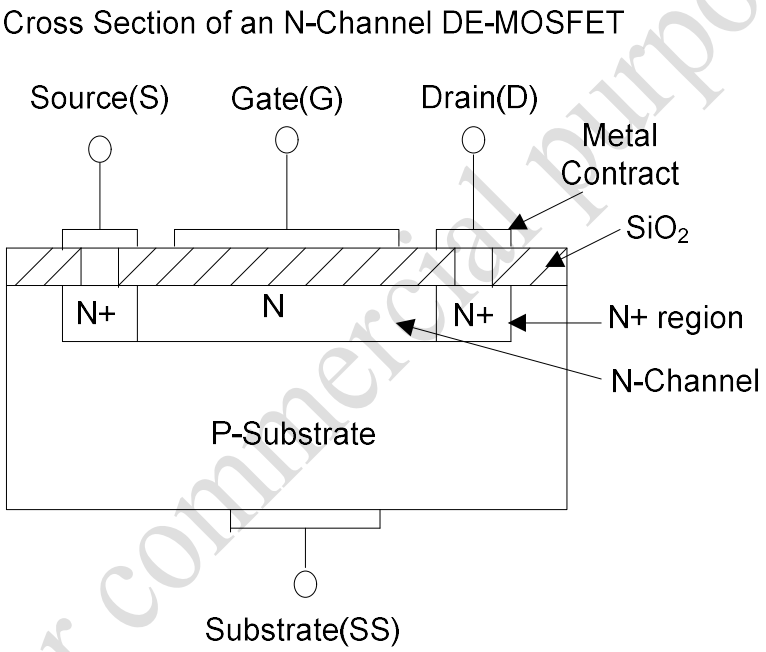
Module 1

1 (a) Explain the working of N-channel DE-MOSFET, with the help of neat diagram.

Answer:

: N-Channel Depletion Metal Oxide Semiconductor Field Effect Transistor (DE-MOSFET)

Construction:



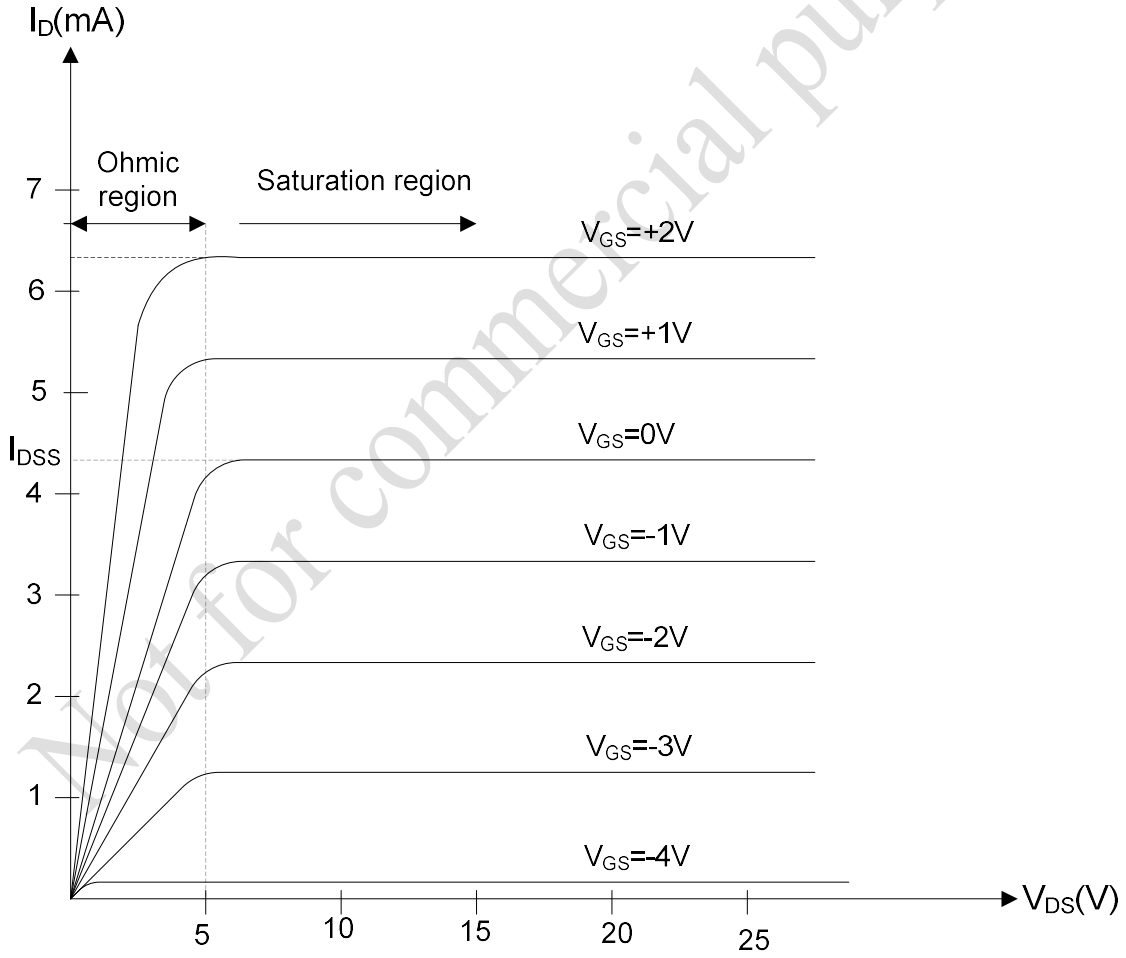
The above figure shows the construction of DE-MOSFET. It consists of a P-type substrate. Two N+ type regions linked by an N-channel are formed in the substrate. The source and the drain terminals are formed by connecting metal contacts to the two N+ regions. The gate terminal is connected to the insulating silicon dioxide (SiO_2) layer on the top of the N-channel. There is no direct connection between the gate terminal and the channel.

Principle of Operation:

When a positive voltage is applied between drain and source terminals ($+V_{DS}$), with gate shorted to the source ($V_{GS}=0$), then there is a flow of electrons towards drain terminal through N-channel as the electrons are attracted to the positive terminal at drain. This constitute Drain Current (I_D). The value of I_D increases with increase of V_{DS} up to a certain value of V_{DS}. After that value of V_{DS}, the I_D remain constant and this value is referred as I_{DSS} (Drain Current with Drain shorted with the source).

For positive gate to source voltage, the electrons (minority carrier) in the P-Substrate are attracted towards the gate terminal and concentration of electrons at the N-channel increases. As a result, the drain current increases. As the application of positive drain to source voltage increases the drain current, the region of positive gate-source voltage is referred to as the enhancement region.
For negative gate to source voltage, the electrons in the N-channel are repelled towards the P-substrate and the concentration of electrons at the N-channel decreases. As a result, the drain current decreases. As the application of negative drain to source voltage decreases the drain current, the region of negative gate-source voltage is referred to as the depletion region. Therefore, gate to source voltage is used to control the gate current.

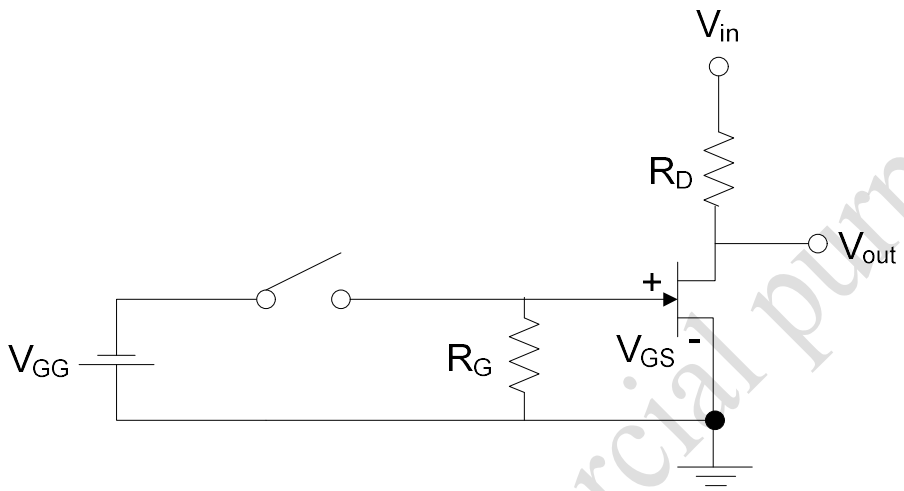
Output Characteristics of N-channel DE-MOSFET



The output characteristic of the N-Channel DE-MOSFET is shown in the above diagram. Drain Current (I_D) is plotted against Drain-Source voltage (V_{DS}) keeping the Gate-Source (V_{GS}) voltage constant. As shown in the diagram, at lower value of Drain-Source voltage (V_{DS}), the Drain Current (I_D) is proportional Drain-Source voltage(V_{DS}) and it follows the Ohm's law. This region

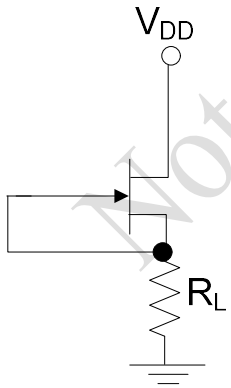
is referred as Ohmic region. As Drain-Source voltage (V_{DS}) increases further, at a certain value Drain Current (I_D) does not increase and this region as shown in the diagram is referred as Saturation region.

1(b) With circuit diagram, explain any two application of FET.
Answer:
FET as Analog Switch



The above circuit shows FET used as Analog Switch using N-channel JFET. When no gate voltage (V_{GG}) is applied, the FET operates in the saturation region and acts as closed switch. When a negative gate voltage (V_{GG}) is applied, the FET operates in the cut-off region and offers very high resistance. Thus, acts as a switch.

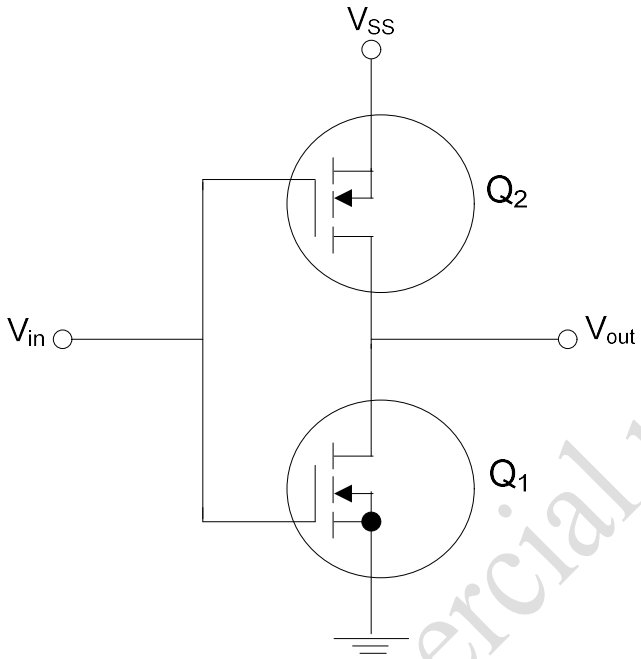
FET as Current Limiter



The above circuit shows FET used as Current Limiter. During the normal operation, the JFET acts in the ohmic region. When the load current increases substantially due to short circuit or any other reason, the JFET operates in the saturation region. Therefore, it acts as a constant current source and prevents excessive current through the load.

1(c) How CMOS can be used as inverting switch?
Answer:

CMOS Inverter Circuit Diagram



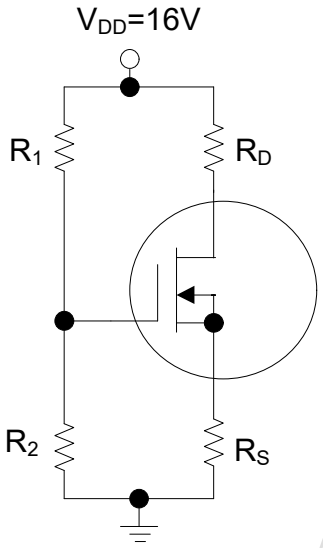
The basic inverter circuit using CMOS is shown above. Inverter is a logic circuit that inverts the applied input signal. The complementary N-type and P-type E-MOSFETs are connected in series with their gate terminals tied together to form input terminal. The drain terminals are connected together to form output terminal.

When the input voltage V_{in} is at logic LOW, the gate-source voltage of Q_2 (P-channel E-MOSFET) is $-V_{SS}$ which makes Q_2 in ON state resulting low resistance path between V_{SS} and V_{out} . The gate-source voltage for Q_1(N-channel E-MOSFET) is zero which makes Q_1 is in OFF state resulting very high resistance between output terminal and ground. As a result the output voltage is equal to V_{SS} , that is, V_{out} is HIGH.

When the input voltage V_{in} is at logic HIGH, the gate-source voltage of Q_2 (P-channel E-MOSFET) is zero which makes Q_2 in OFF state resulting high resistance path between V_{SS} and V_{out} . The gate-source voltage for Q_1(N-channel E-MOSFET) is HIGH which makes Q_1 is in ON state resulting low resistance between output terminal and ground. As a result the output voltage ,V_{out} is HIGH.

2 (a) Design a voltage divider bias network using a DE-MOSFET with supply voltage V_{DD}=16V, I_{DSS}=10mA and V_P =-5V to have to have a quiescent drain current of 5 mA and gate voltage of 4V. (Assume the drain resistor R_D to be four times the source resistor R_S and R_2=1KΩ)

Answer:



Given V_{DD}=16V, Gate Voltage (V_G) = 4V, Drain current (I_D) =5mA, I_{DSS}=10mA and V_P = -5V

As the quiescent drain current (I_D) is less than the saturation drain current (I_{DSS}), the MOSFET is operated in the depletion mode.

We know, in a DE-MOSFET,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \Rightarrow 5\times10^{-3} = 10\times10^{-3}\times[1+\frac{V_{GS}}{5}]^2 \Rightarrow [1+\frac{V_{GS}}{5}]^2 = 0.5$$

$$\Rightarrow 1+\frac{V_{GS}}{5} = \pm\sqrt{0.5} \Rightarrow 1+\frac{V_{GS}}{5} = 0.7 \text{ (Only +ve is considered, otherwise } V_{GS} \text{ will be large negative)}$$

$$\Rightarrow V_{GS} = -1.5V$$

The gate-source voltage,

$$V_{GS} = V_G - V_S \Rightarrow V_{GS} = V_G - I_D R_S \Rightarrow -1.5 = 4 - 5\times10^{-3}\times R_S \Rightarrow R_S = 1.1K\Omega$$

$$R_D = 4\times R_S \text{ (Given)} \Rightarrow R_D = 4.4K\Omega$$

Given R_2=1KΩ

$$\text{Again, } V_G = \frac{R_2}{R_1+R_2}\times V_{DD} \Rightarrow 4 = \frac{1000}{R_1+1000}\times16 \Rightarrow R_1 = 3000\Omega = 3K\Omega$$

2 (b) Explain the performance parameters of Op-amp.

Answer:

Answer: The following are the performance parameters of operational amplifier:

(i) Bandwidth: Bandwidth of operational amplifier is the range frequencies it can amplify for a given amplifier gain.

(ii) Slew rate: It is defined as the rate of change of output voltage time. It gives the idea as to how well the opamp output follows a rapidly changing waveform at the input.

(iii) Open-Loop Gain: Open-loop gain is the ratio of single-ended output to the differential input.

(iv) Common Mode Rejection Ratio (CMRR): It is the ratio of the desired differential gain (A_d) to the undesired common mode gain(A_c). CMRR is a measure of the ability of the opamp to suppress common mode signal. The ratio of CMRR is usually expressed $20\log (A_d/A_c)$dB.

(v) Power Supply rejection Ratio (PSRR): PSRR is defined as the ratio of change in the power supply voltage to corresponding change output voltage. PSRR is also defined as the ratio of change in one of the power supply voltage to the change in the input offset voltage with the other power supply voltage held constant.

(vi) Input Impedance: Input Impedance is the impedance looking into the input terminals of the opamp and mostly expressed in terms of resistance only.

(vii) Output Impedance: Output Impedance is defined as the impedance between the output terminal of the opamp and the ground.

(viii) Settling Time: Settling Time is expressed as the time taken by the opamp output to settle within a specified percentage of the final value in response to a step input. It gives the response of the opamp to large step input.

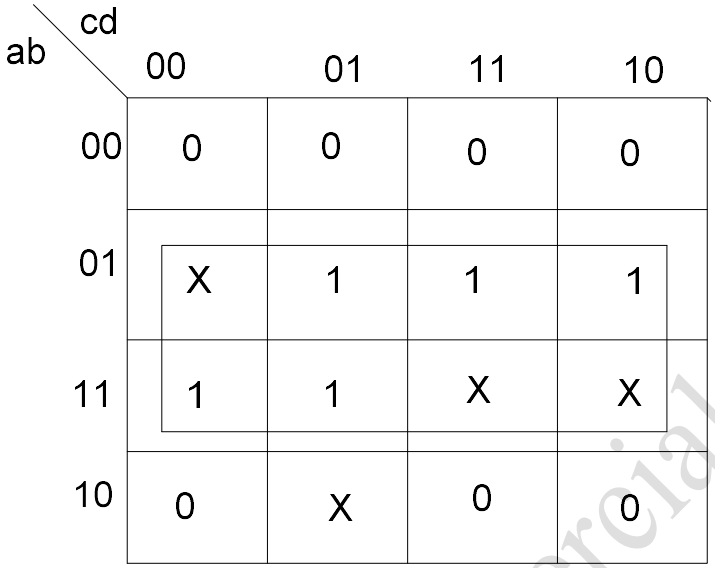
(ix) Offset and Offset Drifts: An ideal opamp should produce a zero output for a zero differential input. But it is not so in the case of practical opamps. It is observed that a DC differential voltage is to be applied externally to get a zero output. This externally applied input is referred to as the input offset voltage. Output offset voltage is the voltage at the output with the both input terminals grounded. Input offset current is the difference between the two bias current flowing towards the inputs of the opamp. Input bias current defined as the average of the two bias currents flowing into the two input terminals of the opamp.

Module 2

3 (a) Minimize the following Boolean function using K-map method:

f(a,b,c,d) = Σm(5,6,7,12,13) + Σd(4,9,14,15)

Answer:



f(a,b,c,d)=b

3(b) Apply Quine McClusky method to find the essential prime implicants for the Boolean expression: f(a,b,c,d) = Σm(1,3,6,7,9,10,12,13,14,15)

Answer:

f(A,B,C,D)=Σm(1,3,6,7,9,10,12,13,14,15)

Stage 1		Stage 2		Stage 3	
ABCD		ABCD		ABCD	
0001	(1)√	00-1	(1,3)	-11-	(6,7,14,15)
		-001	(1,9)		
0011	(3)√	0-11	(3,7)	-11-	(6,14,7,15)
0110	(6)√				
1001	(9)√	011-	(6,7)√	11- -	(12,14,13,15)
1010	(10)√	-110	(6,14)√		
1100	(12)√	1-01	(9,13)		
0111	(7)√	1-10	(10,14)		
1101	(13)√	11-0	(12,14)√		
1110	(14)√				
		-111	(7,15)√		
1111	(15)√	11-1	(13,15)√		
		111-	(14,15)√		

	1	3	6	7	9	10	12	13	14	15
$A'B'D(1,3)$	√	√								
$B'C'D(1,9)$										
$A'CD(3,7)$										
$AC'D(9,13)$					√			√		
$ACD'(10,14)$						√			√	
BC(6,7,14,15)			√	√					√	√
AB(12,13,14,15)							√	√	√	√

From the above table, the prime implicants are AB,BC,A′B′D,AC′D,ACD′

$$f(A,B,C,D) = AB + BC + A'B'D + AC'D + ACD'$$

4(a). A digital system is to be designed in which the month of the year is given as input in four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess number in the input beyond '1011' as don't care condition for the system of four variables (ABCD). Find the following:
(i) Write the truth table and Boolean expression in SOPΣm and POSπM form.
(ii) Using K-map simplify the Boolean expression of canonical minterm form.
(iii) Using basic gates, implement the logic circuit.

Answer:

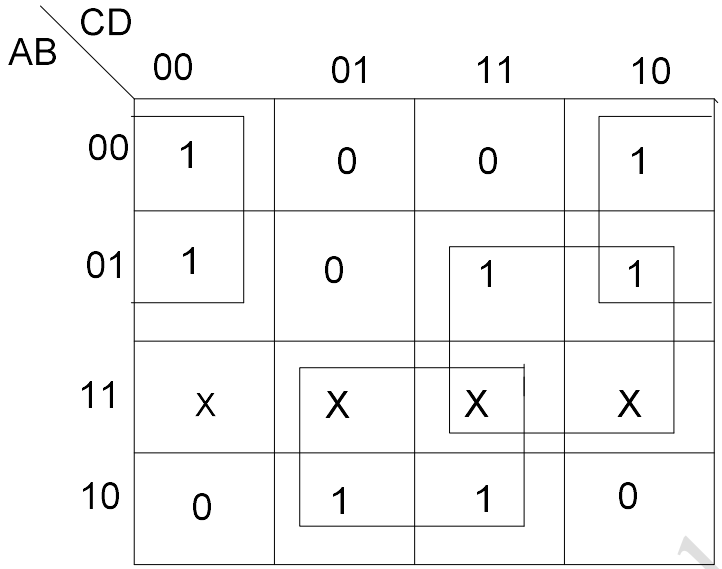
(i) Truth table is shown below:

A	B	C	D	Month	Output=Y
0	0	0	0	January	1
0	0	0	1	February	0
0	0	1	0	March	1
0	0	1	1	April	0
0	1	0	0	May	1
0	1	0	1	June	0
0	1	1	0	July	1
0	1	1	1	August	1
1	0	0	0	September	0
1	0	0	1	October	1
1	0	1	0	November	0
1	0	1	1	December	1
1	1	0	0		x
1	1	0	1		x
1	1	1	0		x
1	1	1	1		x

Boolean expression in SOP form: $Y=\Sigma m(0,2,4,6,7,9,11)+d(12,13,14,15)$

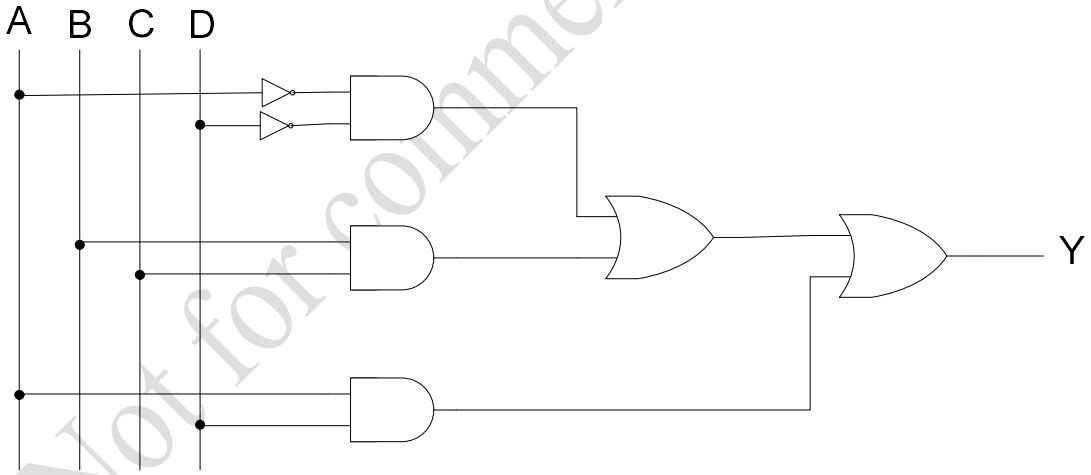
Boolean expression in POS form: $Y=\pi M(1,3,5,8,10)+d(12,13,14,15)$

(ii)



$$Y = \overline{A}\overline{D} + BC + AD$$

(iii)



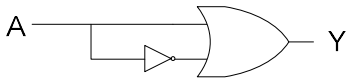
4(b) What is hazard? List the type of hazards and explain static 0 and static 1 hazard.

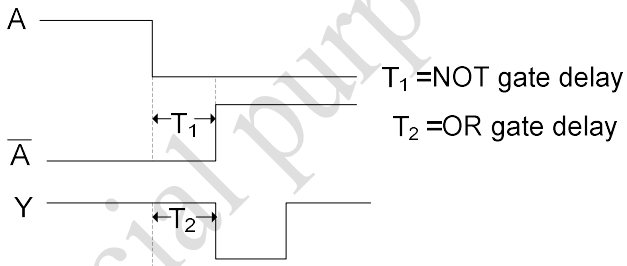
Answer:

Answer: When the input to a combinational circuit changes, unwanted switching transients may appear in the output. These transients occurs when different paths from input to output have different propagation delays.

Static-1 hazard:

This type of hazard occurs when $Y = A + \overline{A}$ type situation appears for a logic circuit and A makes a transition $1 \rightarrow 0$.

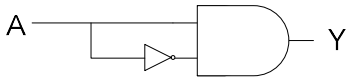


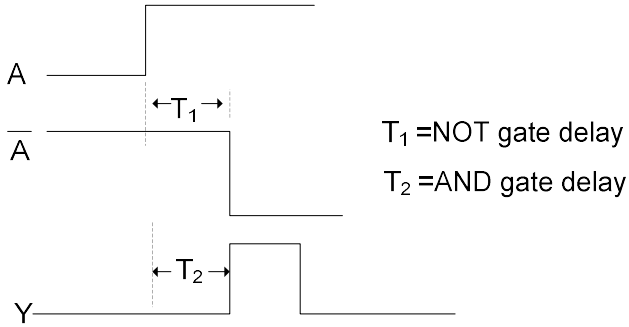


An $A + \overline{A}$ condition should always generate 1 at the output i.e static-1. But the NOT gate output takes finite time to become 1 following $1 \rightarrow 0$ transition of A. Thus for the OR gate there are two zeros appears at the input for that small duration resulting a 0 at the output. The width of this zero is in nanosecond order and is called glitch.

Static-0-hazard:

This type of hazard occurs when $Y = A\overline{A}$ kind of situation occurs in a logic circuit and A makes a transition 0⟶1. A $A\overline{A}$ condition should always generate 0 at the output i.e static-0. But the NOT gate output takes finite time to become 0 following a 0⟶1 transition of A. Thus for final AND gate there are two ones appearing at the inputs for small duration resulting a 1 at its output.





Module 3

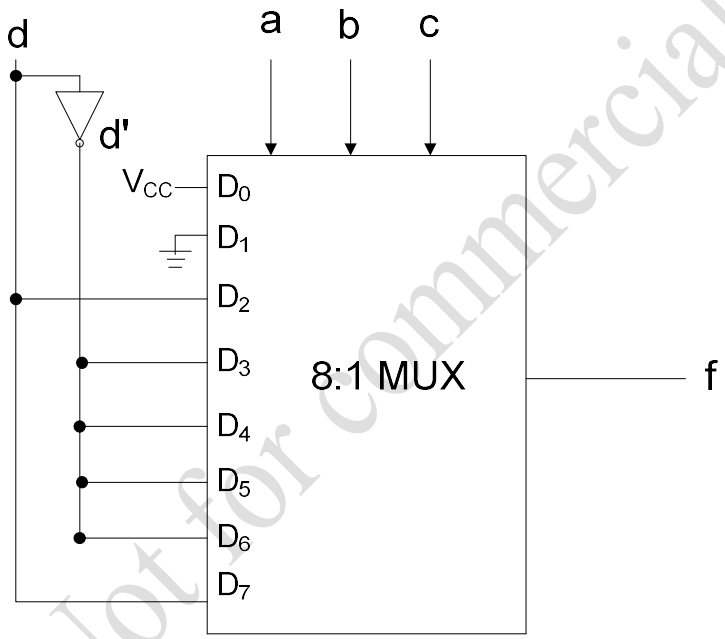
5(a) Implement the following function using 8:1 multiplexer:

f(a,b,c,d)=Σm(0,1,5,6,8,10,12,15)

Answer:

abc	000	001	010	011	100	101	110	111
d=0	1	0	0	1	1	1	1	0
d=1	1	0	1	0	0	0	0	1
f	1	0	d	d'	d'	d'	d'	d
8:1 MUX data input	D_0=1	D_1=0	D_2=d	D_3=d'	D_4= d'	D_5= d'	D_6= d'	D_7=d

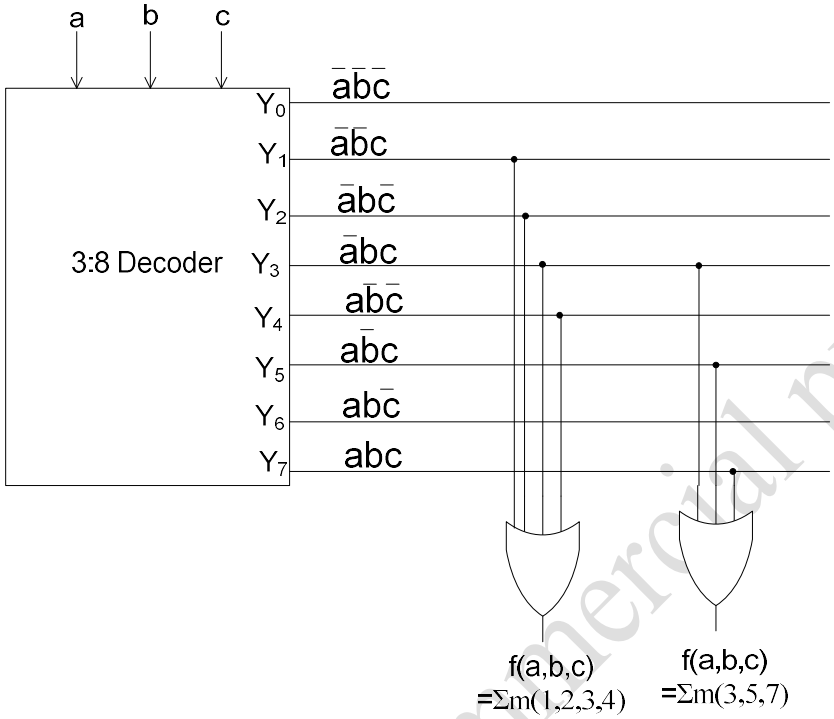
Circuit diagram:



5(b) Realize the following function using 3:8 decoder:

(i) f(a,b,c)=Σm(1,2,3,4) (ii) f(a,b,c)=Σm(3,5,7)

Answer:

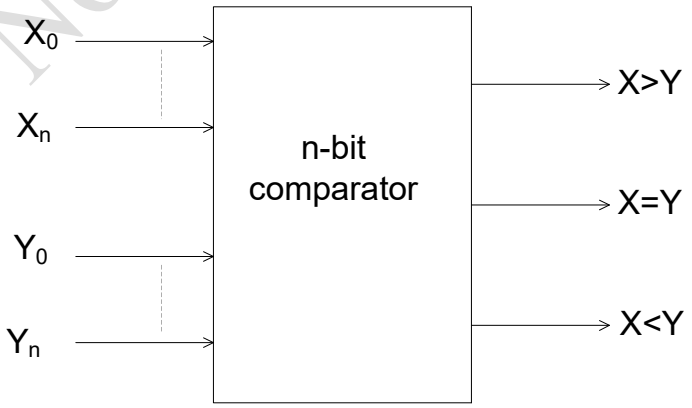


5(c) What is Magnitude Comparator? Explain 1 bit Magnitude comparator.

Answer:

A magnitude comparator compares two binary numbers and it produces an output showing the comparison of the two input numbers.

For example, two n-bit binary numbers $X=X_0X_1..X_n$ and $Y=Y_0Y_1\ldots Y_n$ are compared. There are three ouputs. The outputs are for X>Y, X=Y and X<Y as shown in the figure below.



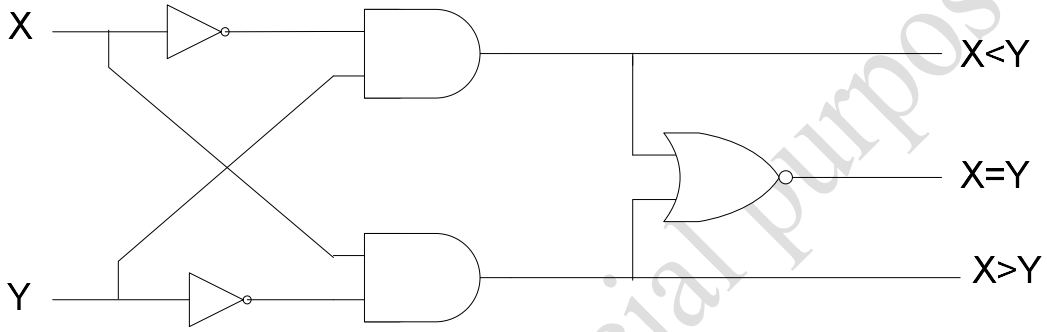
Designing of one bit comparator:

Truth table

Input		Output		
X	Y	X>Y	X=Y	X<Y
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

If G, L, E stand for greater than, less than and equal to respectively, then

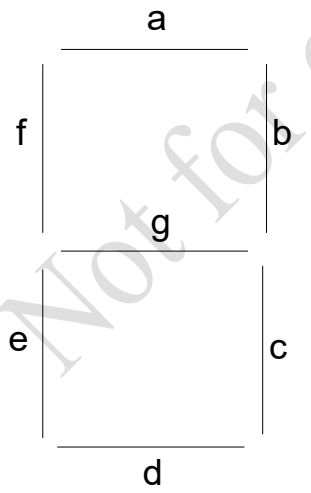
(X>Y): G=XY′; (X<Y):L=X′Y; (X=Y): E=X′Y′+XY=(XY′+X′Y)′=(G+L)′



6(a) Design 7-segment decoder using PLA.

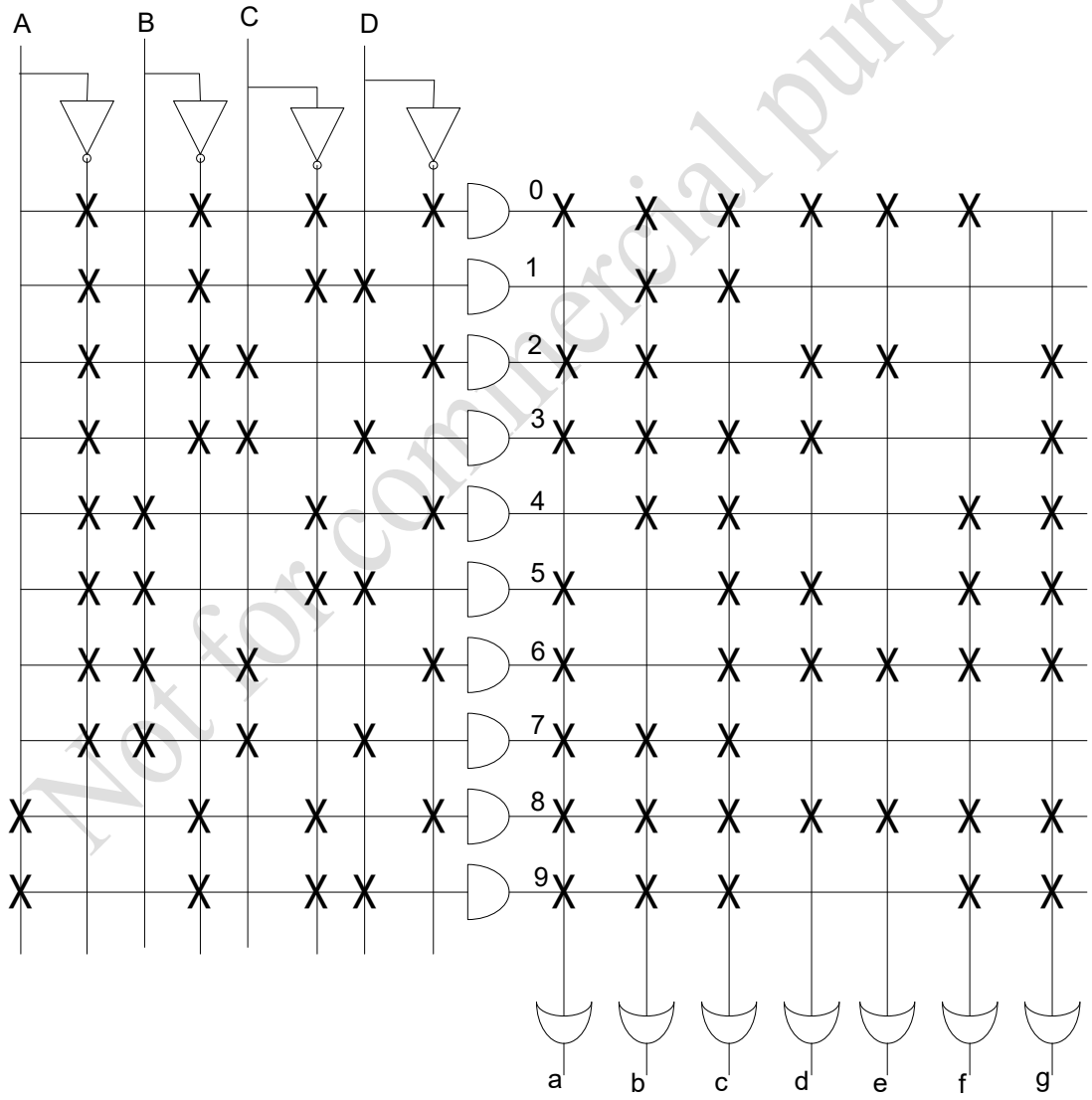
Answer:

Seven segment indicator:



Following table shows the segments should light up to display a number.

Number to display	Segments to light up
0	a,b,c,d,e,f
1	b,c
2	a,b,d,e,g
3	a,b,c.d,g
4	b,c,f,g
5	a,c,d,f
6	a,c,d,e,f,g
7	a,b,c
8	a,b,c,d,e,f,g
9	a,b,c,f,g



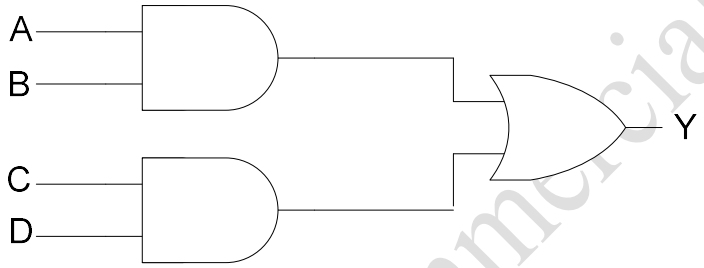
6(b) Differentiate between combinational and sequential circuit.

Answer:

Difference between combinational and sequential circuit:

Combinational Circuit	Sequential Circuit
Output is a function of the present inputs.	Output is a function of clock, present inputs and the previous states of the system.
Independent of clock and hence triggering is not required.	Clock and hence triggering is required.
Do not store data.	Store the previous states.
Used mainly for arithmetic and Boolean operations. For example, adder, multiplexers, encoder etc.	Used for storing data. For example, latch.
No feedback is required.	Feedback is required.

6(c) Write VHDL code for the given circuit



Answer:

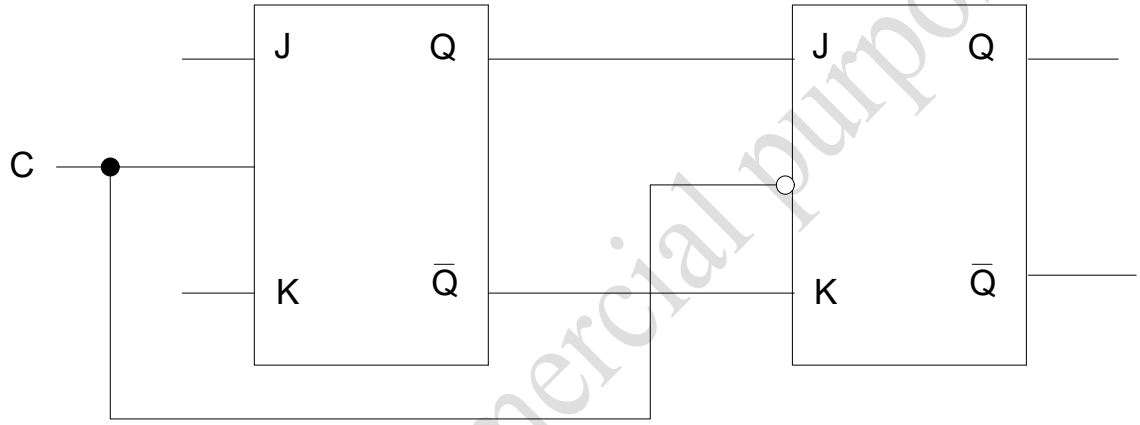
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity fig is
Port( A: in std_logic;
      B: in std_logic;
      C: in std_logic;
      D: in std_logic;
     Y:out  std_logic);
architecture  Behavioral of  fig  is
begin
Y<=(A and B) or (C and D);
end Behavioral;
```

Module 4

7(a) What is race condition? With block diagram and truth table, explain the working of JK Master-Slave flip flop.

Answer:

When the S and R inputs of an SR flip flop is at logic 1 , then the output becomes unpredictable when input changes. This is called race around condition.



Master Slave flip flop

Master is positive-level-triggered and the slave is negative-level-triggered. The master responds to its J and K inputs before the slave.

If J=1 and K=0, the master sets on the positive clock transition. The high Q output of the master drives the J input of the slave. So, on the negative clock transition, the slave sets, thus copying the action of the master.

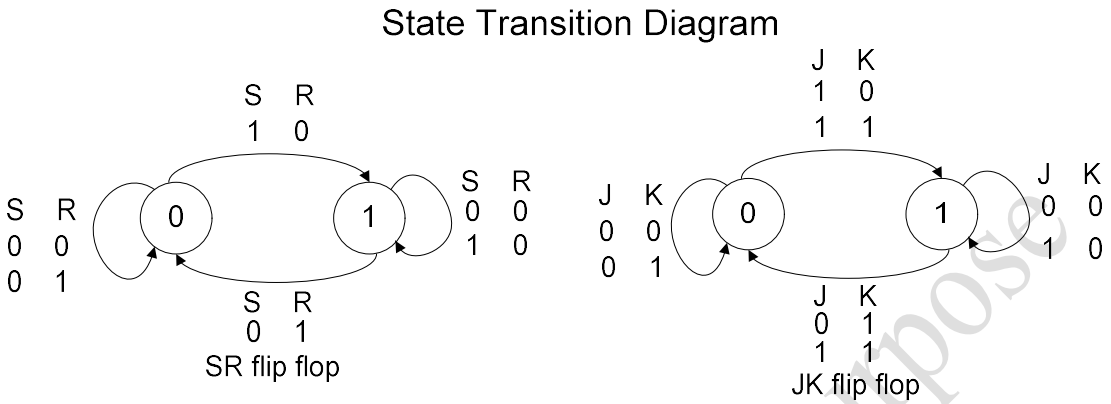
If J=0 and K=1, the master resets on the positive clock transition. The high $\overline{Q}$ output of the master drives the K input of the slave. So, on the negative clock transition, the slave resets, thus copying the action of the master.

If J=1 and K=1, the master toggle on the positive clock transition. The slave also toggle at the negative clock transition thus copying the action of the master.

If J=0 and K=0, the master and the slave both are disabled, thus copying the action of the master.

7(b) Give the state transition diagram and characteristic equation for JK and SR flip flop.

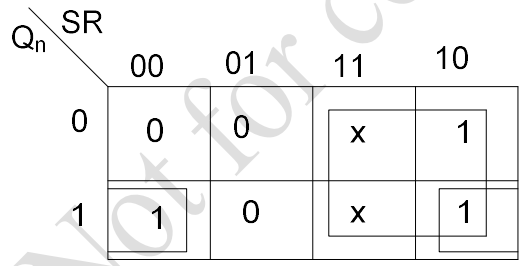
Answer:



Excitation Table for SR, JK flip flop shown below prepared from the above State transition diagram.

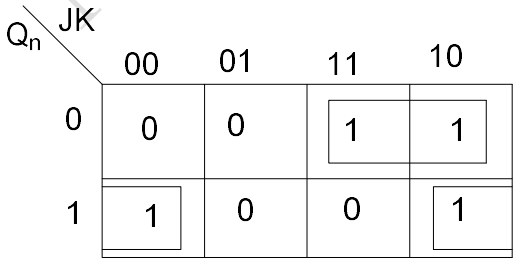
$Q_n \rightarrow Q_{n+1}$	S	R	J	K
0 0	0	X	0	X
0 1	1	0	1	X
1 0	0	1	X	1
1 1	X	0	X	0

From the Excitation Table, K-map is formed and then the characteristic equation is determined.



Characteristic Equation for SR flip flop is

$$Q_{n+1}=S+\overline{R}Q_n$$



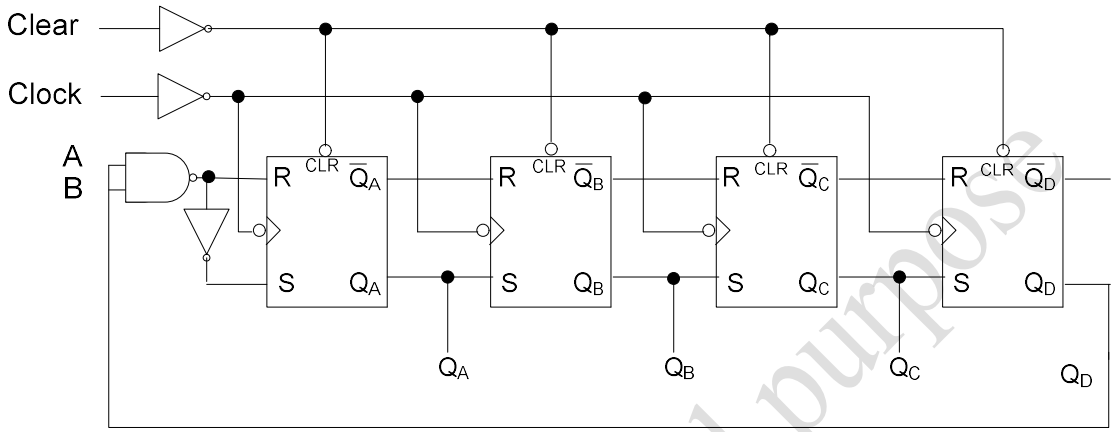
Characteristic Equation for JK flip flop is

$$Q_{n+1}=J\overline{Q}_n+\overline{K}Q_n$$

8(a) With neat diagram, explain ring counter.

Answer:

Answer: Following is the 4-bit ring counter.



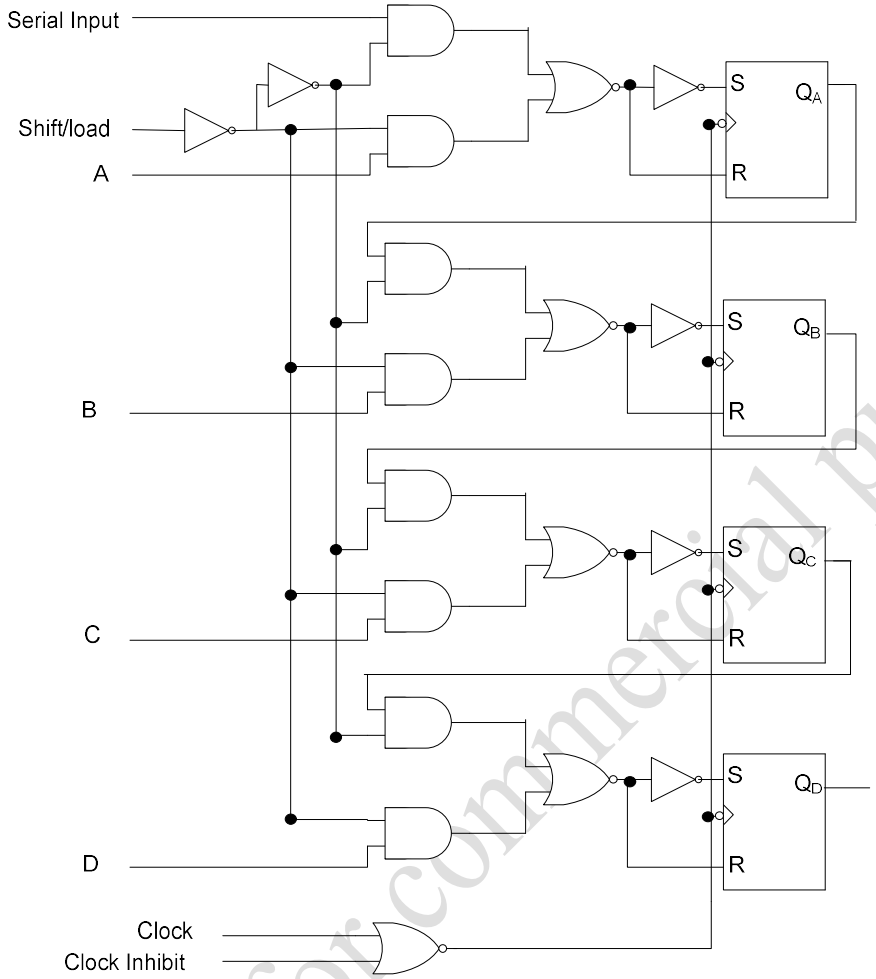
Output of the last flip flop Q_D is feedback to the input of the first flip flop.

State table of Ring Counter is shown below:

Clock	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

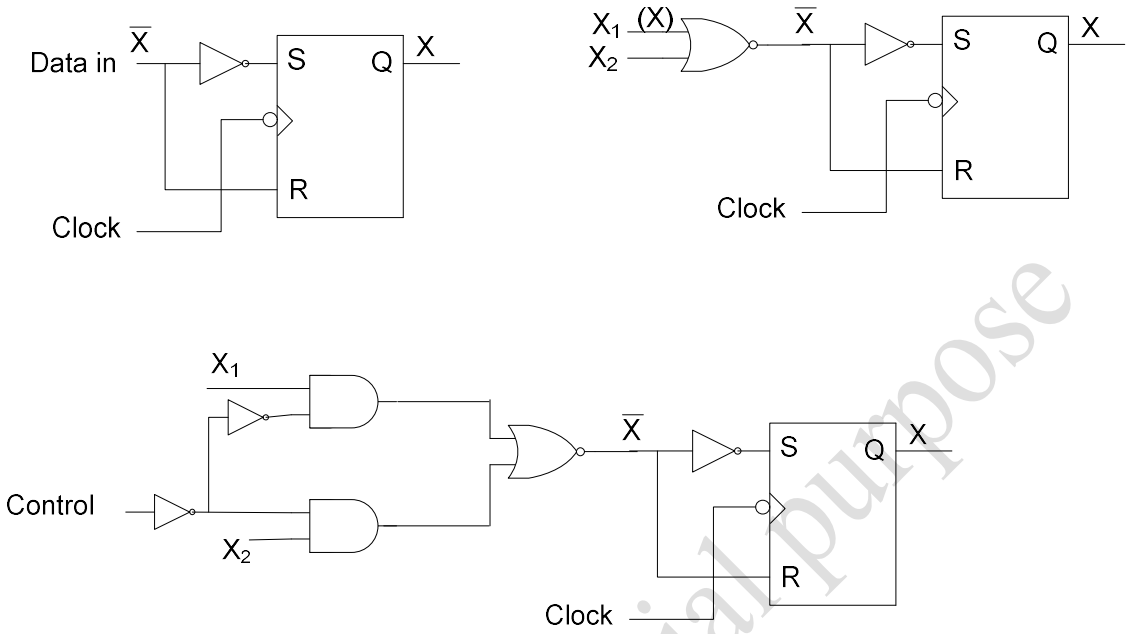
8(b) What is shift register? With neat diagram, explain 4 bit parallel in serial out shift registers.

Answer: 4-bit parallel in serial out is shown below.



The above logic block diagram shows 4-bit parallel in (A, B, C and D) and serial out register. This can also be used as serial in if data is entered at Serial Input terminal as shown.

Analysis of the above circuit is given below:



The clocked RS flip flop and the attached inverter form a type D flip flop. If a data bit X is to be clocked into the, the complement of X must be present at the input.

If one leg of the NOR gate is at ground level, a data bit X at the other leg is inverted. This NOR gate provide option of entering data from two different sources, either X_1 or X_2 .

Addition of two AND gates and two inverters allow the selection of data selection of data X_1 or data X_2.

If the control line is high, the upper AND gate is enabled and lower AND gate is disabled.

If the control line is low, upper AND gate is disabled and the lower AND gate is enabled.

Control line is high: Data bit at X_1 will be shifted into the flip flop at the next clock pulse.

Control line is low: Data bit at X_2 will be shifted into the flip flop at the next clock pulse.

Shift/Load is low: A single clock transition load data into the register in parallel.

8(c) Compare synchronous and asynchronous counter.

Answer:

Synchronous Counter	Asynchronous Counter
Clock input is common to all flip flops.	Clock is applied to Least Significant Bit flip flop. The output of this flip flop is the clock of the next flip flop and so on.
Any flip flop can be used.	All flip flops are toggle flip flops.
Speed is independent of the number of flip flops.	Speed is dependent of the number of flip flops.
Extra logic gates are required as per the design.	No extra logic gates are required.
Cost is more.	Cost is less.

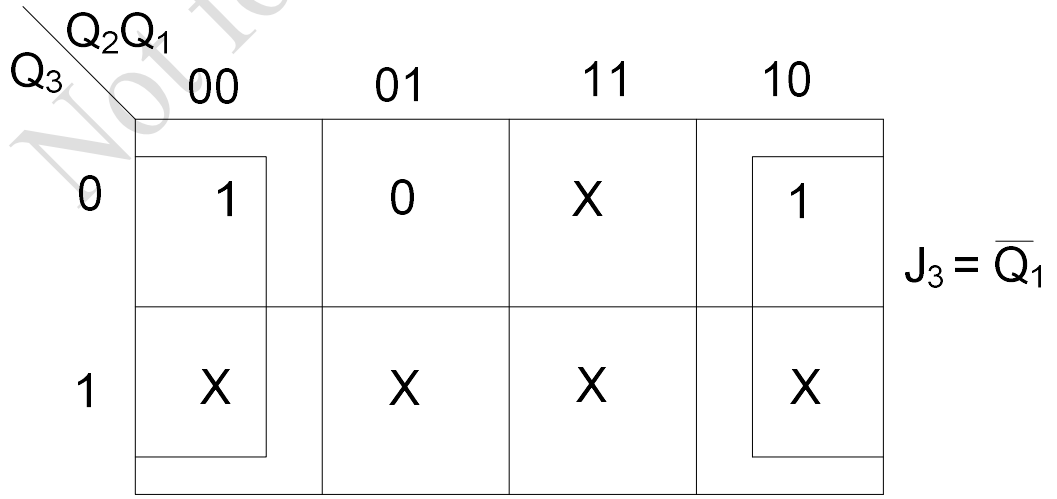
Module 5

9(a) Define counter. Design a synchronous counter for the sequence 0→4→1→2→6→0→4 using JK flip flop.

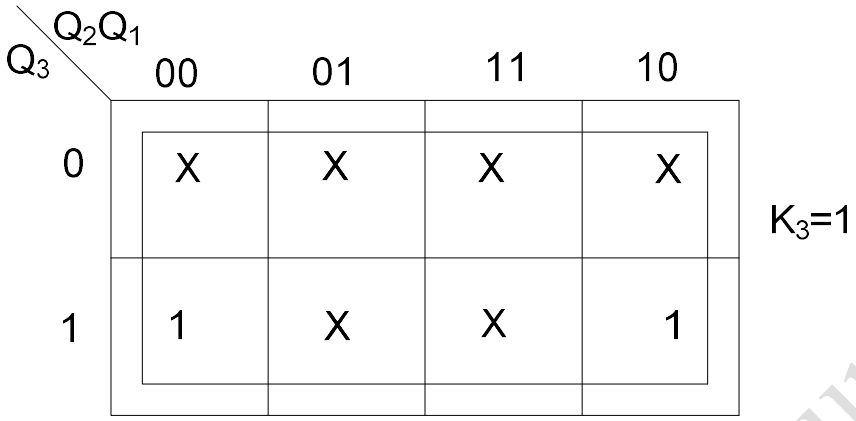
Answer:

Present State			Next State			J_3	K_3	J_2	K_2	J_1	K_1
Q_3	Q_2	Q_1	Q_3+	Q_2+	Q_1+						
0	0	0	1	0	0	1	X	0	X	0	X
1	0	0	0	0	1	X	1	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	1	0	1	X	X	0	0	X
1	1	0	0	0	0	X	1	X	1	0	X

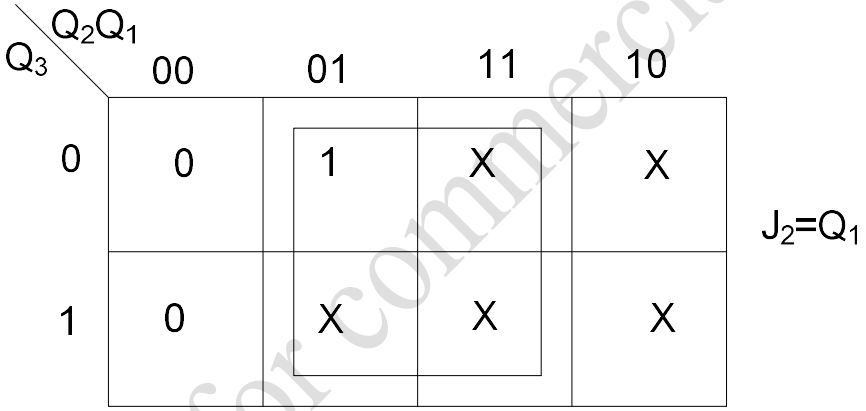
K-map for J_3:



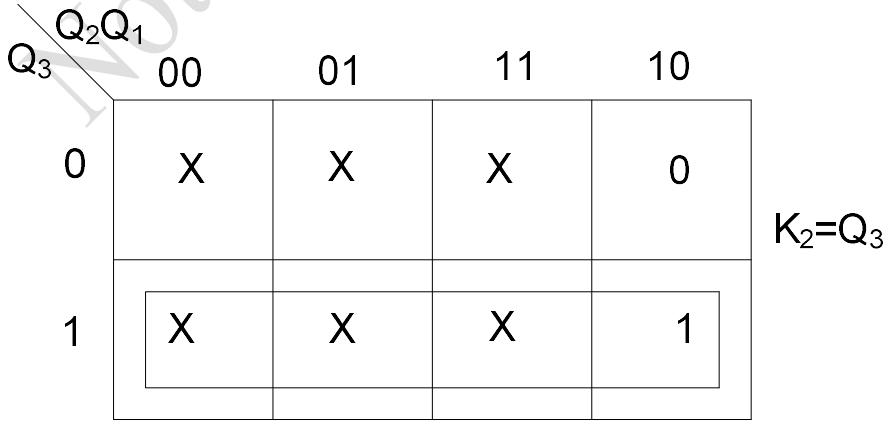
K-map for K_3:



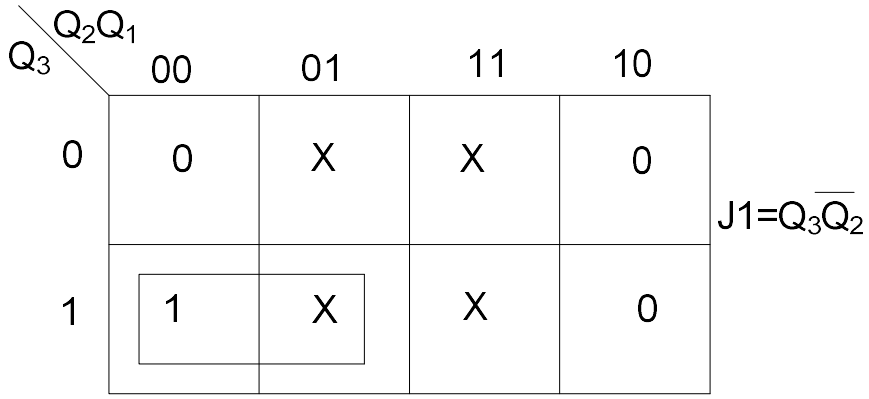
K-map for J_2:



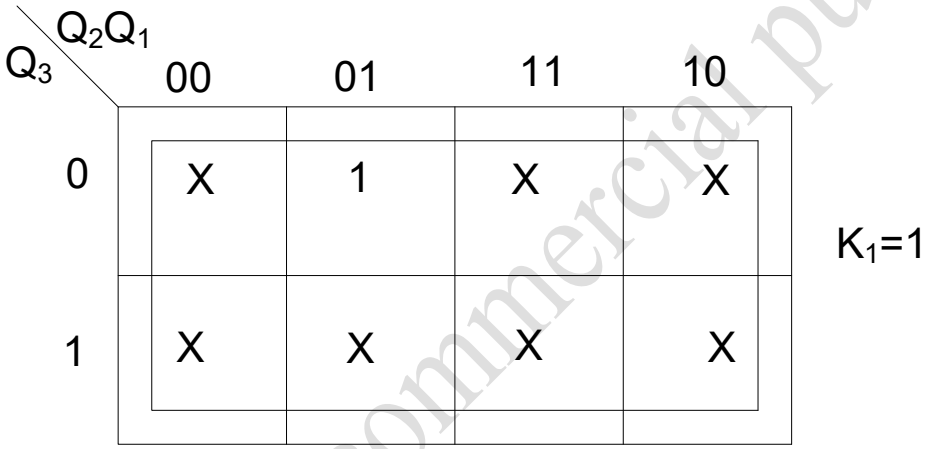
K-map for K_2:



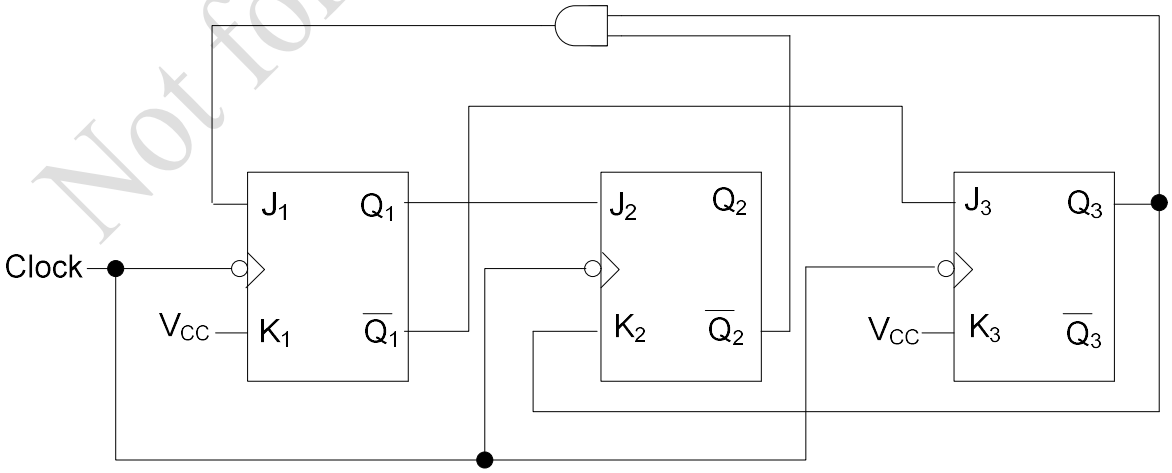
K-map for J_1:



K-map for K_1:



Circuit diagram:



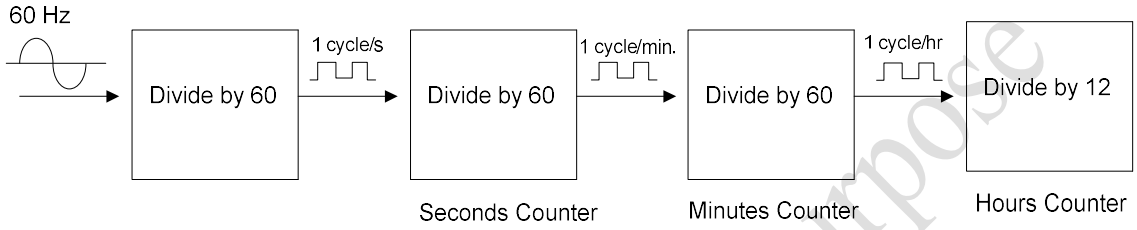
(Note: Tested in laboratory)

9(b) Explain digital clock, with neat diagram.

Answer:

In several countries power supply is 50Hz. There one can use standard variable frequency signal generator to get 60Hz.

Block diagram of a digital clock:



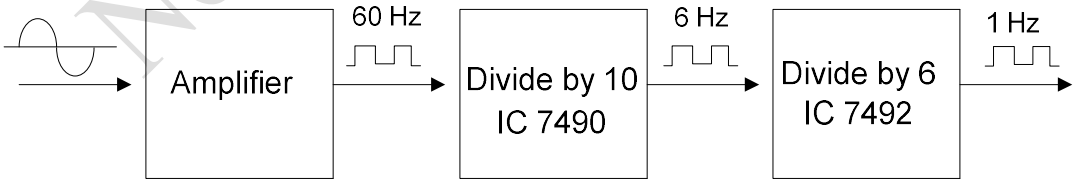
Block diagram shows the functions to be performed. The first divide by 60 counter divides the 60 Hz power signal down to a 1 Hz square wave. This 1 Hz square wave is the input to the second counter.

The second divide by 60 counter changes its state once each second and has 60 discrete states. It can be decoded to provide signal to display second. This counter produces output square wave of 1 cycle per minute and this is the input to the third counter.

The third divide by 60 counter changes its state once each minute and has 60 discrete states. It can be decoded to provide signal to display minute. This counter produces output square wave of 1 cycle per hour and this is input to the fourth counter.

The last counter changes its state once each hour and has12 discrete states. It can be decoded to provide signal to display hour. The last counter reset at every 12 hours.

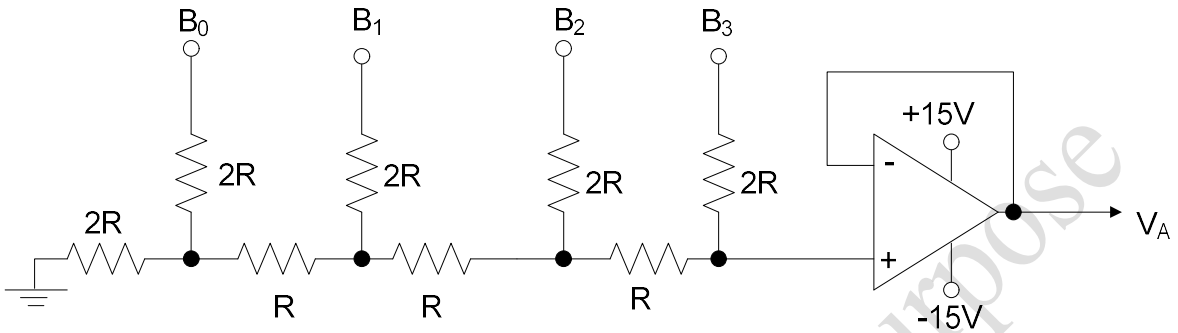
Divide by 60 counter can be implemented by cascading divide by 10 counter (IC 7490) and divide by 6 counter (IC 7492). This is in the block diagram below.



10(a) Explain the binary ladder with digital input of 1000.

Answer:

4-bit binary ladder shown below:



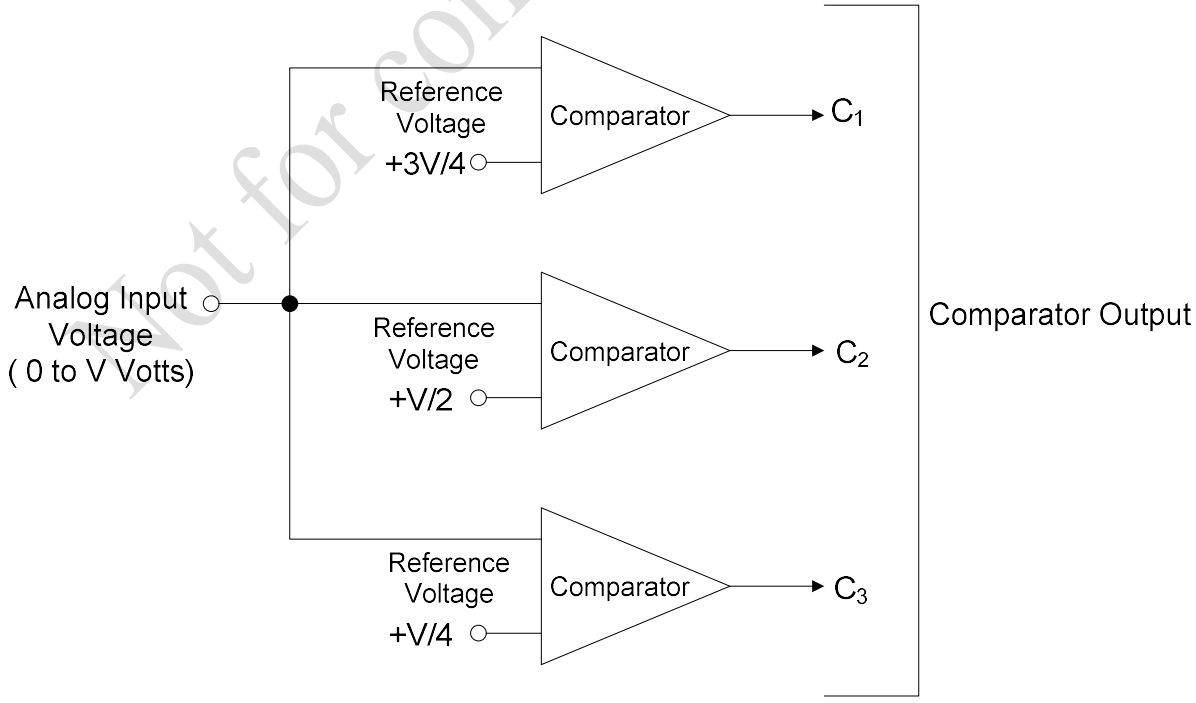
If the input $B_3B_2B_1B_0$=1000 and if 0=0V and 1 =10V, then

$$V_A = V(\frac{1}{2}.B_3 + \frac{1}{4}.B_2 + \frac{1}{8}.B_1 + \frac{1}{16}.B_0) = 10(\frac{1}{2}.1 + \frac{1}{4}.0 + \frac{1}{8}.0 + \frac{1}{16}.0) = 5V$$

10(b) Explain 2 bit simultaneous A/D counter.

Answer:

Answer: Following is the logical diagram for 2-bit simultaneous A/D converter.



Following table shows the comparator output for input voltage ranges

Input Voltage	Comparator Output		
	C_3	C_2	C_1
0 to +V/4	Low	Low	Low
+V/4 to +V/2	Low	Low	High
+V/2 to +3V/4	Low	High	High
+3V/4 to V	High	High	High

The simultaneous method of A/D conversion using three comparators is shown in the above figure. The analog signal to be digitized serves as one of the inputs to each comparator. The second input is a standard reference voltage. The reference voltages used are +V/4, +V/2 and +3V/4. The system is then capable of accepting an analog input voltage between 0 and +V.

If the analog signal exceeds the reference voltage to any comparator, that comparator turns on. Now, if all the comparator are off, the analog input signal must be between 0 and +V/4. If C_1 is high and C_2 and C_3 are low, the input must be between +V/4 and +V/2. If C_1 and C_2 are high and C_3 is low, the input must be between +V/2 and +3V/4. If all the comparator outputs are high, the input signal must be between +3V/4 and +V.