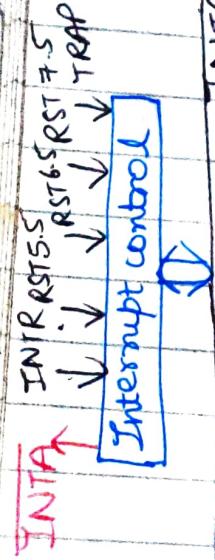


Pin Description / Layout

X ₁	1	40	VCC
X ₂	2	39	HOLD
Reset out	3	38	HLDA
SOD	4	37	Clock out
SID	5	36	Reset in
TRAP	6	35	Ready
RST7.5	7	34	I/O/M
RST6.5	8	33	SI
RST5.5	9	32	RD
INTR	10	31	WR
TINTA	11	30	ALE
ADO	12	29	SO
	13	28	A15
	14	27	
	15	26	
	16	25	
	17	24	1
	18	23	1
AD7	19	22	1
Cmd	20	21	AB

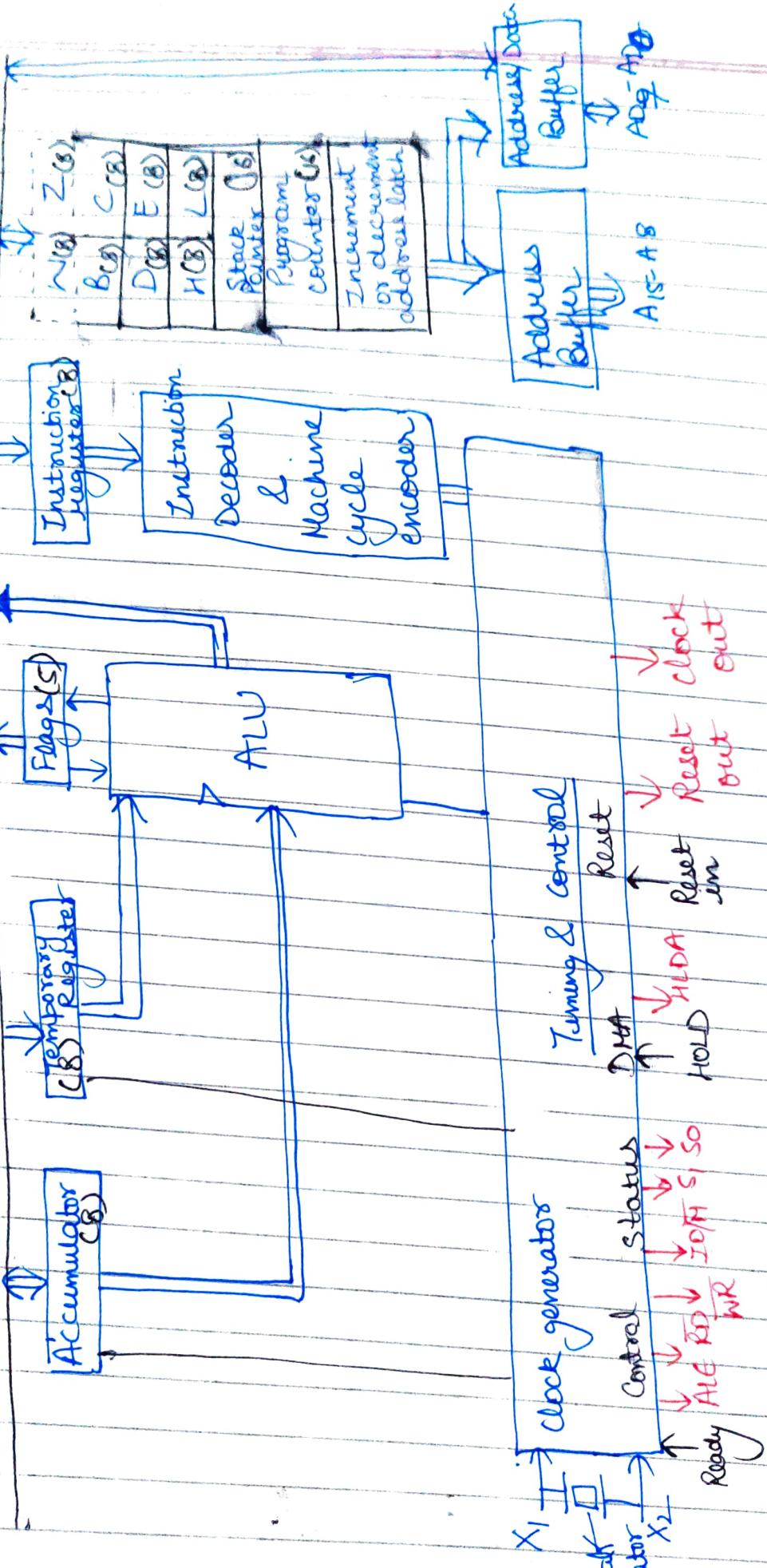
8085

8085 is an 8 bit processor, having 16 address lines, i.e. a memory of 64 KB can be connected. It operates with 3MHz clock, +5V dc supply. It is a 40 pin IC present in DIP Dual in line Package (same no. of pins on both the side).



↑ SOD
 Serial I/O control

INTERNAL DATA BUS



Internal Architecture of 8085

Internal architecture is divided into 5 functional units

- 1) Register unit
- 2) ALU
- 3) Timing & control unit.
- 4) Interrupt control unit
- 5) Serial I/O control unit.

1) Register Unit There are two types of registers:-

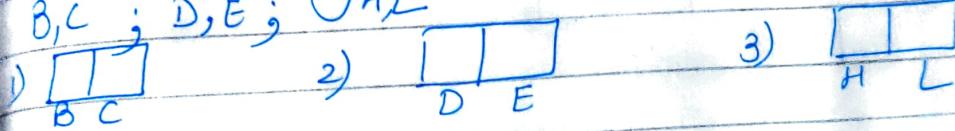
(a) General Purpose Register.

(b) Special Purpose Register

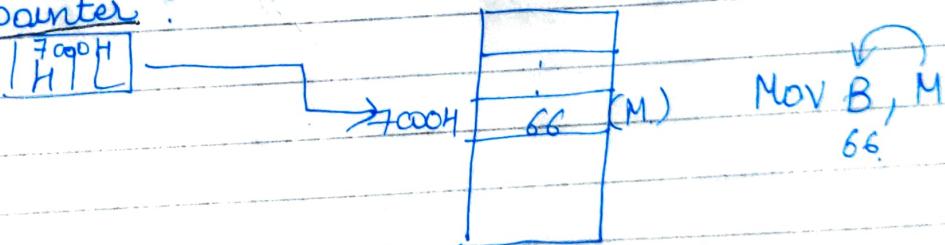
(GPR) General Purpose Register There are 68·8 bits GPR.
namely B, C, D, E, H, L.

There are 3 registers pairs of 16 bits length

B, C ; D, E ; H, L



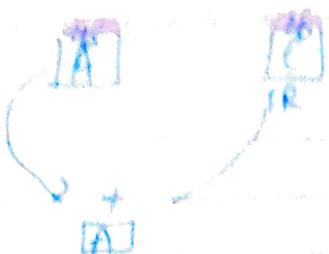
Any of the register pairs can be used to point the memory but HL register pair is considered to be Default memory pointer.



e.g. MOV B, M

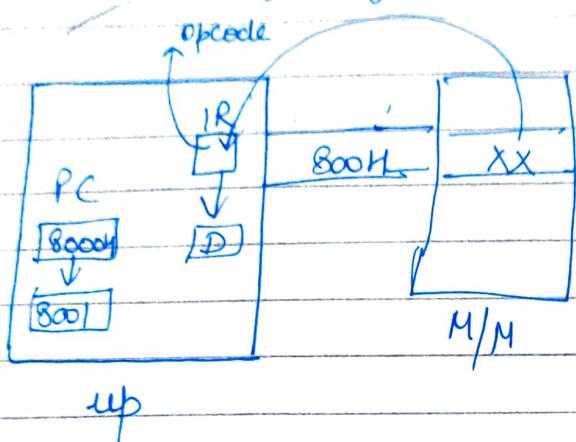
M → indicates memory content or register whose address is present in HL pair only.

Accumulator It is a multipurpose 8 bit register by which almost all arithmetic & logical operations are performed. One of the data bytes must be present in accumulator. Result is stored in accumulator.



Special Purpose Registers:

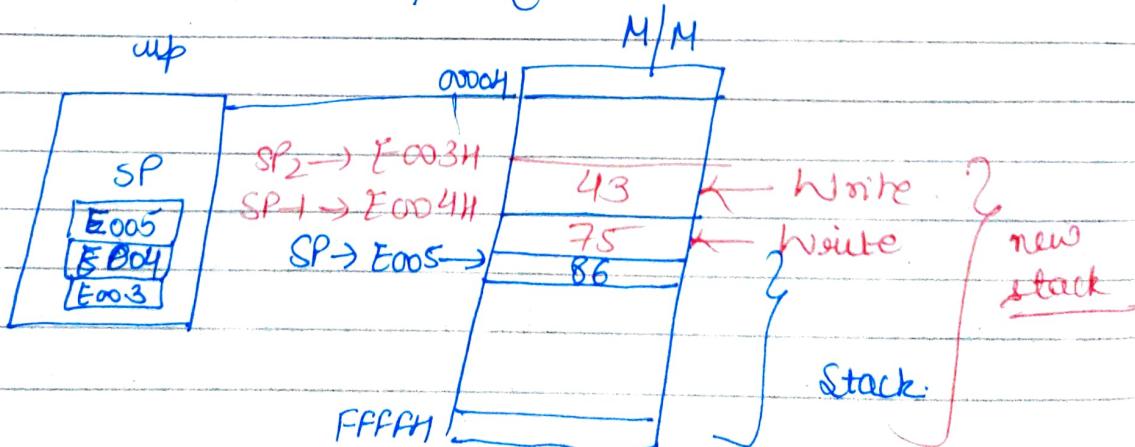
i) Program Counter (PC): It is a 16 bit register which contains the address of next instruction to be executed or it takes care of program flow.



ii) Instruction Register (IR)

It is an 8 bit register which contains opcode of present instruction.

iii) Stack Pointer (SP) It is a 16 bit register which points to top of the stack memory or it contains the address of data present at the top of the stack.



x In 8085, there

(PC, IR, SP) \rightarrow 1 Question in objective exams

Stack is a part of Read/Write memory.
" is to store temporary data
new value is stored at 1 decremented value of SP.

What is stack?

It is a part of Read Write memory which is used to store temporary data & also the content of program counter when subroutines are used.

Technique involved in stack is Last in first out (LIFO)

Note When data is stored in stack memory, stack pointer is decremented.

\Rightarrow When data is accessed from stack memory, stack pointer is incremented.

\Rightarrow In 8085, there is no provision to store a single byte temporarily in stack memory. A register pair can be stored $\frac{1}{2}$ doubt

Flag Register

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z	X	AC	X	P	X	CY

S \rightarrow sign flag

Z \rightarrow zero flag

AC \rightarrow Auxiliary carry flag.

P \rightarrow Parity

CY \rightarrow carry flag.

It is an 8 bit register. There are 5 flags which give the status of after an arithmetic & logic operation

As the result for most of the ALU operations is present in accumulator. Flags are modified or affected by the content of accumulator except for few instructions.

1) Sign Flag (S)

$S \rightarrow$ of according to D₇ bit of accumulators.

In signed operations, 0 indicates +ve result & 1 indicates negative result.

Q) Zero Flag

$Z \rightarrow 1$; if result in accumulator = 00H
 $\Rightarrow 0$; otherwise.

3) Auxiliary Carry

$AC \rightarrow 1$; if there is carry from D_4 & D_3 bit
or

Higher nibble. ← Lower nibble

$\rightarrow 0$; otherwise.

4) Parity Flag

5) Carry Flag

$CY \rightarrow 1$; if there is a carry i.e. out
 of D₇ bit
 $\rightarrow 0$; otherwise.

Note Zero flag may also be affected for general purpose Registers in some instructions.
e.g. increment or decrement operation

eg) Increment & decrement operation)

$$\begin{array}{r}
 97H \\
 + 89H \\
 \hline
 120H
 \end{array}
 \quad
 \begin{array}{l}
 \rightarrow A \\
 \rightarrow B
 \end{array}$$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	1	1	1
+ 1	0	0	0	0	1	0	1
<u>1</u>	0	0	1	0	0	0	0

CY 2 0

$$\left\{
 \begin{array}{ccccccccc}
 D_7 & D_6 & D_5 & D_4 & D_3 & D_2 & D_1 & D_0 \\
 S & Z & X & AC & X & P & X & CY \\
 0 & 0 & X & 1 & 0 & 0 & 0 & 1 \\
 \hline
 1 & & & & & & &
 \end{array}
 \right\}$$

$$PSW = \boxed{\begin{array}{|c|c|} \hline A & F \\ \hline 1 & 1 \\ \hline \end{array}} H$$

11 H. Ans
top F

$$\begin{array}{r}
 \begin{array}{r}
 C A H \\
 + 7 D \\
 \hline
 147
 \end{array}
 - A \\
 \hline
 0100 0111
 \end{array}
 \quad
 \begin{array}{r}
 - B \\
 \hline
 23
 \end{array}$$

$$\begin{array}{r}
 S Z X AC X P X C \\
 0 0 0 1 0 1 0 1 \\
 \hline
 1 \quad S \quad H
 \end{array}$$

$$\begin{array}{r}
 AC = \emptyset \\
 P = 1 \\
 C = 1
 \end{array}$$

$$PSW \boxed{47 \ 15} H$$

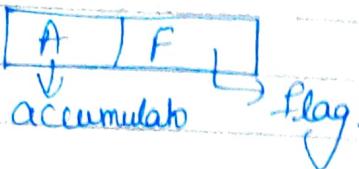
$$\begin{array}{r}
 \begin{array}{r}
 694 \\
 97H \\
 \hline
 100H
 \end{array}
 \quad
 \begin{array}{r}
 (01010101) \\
 S \quad S \quad H
 \end{array}
 \end{array}$$

$$\begin{array}{r}
 S = 0 \\
 Z = \emptyset \\
 AC = 1 \\
 P = 1 \\
 C = 1
 \end{array}$$

$$PSW \boxed{100111} H$$

P 8

PSW (Program Or Processor Status Word)



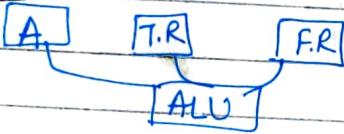
It is not a separate register. It is the combined status of Accumulator & flag register together where accumulator is higher byte.

Temporary Register

W & Z are the two 8 bit temporary registers which are not accessible by the user. They are used by processor in some instructions.

(W, Z, Flag register are not used by programmer)

ALU



It is a combination of accumulator, temporary Register, flag register & arithmetic & logic circuits.

Arithmetic operation

- 1) Addition, 2) Subtraction, 3) Increment, 4) Decrement

Logical operations

- 1) AND, 2) OR, 3) Ex-OR, 4) Complement, 5) Compare,
6) Rotate

Note

There are no separate instruction for multiplication & division in 8085.

Flags are affected or modified for ALU operations only.

Instruction Decoder & Machine Cycle encoder

After the opcode is fetched into instruction register it is decoded in this block with the help of microprogram. The no. of operations or machine are assigned according to type of instructions.

Microprogram, It is a program written by chip designer to make the processor understand what an instruction is or it indicates the type of operation to be performed for an instruction.

Timing & Control Unit

It is responsible for generating various control & status signals required for the operation of the processor.

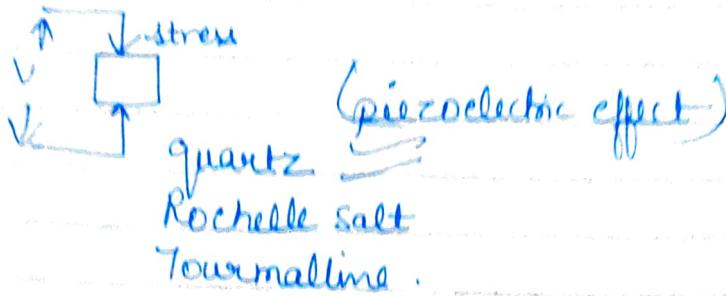
RC & LC oscillations are temperature dependent but crystal oscillators are not temp. dependent & generate stable oscillations

externally crystal oscillator is connected to up to

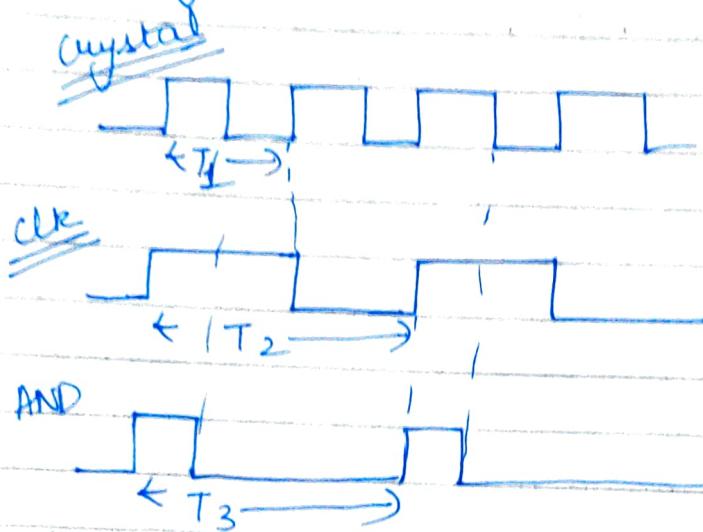
X_1, X_2 A crystal oscillator is connected b/w X_1 & X_2 to provide reference clock for the processor. Crystal oscillator is used as it is more stable compare to RC & LC oscillators. In A built in clock generator in processor, takes the reference clock frequency & produces operating frequencies which is half of crystal frequency. It generates other frequencies required for internal operations of the processor. The operating frequency of 8085 is 3MHz

FCR = Frequency

It may range between 3 to 6 MHz.



(Every crystal to oscillator has a one resonant frequency.)



So up will generate internal frequencies in Δ/ω crystal & clock frequency.

Address Latch Enable (ALE)

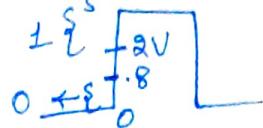
Control signals

ALE \rightarrow ; All 16 lines are address Bus

\rightarrow O ; higher bits ($AD_{15} - AD_8$) \rightarrow address bus
lower bits ($AD_7 - AD_0$) \rightarrow Data bus.

\overline{RD} \rightarrow Read control signal.
 \rightarrow O ; Active

\overline{WR} \rightarrow Write control signal
 \rightarrow O ; Active



RD & WR operations are regularly done, therefore these signals are active low (0-0.8V is easy to generate)

(.9-2V is not allowed) + High impedance state (no current drawn)
↑ ambiguity or confusion.

I/O/M : I/O / M status lines which indicates either memory or I/O operation.

I/O/M → 0 ; M/M operation,
1 ; I/O " .

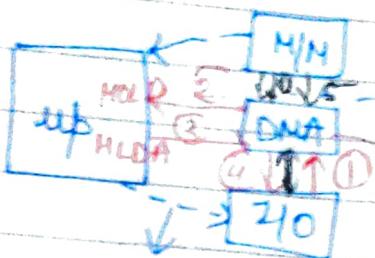
S₁, S₀ These are status lines which give the status of bus for an cycle of operation.

<u>I/O/M</u>	<u>RD</u>	<u>WR</u>	<u>Control signal</u>	<u>Operation</u>	only from memory ✓
0	0	1	MEMR	M/M read / fetch.	
0	1	0	MEMW	M/M write	
1	0	1	IOR	I/O Read	
1	1	0	IOW	I/O Write	

<u>I/O/M</u>	<u>S₁</u>	<u>S₀</u>	<u>Status</u>
z	0	0	Halt
0	0	1	M/M write
0	1	0	M/M Read
0	1	1	opcode fetch
1	0	1	I/O Write
1	1	0	I/O Read
1	1	1	INTA
→x z	0	0	Halt
z	x	x	HOLD
z	x	x	RESET

HOLD & HLDA

→ Conventional (DMA)



1 byte
DMA To transfer data to
operation I/O we need 200 instruction
200 bytes → 200 Instruction

Regular Path:

ask for control of buses from up
by HOLD, up will send HLDA to DMA
& then DMA will send a signal to
I/O so that it will get ready to
receive data HOLD

Y ← hold signal
will be low

by DMA, when whole
data is transmitted
so that up again
regain the control of buses.

When more or huge data is to be transferred b/w
memory & i/o, direct memory access is used with
the help of DMA controller at a faster rate.

⇒ HOLD → High active input signal to the processor
from DMA controller requesting the buses for DMA
operation.

⇒ A Processor completes the current machine after
receiving HOLD request & responds with HOLD
acknowledgement (HLDA). After this state, the control
of buses is given to DMA controller i.e. it
relinquishes the buses to DMA controller.

⇒ After the completion of Data Transfer HOLD signal
is pulled down by DMA controller & it relinquishes
the buses to processor. This operation is known as
Direct Memory access (DMA)

HOLD High active output signal in response to HOLD request.

Modes of DMA operation

1) Burst Mode

2) Cycle Stealing technique or Shoot Burst Mode

Burst Mode The HOLD signal remains high unless & until data is completely transferred b/w memory & I/O. Therefore, the processor has more interference. e.g. accessing data from hard disk.

Best

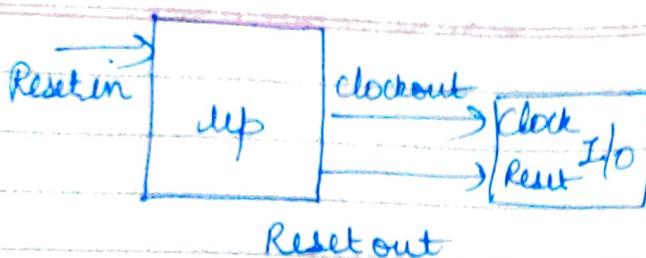
Cycle Stealing Technique The total data that has to be transferred is divided into blocks. Blocks are transferred in a sequence of interval of time. The time of processor is efficiently used as it is interrupted only when there is data transfer. Interference is less.

Reset in Low active input signal used to ~~reset~~ reset the process.

When process is reset, PC is initialized to 0000H.

Reset-out Output signal which indicates processor is reset. It can be used to reset I/O device.

Clock out output pin on which the same operating frequency of the processor is available. It can be connected to I/O to have synchronous ~~comme~~ operation.



Ready High active input signal to the processor from slow speed peripheral device. If ready is high then only processor will either transmit data to or receive data from I/O device.

Interrupt Control Unit

There are 5 hardware interrupts in 8085 according to priority TRAP, INTR, RST 7.5, RST 6.5, RST 5.5
TRAP → highest Priority

INTR → Lowest Priority

INTA Interrupt acknowledgement → Low active output signal in response to INTR.

Serial I/O control Unit It is used for serial communication between processor & I/O devices. bit by bit transmission.

	<u>Serial</u>	<u>Parallel</u>
Speed	Low	High
Distance	Long	Short
Complexity	More complex	Less complex.
Cost		

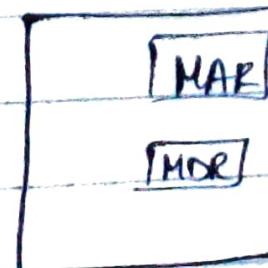
SID Serial Input Data : Input pin ~~to~~ through which processor receives serial data.

SOD → Serial output Data

Output pin by which ~~by which~~ processor transmits serial data

Note: Both SID & SOD are internally connected to D₇ bit of accumulator.

Address/Data Buffer



Memory address register
Memory data register.

address will move from address bus to MAR