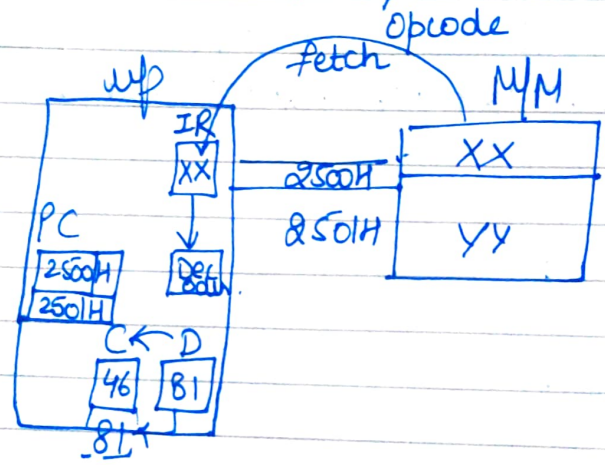
① Data Transfer / Copy Inst.

	Length of Inst	No. of M/C	T states
① MOV Rd, Rs	1 Bytes	1	4

More/Transfer/copy the content of source register to destination register. ← Register addressing mode.

② eg. 2500H : MOV C, D

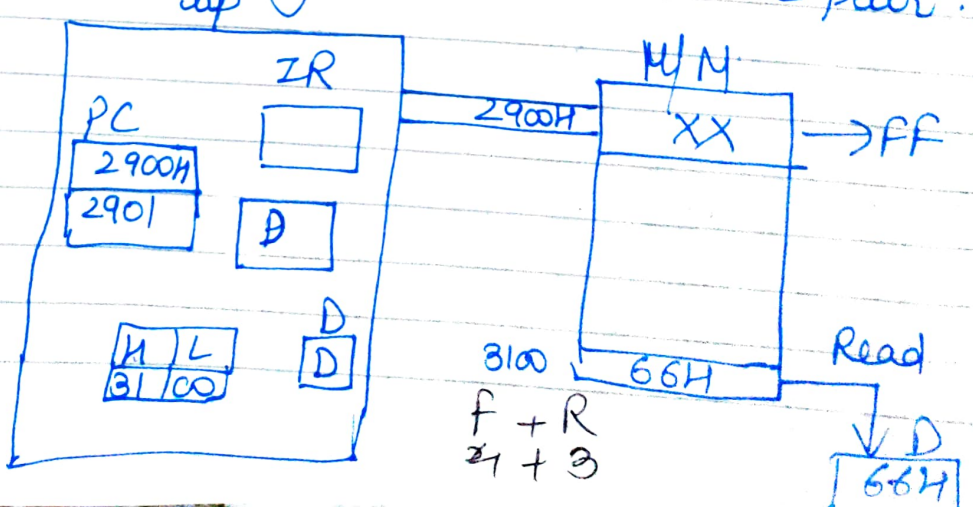


Name of m/c cycle → fetch.

③ MOV R, M → 1 Byte, 2, 7 (HL Pair) Indirect addressing mode

eg. 2900H : MOV D, M

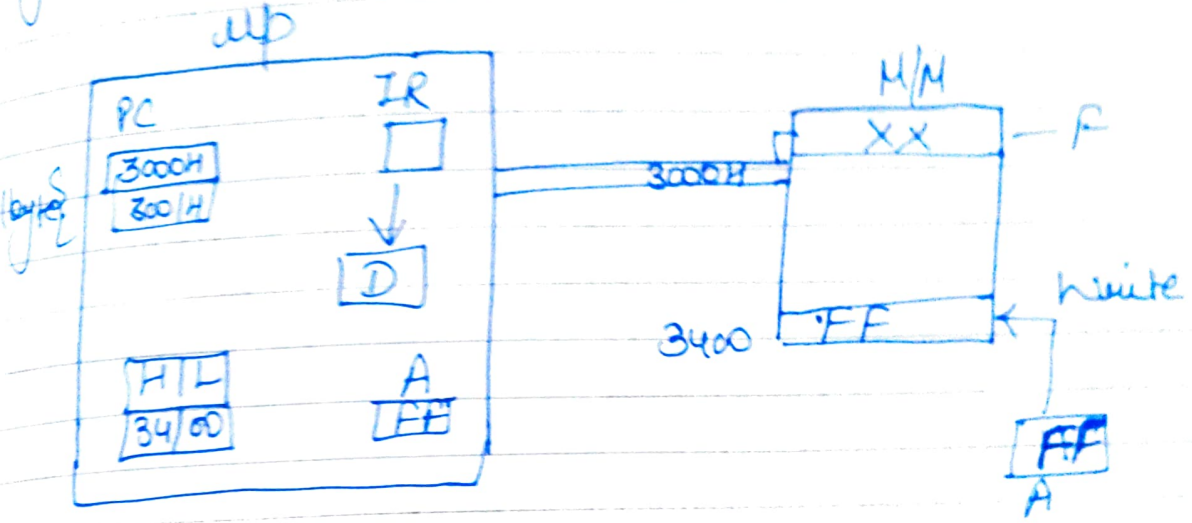
More the content of memory to register whose memory address is in HL pair.



③ MOV M, R — 1 Bytes, 8, 7 (Indirect Addressing Mode)

Move the content of Register to Memory.

eg. 3000H : MOV M, A

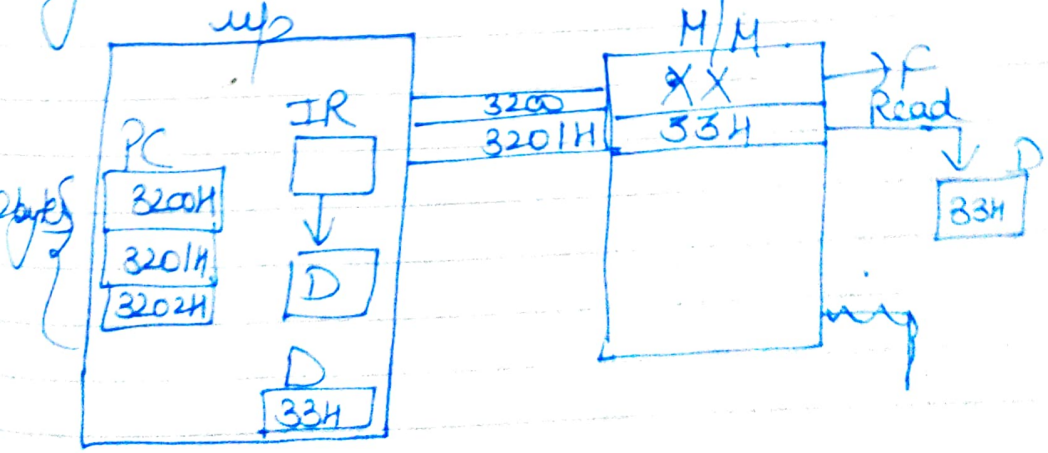


Fetch + Write
4 + 3 = 7 States

④ MVI, R, 8 bit data — 2B, 2, 7 (Immediate AM)

Move immediate 8 bit data to register

eg. 3200H : MVI D, 33H



1 byte → PC will take care, then HL pair eg ②, ③
2 byte → PC will take care ④.

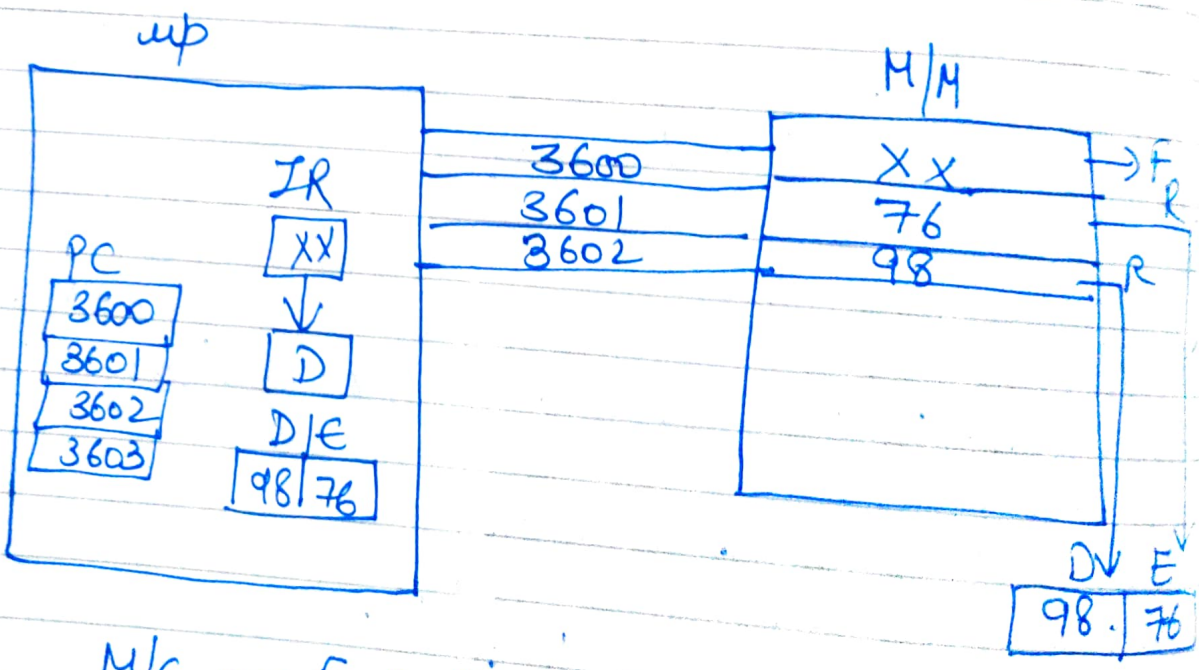
⑤ LXI RP, 16 bit value. — 3 Byte, 3 M/C, 10T.

Load immediate 16 bit value into Register pair.

LXI B, ____
LXI D, ____
LXI H, ____
LXI SP, ____.

3600H:

eg ∧ LXI D, 9876H

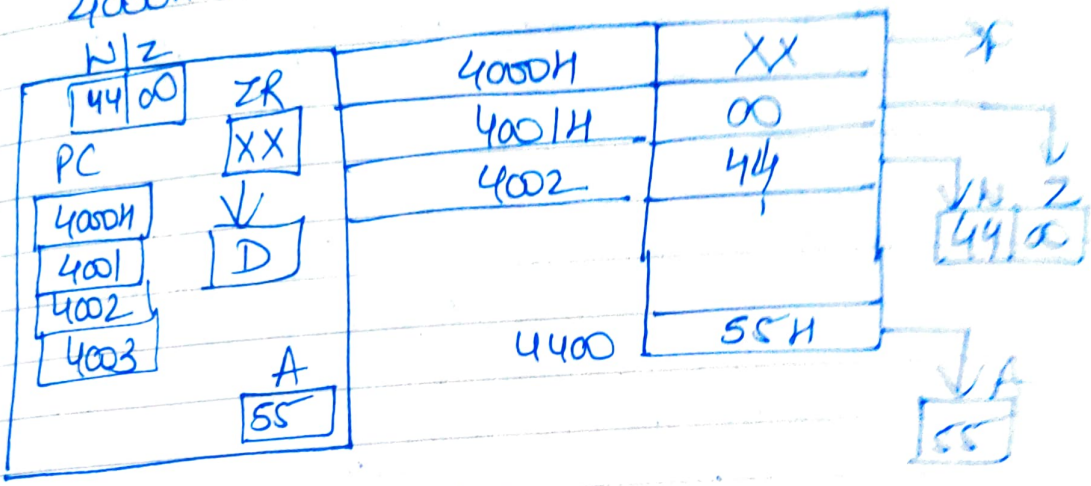


M/C — F, R, R → 3
Tstates 4+3+3 = 10 Tstates.

ALE	$\overline{RD}$	$\overline{WR}$	
3	3	0	→ activated

⑥ LDA 16 bit address → 3B, 4, 13
Load accumulator with data present at 16 bit address

eg. 4000H : LDA 4400 H

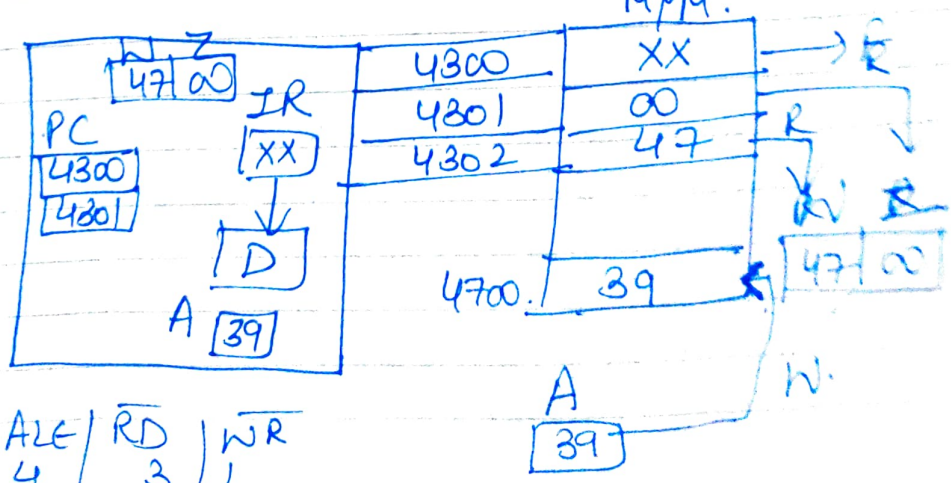


W|Z
After 4002, Address in W|z pair will loaded on address bus.

⑦ STA 16 bit Address — 3B, 4, 13
(Direct addressing mode)

Store the content of accumulator at 16 bit address.

eg. 4300H: STA 4700H if A = 39



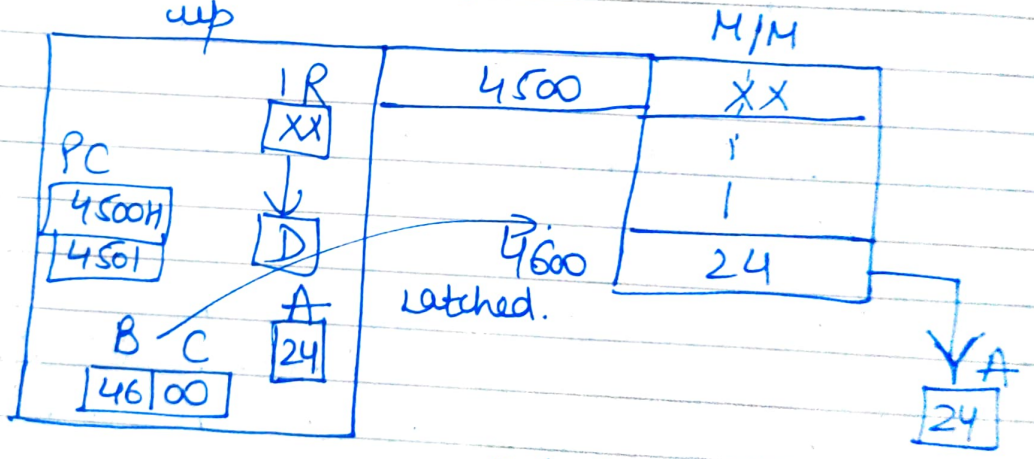
8) LDAX Rp (RP) — 1 Byte, 2, 7 (Indirect AM)

Load Accumulator with the data whose address is present in register pair.

X in an instruction indicates that operation is performed on a register pair.

LDA X B
LDA X D
X LDAX H ⇒ MOV A, M (HL)

eg. 4500H: LDAX B



F & R
4 3 → 7 T states

9) STAX Rp — 1Byte, 2, 7

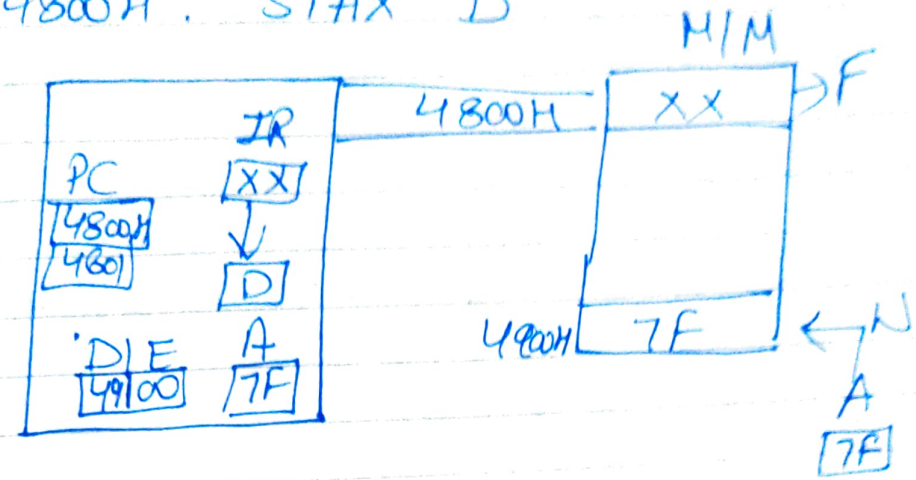
Store the content of Accumulator at the address present in Register pair

eg STA X B
STA X D
X STAX H — MOV M, A

BC
DE
HL → Memory

LDAX RP
STAX RP
MOV M, R
MOV R, M

eg. 4800H : STAX D



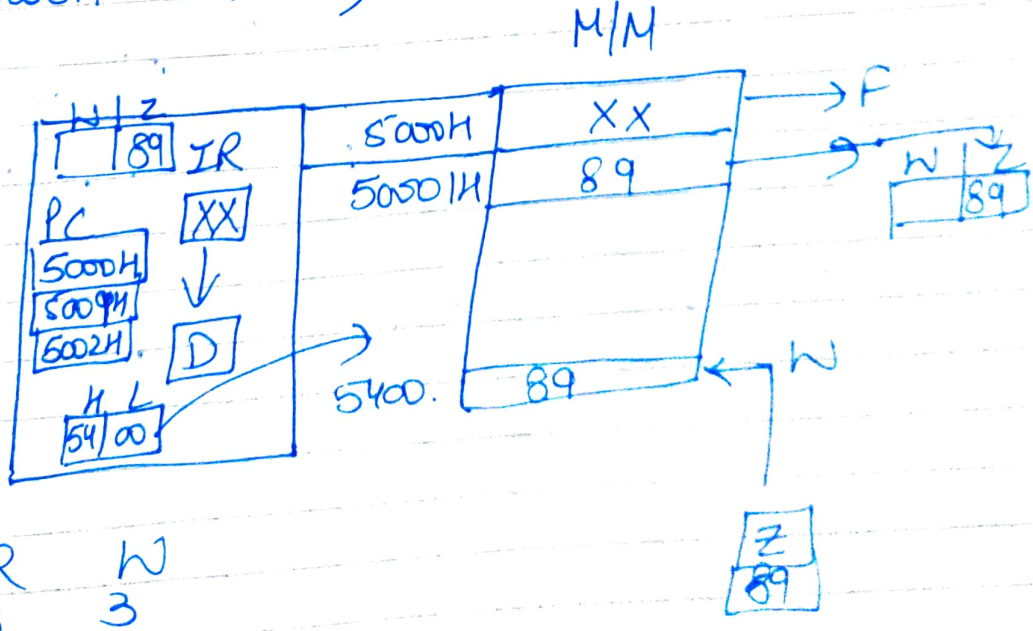
Indirect addressing mode.

1) MVI, M, 8 bit data → 2 Bytes, 3, 10

Move immediate 8 bit data to memory.

F, R, W.

eg 5000H MVI M, 89H.



F R W
4 3 3

10 T states.

Stack operations

1) PUSH Rp 1B, 3, 12

Store or push the contents of Registers pair on to stack memory

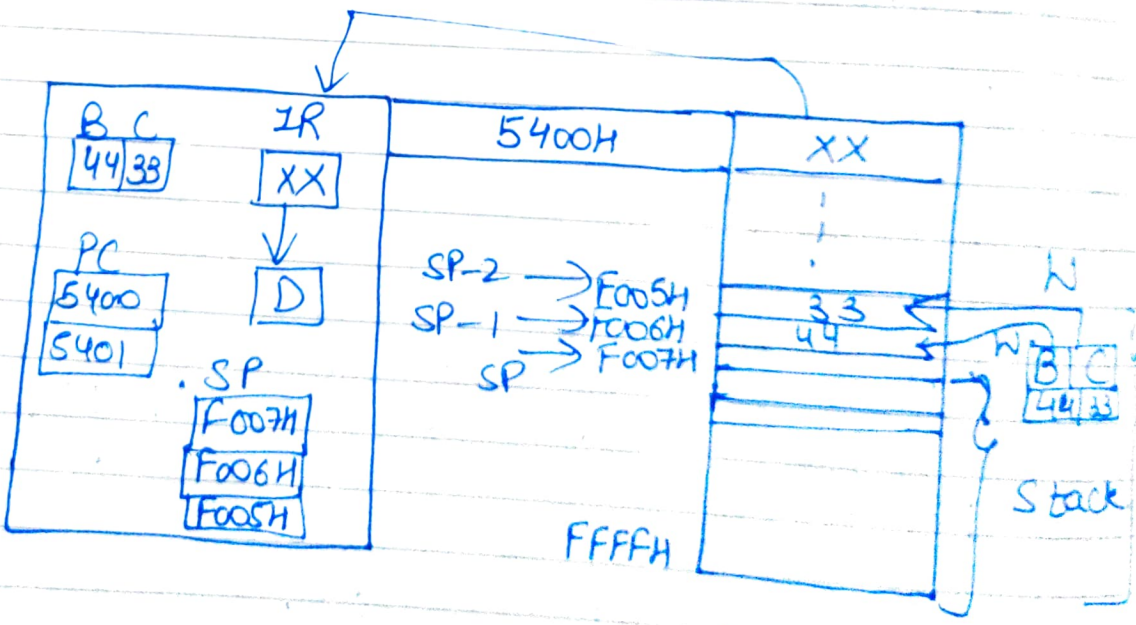
SP → SP-2

Stack Pointer is decremented by two. or stack grows down.

PUSH B
PUSH D
PUSH H
PUSH PSW

PSW | A | F |

eg: 5400H: PUSH B

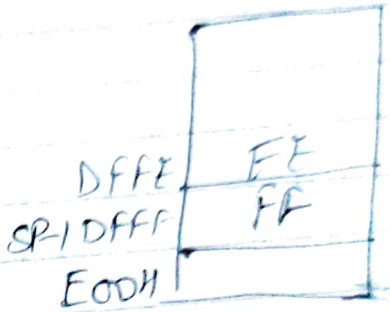


F W W
6 3 3

12 T states.

To decrement the Stack pointer by 1 we need 2 T states.

SP → E000H
BC → FFEEH
After PUSH B
SP → = DFFE
Dat @ Top of Stack. = EE



FF10H
E000
- 2
DFFE

R. 10
2
FE

E000
+ FE
DFFE

SP → SP-2 = DFFE = EE.

POP instruction

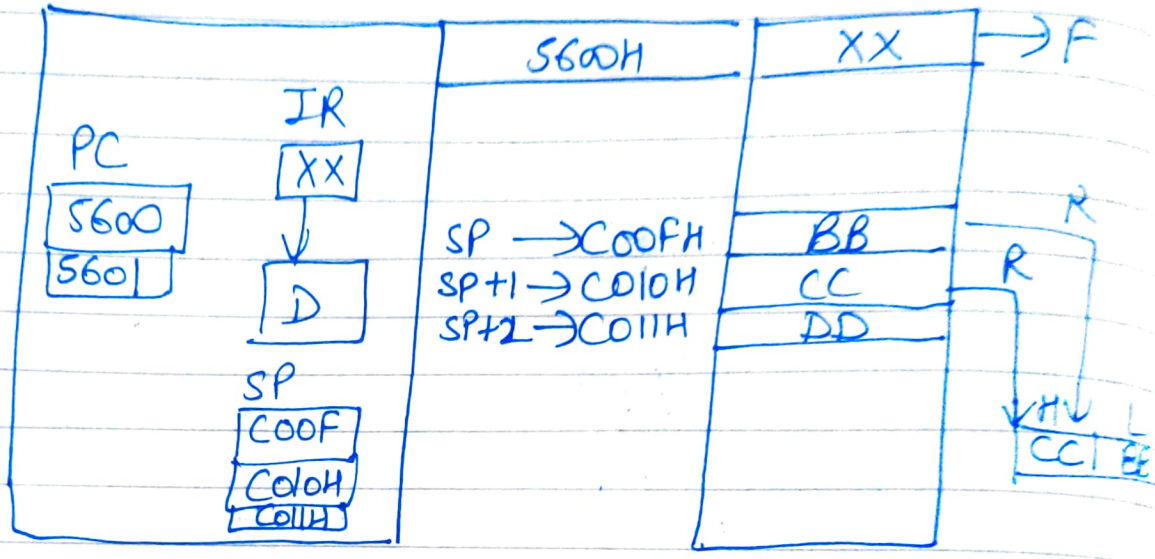
POP Rp → 1 byte, 3 byte., 10

SP → SP+2
Read or access data present at top of the stack memory. pointed by SP into register pair.

SP → SP+2
Stack Pointer is incremented by two. or Stack goes up.

- POP B
- POP D
- POP H
- POP PSW

eg. 5600 : POP H

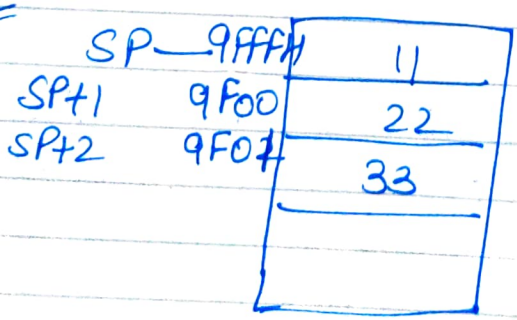


SP is at C011H
Data DD.

F R R
4 3 3
10 T states.

C00FH C010H content doesn't not change.

Q



POP D

SP — ? 9F01

Dat @ Top of stack. = 33
Data.

~~9F00~~ - ~~SP~~. [9F00 + 1] = ~~FF00~~ 22.

Nay(?) ...

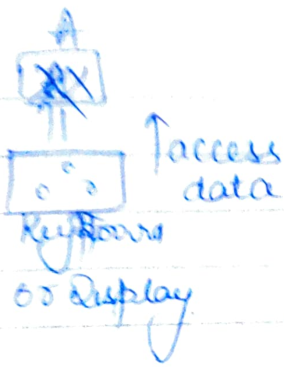
IN 8 bit Port Address → 2B, 8, 10

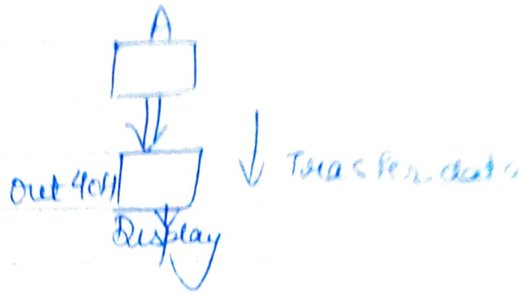
Read or access data from 8 bit port address into accumulator.

$2^8 = 256$, 8 bit → 256 address
(The Port can act as Input & output)

00000000
- 00H — IN 00H } 256 i/p — Out 00H }
- FFH — IN FFH } — out FFH } 256 o/p

IN 30H



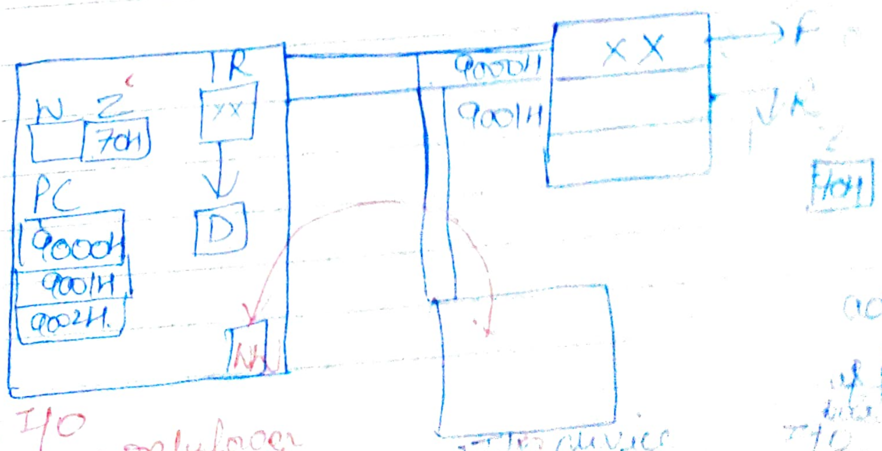


Port indicates the connection of I/o device as I/o given 8 bit port address, there can be 256 input devices & 256 output devices.

The processor identifies an I/o device in two types

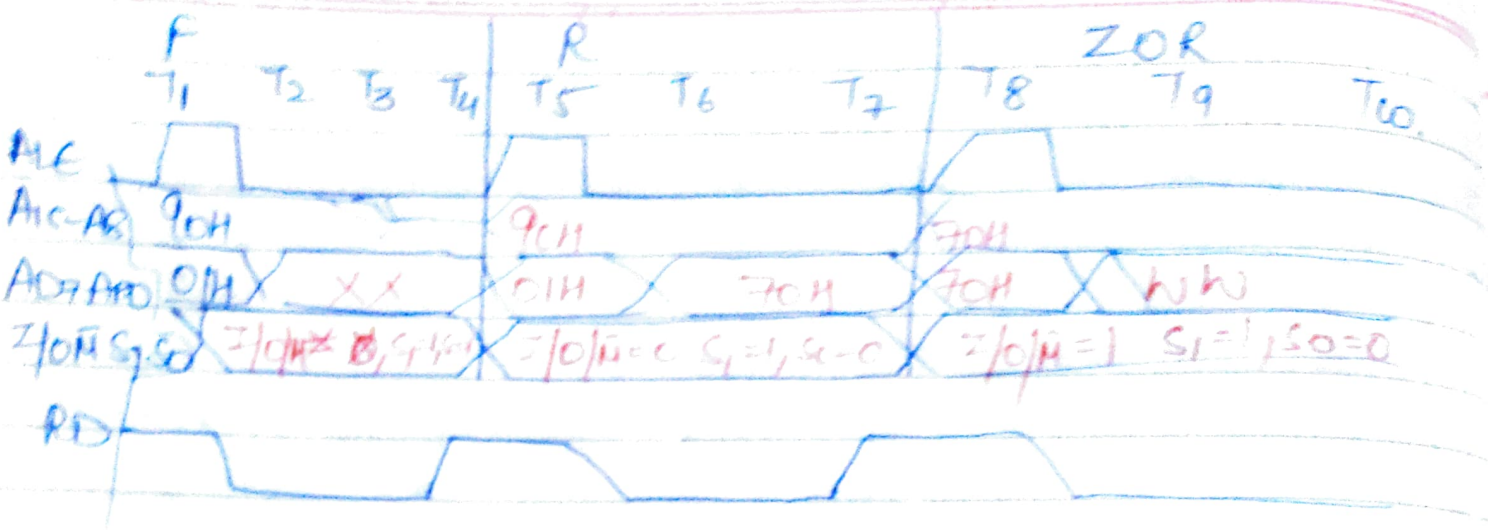
1] I/o mapped I/o → I/o has 8 bit port address
2] Memory mapped I/o → I/o has 16 bit address (64KB) (2^{16} 64KB)

Ex: IN 70H



But for I/O Data bus is only used once.

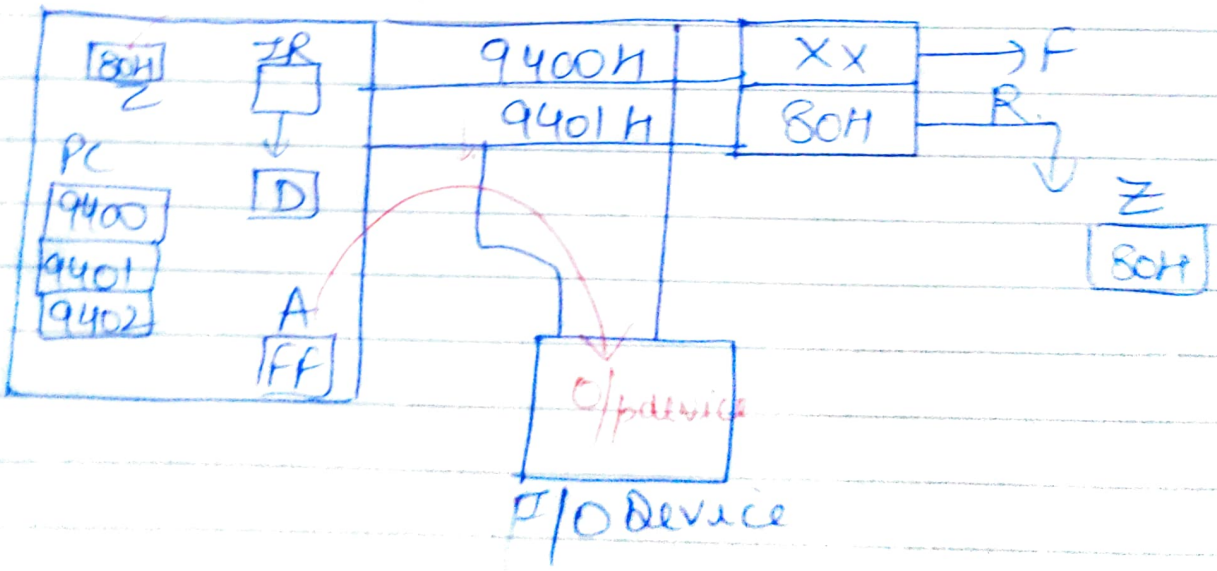
address of i/p 70H is placed on address bus of memory of I/O



Out 8 bit port address → 8B, 3, 10

Transfer the content of accumulator to 8 bit port address

eg 9400H Out 80H



F R IOW
4 3 3 → 10T states.

Conventional

Q Draw the timing diagram for the above instruction (Out 80H). Considering an operating frequency of 5MHz. (20 Marks)