DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

2x2 DRAM ARRAY USING 3T-1D CELL

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ABSTRACT

- To build a 2x2 array of memory using 3T-1D cell.
- Peripherals include precharge circuit , decoder.
- Read and write operation are performed.
- Designed and simulated using LTSpice.

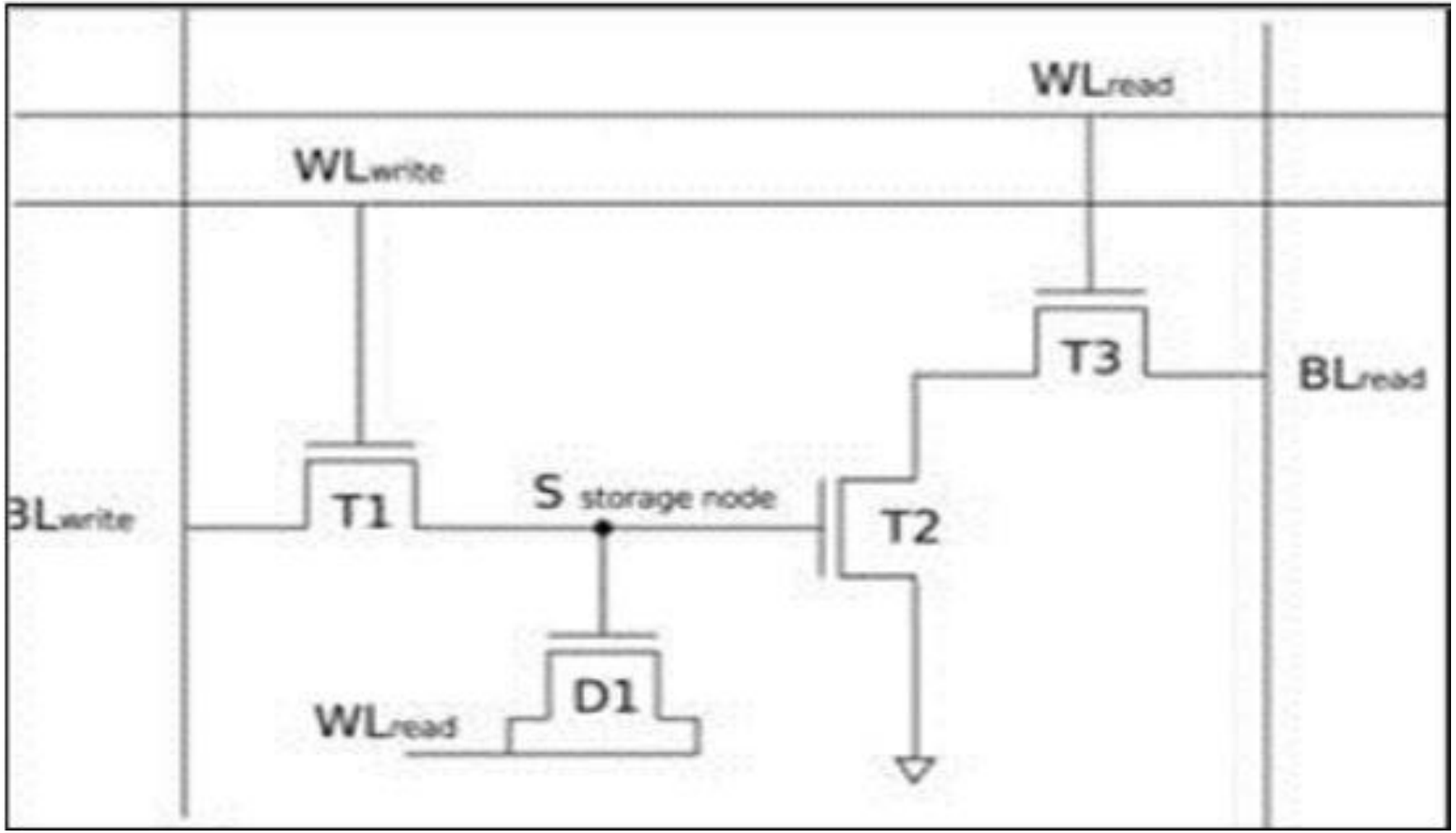
INTRODUCTION

- derived form of 3T cell.
- uses the gated diode instead of capacitor to store the data value.
- which has a comparatively less read and write access time compared to 1T1C
- fewer number of transistors (similar to DRAM) with longer data retention

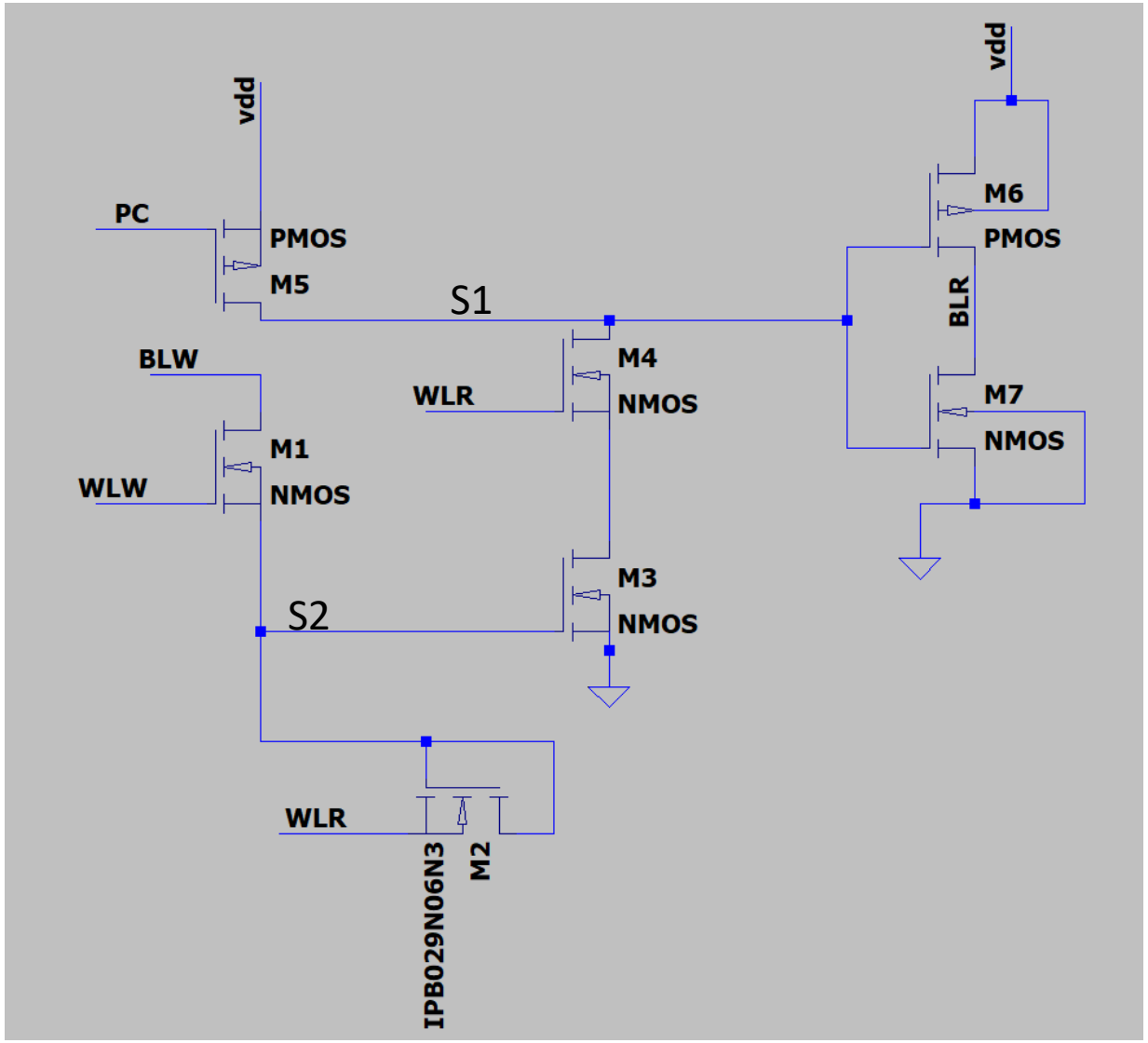
ADVANTAGES

- It possess the feature of greater resistivity towards process variations which can be an advantage over SRAMs
- Another advantage over SRAMs is it **does not slows down** by scaling it down.
- It allows non-destructive read operation which is an advantage over DRAM but still has a working nature similar to DRAM.
- Power consumption is greatly reduced as it uses diode instead of capacitors to store the data

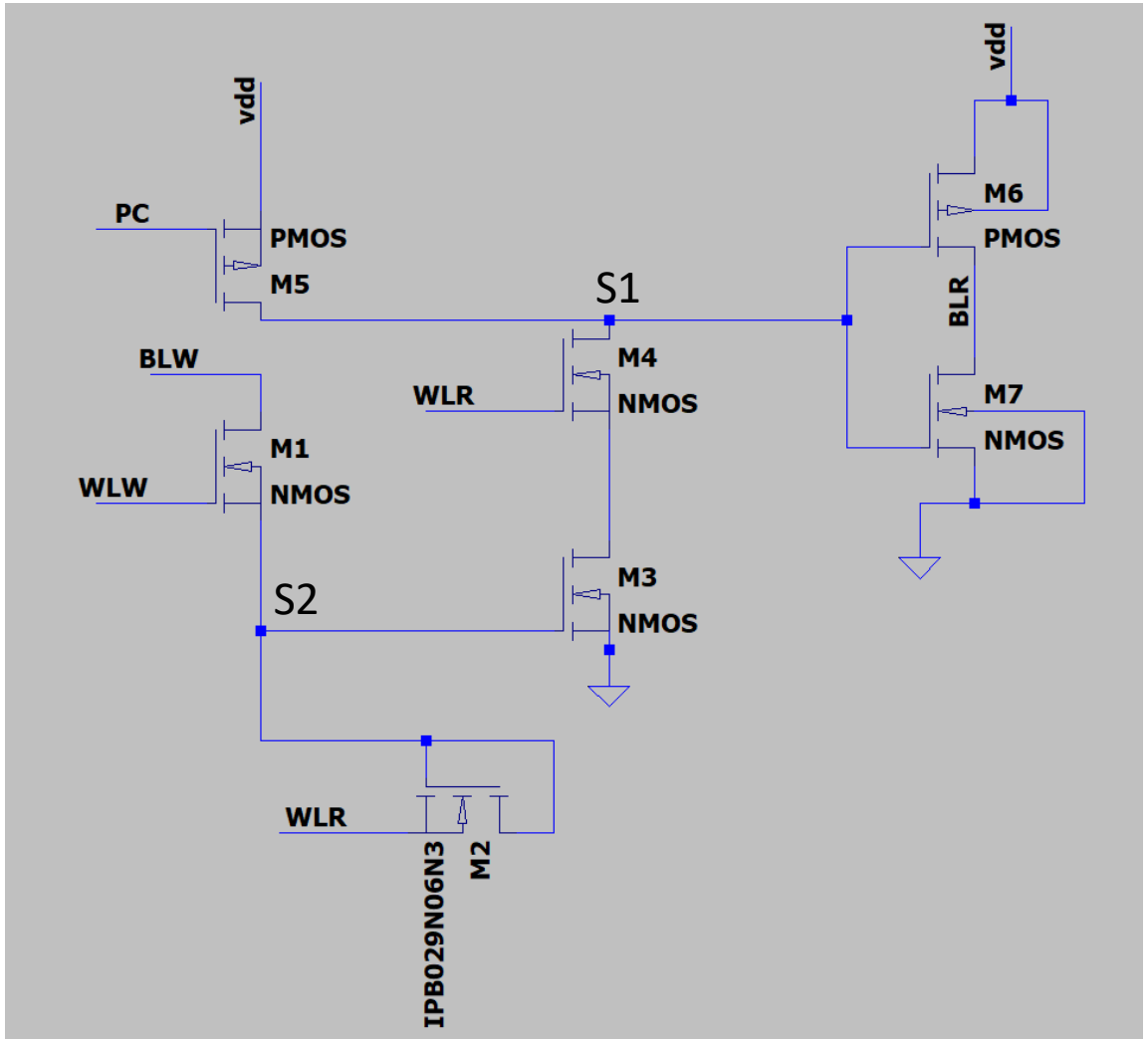
CIRCUIT DIAGRAM OF SINGLE 3T-1D CELL



SINGLE CELL CIRCUIT

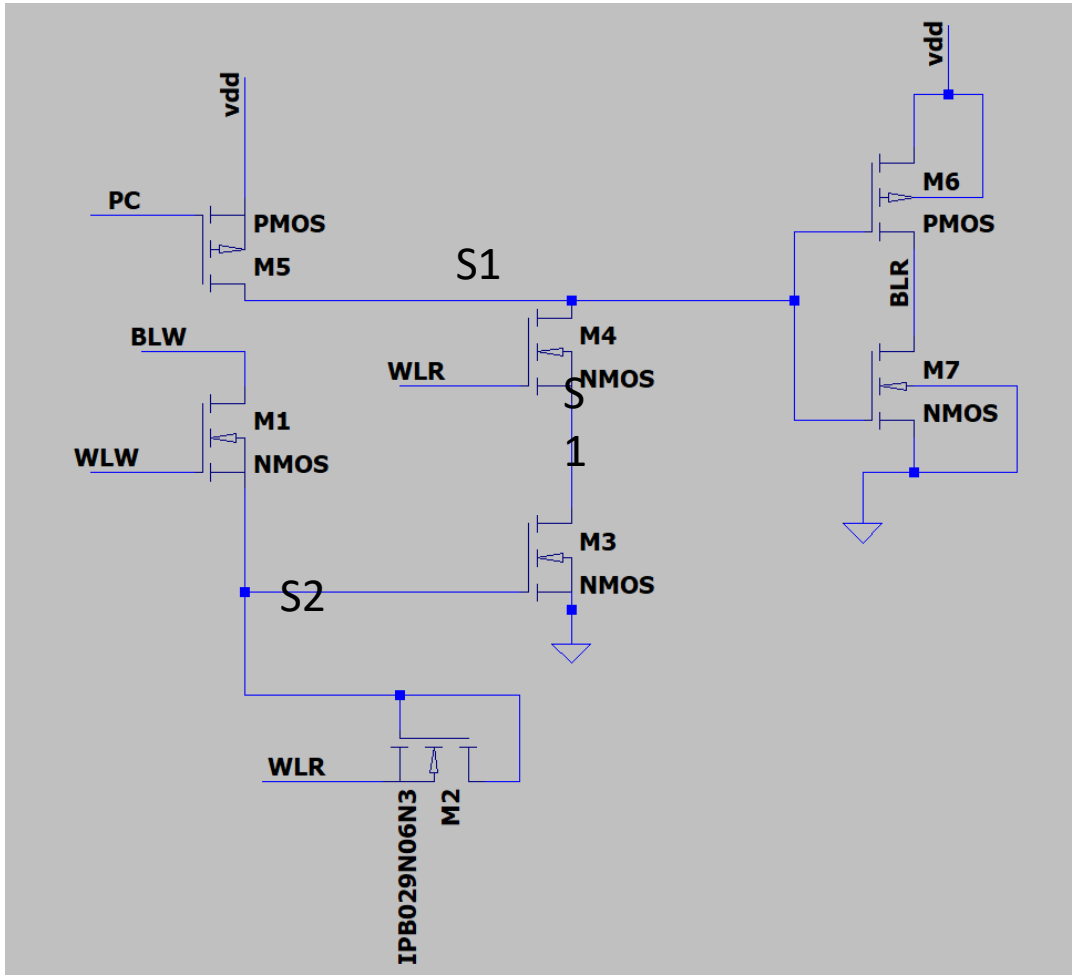


SINGLE CELL CIRCUIT WORKING : WRITE OPERATION

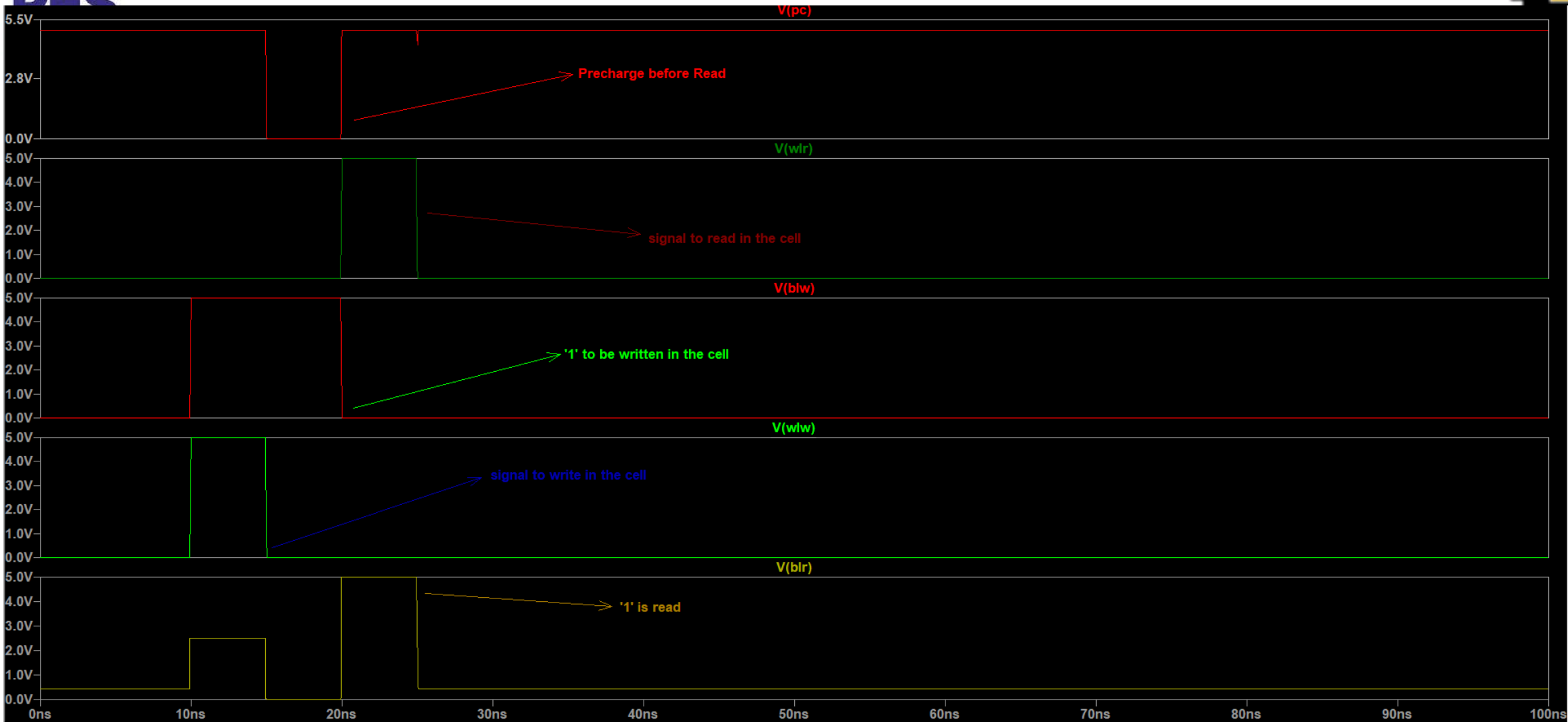


- In order to write the cell at the BL write line level it is only required to activate M1 through the WL write line.
- Hence, the S2 node stores either a 0 or a 1 depending on the logic value.
- This voltage results in the accumulation of charge at the gate of devices M2 and M3.
- This way the write operation is done by charging the values at M2, which then can be used for read operation.

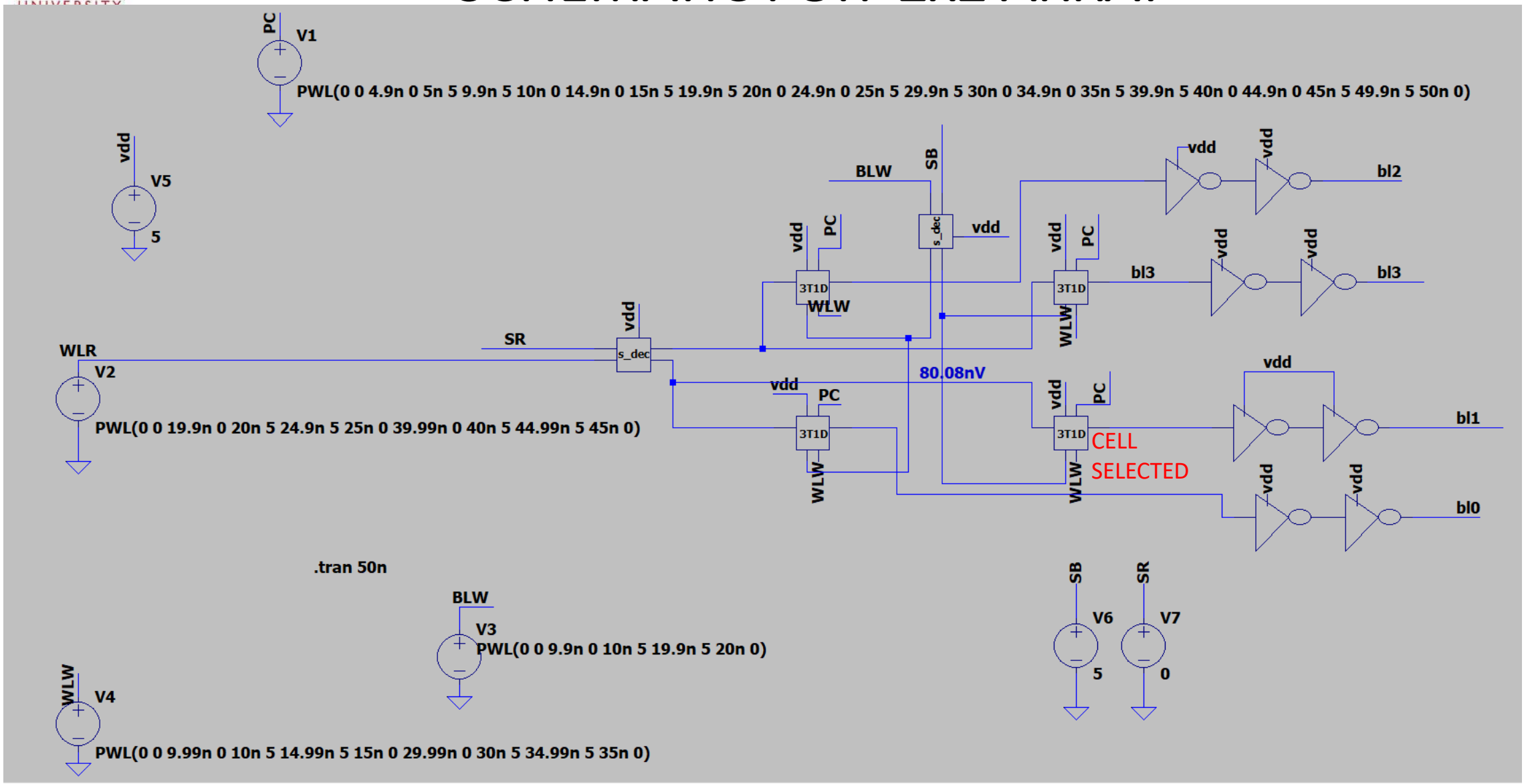
WORKING : READ OPERATION

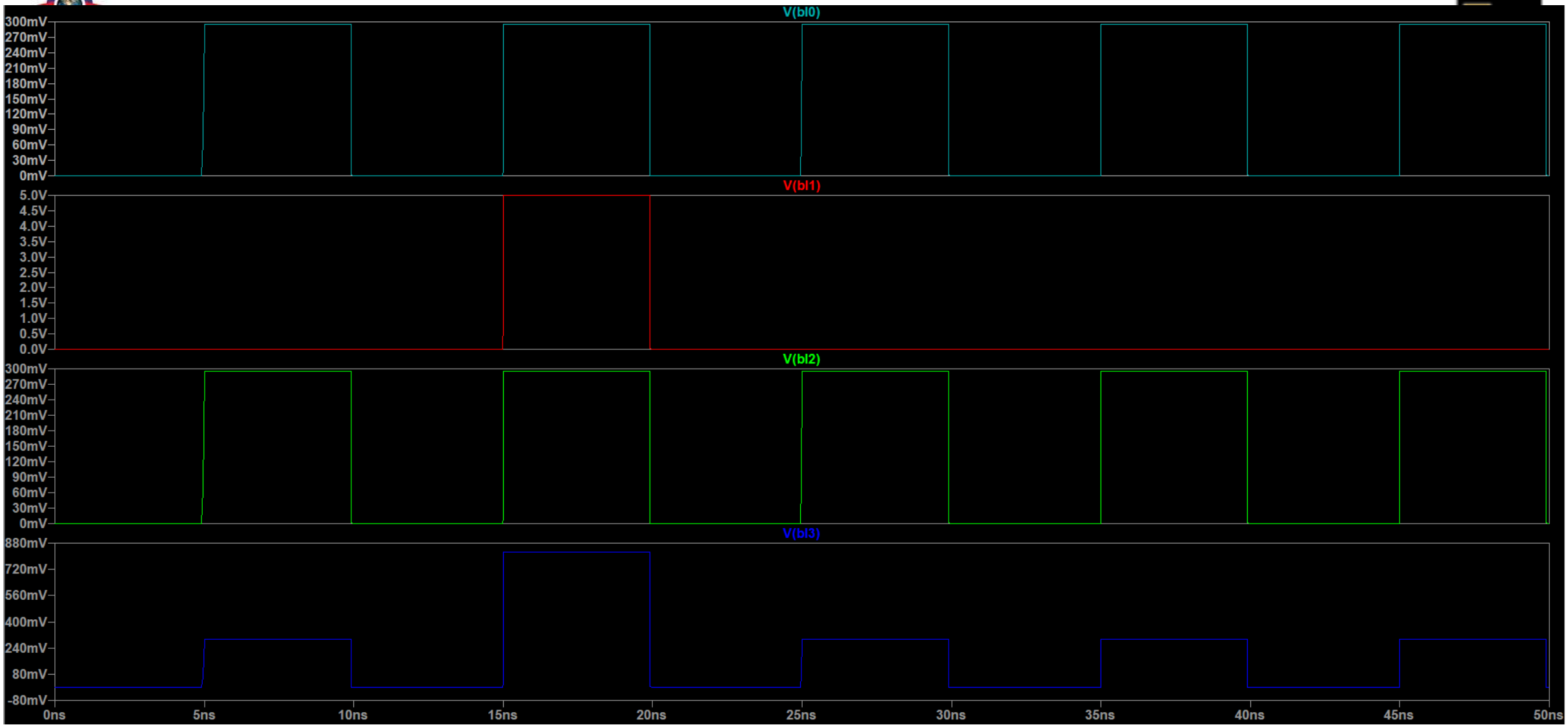


- In order to read the cell, the read bit line BL read has to be previously pre-charged at VDD level. Then M4 is activated from WL read line.
- If 1 is stored in S2, transistor M3 turns on and discharges the bit line. And an inverter is used to get 1 as output, Indicating that data 1 is read.
- If 0 is stored in S2, transistor M3 does not reach enough conduction level does not discharge the bit line.And an inverter is used to get 1 as output,Indicating that data 0 is stored.


V(pc)
5.5V
2.8V
0.0V
Precharge before Read
V(wlr)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
signal to read in the cell
V(blw)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
'1' to be written in the cell
V(wlw)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
signal to write in the cell
V(blr)
5.0V
4.0V
3.0V
2.0V
1.0V
0.0V
'1' is read
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

SCHEMATIC FOR 2x2 ARRAY




V(bl0)
300mV
270mV
240mV
210mV
180mV
150mV
120mV
90mV
60mV
30mV
0mV
V(bl1)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
V(bl2)
300mV
270mV
240mV
210mV
180mV
150mV
120mV
90mV
60mV
30mV
0mV
V(bl3)
880mV
720mV
560mV
400mV
240mV
80mV
-80mV
0ns
5ns
10ns
15ns
20ns
25ns
30ns
35ns
40ns
45ns
50ns

CONCLUSION

- We have tried to implement design a 3T-1D cell, which has a **comparatively less** read and write access time & POWER CONSUMPTION compared to the traditional 1T-1C DRAM and also reduce the number of transistors per bit when compared to 6T SRAM cell.
- The discussed new model has tried to manage the tradeoff between the access time and the area consumed per bit.

REFERENCES

Asthana, Prateek & Karyakarte, Sangeeta. (2014). Design and Implementation of 4T, 3T and 3T1D DRAM Cell Design on 32 NM Technology. International Journal of VLSI Design & Communication Systems. 5. 47-64. 10.5121/vlsic.2014.5404.

“Analysis of Different Parameters of DRAM cell n type and p type Gated Diode in VLSI Technology”, Prof. Y N Thakare and et.al

Contributions

- Amogh Inamdar- Design and Simulation
- Abhay Naik- Power point Presentation

THANK YOU