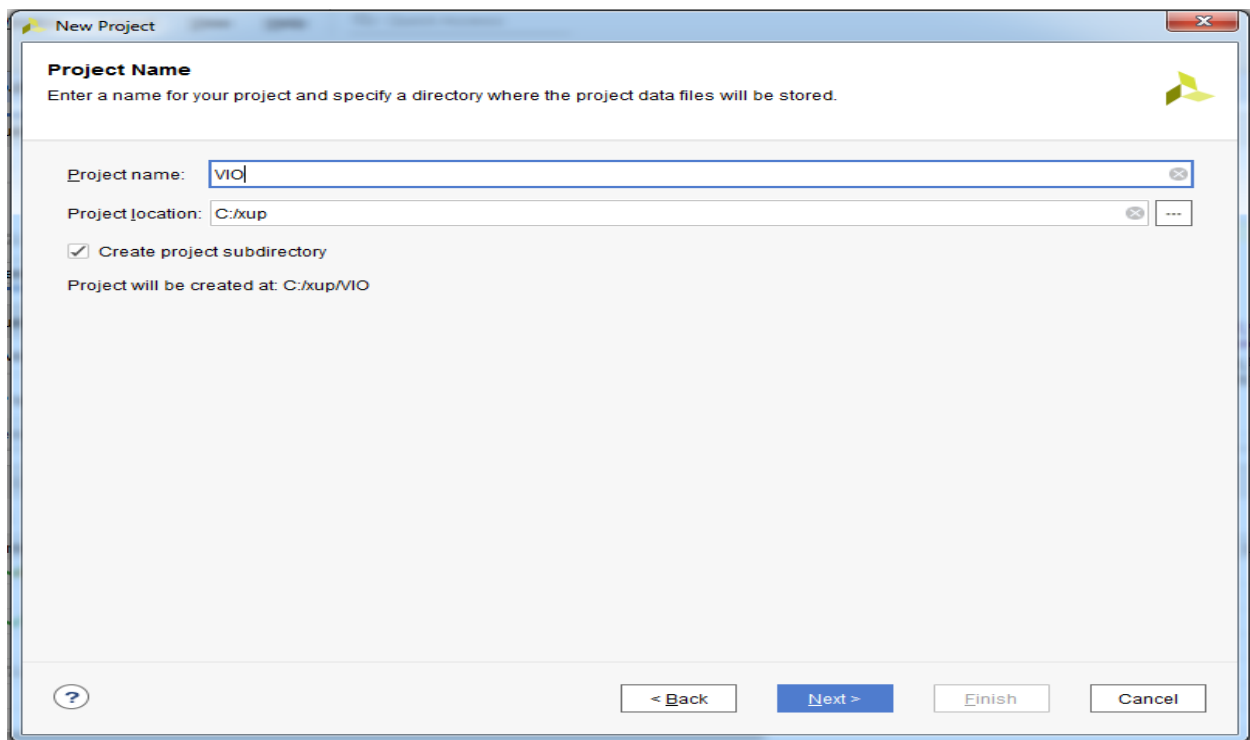


VIO Core Manual

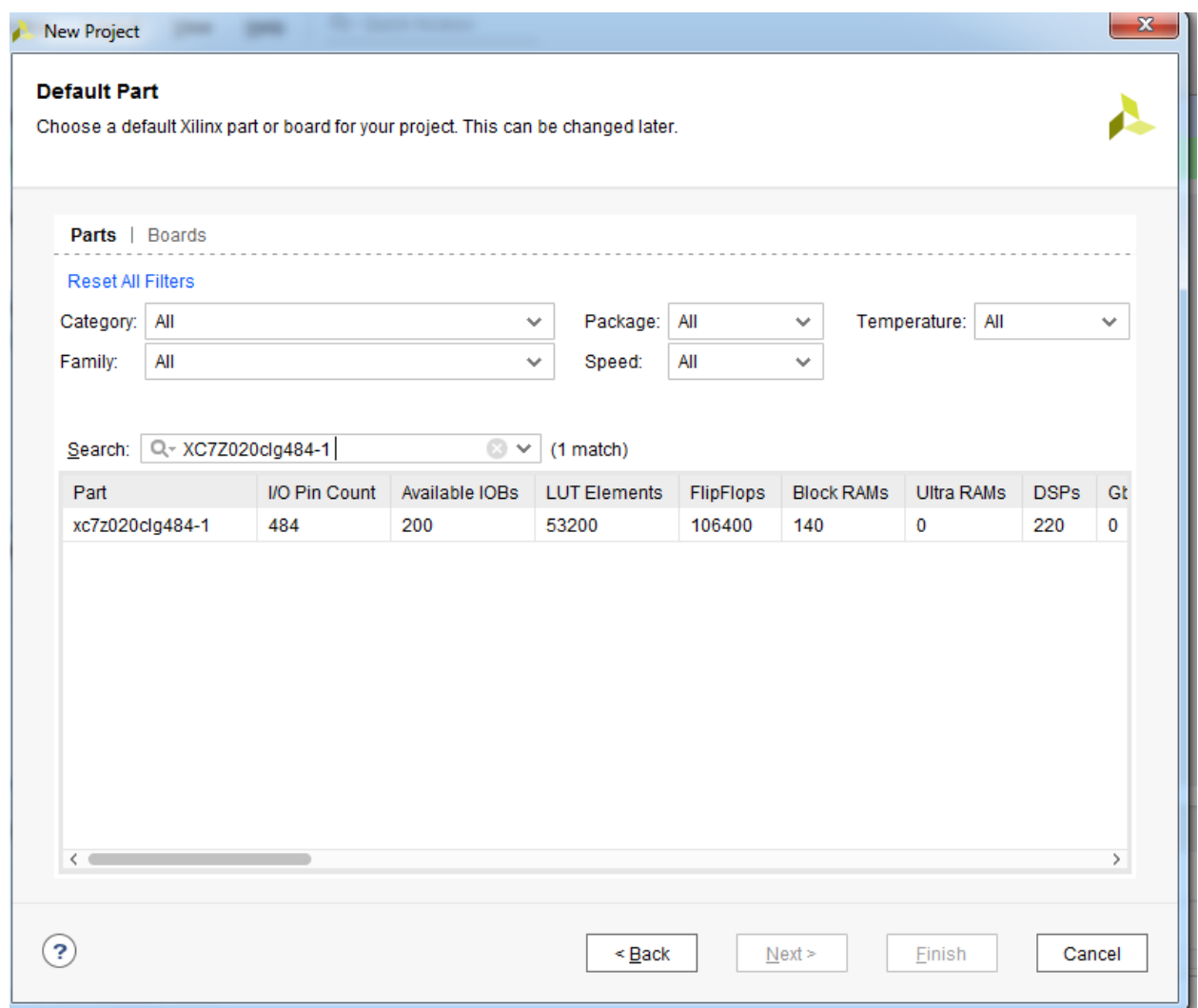
Create a Vivado Project using IDE

Step 1

- 1-1. Launch Vivado and create a project targeting the XC7Z020clg484-1 device (ZedBoard), or the XC7Z010clg400-1 (Zybo), and using the Verilog HDL. Use the provided lab1.v and lab1_<board>.xdc files from the 2018_2_ZYNQ_sources\lab1 directory.
- 1-1-1. Open Vivado by selecting **Start > All Programs > Xilinx Design Tools > Vivado 2018.2 > Vivado 2018.2**
- 1-1-2. Click **Create New Project** to start the wizard. You will see *Create A New Vivado Project* dialog box. Click **Next**.
- 1-1-3. Click the Browse button of the *Project location* field of the **New Project** form, browse to **c:\xup\fpga_flow\2018_2_ZYNQ_labs**, and click **Select**.
- 1-1-4. Enter **vio** in the *Project name* field. Make sure that the *Create Project Subdirectory* box is checked. Click **Next**.



- 1-1-5. Select **RTL Project** option in the *Project Type* form, and click **Next**.
- 1-1-6. Using the drop-down buttons, select **Verilog** as the *Target Language* and *Simulator Language* in the *Add Sources* form.
- 1-1-7. Since we do not have any source, click **Next** to get to the *Add Constraints* form.
- 1-1-8. Bypass this step as we will create XDC file afterwards.
- 1-1-9. In the *Default Part* form, use the **Parts** option and various drop-down fields of the **Filter** section. If using the ZedBoard, select the **XC7Z020clg484-1** part. If using the Zybo, select the **XC7Z010clg400-1**.



Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

[Reset All Filters](#)

Category: All Package: All Temperature: All

Family: All Speed: All

Search: (1 match)

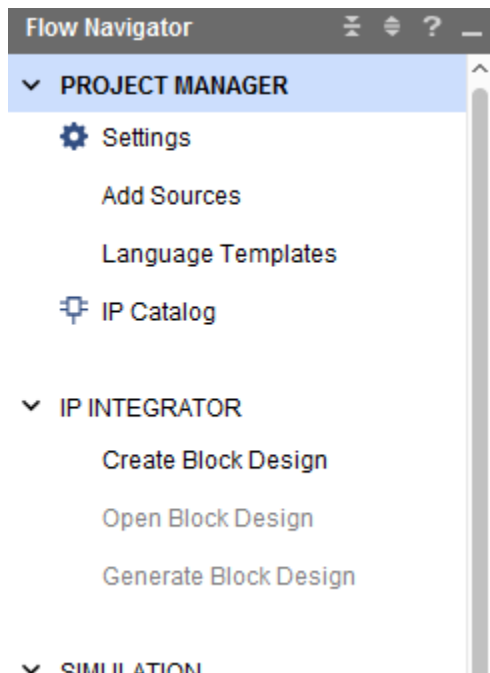
Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gt
xc7z020clg484-1	484	200	53200	106400	140	0	220	0

< Back Next > Finish Cancel

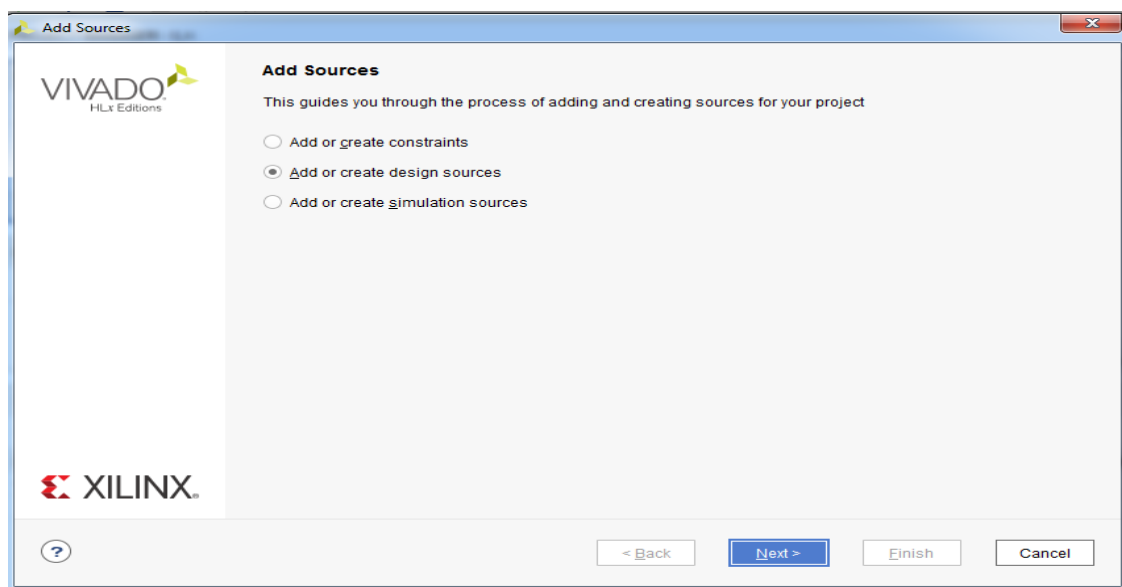
- 1-1-10. Click **Next**.
- 1-1-11. Click **Finish** to create the Vivado project.

1-2. Creating Project and writing rtl Code.

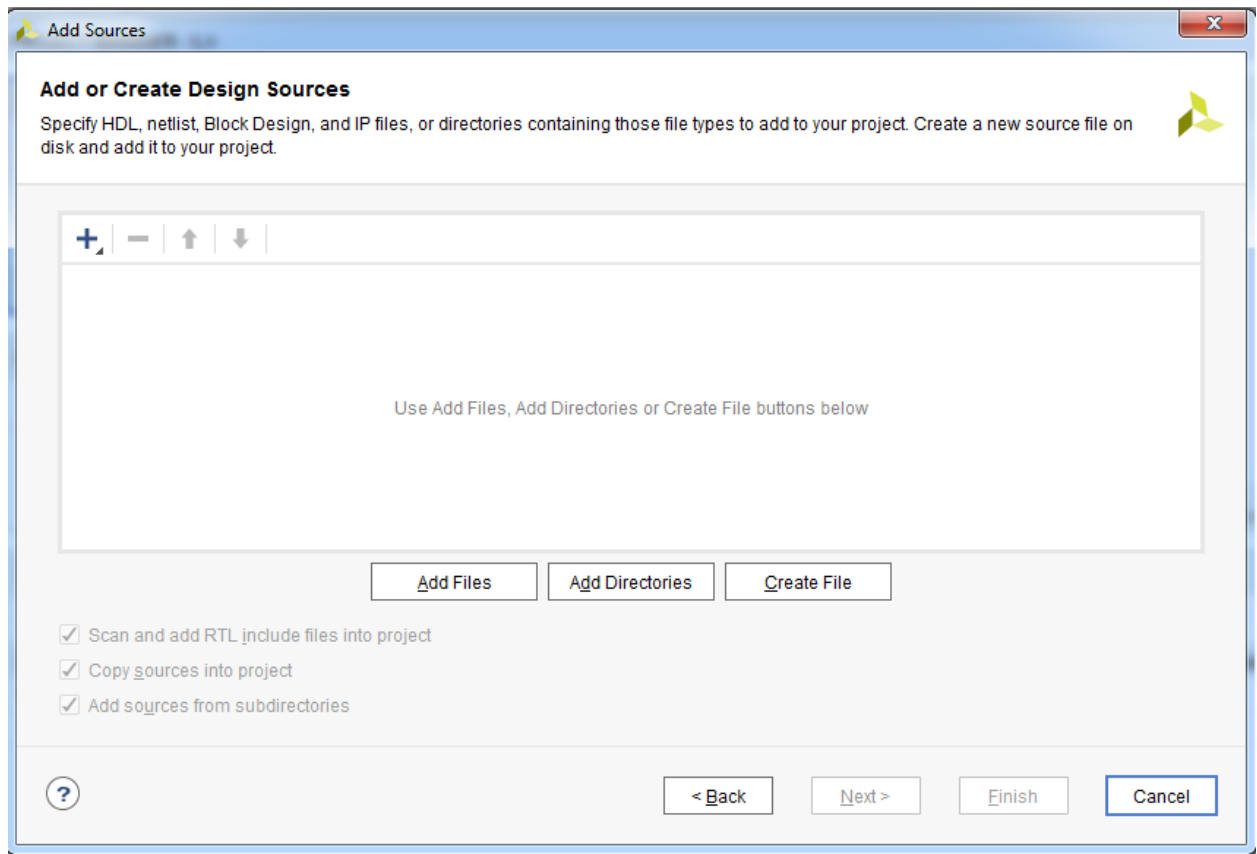
1-2-1. In the project Manager click on add source .



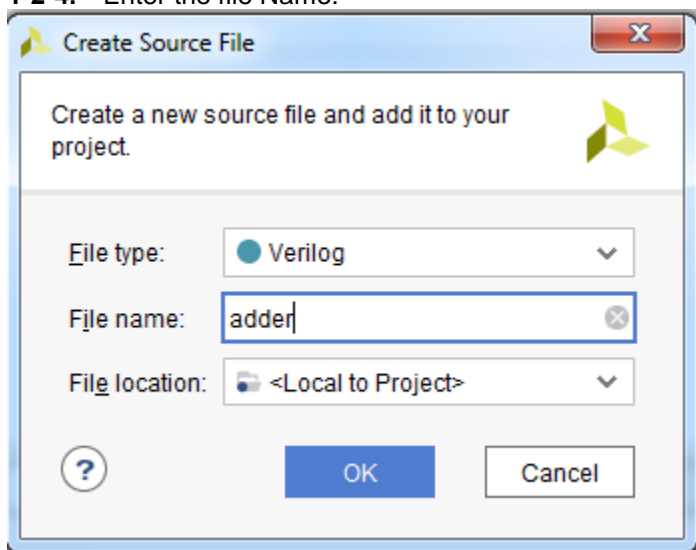
1-2-2. Select option of add or create Design Source .



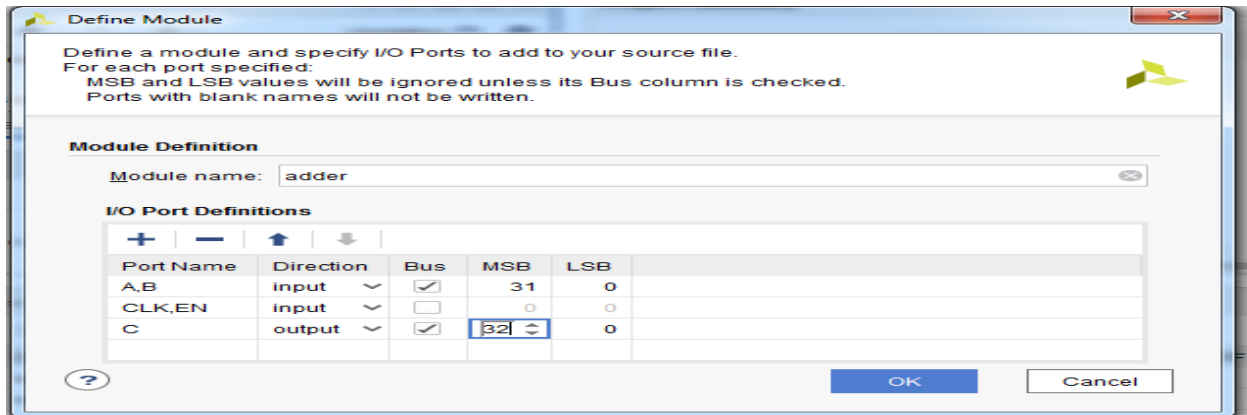
1-2-3. Select option of create file .



1-2-4. Enter the file Name.



1-2-5. Click Ok and enter ports



1-2-6. Click Ok ,you can see under Project Manager in Sources ,the .v file has been added.

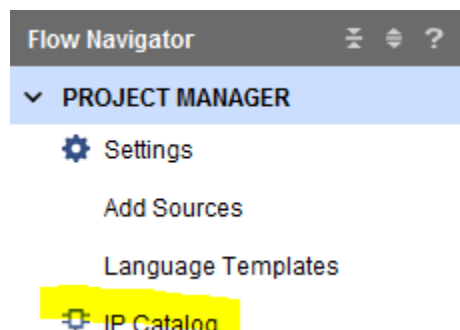
1-2-7. Double click on adder.v and make design entry in counter.v file.

```

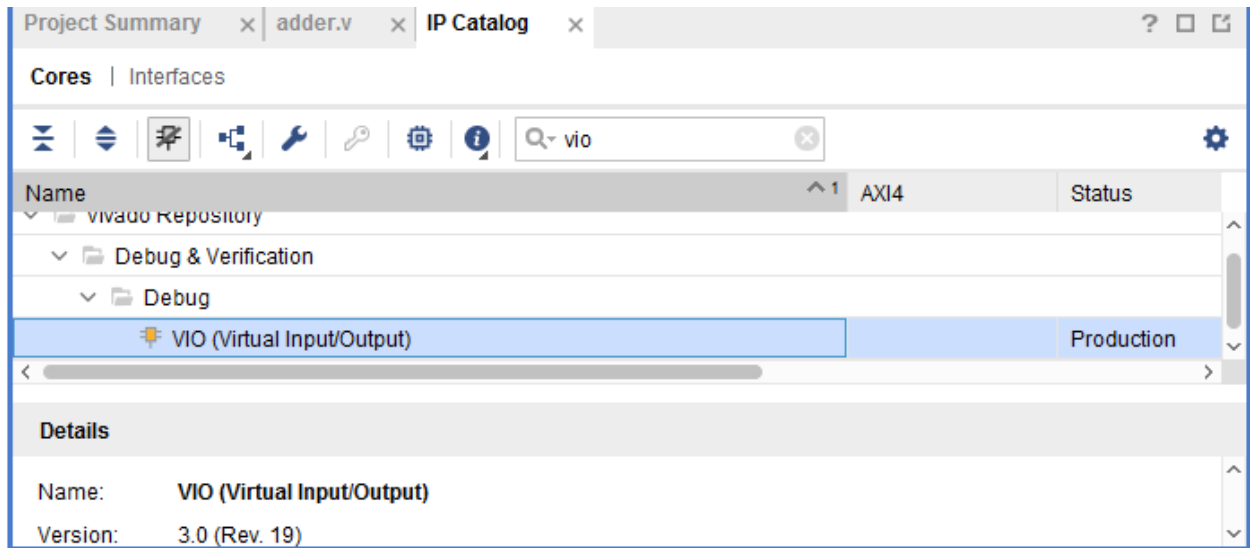
21
22
23 module adder(
24     input [31:0] A,B,
25     input CLK,EN,
26     output reg [32:0] Y
27 );
28
29     always @ (posedge CLK)
30
31         if (EN)
32             Y <= A+B;
33         else
34             Y <= A-B;
35
36 endmodule
37

```

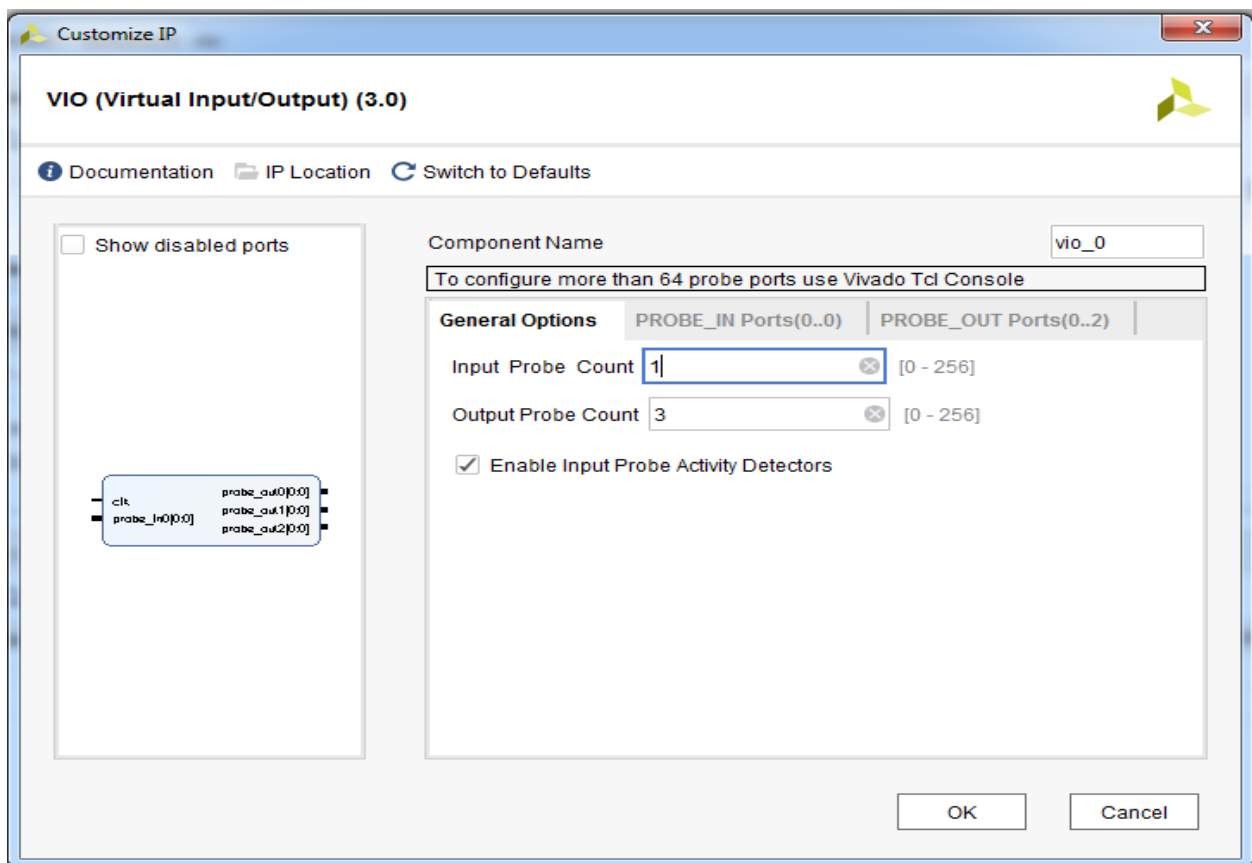
1-2-8. Now Add via ip Core for that click onto



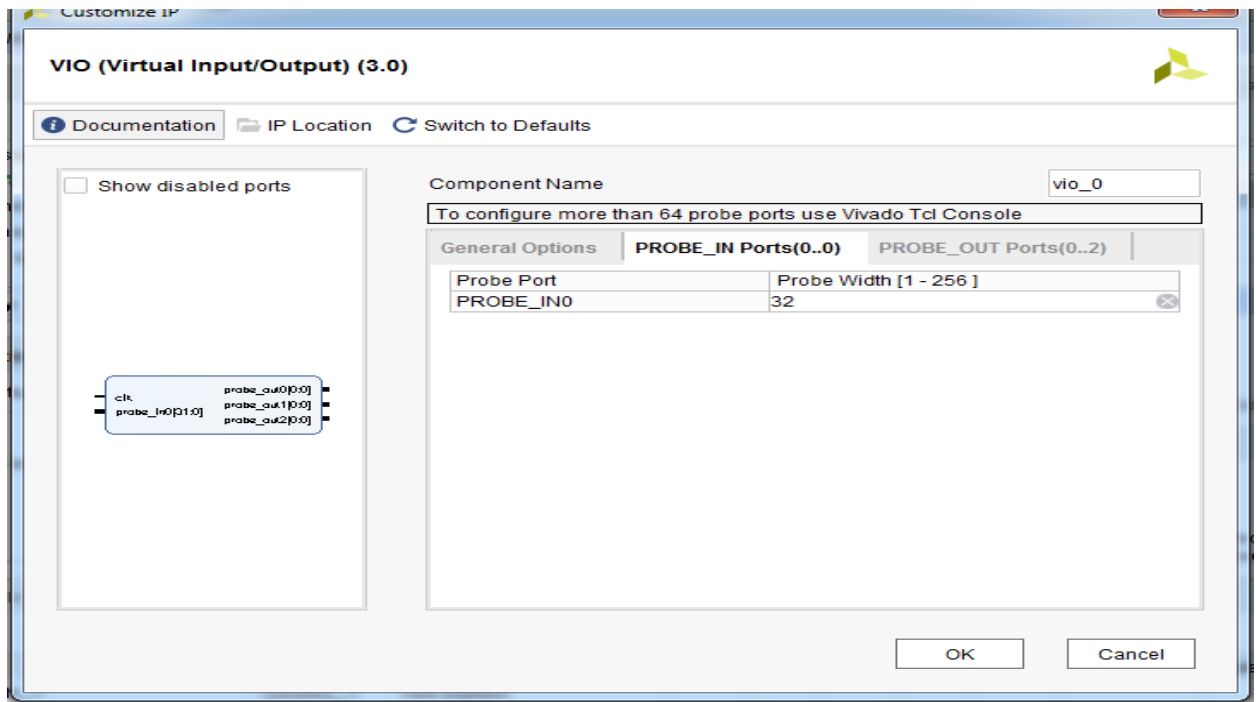
1-2-9.



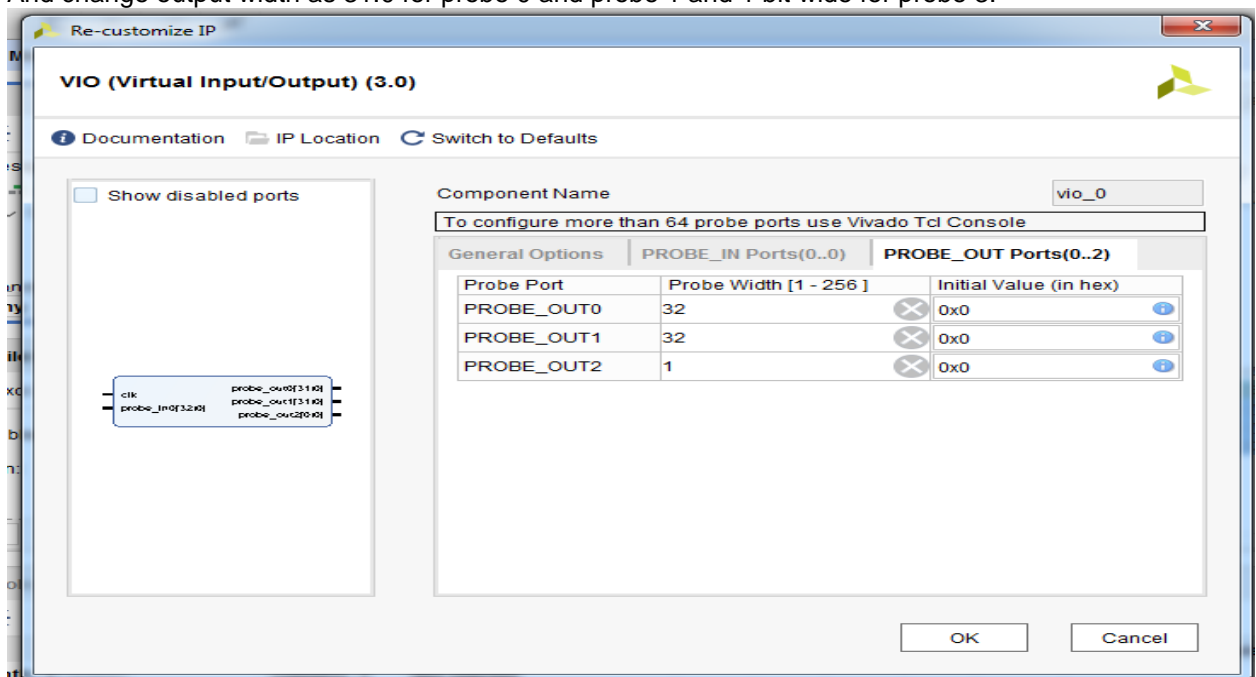
1-2-10. Now give input probe as 1 and output probe as 3 .click OK and Generate and Then OK .



1-2-11.



1-2-12. And change output width as 31:0 for probe 0 and probe 1 and 1 bit wide for probe 3.



1-2-13. Go to IP Sources under Sources Panel, click onto IP instantiation and click on via_0.vio and

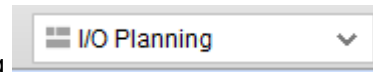
```

20 ///////////////////////////////////////////////////////////////////
21
22
23 module adder(
24     input [31:0] A,B,
25     input CLK,EN,
26     output reg [32:0] Y
27 );
28
29     vio_0 v1 (
30         .clk(CLK),           // input wire clk
31         .probe_in0(Y),       // input wire [0 : 0] probe_in0
32         .probe_out0(A),      // output wire [0 : 0] probe_out0
33         .probe_out1(B),      // output wire [0 : 0] probe_out1
34         .probe_out2(EN)      // output wire [0 : 0] probe_out2
35     );
36
37     always @ (posedge CLK)
38     begin
39         if (EN)
40             Y <= A+B;
41         else
42             Y <= A-B;
43     end
44 endmodule
45

```

1-2-14. Run synthesis

1-2-15. click onto option of run Synthesis and select I/O Planing



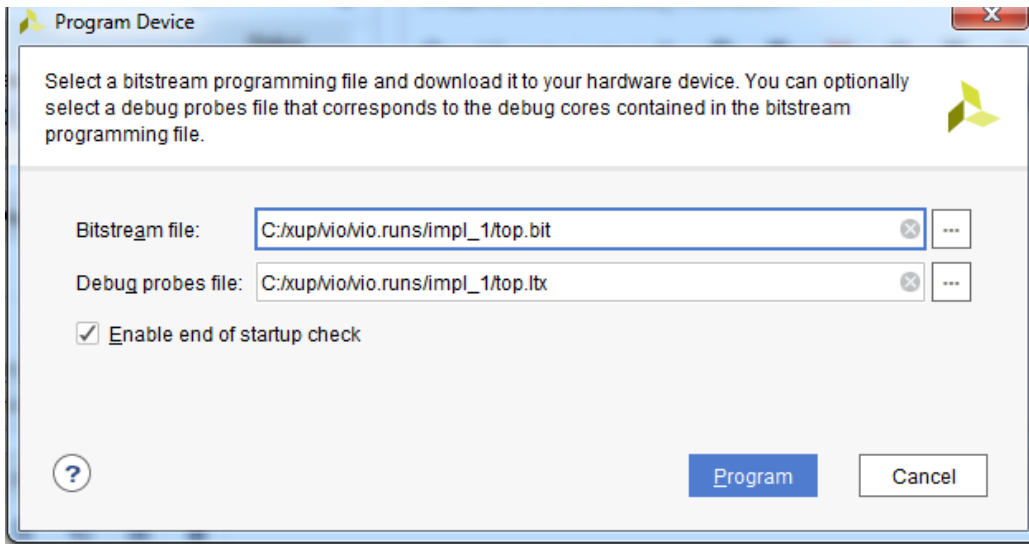
and enter Clk pin location and respective IO standards in IO Ports as

	Package Pin	I/O Standard
clk	Y9	LVCMOS18

3-1. Dumping Bitstream File

3-1-1. Open Hard ware Manager .

3-1-2.



3-1-3. Click onto (+) to add all signals into windows panel ,and change values and analyze results

