Experiments:

Experiment Number	1	2	3
Number of data cache load accesses	25531	25531	25531
Number of data cache store accesses	23052	23052	23052
Number of instruction cache accesses	123657	123657	123657
Number of hits for instruction cache	122157	121906	122870
Number of hits for data cache	43558	42793	46582
Number of ALU instruction type	53060	53060	53060
Number of branch instruction type	11502	11502	11502
Number of load instruction type	25531	25531	25531
Number of store instruction type	23052	23052	23052
Number of jump instruction type	10508	10508	10508
Number of No-Op instruction type	4	4	4
Number of taken branches	4501	4501	4501
Number of forwarding from EX stage	19508	20007	19794
Number of forwarding from MEM stage	16012	16762	16799
Number of stalled cycles in ID stage	1500	1500	1500
Total cycles	256542	272782	201345
Instruction cache hit ratio	0.98787	0.98584	0.993636
Memory cache hit ratio	0.896569	0.880823	0.958813
Instruction Per Cycle (IPC)	0.482015	0.453318	0.614155
Percentage of taken branches over total branches	39.13%	39.13%	39.13%
Instruction frequency for ALU	42.91%	42.91%	42.91%
Instruction frequency for load	20.65%	20.65%	20.65%
Instruction frequency for store	18.64%	18.64%	18.64%
Instruction frequency for branch	9.30%	9.30%	9.30%
Percentage of stalled cycles over total cycles	56.67%	58.88%	44.37%

Analysis:

1.In experiment 2, the miss rate for the instruction cache is doubled i.e. (clock_cycle%**64**). It can be observed that the total number of cycles will be increased as there will be more misses compared to the previous experiment and for each extra miss the processor must fetch the instruction from the main memory, which will take additional 15 cycles, as a result, the number of stall cycles will also be increased. As the number of stalls increases, IPC will also come down.

And, the instruction cache hit ratio will also be decreased.

2.In experiment 3, the miss rate for the data cache is halved i.e. (clock_cycle%**32**). It can be observed that the total number of cycles will be decreased as there will be less misses compared to the original experiment. as a result, the number of stall cycles will also be decreased. As the number of stalls decreases, IPC will also increase. And, the data cache hit ratio will also be increased.

Q: If load operation is a cache miss and next instruction is ALU or branch without any data dependency on the load destination register?

A: If load operation is a cache miss then we are stalling the pipeline for 15 cycles. i.e., the instruction will be not allowed move forward until the data is fetched from the main memory for the previous instruction.

Screen shots:

Experiment – 1:

```
------------------------------------------------------------------
Statistical data
------------------------------------------------------------------
Number of data cache load accesses = 25531
Number of data cache store accesses = 23052
Number of instruction cache accesses = 123657
Number of hits for instruction cache = 122157
Number of hits for data cache = 43558
Number of ALU instruction type = 53060
Number of branch instruction type = 11502
Number of load instruction type = 25531
Number of store instruction type = 23052
Number of jump instruction type = 10508
Number of No-Op instruction type = 4
Number of taken branches = 4501
Number of forwarding from EX stage = 19508
Number of forwarding from MEM stage = 16012
Number of stalled cycles in ID stage = 1500
Total cycles = 256542

------------------------------------------------------------------
Calculations
------------------------------------------------------------------
Instruction cache hit ratio = 0.9878697
Memory cache hit ratio = 0.8965688
Instruction Per Cycle (IPC) = 0.48201463
Percentage of taken branches over total branches = 39.132324%
Instruction frequency for ALU = 42.909016%
Instruction frequency for load = 20.646627%
Instruction frequency for store = 18.64189%
Instruction frequency for branch = 9.301536%
Percentage of stalled cycles over total cycles = 56.670254%
------------------------------------------------------------------
```

Experiment – 2:

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------------------------------------------------------------------
Statistical data
------------------------------------------------------------------
Number of data cache load accesses = 25531
Number of data cache store accesses = 23052
Number of instruction cache accesses = 123657
Number of hits for instruction cache = 121906
Number of hits for data cache = 42793
Number of ALU instruction type = 53060
Number of branch instruction type = 11502
Number of load instruction type = 25531
Number of store instruction type = 23052
Number of jump instruction type = 10508
Number of No-Op instruction type = 4
Number of taken branches = 4501
Number of forwarding from EX stage = 20007
Number of forwarding from MEM stage = 16762
Number of stalled cycles in ID stage = 1500
Total cycles = 272782

------------------------------------------------------------------
Calculations
------------------------------------------------------------------
Instruction cache hit ratio = 0.98583984
Memory cache hit ratio = 0.88082254
Instruction Per Cycle (IPC) = 0.45331803
Percentage of taken branches over total branches = 39.132324%
Instruction frequency for ALU = 42.909016%
Instruction frequency for load = 20.646627%
Instruction frequency for store = 18.64189%
Instruction frequency for branch = 9.301536%
Percentage of stalled cycles over total cycles = 58.883286%
------------------------------------------------------------------
```

Experiment – 3:

```
------------------------------------------------------------
Statistical data
------------------------------------------------------------
Number of data cache load accesses = 25531
Number of data cache store accesses = 23052
Number of instruction cache accesses = 123657
Number of hits for instruction cache = 122870
Number of hits for data cache = 46582
Number of ALU instruction type = 53060
Number of branch instruction type = 11502
Number of load instruction type = 25531
Number of store instruction type = 23052
Number of jump instruction type = 10508
Number of No-Op instruction type = 4
Number of taken branches = 4501
Number of forwarding from EX stage = 19794
Number of forwarding from MEM stage = 16799
Number of stalled cycles in ID stage = 1500
Total cycles = 201345

------------------------------------------------------------
Calculations
------------------------------------------------------------
Instruction cache hit ratio = 0.9936356
Memory cache hit ratio = 0.9588128
Instruction Per Cycle (IPC) = 0.6141548
Percentage of taken branches over total branches = 39.132324%
Instruction frequency for ALU = 42.909016%
Instruction frequency for load = 20.646627%
Instruction frequency for store = 18.64189%
Instruction frequency for branch = 9.301536%
Percentage of stalled cycles over total cycles = 44.365643%
------------------------------------------------------------
```