Dilawar Singh

Curriculum Vitae

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Info

Born	June 5th, 1985 at Nichalpur (India)	Citizenship	Indian
Additional Address	Nichalpur village, Bugbara Post, Bijnor, U.P. - 246745		
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Github	https://github.com/dilawar	Skype	dilawar_s

Academic Backgroud

Ph. D., **IIT Bombay**, 2010-Present

Currently working on partition of large scale digital systems. Also on numerical computation on FPGAs and many-core architectures, circuit simulation, algorithms in VLSI cad. My thesis adviser is Prof. Sachin Patkar.

M. Tech., *Microelectronics and VLSI*, **IIT Bombay** 2007-2009

My thesis was on **Fabrication of micro-electrode arrays for retinal prosthesis**. My training was in the area of VLSI design and device engineering. I also took courses on signal processing. My thesis advisor was Prof. Dinesh K. Sharma.

B. Tech., *Instrumentation and Control*, **Dr. MGR ERI, Chennai**

My project was on **Stabilization of laser-head in CD-ROM using PID controllers**. I took various courses on control engineering and developed algorithms in Matlab.

Current Skills

Theoretical

I am trained in the area of VLSI, control and instrumentation. I took a keen interest in **algorithms and programming**. Currently I am active in the area of VLSI cad : synthesis and translation processes; numerical computations on FPGAs and many-core platforms; and circuit simulations. I have more than layman's interest in social-anthropology.

Computer Skills

Languages	Haskell, Python, JAVA, C/C++, VHDL, Verilog, Bluespec, SQL, PHP, LUA, PERL, BASH, Scheme, Lisp LaTeX		
Platforms	Unix, Linux, Windows, Apache, Lighttpd	DB	MySQL, sqlite3

Tools	**VIM**, Eclipse IDE, CMAKE Build system, Git, SVN, *NIX, Xilinx and Altera tools, shell tools, OpenGL 4.2, JSON, Matlab/Scilab, Office Suite, Gimp, AutoCad

Experience

Working

2009-2010	**Design Engineer, System Admin, Programmer at Kritikal Solutions**, *Noida*, Uttar Pradesh, India.
	Development of firmware for movie-cameras on DINI board with RTOS Multi. Image stabilization using Kalman filtering. Maintenance of version control system and servers hosted on Solaris OS.

Accademic

2012	Verilog parser in JAVA : Parsing of verilog to VerilogXML. VerilogXML is XML representation of Verilog. Two other students have also contributed to the code.
2013	Fast matrix inversion on FPGA : Published work. I wrote the algorithm in C to simulate the algorithm on computer. Verilog design was implemented on FPGA by first author.
2009	Circuit simulator : A MNA based circuit simulator implemented in Scilab.
2012-13	Teaching assistant system : It is written in PHP/sqlite3. It collects preferences of department teaching assistants and allot them a job. It uses Network-flow based method to find a optimal solution.

Other

2007-2013	Various other projects don are available on my github. Notable among them are **code-sniffer** which search the common pattern in codes submitted by students. Automated system to download and extract the assignments posted by students on moodle. Python scripts to generate VHDL and verilog test-benches. A primitive implementation of Binary Decision diagrams. Various algorithms implemented as teaching assistants are also in public-domain.

Interests and Hobbies

I enjoy reading social-anthropology and sociology. I also have soft corner of Indian history and Indus scripts. If not reading, writing or coding, I can tolerate going to movies with friends and playing cricket.

Extra

qoo	Simple PHP framework written with MVC (OOP) programming in mind that I worked on with a friend of mine.

- GitHub Repository
- Qoo Framework Blog