Dilawar Singh

Curriculum Vitae

Room D207/H12
IIT Bombay Mumbai, India
+91 9004 005270
dilawars@iitb.ac.in

Info

Born	June 5th, 1985 at Nichalpur (India)	Citizenship	Indian
Additional Address	Nichalpur village, Bugbara Post, Bijnor, U.P. - 246745		
LinkedIn	`http://in.linkedin.com/dilawarsingh`	Web	`http://www.ee.iitb.ac.in/student/~dilawar`
Github	`https://github.com/dilawar`	Skype	dilawar_s

Academic Backgroud

Ph. D., **IIT Bombay**, Aug 2010-Present

Currently working on partition of large scale digital systems. In addition, I also worked on numerical computation on FPGAs, circuit simulation, algorithms in VLSI cad. My thesis adviser is Prof. Sachin Patkar.

M. Tech., *Microelectronics and VLSI*, **IIT Bombay** Jul 2007- Jun 2009

My thesis project was on **fabrication of micro-electrode arrays for retinal prosthesis**. My training was in the area of device fabrication and VLSI design. I also took courses on signal processing. My thesis advisor was Prof. Dinesh K. Sharma.

B. Tech., *Instrumentation and Control*, **Dr. MGR ERI, Chennai**

My project was on **Stabilization of laser-head in CD-ROM using PID controllers**. I simulated some controllers designed in Matlab.

Publication

2013 **Hardware-software Scalable Architectures for Gaussian Elimination over GF(2) and Higher Galois Fields**, Prateek Saxena, Vinay B. Y. Kumar, Dilawar Singh, H Narayanan and Sachin B. Patkar

Skills

Theoretical

I am trained in the area of semiconductor devices, VLSI design, control and instrumentation. My skills are mainly in the area of **algorithms and programming**. Currently I am active in the area of VLSI cad: translation processes from HDL design to hardware; numerical computations on FPGAs and many-core platforms; and circuit simulations. I have more than layman's interest in social-anthropology.

Engineering Skills

Languages Haskell, Python, JAVA, C/C++, VHDL, Verilog, Bluespec, SQL, PHP, LUA, PERL, BASH, Scheme/Lisp LaTeX

CAD Tools Technology CAD related to MOS-FETS, Cadence, Xilinx and Altera tools, Ngspice

Tools **VIM**, Build tools, Git/SVN, *NIX, Matlab/Scilab

Experience

Industry

2009-2010 **Design Engineer, System Admin, Programmer at Kritikal Solutions**, *Noida*, Uttar Pradesh, India.
Development of firmware for movie-cameras on DINI board with RTOS Multi. Image stabilization using Kalman filtering. Maintenance of version control system and servers hosted on Solaris OS.

Accademic

2012 Verilog parser in JAVA : Parsing Verilog and translating it to VerilogXML. VerilogXML is XML representation of Verilog.

2013 Fast matrix inversion on FPGA : Published work. I wrote the algorithm in C to simulate the algorithm on computer. Verilog design was implemented on FPGA by its first author.

2009 Circuit simulator : A MNA based circuit simulator implemented in Scilab.

2012-13 Teaching assistant management system : PHP/sqlite3. It collects preferences of department teaching assistants and allot them a job. It uses Network-flow based method to find a optimal solution.

Other

2007-2013 Some other hobby projects are available on my github. Notable among them are **code-sniffer** which search the common pattern in codes submitted by students. Automated system to download and extract the assignments posted by students on moodle. Python scripts to generate VHDL and verilog test-benches. A primitive implementation of Binary Decision diagrams. Various algorithms implemented as teaching assistants are also in public-domain.

Interests and Hobbies

I enjoy reading social-anthropology and sociology. I also have soft corner of Indian history and Indus scripts. If not reading, writing or coding, I can tolerate travelling inside India and playing cricket.