

# *Designing, Simulating, and Building a 3-stage Audio Amplifier using 'BJT' Transistors*

Adrian Moreno Talavera, Electrical and Computer Engineering (EECE), California State University, Chico  
Chico, CA, amorenotalavera@csuchico.edu

Carson Middaugh, Electrical and Computer Engineering (EECE), California State University, Chico  
Chico, CA, cbmiddaugh@csuchico.edu

## I. ABSTRACT

This project presents the design, simulation, and experimental procedures of a three-stage audio amplifier implemented using bipolar junction transistors. The amplifier consists of two cascaded common-emitter voltage amplification stages followed by an emitter-follower buffer stage. The system is designed to operate over the audible frequency range of 20 Hz to 20 kHz while maintaining stable biasing and predictable small-signal performance. Large-signal and small-signal analyses are performed to determine component values and operating points, ensuring that all transistors remain in the active region. The first and second stages achieve decoupled voltage gains of 17.5 and 66.04, respectively, while the buffer stage provides a gain of 548. When cascaded, the overall measured voltage gain of the amplifier is 244.9, showing the effects of impedance bridging. Impedance bridging is employed throughout the design, with the input impedance of each stage maintained at least ten times greater than the output impedance of the preceding stage, resulting in improved gain preservation and signal integrity. SPICE simulations confirm predictions and indicate a frequency response extending from 200 Hz to 200 kHz within 245 volts. These results demonstrate the effectiveness of impedance bridging and proper biasing in achieving stable, high-gain audio amplification using distinct BJT stages.

amplifier using bipolar junction transistors (BJTs). The amplifier is structured to be built with distinct components and to ensure the performance of both large-signal (DC) and small-signal (AC) biasing. Every stage is designed to be built in the Active operating mode of the transistors and would not function correctly otherwise.

Our schematic consists of two cascaded common-emitter amplifier stages and one buffer stage, which is implemented as an emitter-follower after the previous two stages. The common-emitter stages served as a way to multiply their individual gains to attain a gain unachievable through a single transistor. The third stage served to change impedance output without any voltage (gain) loss.

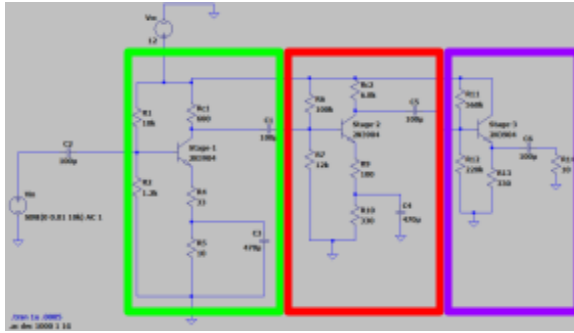
Once values for resistors in each stage were calculated to achieve Active operating mode, it was necessary to cascade all stages together and bridge them with impedance bridging. Input impedances in each stage had to be ten times higher than the output impedance from the previous stage, so there were many modifications made to resistor values in order to achieve this. This approach minimizes loading effects, preserves the intended voltage gains of each stage when they are cascaded, and is overall essential for optimal amplifier performance.

## II. INTRODUCTION

The objective for this project is to design, analyze, simulate, and build a three-stage audio

### III. METHODOLOGY

#### A. Circuit Schematic and Description



The schematic above shows a functional, cascaded amplifier with three individual stages.

In the first stage, highlighted by the green block, the gain ideally becomes 15.6. This is made possible by the resistor values that were solved for by using known values such as the collector current,  $V_{BE}$ ,  $V_T$ ,  $V_{CC}$ , and each gain (-15.6, -16.8, 1). In this stage, it was important to choose a common-emitter BJT amplifier design because the purpose of common-emitting transistors is to provide high voltage, ideal for amplification.

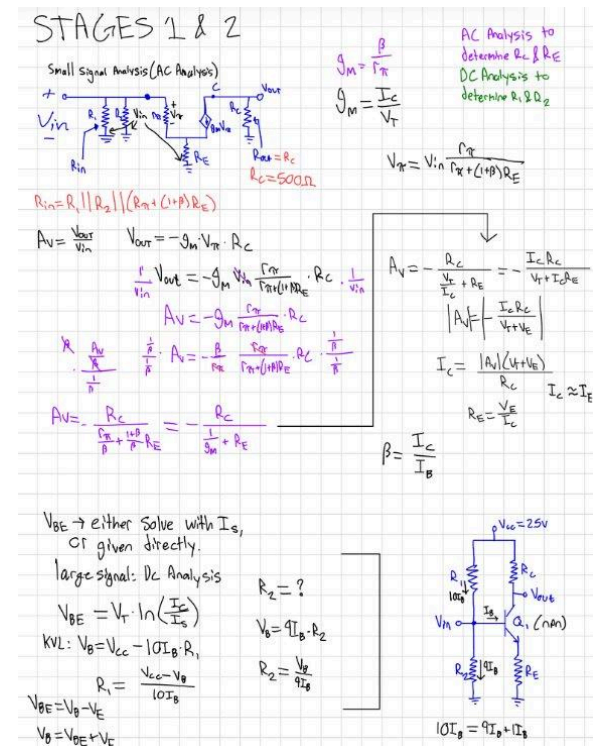
The second stage, highlighted by the red block, operates similarly to stage 1, but with different resistor values in order to attain a different gain (-16.8). It is important that the second stage also uses a common-emitter circuit design, as the goal is to also amplify its input voltage, with the overall goal to multiply the gains acquired from stages 1 and 2.

Stage 3, highlighted by the purple block, does not function like the previous stages. Instead of multiplying the input voltage, it instead functions as a buffer with a gain of 1. Having a gain of 1 allows it to push along the multiplied voltage gains from stages 1 and 2 while reducing output impedance for the final output. To achieve this buffering effect, this stage must use a common-collector BJT circuit design. The common-collector circuit has high impedance, extremely low output impedance, and unity voltage gain; ideal for buffering a voltage, just like our amplifier required.

After all the resistor values were calculated for each stage, the matter of impedance bridging was the next step in the simulation process. Without impedance bridging, the calculated values alone would not accurately amplify the input voltage as required. To start, the specifications for impedance bridging call for the input impedance of the next stage to be ten times the output impedance of the previous stage. Implementation of this went through hours of trial and error, adjusting resistors to try and accomplish a combined gain close to 262.08, before a solution was found.

Stage 1 is adjusted to have all resistor values divided by ten. After ensuring that the circuit is still in Active mode, we only minutely adjusted resistors in stage 2 to match the resistor values accessible to us, while also having ten times the impedance of stage 1. Stage 3 remains mostly unchanged, only having small changes made to it to match resistor values accessible to us.

#### B. Analysis Calculations





```
%stage 3 transistor decoupled
% specifications of stage 3 common emitter amplifier design
Vt = 0.025;
beta = 100;
Vcc = 12;
Av = 1;
Ve = 0.4;
Ic = .001;
Vbe = 0.7;

% solving for Rx
Ib = Ic/beta;
Re = Ve/Ic;

Rpi = Vt/Ib;
vin = Ib*(Rpi+Re*(1+beta))

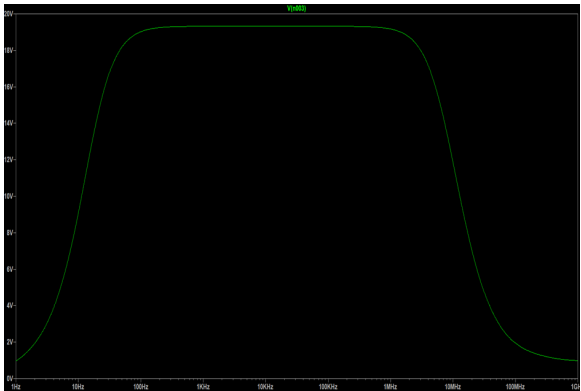
Rx = Vin/Ib

R1 = (Vcc-(Vbe + Ve))/(10*Ib)
R2 = 15000
Gm = Ic/Vt;
ROUT = (1/Rpi + 1/(1/Gm) + 1/Re)^-1;

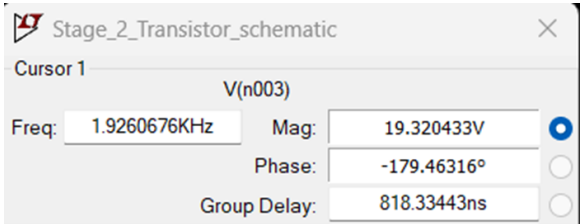
% testing the region of operation of bipolar transistor
Vc = Vcc
Vb = Vbe + Ve

% solving for thevenins
Vth=(Vcc*R2)/(R1+R2);
Rth = (R1*R2)/(R1+R2);
```

Stage 3



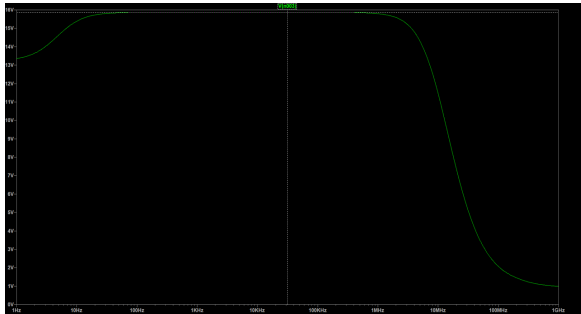
Bode Plot for Stage 2 (Decoupled)



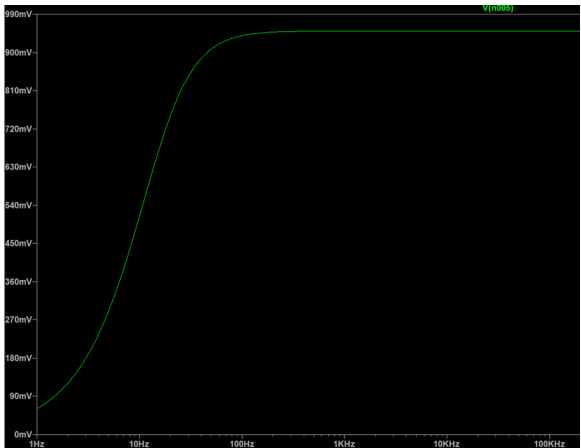
Gain for Stage 2 (Decoupled)

IV. RESULTS AND DISCUSSION

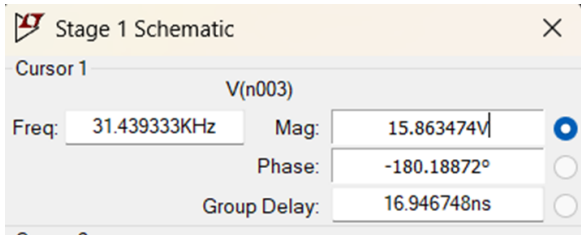
A. Simulations



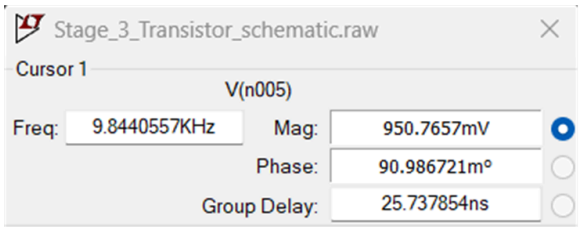
Bode Plot for Stage 1 (Decoupled)



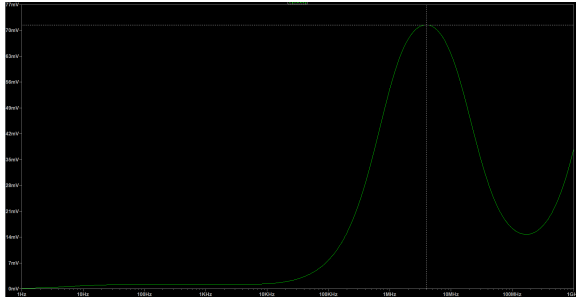
Bode Plot for Stage 3 (Decoupled)



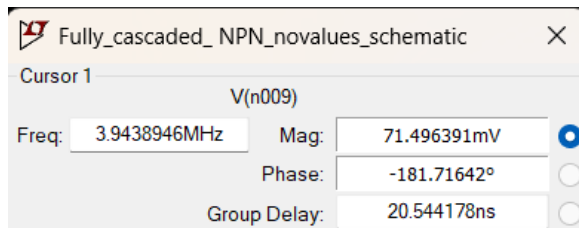
Gain for Stage 1 (Decoupled)



Gain for Stage 3 (Decoupled)



Bode Plot for Cascaded Amplifier (No Impedance Bridging)



Gain for Cascaded Amplifier (No Impedance Bridging)

As seen with all of the decoupled stages based solely on the hand calculations we derived, although the decoupled voltage gains are close to what we anticipated, it is not the same case after everything is cascaded. The cascaded circuit had a peak voltage gain of 71 mV, and only in the frequency range of 2.8 MHz to 5.2 MHz.

This was the reason that impedance bridging was a critical component of the finalized circuit, as we needed to make sure that input impedances would be ten times greater than the previous output impedances.

### B. Experiments

While experimenting to verify our schematic design, we built and tested decoupled and coupled stages and checked their gains. Their values will be shown in tables, comparing them below.

Component	Analysis Calculations	Post-Impedance Bridging
$R_1$	109k	10k
$R_2$	12.2k	1.2k
$R_C$	6630	680
$R_{E1}$	390	33
$R_{E2}$	10	10
$A_V$	15.6	19.05

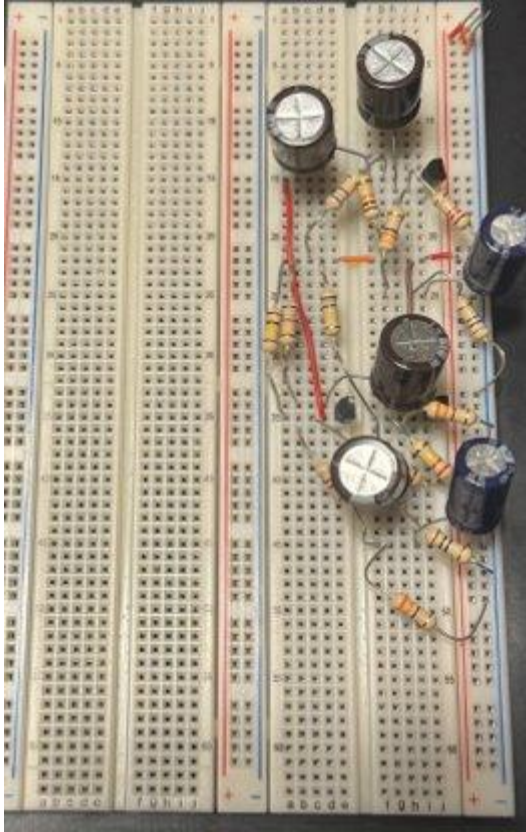
Stage 1 Table Values

Component	Analysis Calculations	Post-Impedance Bridging
$R_1$	109k	100k
$R_2$	12.2k	12k
$R_C$	6630	6.8k
$R_{E1}$	390	100
$R_{E2}$	10	330
$A_V$	16.8	55.8

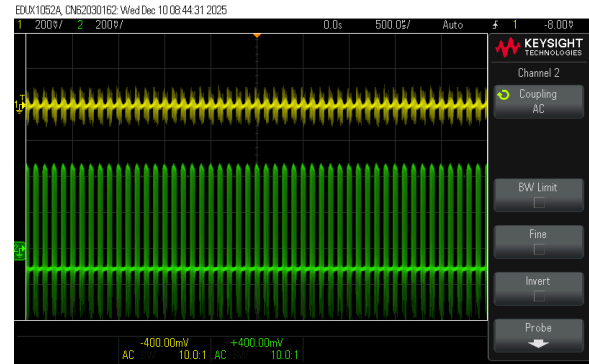
Stage 2 Table Values

Component	Analysis Calculations	Post-Impedance Bridging
$R_1$	109k	560k
$R_2$	12.2k	220k
$R_E$	390	330
$A_V$	1	0.548

Stage 3 Table Values



This circuit is our final working circuit. It amplified our input signal, although we did not get to testing it with a real speaker.



These are the oscilloscope traces that we got for our circuit. The outcome of our gain matched very well with what we were expected to achieve. There was one big tradeoff that we had to deal with in obtaining this output gain, which was the decoupled gains. Our original gain for each stage differed from the final gain after impedance bridging our circuit, but the final result remained.

## V. CONCLUSION

In this project, we successfully designed, analyzed, and simulated a three-stage audio amplifier. This amplifier used an emitter-follower preceded by two common-emitter amplification stages. Using our assumption that the current through  $R_1$  was equal to 10 times the base current, we were able to ensure our transistors were in the Active mode of operation.

Being able to minimize the loading effect through impedance bridging was a crucial component of this project. Making sure that the input impedance of each stage was at least ten times the previous stage allowed us to minimize the loading effect and have a final result of the intended gain. Through all of our simulations, we have shown the significance of impedance bridging and how it improved our results and achieved the output we were looking for.

## REFERENCES

- [1] H. Salehi, "Lecture Notes Week 1-14", December 2025
- [2] H. Salehi, "Design Project Document", December 2025