Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

Design Project: Progress Report 1

Table 1: Specifications of Amplifier Design

V_T	□	V_{CC}	A_{V1}	A_{V2}	A_{V3}	V_E	I_C	V_{BE}	□/(1+□)	iR1
25 mV	100	12 V	-15.6	-16,8	1	0.4 V	1 mA	0.7 V	1	10Ib

Analysis/Calculations:

Provide appropriate calculations that explain/show how the important parameters associated with each block in the system were determined/designed. Your discussion must also include the process/calculations followed towards determining the schematic component (e.g. resistor, capacitor, etc.) values.

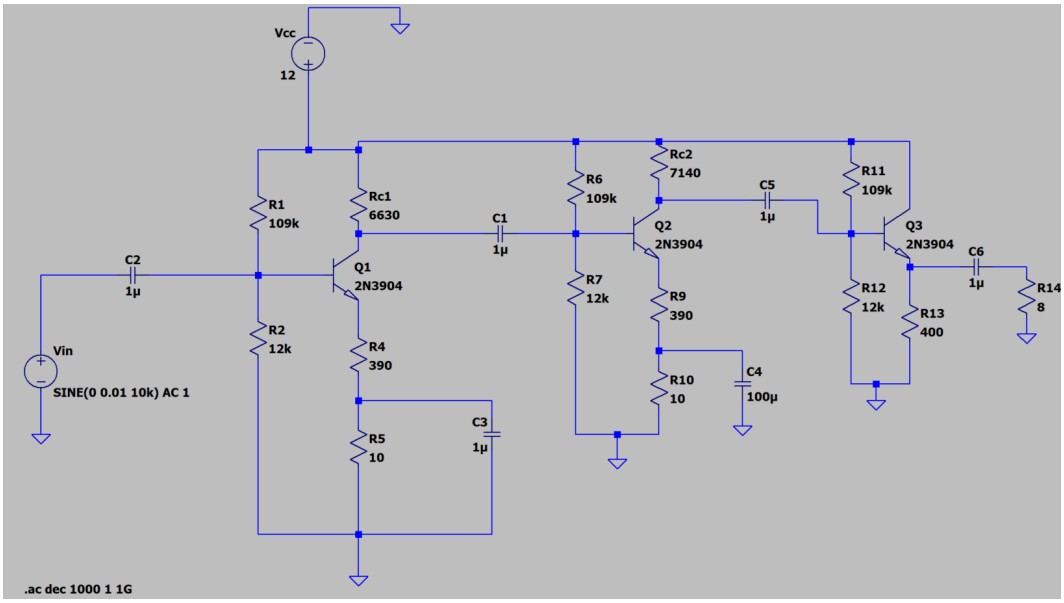


Figure 1: Cascaded Amplifier Schematic

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

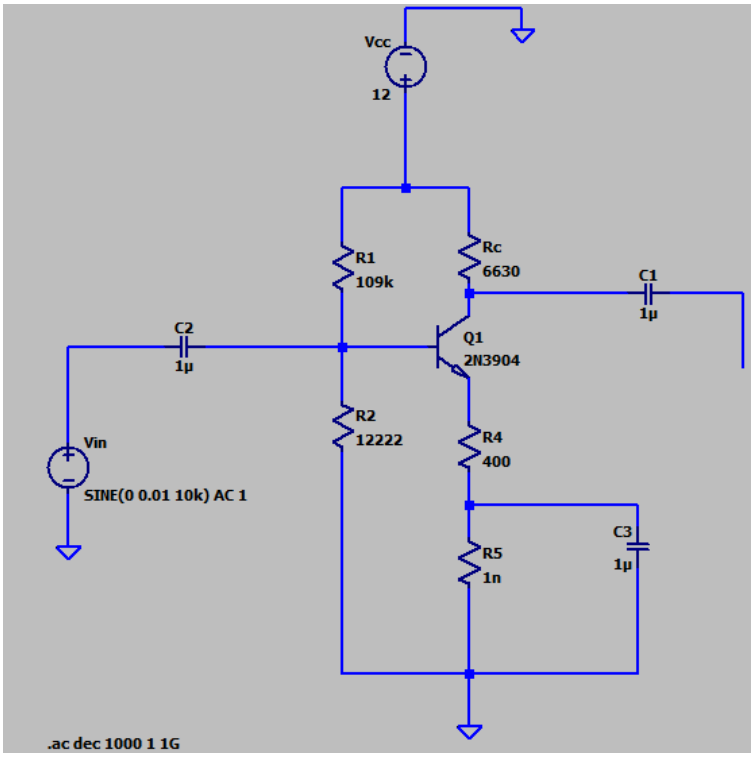


Figure 2: LTspice Schematic for Stage 1 (Decoupled)

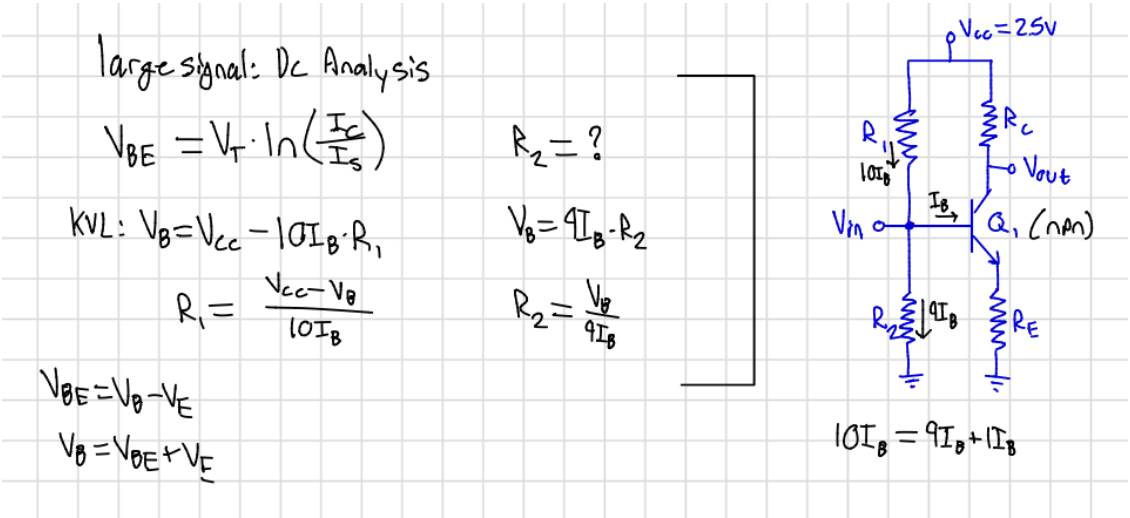


Figure 3: DC Analysis for ALL Stages

With our assumption listed in Table 1 that iR1 = 10Ib, all stages will have the same DC analysis. This is because, as shown in Figure 3, the only “AC” values that we need for these calculations of R1 and R2 are values that have been assumed in Table 1.

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

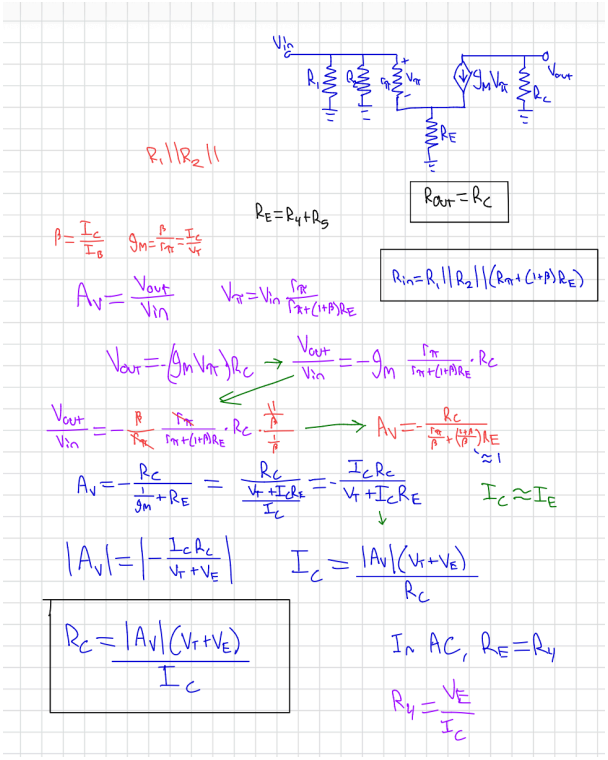
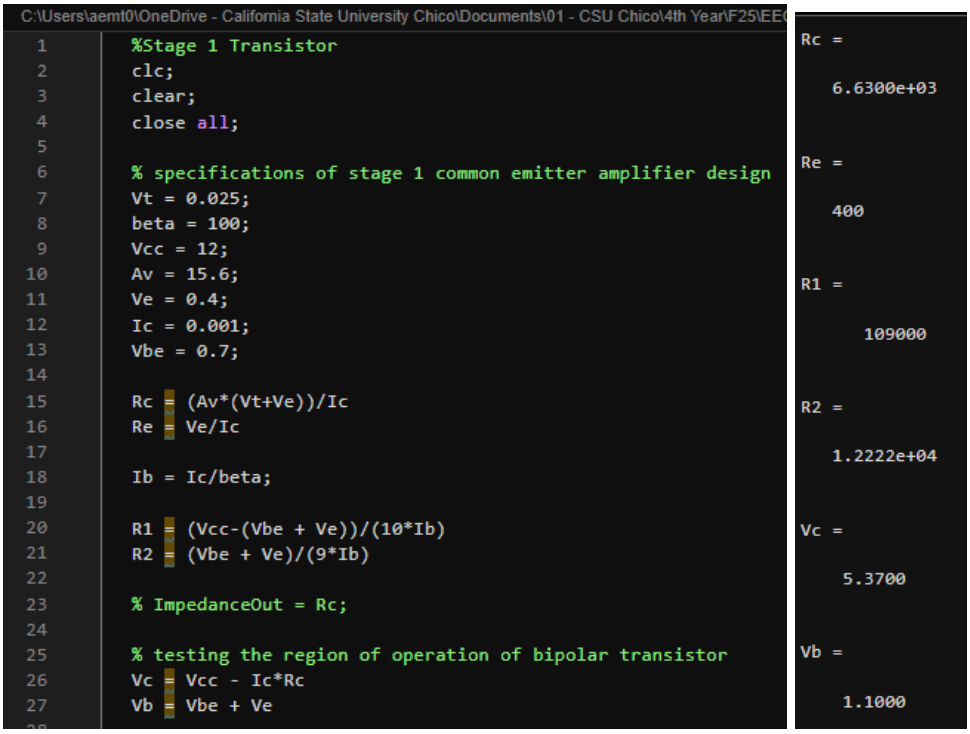


Figure 4: Small Signal (AC) Analysis for Stage 1 & 2



```
C:\Users\aemt0\OneDrive - California State University Chico\Documents\01 - CSU Chico\4th Year\F25\EE
1   %Stage 1 Transistor
2   clc;
3   clear;
4   close all;
5
6   % specifications of stage 1 common emitter amplifier design
7   Vt = 0.025;
8   beta = 100;
9   Vcc = 12;
10  Av = 15.6;
11  Ve = 0.4;
12  Ic = 0.001;
13  Vbe = 0.7;
14
15  Rc = (Av*(Vt+Ve))/Ic
16  Re = Ve/Ic
17
18  Ib = Ic/beta;
19
20  R1 = (Vcc-(Vbe + Ve))/(10*Ib)
21  R2 = (Vbe + Ve)/(9*Ib)
22
23  % ImpedanceOut = Rc;
24
25  % testing the region of operation of bipolar transistor
26  Vc = Vcc - Ic*Rc
27  Vb = Vbe + Ve
```

```
Rc =

   6.6300e+03


Re =

   400


R1 =

      109000


R2 =

   1.2222e+04


Vc =

    5.3700


Vb =

    1.1000
```

Figure 5: MATLAB Calculations for Stage 1 Amplifier

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

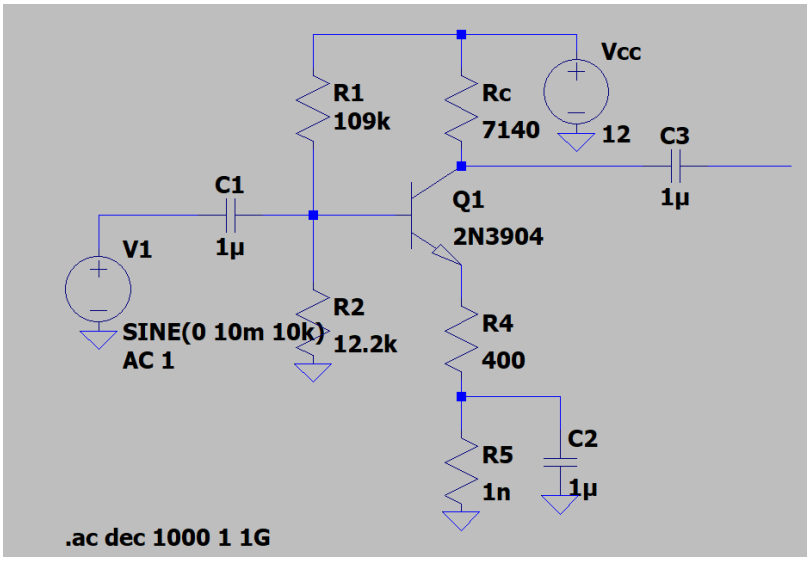


Figure 6: LTspice Schematic for Stage 2 (Decoupled)

The analysis on stage 2 followed exactly the same as stage 1, so refer to Figure 3 and 4 if you would like to look at analysis. The only difference between the analysis of these two was the value of the gain, specified in Table 1.

```
C:\Users\aeml0\OneDrive - California State University Chico\Documents\01 - CSU Chico\4th Year\F25\EE
1   %Stage 2 Transistor
2   clc;
3   clear;
4   close all;
5
6   % specifications of stage 2 common emitter amplifier design
7   Vt = 0.025;
8   beta = 100;
9   Vcc = 12;
10  Av = 16.8;
11  Ve = 0.4;
12  Ic = 0.001;
13  Vbe = 0.7;
14
15  Rc = (Av*(Vt+Ve))/Ic
16  Re = Ve/Ic
17
18  Ib = Ic/beta;
19
20  R1 = (Vcc-(Vbe + Ve))/(10*Ib)
21  R2 = (Vbe + Ve)/(9*Ib)
22
23  % ImpedanceOut = Rc;
24
25  % testing the region of operation of bipolar transistor
26  Vc = Vcc - Ic*Rc
27  Vb = Vbe + Ve
```

```
Rc =

   7.1400e+03


Re =

   400


R1 =

      109000


R2 =

   1.2222e+04


Vc =

    4.8600


Vb =

    1.1000
```

Figure 7: MATLAB Calculations for Stage 2 Amplifier

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

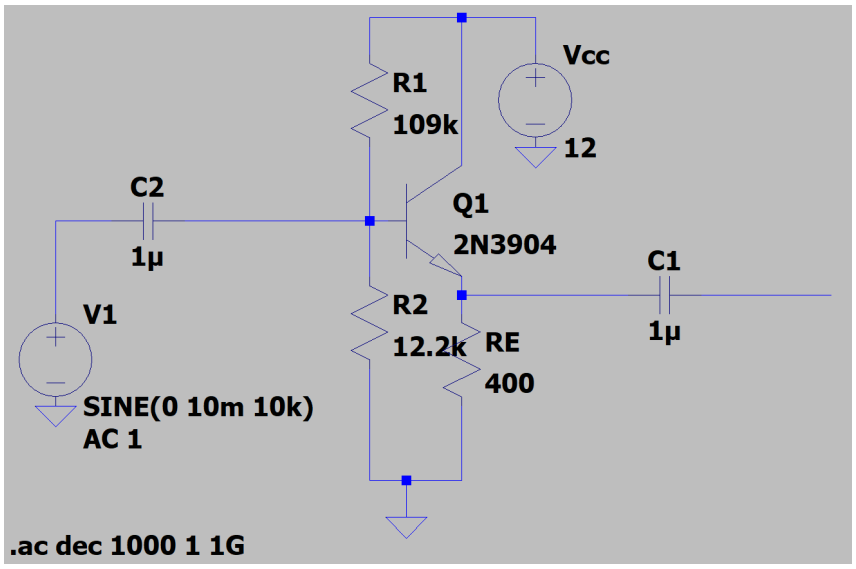


Figure 8: LTspice Schematic for Stage 3 (Decoupled)

```
%stage 3 transistor decoupled

% specifications of stage 3 common emitter amplifier design
Vt = 0.025;
beta = 100;
Vcc = 12;
Av = 1;
Ve = 0.4;
Ic = .001;
Vbe = 0.7;


%solving for Rx
Ib = Ic/beta;

Re = Ve/Ic


Rpi = Vt/Ib;

Vin = Ib*(Rpi+Re*(1+beta));


Rx = Vin/Ib;



R1 = (Vcc-(Vbe + Ve))/(10*Ib)
R2 = 15000

Gm = Ic/Vt;

Rout = (1/Rpi + 1/(1/Gm) + 1/Re)^-1;


% testing the region of operation of bipolar transistor
Vc = Vcc
Vb = Vbe + Ve
```

```
Re =

   400


Vin =

    0.4290


Rx =

       42900


R1 =

      109000


R2 =

       15000


Vc =

    12


Vb =

    1.1000
```

Figure 9: MATLAB Calculations for Stage 3 Amplifier

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

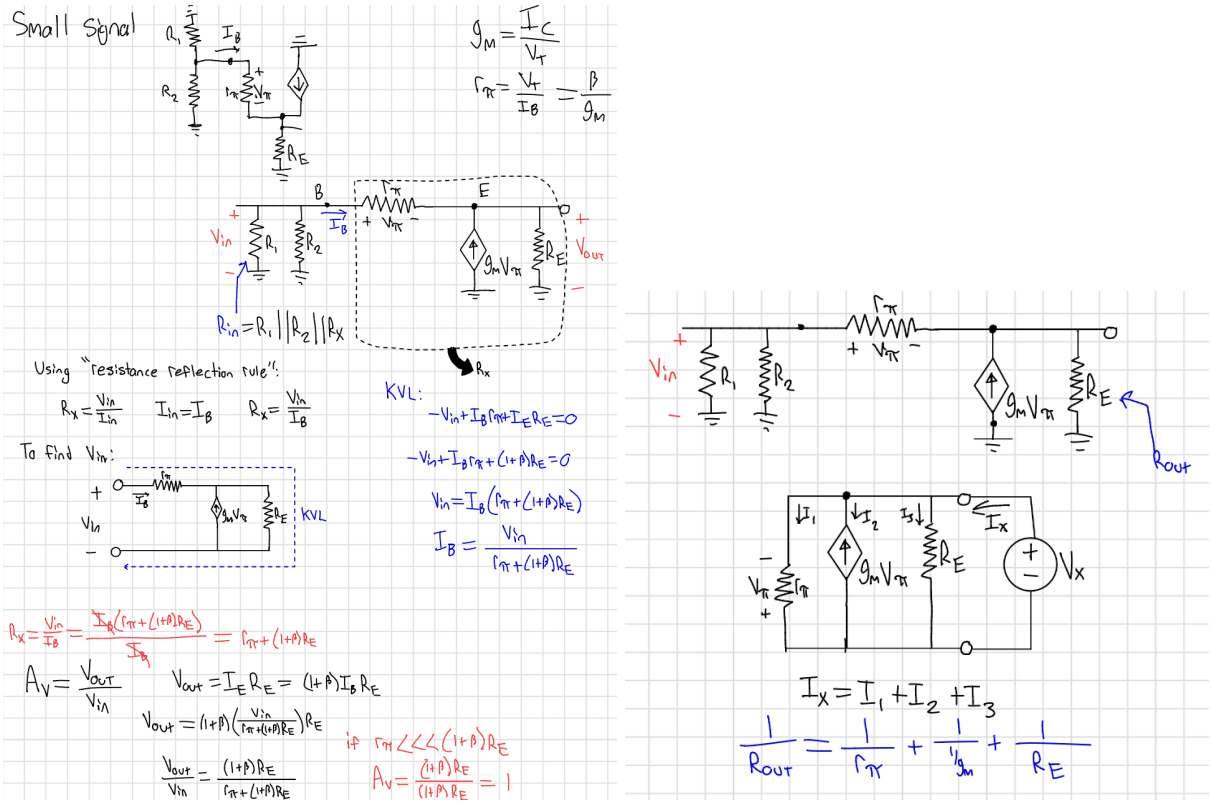


Figure 10: Small Signal (AC) Analysis for Stage 3

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

Simulations:

Simulating our cascaded amplifier without any modifications and solely with the calculations that we derived from large signal and small signal analysis, we saw that our Bode plot did not give the results we were looking for. Our overall gain was about 18.5, so we worked to change with impedance bridging. Below were some of our tests as we tried to determine the best course of action.

Table 2: Trial Runs Modifying Impedance Values (For Impedance Bridging)

Iteration	R1	R2	Rc1	R6	R7	Rc2	R11	R12	C
1 (no modification)	109k	12k	6.6k	109k	12k	7140	109k	12k	1u
2	109k	12k	6.6k	109k	12k	7140	109k	12k	100u
3									
4									
5									

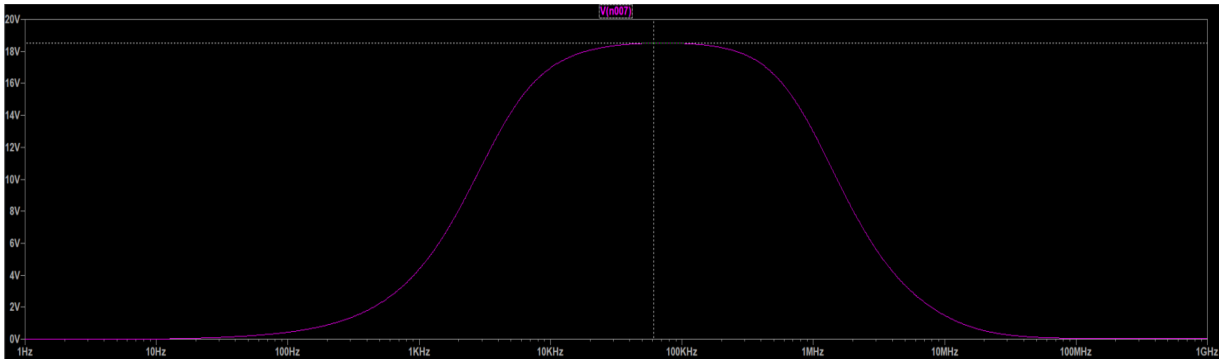


Figure 11: Gain for unmodified Amplifier (Gain = 18.5)

Adrian Moreno Talavera (SID: 011479859)

Carson Middaugh (SID: 011845185)

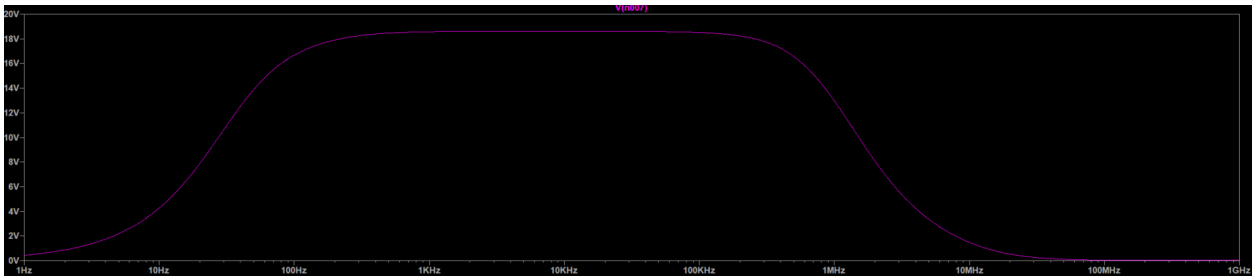


Figure 12: Gain for Amplifier (Iteration 2; Gain = 18.6)

In our second iteration, we wanted to shift the bode plot to the left, so we increased the capacitor values across the entire schematic to be 100 Microfarads instead of 1 microfarad. Although it shifted our bode plot to the left, it wasn't as much as was needed, so there will eventually be more iterations with the capacitors to get the bode plot to where it needs to be.

Group member contributions (Roughly):

Adrian: Adding all of the schematics, matlab for stage 1 and 2, both tables, and starting the impedance iterations.

Carson: Adding all of the theory for all stages, matlab and schematic for stage 3, adding onto table 1.