Current-Mode Control Small-Signal Model[1]

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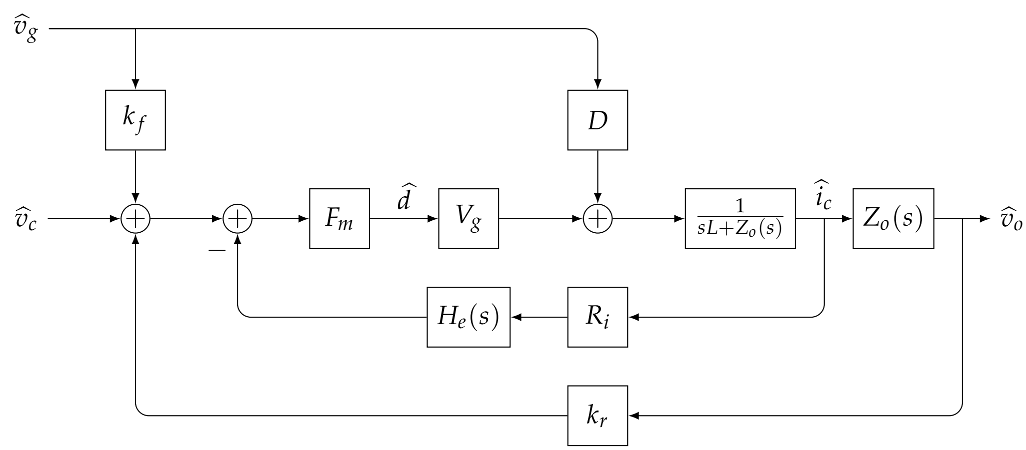
[1] Original derivations by Dr. Raymond B. Ridley of Ridley Engineering.

This document seeks to clarify the block diagrams and equations presented in Dr. Raymond B. Ridley's PhD dissertation, "A New Small-Signal Model for Current-Mode Control." All equations presented herein are as applied to a buck converter with constant-frequency, trailing-edge peak current-mode control.

Small-Signal Block Diagram



Dr. Ridley's diagrams generally mix transfer function blocks with circuit element symbols. As an alternative, a complete transfer function block diagram is provided above. Transfer function descriptions and key parameter definitions are in the margins.

$$F_m = \frac{1}{(S_n + S_e)T_s}$$

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1} \approx 1 - s\frac{T_s}{2} + s^2\left(\frac{T_s}{\pi}\right)^2$$

$$k_f = \frac{-DT_sR_i}{L}\left(1 - \frac{D}{2}\right)$$

$$k_r = \frac{T_sR_i}{2L}$$

Multiple forms of the modulation gain F_m can be found in literature; their differences stem from how the average inductor current is defined relative to the peak. Dr. Ridley has experimentally verified the modulation gain used in this model is correct.

V_g steady-state input voltage
V_o steady-state output voltage
$D = V_o/V_g$ steady-state duty cycle
$\widehat{v}_g$ small-signal input voltage
$\widehat{v}_o$ small-signal output voltage
$\widehat{d}$ small-signal duty cycle
$\widehat{i}_c$ small-signal inductor current
$\widehat{v}_c$ small-signal control voltage
sL inductor impedance
$Z_o(s)$ output impedance
R_i sense resistor
$H_e(s)$ sample-and-hold effect
F_m modulation gain
k_f input feed-forward gain
k_r output feed-forward gain
S_e slope compensation ramp
$S_n = (V_g - V_o)R_i/L$ on-time ramp
$S_f = V_oR_i/L$ off-time ramp
T_s switching period

Dr. Ridley uses a curve-fitting approach to approximate $H_e(s)$; his approximation is only valid up to one-half the switching frequency. Such an approximation will suffice because a stable system must have a crossover frequency beneath the Nyquist frequency of the system. The Padé Approximant could alternatively be used for an approximation that is valid beyond one-half the switching frequency.

In order to simplify the design of the outer voltage loop feedback compensation network, a transfer function from the duty cycle to inductor current F_i can be defined that is independent of the output impedance $Z_o(s)$. Such a transfer function will only be valid for frequencies where $Z_o(s) \ll sL$. Assuming the output impedance is predominantly capacitive, this transfer function would apply above the resonant frequency.

$$F_i = \frac{\hat{i}_c}{\hat{d}} = \frac{V_g}{sL + Z_o(s)} \approx \frac{V_g}{sL} = \frac{S_n + S_f}{sR_i}$$

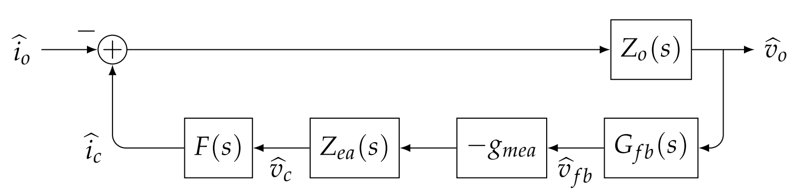
$$\alpha = \frac{S_f - S_e}{S_n + S_e}$$

$$F_m F_i \approx \frac{1+\alpha}{sR_i T_s}$$

The output voltage feed-forward gain k_r can be ignored unless analyzing the low frequency gain of a converter operating near discontinuous conduction mode. The transfer function from the control voltage to inductor current $F(s)$ then becomes rather simple.

$$\begin{aligned} F(s) = \frac{\hat{i}_c}{\hat{v}_c} &= \frac{F_m V_g}{sL + Z_o(s) + F_m V_g (R_i H_e(s) - k_r Z_o(s))} \\ &\approx \frac{F_m F_i}{1 + F_m F_i R_i H_e(s)} \end{aligned}$$

Closed-Loop Design Procedure



A typical network to close the loop around $F(s)$ is shown above. The load is assumed to be an ideal current sink $\hat{i}_o$. The output voltage passes through the feedback network $G_{fb}(s)$ and is compared against a fixed reference voltage. A transconductance error amplifier g_{mea} is loaded by the error amplifier compensation network $Z_{ea}(s)$ to generate the control voltage.

The loop gain $T(s)$ is designed for the appropriate stability margin. The step response is derived from the closed-loop transfer function $Y(s)$.

$$T(s) = F(s)Z_o(s)G_{fb}(s)g_{mea}Z_{ea}(s)$$

$$Y(s) = \frac{\widehat{v}_o}{\widehat{i}_o} = \frac{Z_o(s)}{T(s)-1} = \frac{Z_o(s)}{F(s)Z_o(s)G_{fb}(s)g_{mea}Z_{ea}(s)-1}$$

An iterative design procedure will yield good results. In general, reducing $Z_o(s)$ and increasing the gain and bandwidth of $T(s)$ will yield a step response with less overshoot and faster settling time.

1. Select a ripple current relative to the maximum load current, 10% to 30% is typical. Select a switching frequency and inductance L. Design $Z_o(s)$ to have low impedance at the switching frequency to meet the required voltage ripple.

2. Use the approximate form of $F(s)$ to design $Z_o(s)$, $G_{fb}(s)$, and $Z_{ea}(s)$ to stabilize the loop gain. This will require an initial guess for the required low frequency impedance of $Z_o(s)$. $G_{fb}(s)Z_{ea}(s)$ must, at a minimum, be a Type-II network.

3. Use the exact form of $F(s)$ to simulate the closed-loop step response. Iterate the design of $Z_o(s)$, $G_{fb}(s)$, and $Z_{ea}(s)$ to achieve the desired step response.