

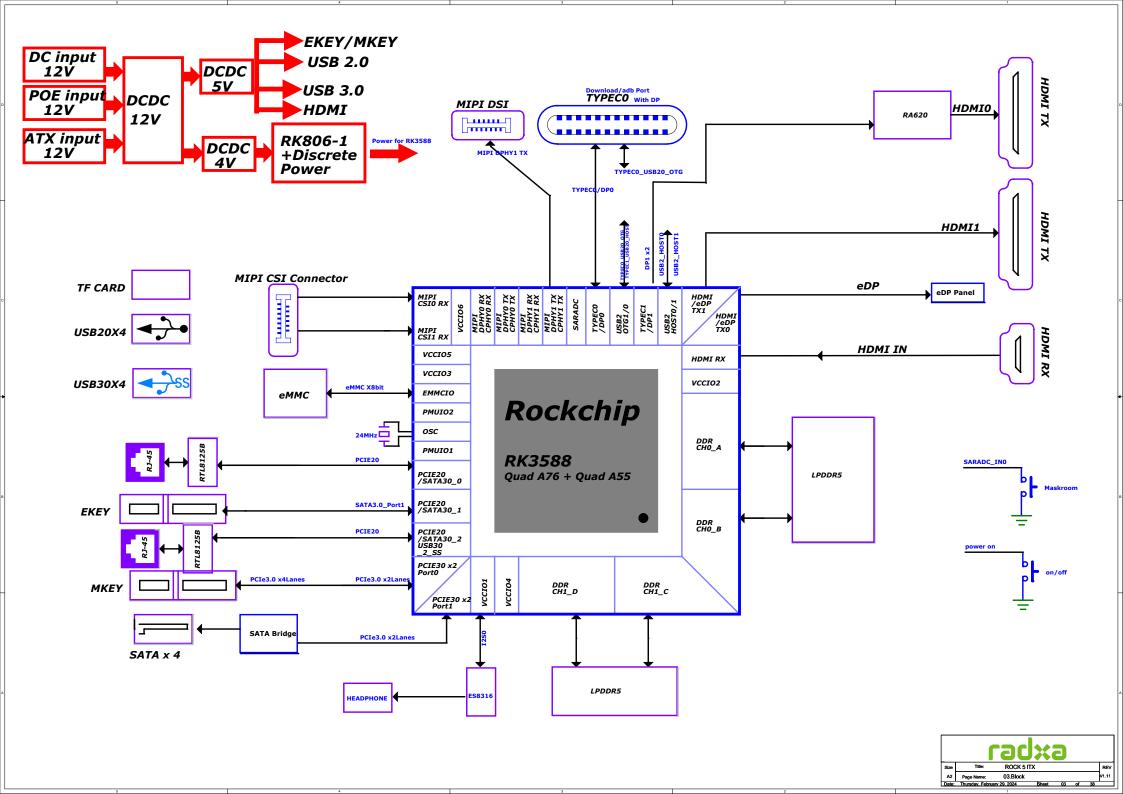
# Radxa ROCK 5 ITX schematic

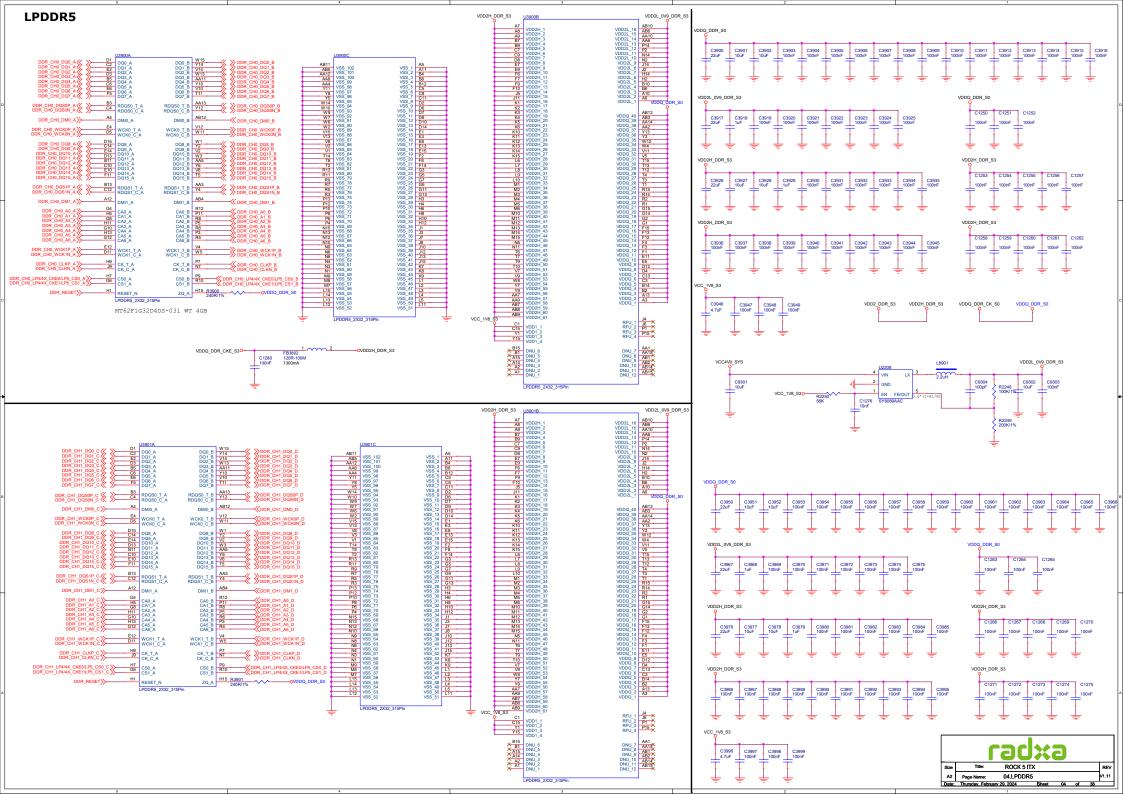


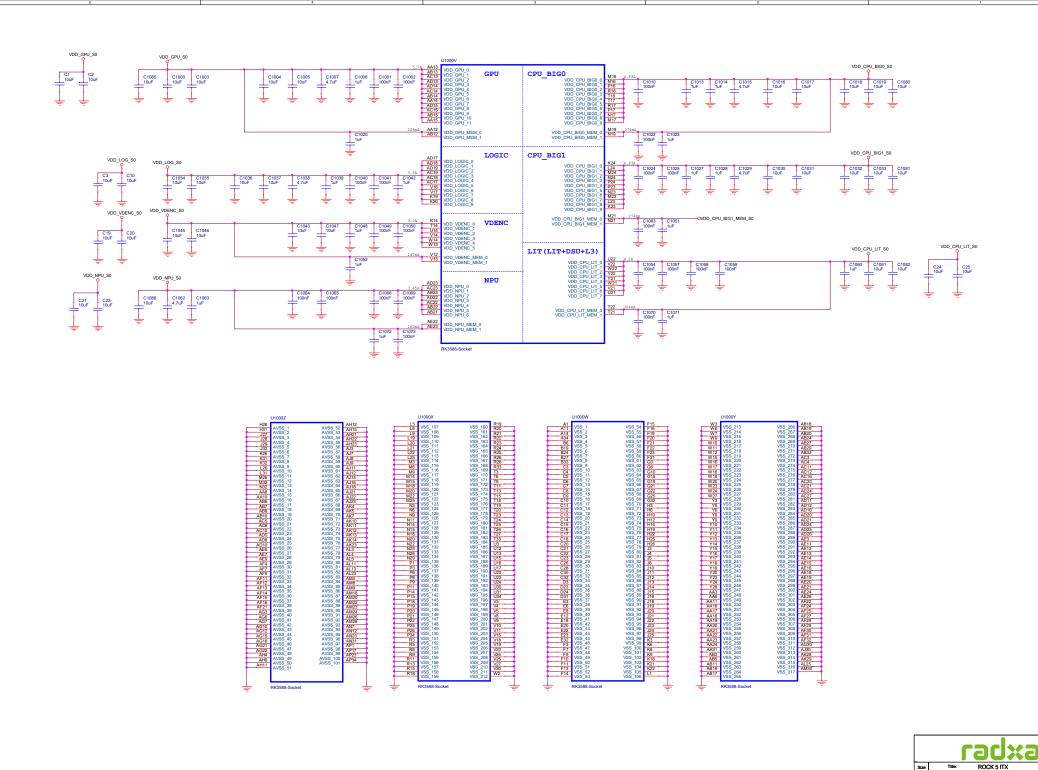
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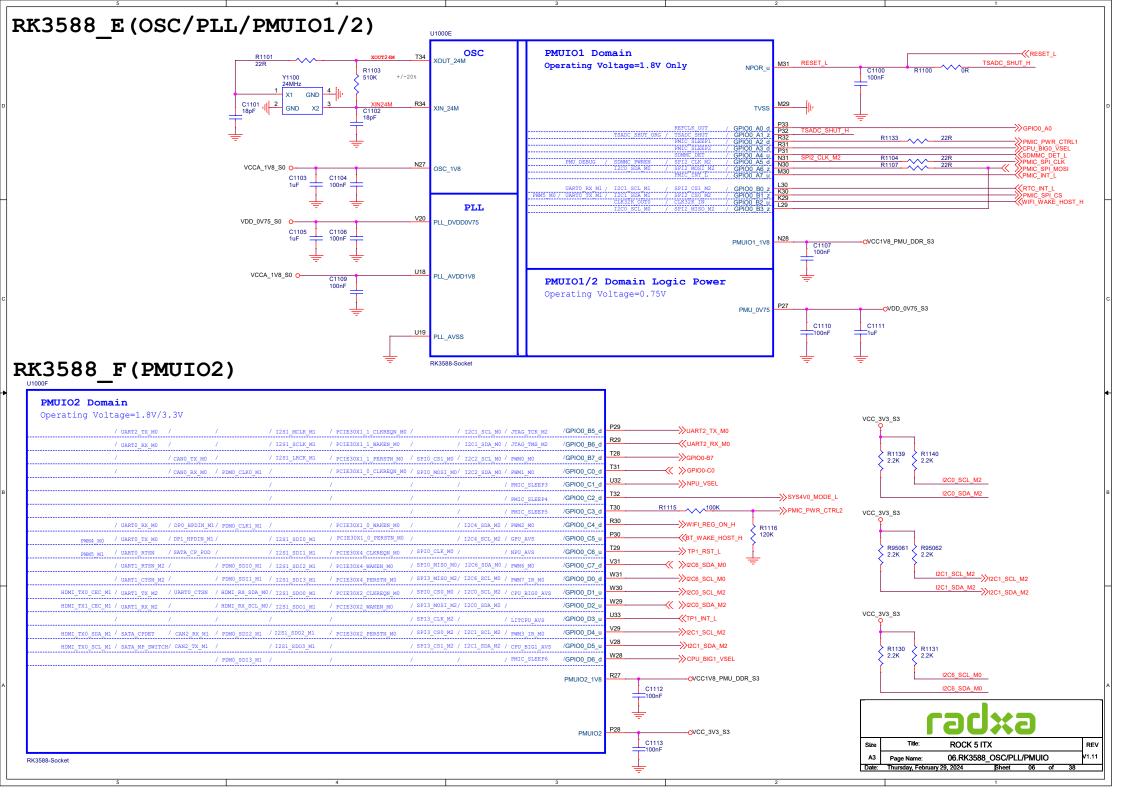


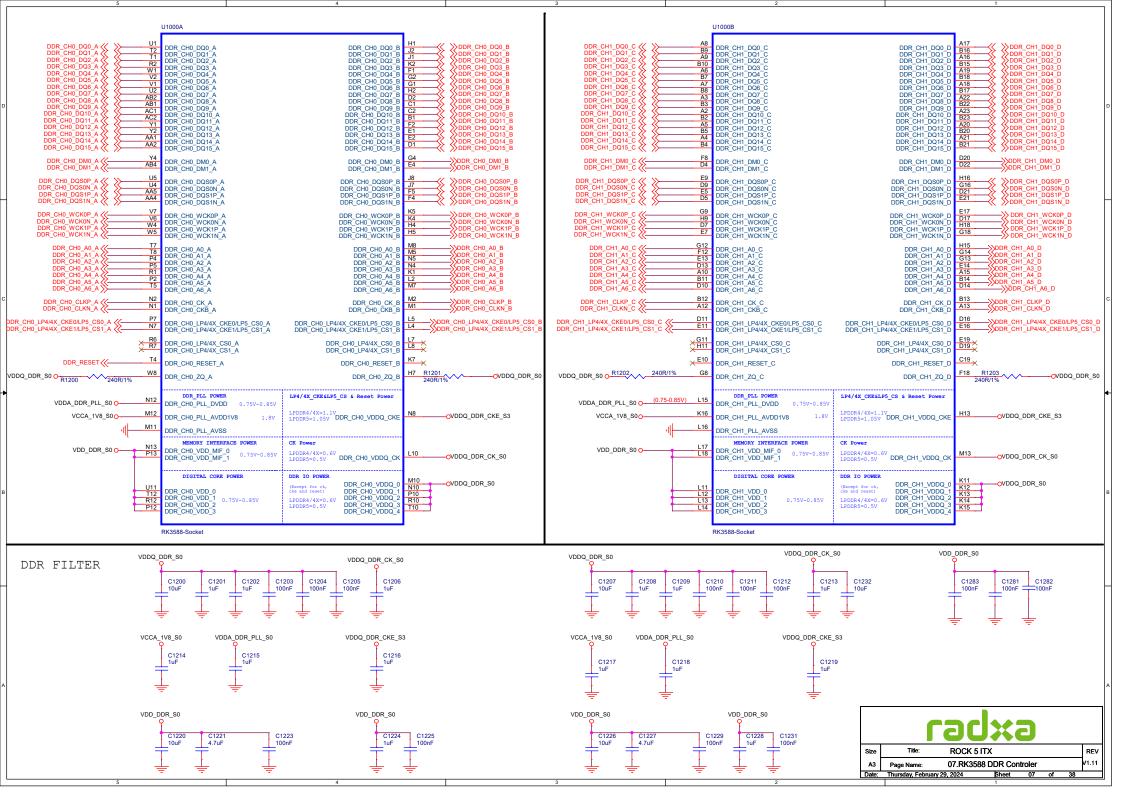


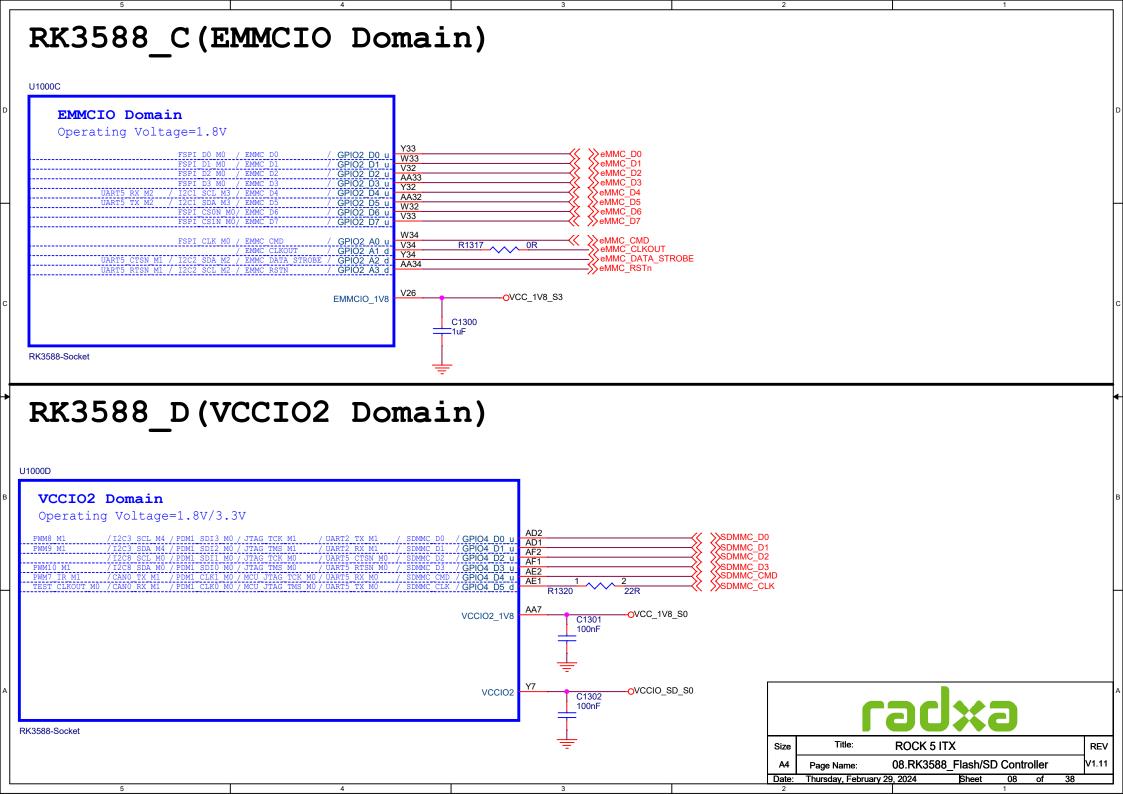


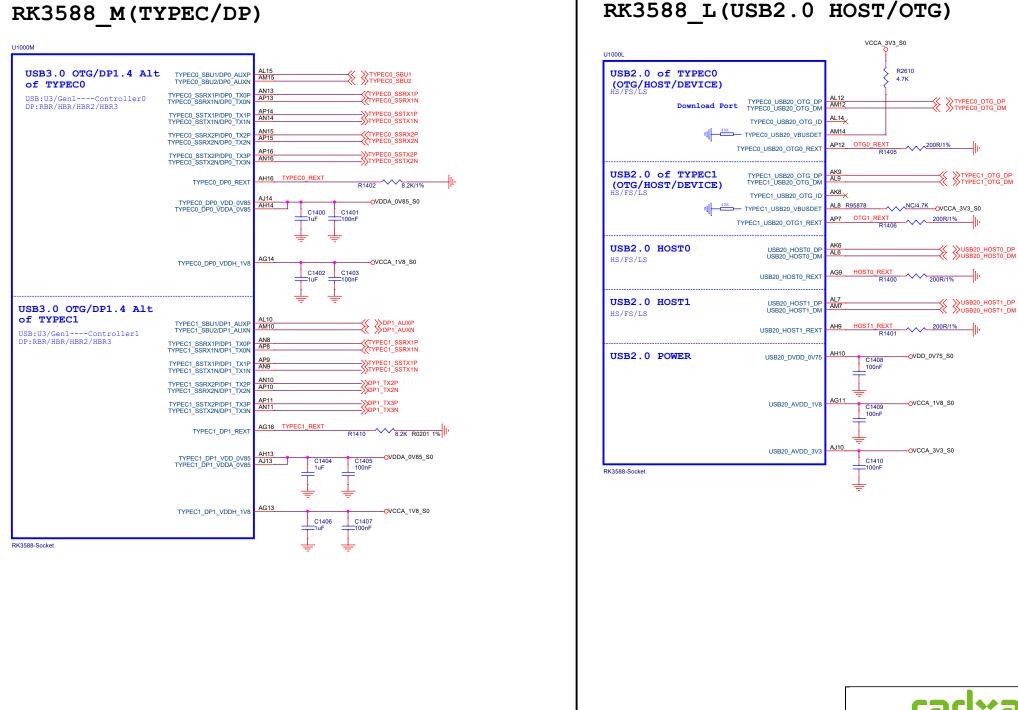
REV V1.11

A2 Page Name: 05.RK3588\_Power/GND

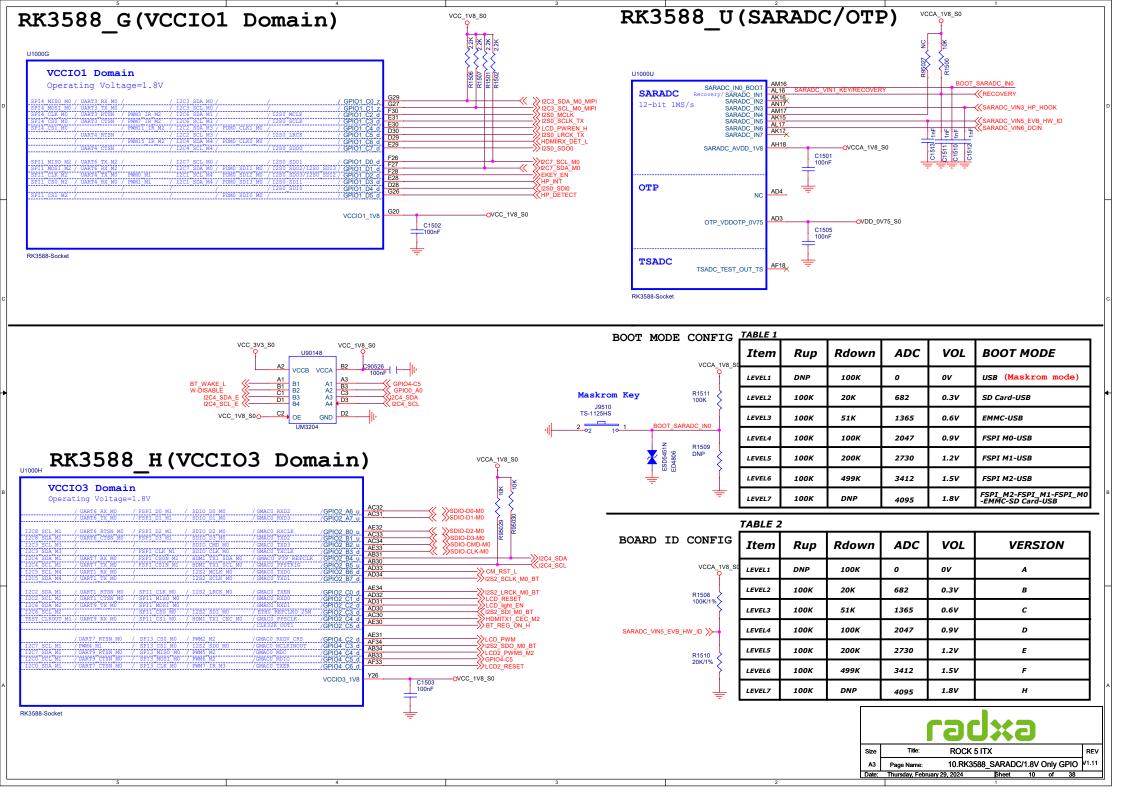


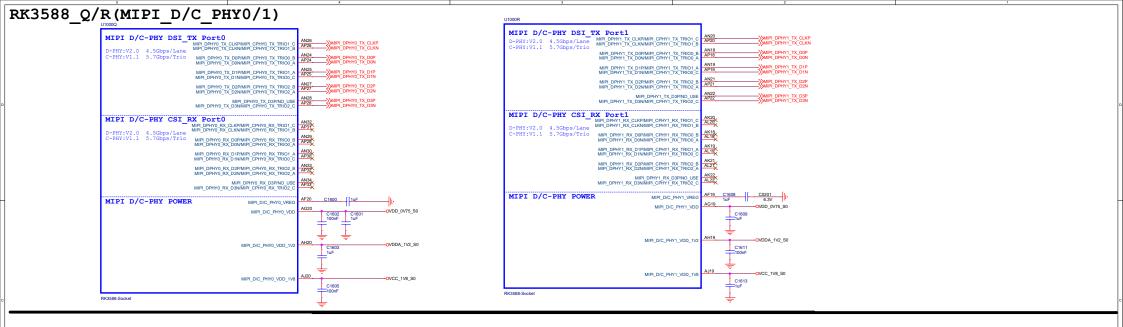




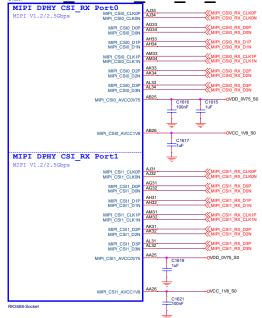


**ROCK 5 ITX** REV 09.RK3588 USB30/USB20 Ctrl Page Name: Date: Thursday, February 29, 2024 Sheet 09 of



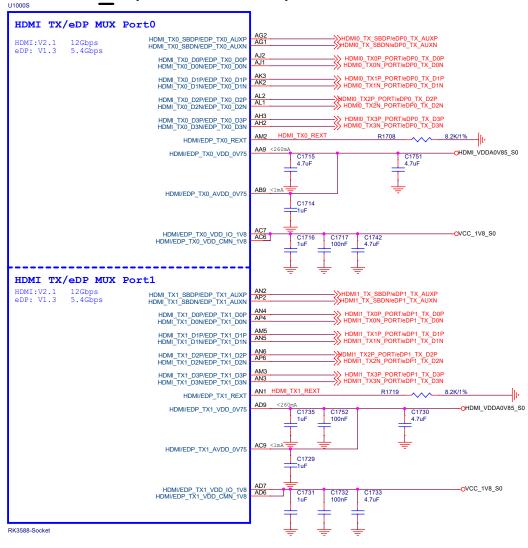




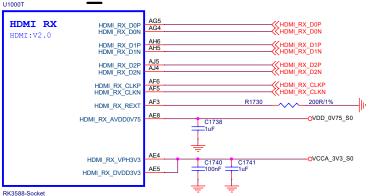




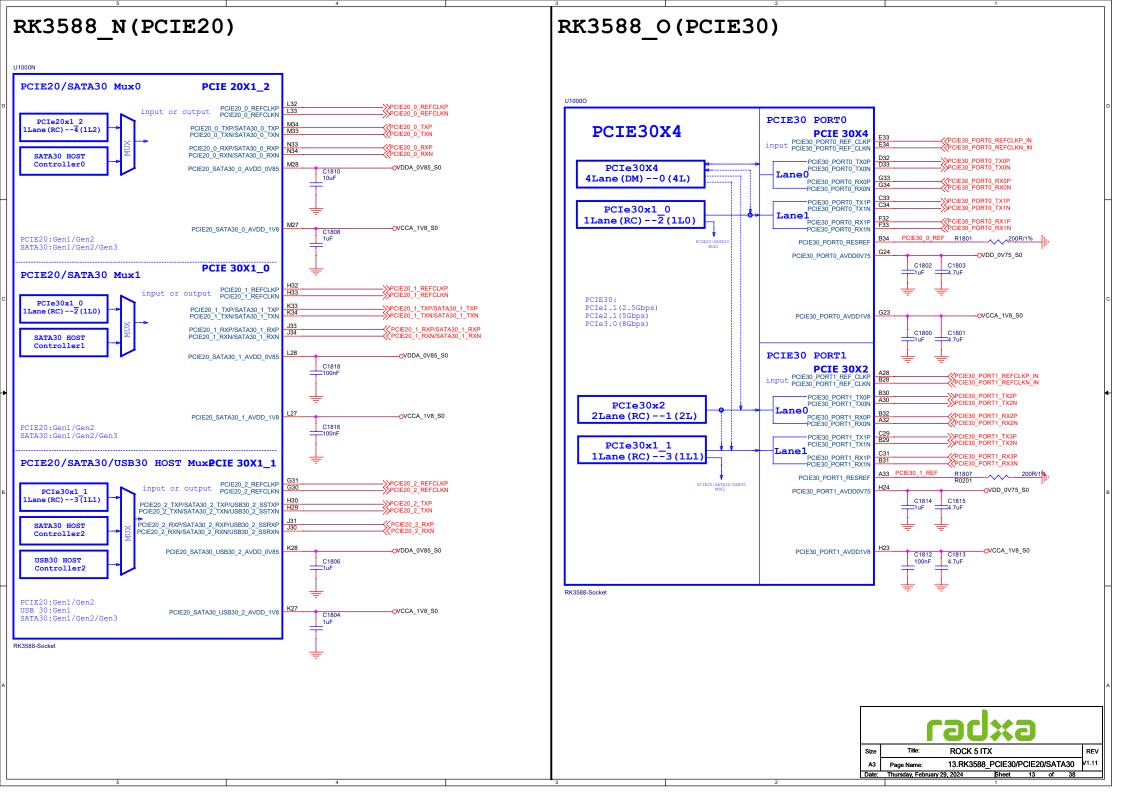
## RK3588 S(HDMI2.1 TX)



## RK3588 T(HDMI20 RX)

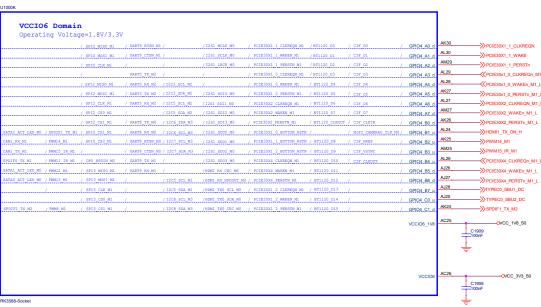




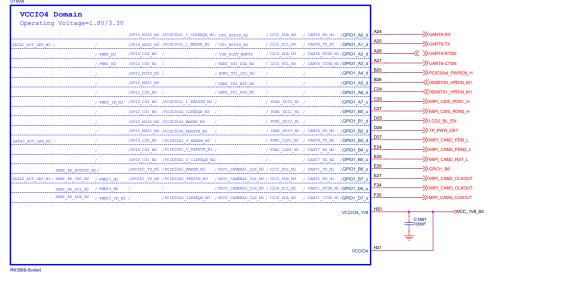


#### RK3588 J(VCCIO5 Domain) VCCIO5 Domain VCCIO6 Domain Operating Voltage=1.8V/3.3V PWM11 IR M0 /12C6 SCL M4 /FSFI D1 M2 /12S3 SCLK / SDIO D1 M1 /GMAC1 TXD3 /\_GPI03\_A1\_ →>>FSPI-D1 / GPIO3 A2 u /I283\_SDO --≪FSPI-D3 AUDDSM RP / SPI4 CS1 M1 / UART8 RTSN M1 / /I2S3 SDI / SDIO CMD M1 / GMAC1 TXCLK / GPIO3 A4 →>>EDP BL EN / MIPI CAMERAO CLK M1 / UART8 CTSN M1 / I2C4 SDA M0 /FSPI CLK M2 / / GPIO3 A5 / MIPI CAMERA1 CLK M1 / / MIPI\_CAMERA2\_CLK\_M1 / EDP\_BL\_PWM / GMAC1 RXD0 / GPIO3 A7 ── ✓ PCIE20X1 2 PERST / GPIO3 B0 u FWM2 M1 / MIPI CAMERA4 CLK M1 / UART2 TX M2 / / GMAC1 RXDV CRS / GPIO3 B1 GL3523 RESET PWM3\_IR\_M1 / / UART2 RX M2 / /I2S2 SDI M1 / / GMAC1\_TXER <pre / GPIO3 B2 /I2S2 SDO M1 / / GMAC1 TXD0 / GPIO3 B3 i -KSENSOR INT LCD2 / UART2 CTSN /12S2 MCLK M1 / GMAC1\_TXD1 GPIO3 B4 -≪CC INT L / UART3 TX M1 /1282 SCLK M1 / GMAC1 TXEN / GPIO3 B5 i / GMAC1 MCLKINOUT / GPIO3 B6 TP3\_INT\_L / I2C3 SCL M1 / SPI1 MOSI M1 / HDMI\_TX1\_HPD\_M1 / / GMAC1 PTP REF CLK / GPIO3 B7 →> USB HOST PWREN H / GMAC1\_PPSTRIG / GPIO3 CO d -≪EINT CTP2 / UART7 TX M1 / I2C3 SDA M1 / SPI1 MISO M1 / / PCIE30X2 BUTTON RSTN / UART7 RX M1 / / SPI1 CLK M1 / GMAC1 PPSCLK >>> 12C8\_SCL\_M4 / UART7 RTSN M1 / I2C8 SCL M4 / SPI1 CSO M1 / / GMAC1 MDC / GPIO3 C2 ( / UART7 CTSN M1 / I2C8 SDA M4 / SPI1 CS1 M1 / / GPIO3 C3 d —S ESPI-CS0 CAN2\_RX\_MO / PCIE30X4 CLKREQN M2 / UART5 TX M1 / FSPI\_CSON\_M2 / SPI3 CSO M3 / HDMI TX1 CEC M2 / / CIF D8 / GPIO3\_C4 CAN2\_TX\_M0 / PCIE30X4\_WAKEN\_M2 / UART5\_RX\_M1 / FSPI\_CS1N\_M2 / SPI3\_CS1\_M3 / HDMI\_TX1\_SDA\_M1 / / CIF D9 / GPIO3 C5 / SPI3 MISO M3 / HDMI TX1 SCL M1 / →>> HDMITX1 SCL M1 PCIE20X1 2 CLKREQN M0 / / I2C5 SCL M0 / SPI3 MOSI M3 / HDMI TX0 SCL M2 / →>> PCIE20 1 2 CLKREQn GPIO3 C7 PCIE20X1 2 WAKEN M0 / UART4 RX M1 / I2C5 SDA M0 / SPI3 CLK M3 / HDMI TX0 SDA M2 / GPIO3 D0 / PCIE20X1 2 PERSTN M0 / UART4\_TX\_M1 / / CIF D13 / GPIO3 D1 --≪HDMLRX CEC / PCIE30X2\_CLKREQN\_M2 / UART9\_RTSN\_M2 / I2C7\_SCL\_M2 / SPI0\_MOSI\_M3 /HDMI\_RX\_SCL\_M1 / →>> HDMI\_RX\_SCL\_M1 / GPIO3 D2 RK3588-Socke PMM10 M2 / PCIE30X2 WAKEN M2 / UART9 CTSN M2 / I2C7 SDA M2 / SPIO CLK M3 / HDMI RX SDA M1 / / PCIE30X2 PERSTN M2 / UART9 RX M2 / SPIO CSO M3 /HDMI RX HPDOUT M1/ HDMI TXO HPD M1/ MCU JTAG TCK M1 / GPIO3 D4 → SHDMIRX HPDOUT F / MCU JTAG TMS M1 / GPIO3 D5 VCCIO5 1V -OVCC 1V8 S0 OVCC 3V3 S0 C1902 VCCIO4 Domain √( )>12C8 SDA M4

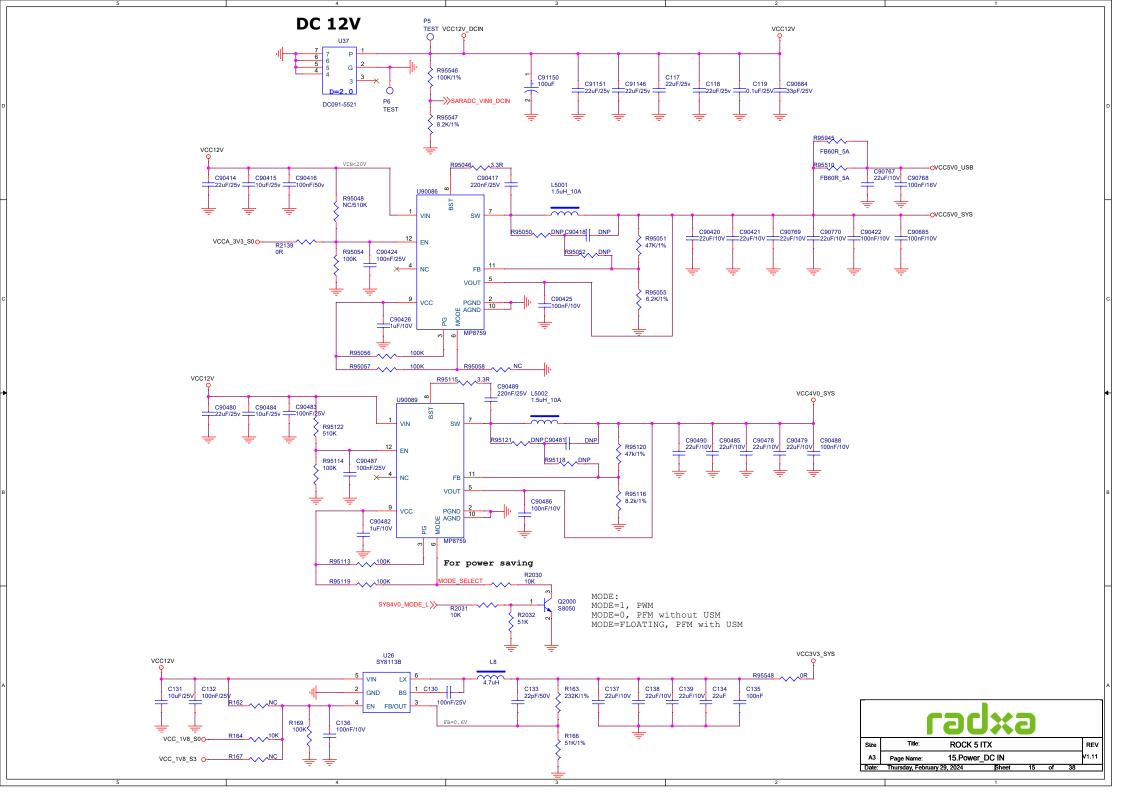
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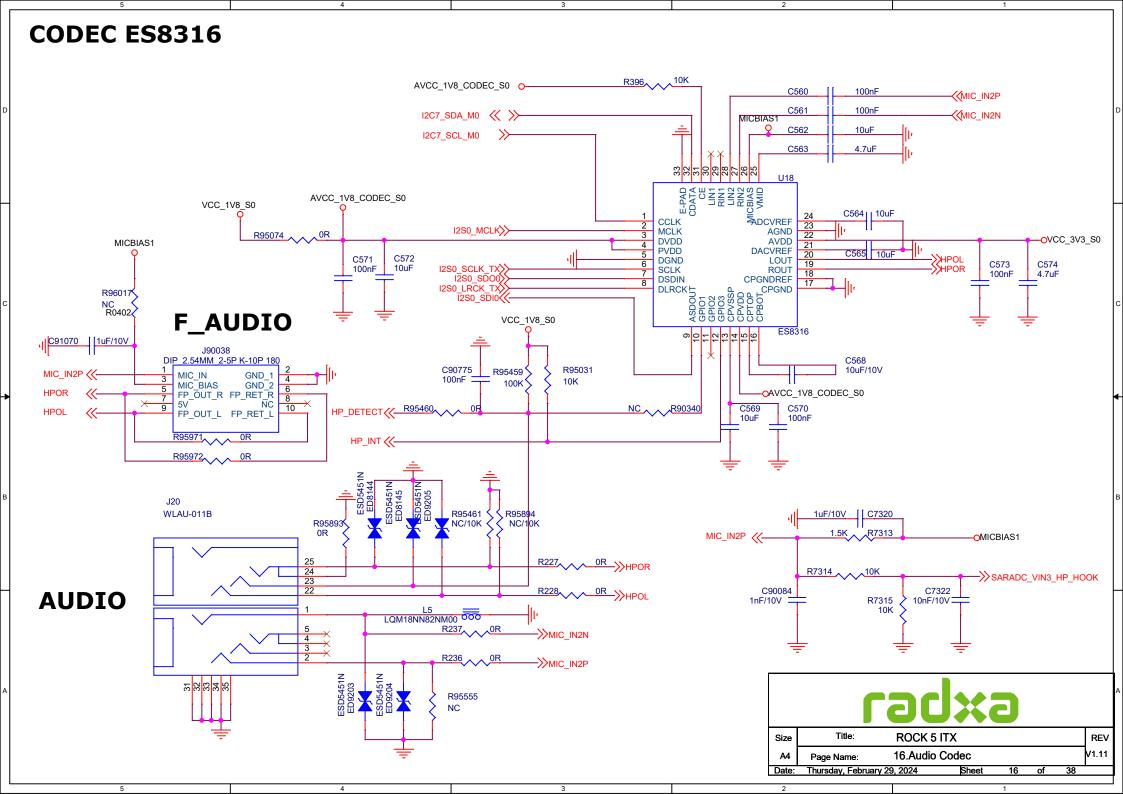


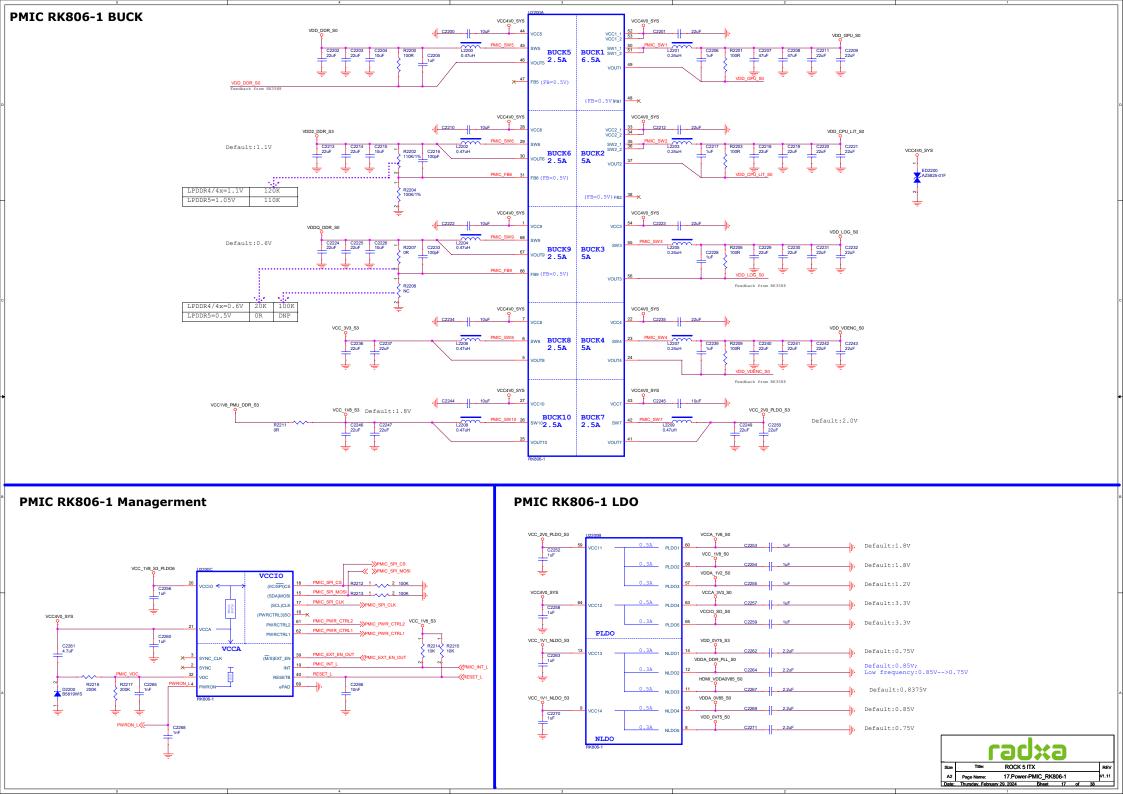
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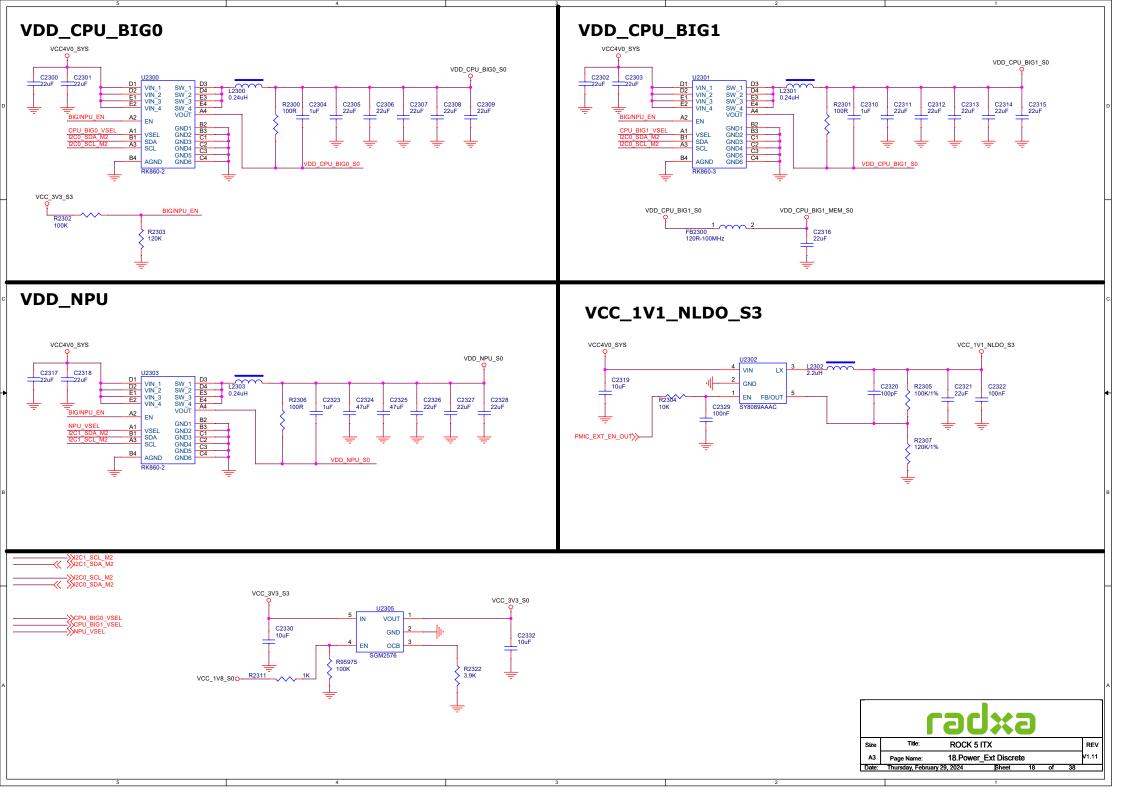


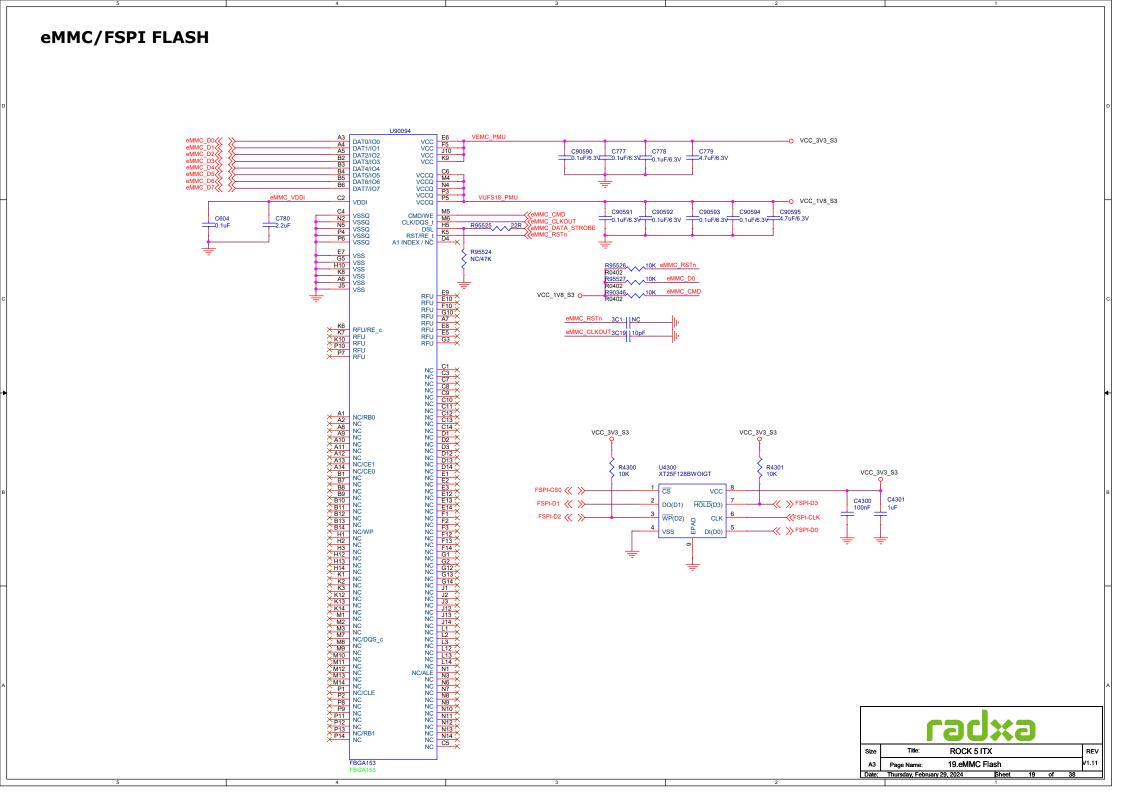
A2 Page Name: 14.RK3588\_1.8V/3.3V GPIO

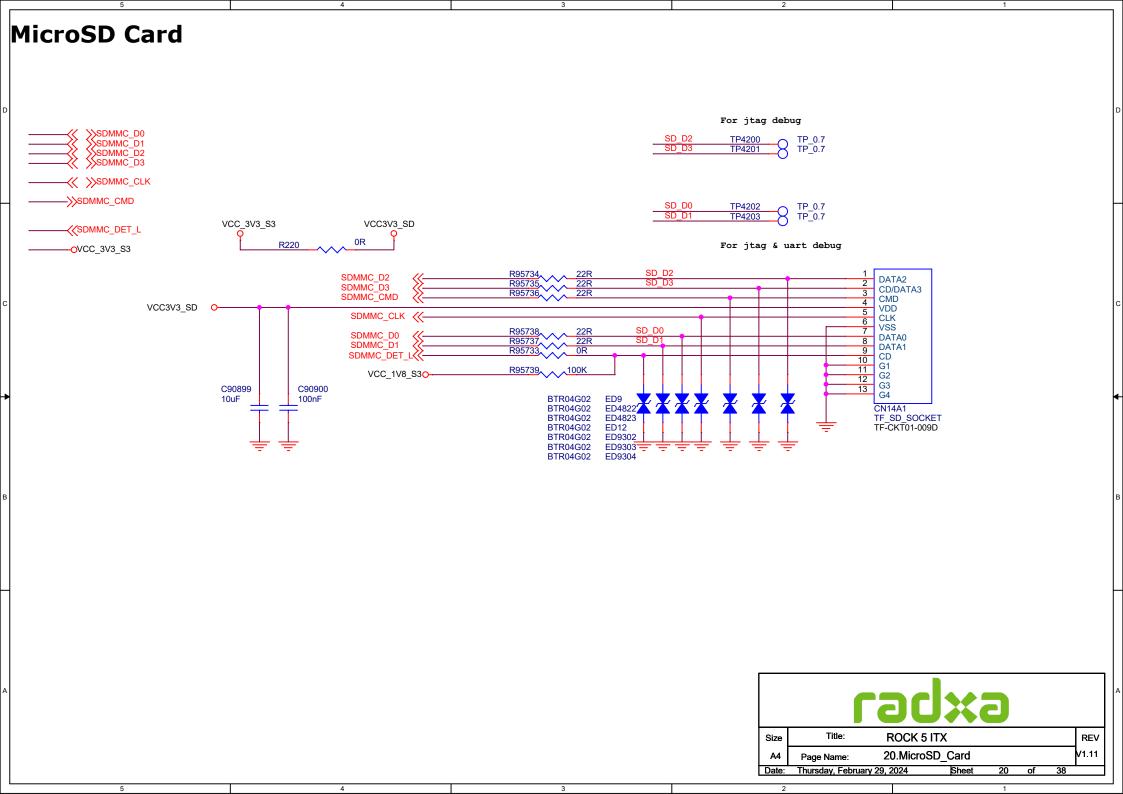


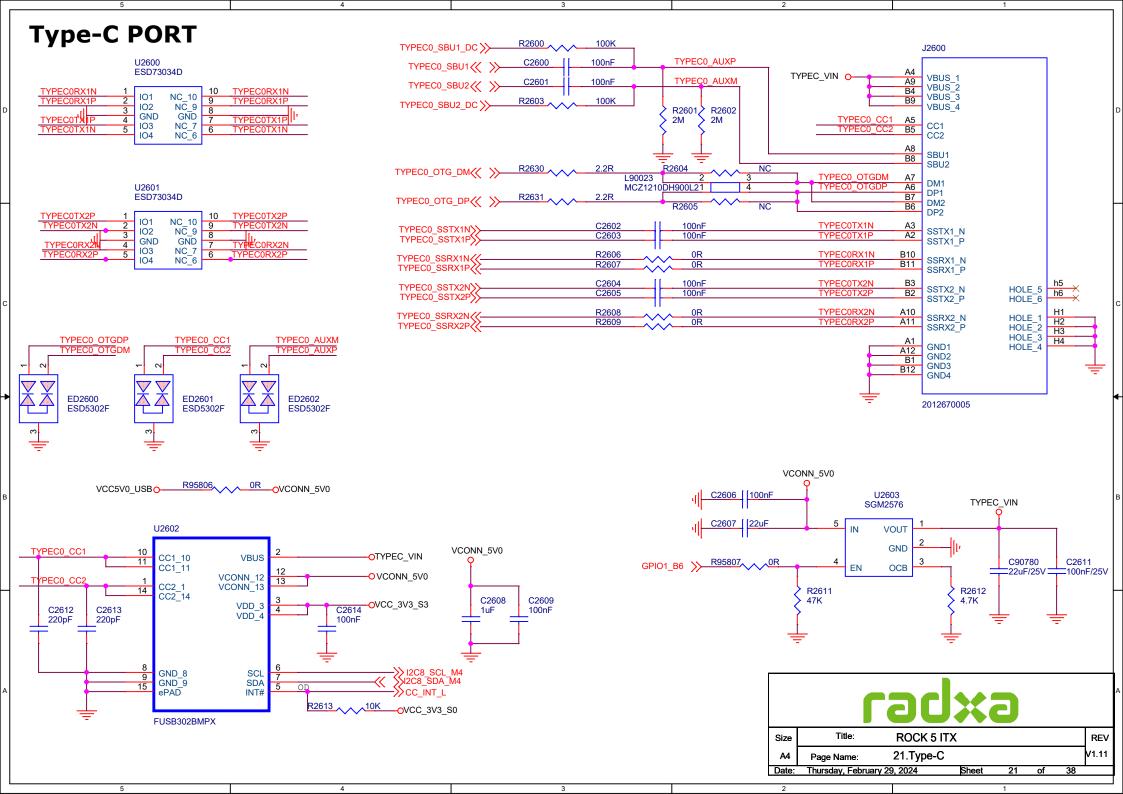






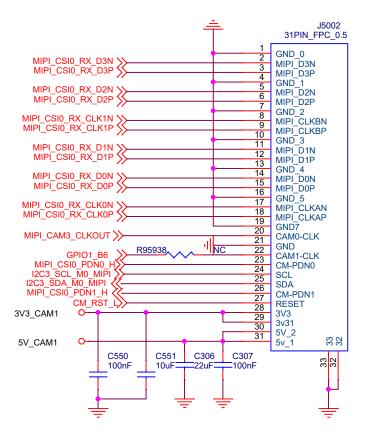


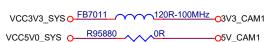




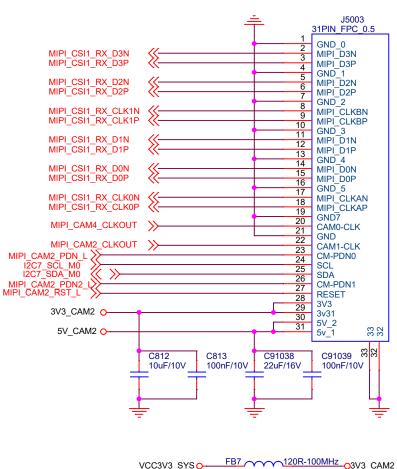
MIPI CSI RX

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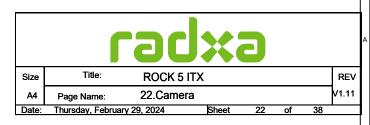




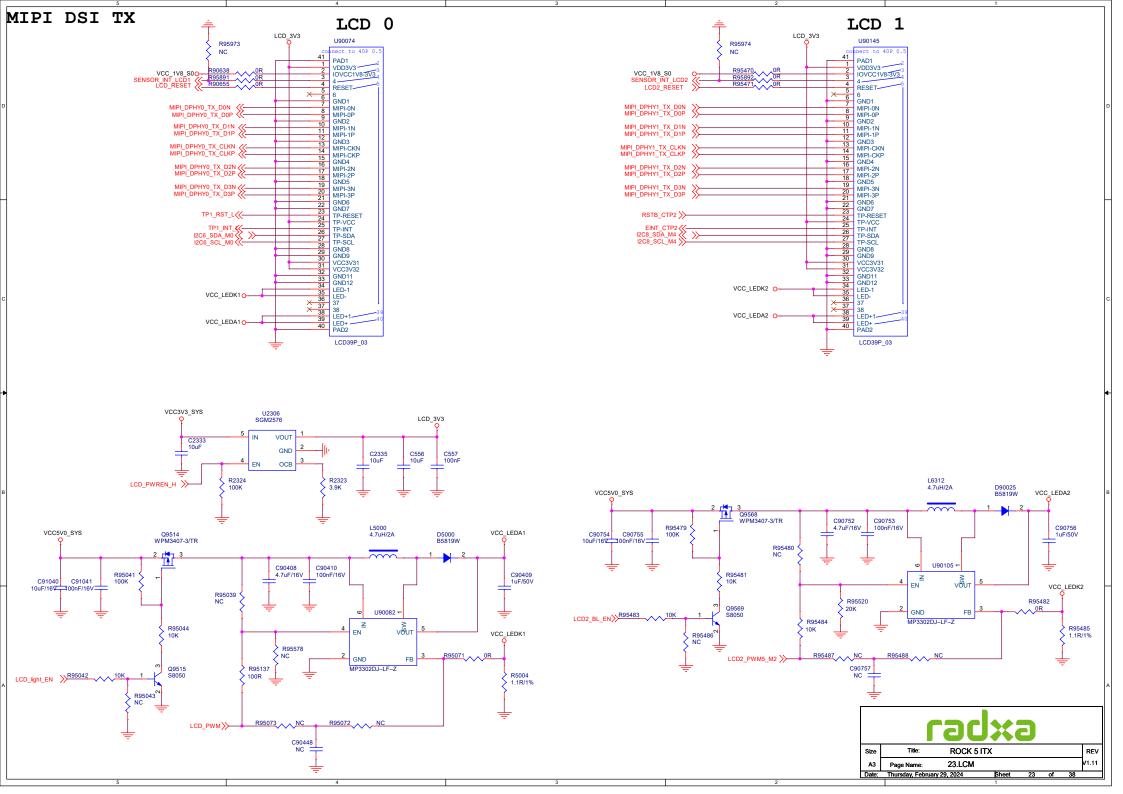
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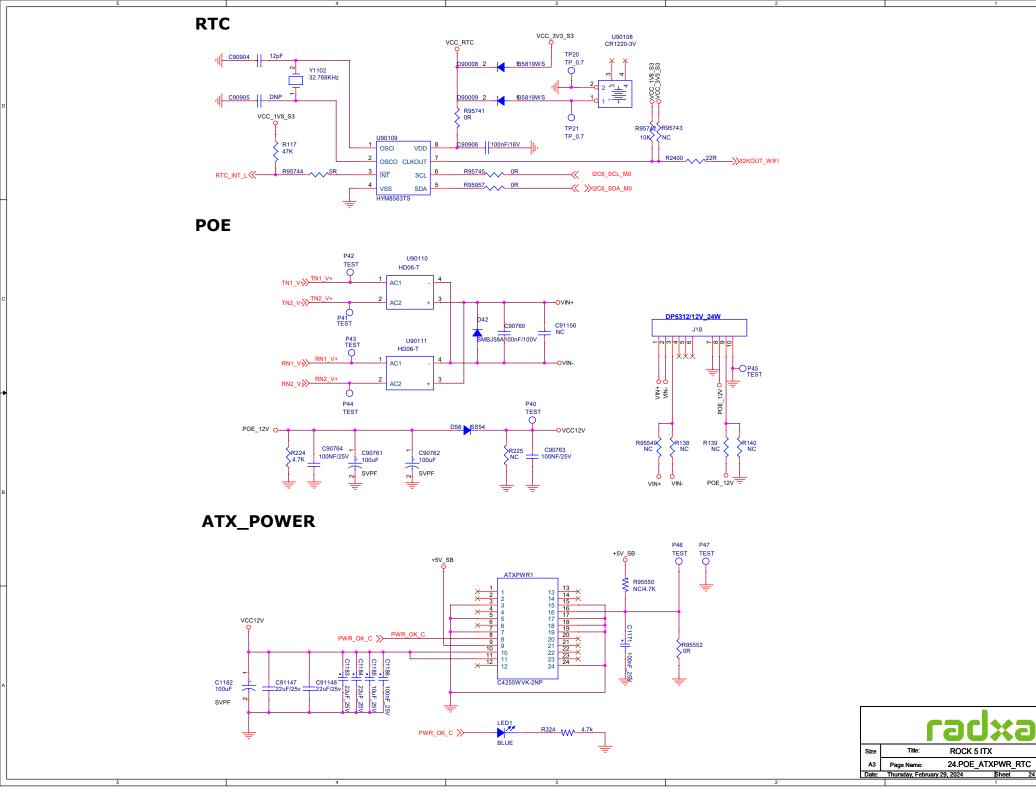




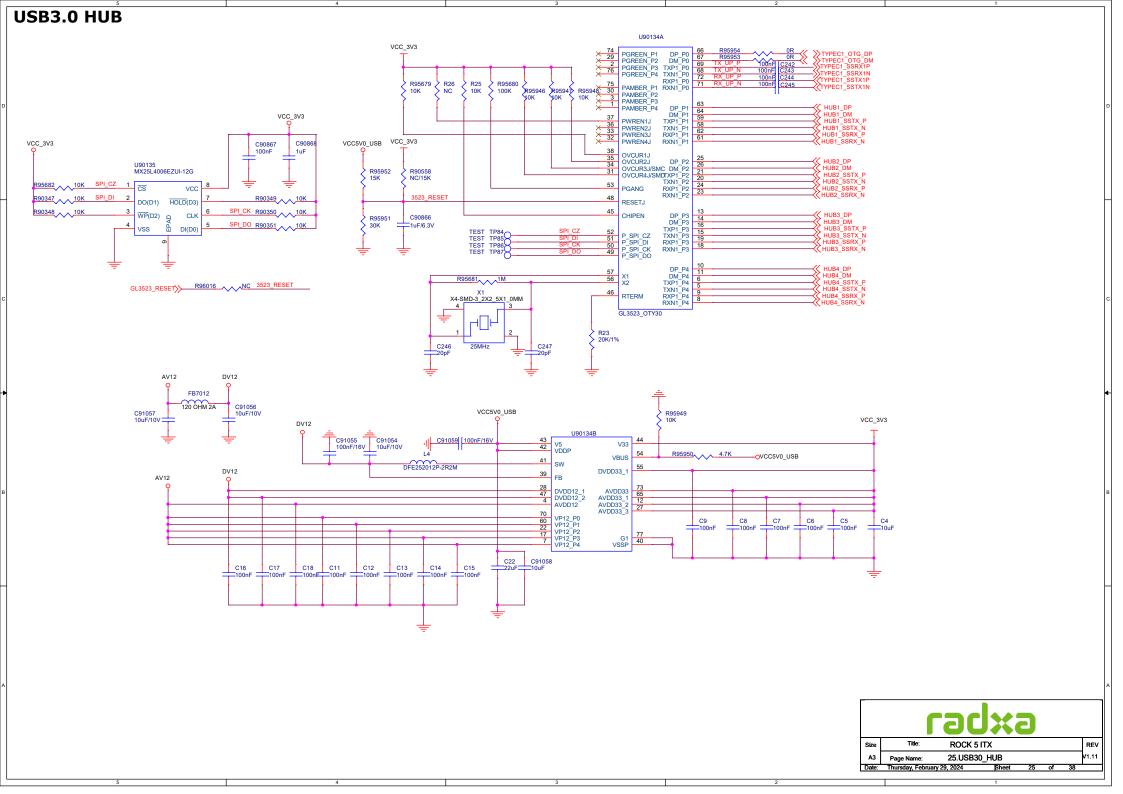


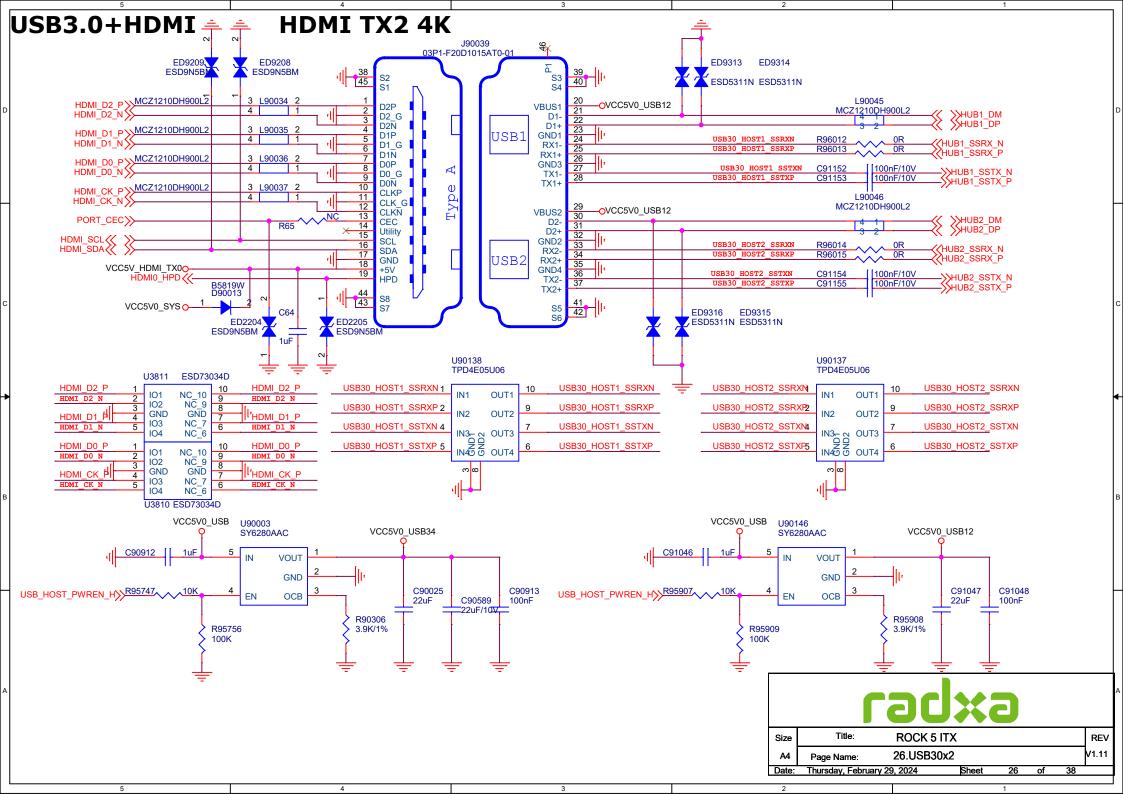
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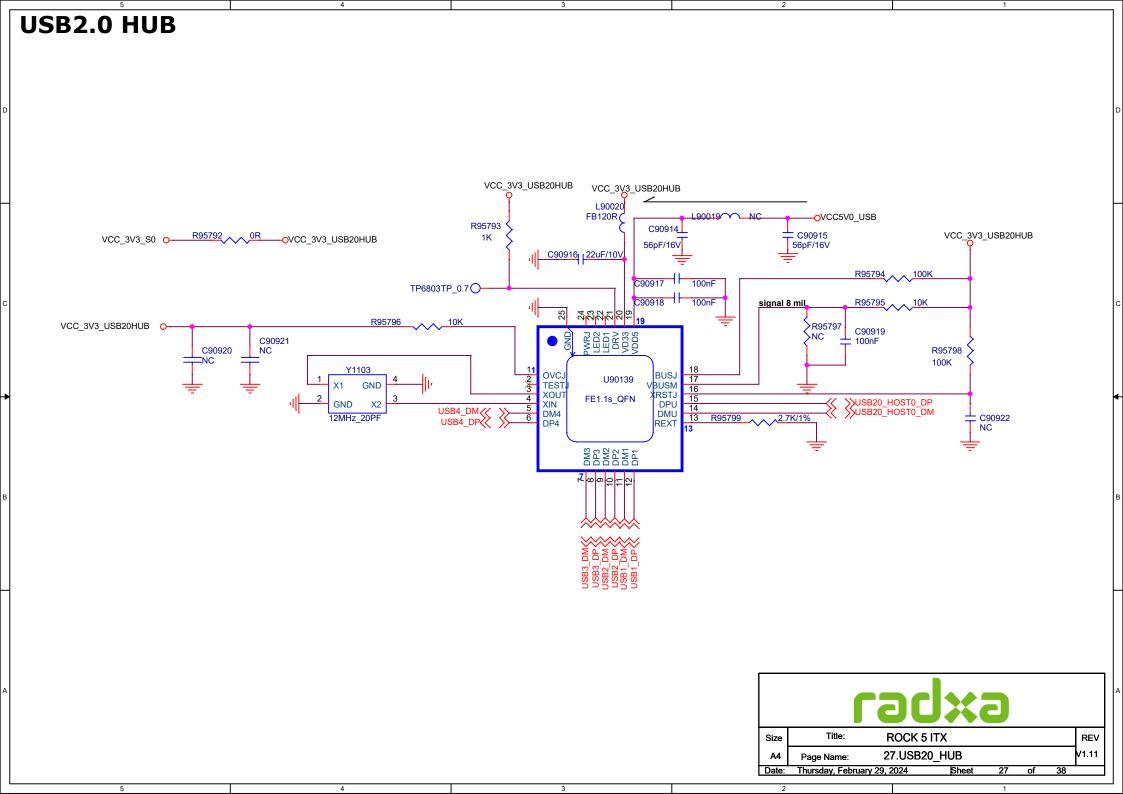


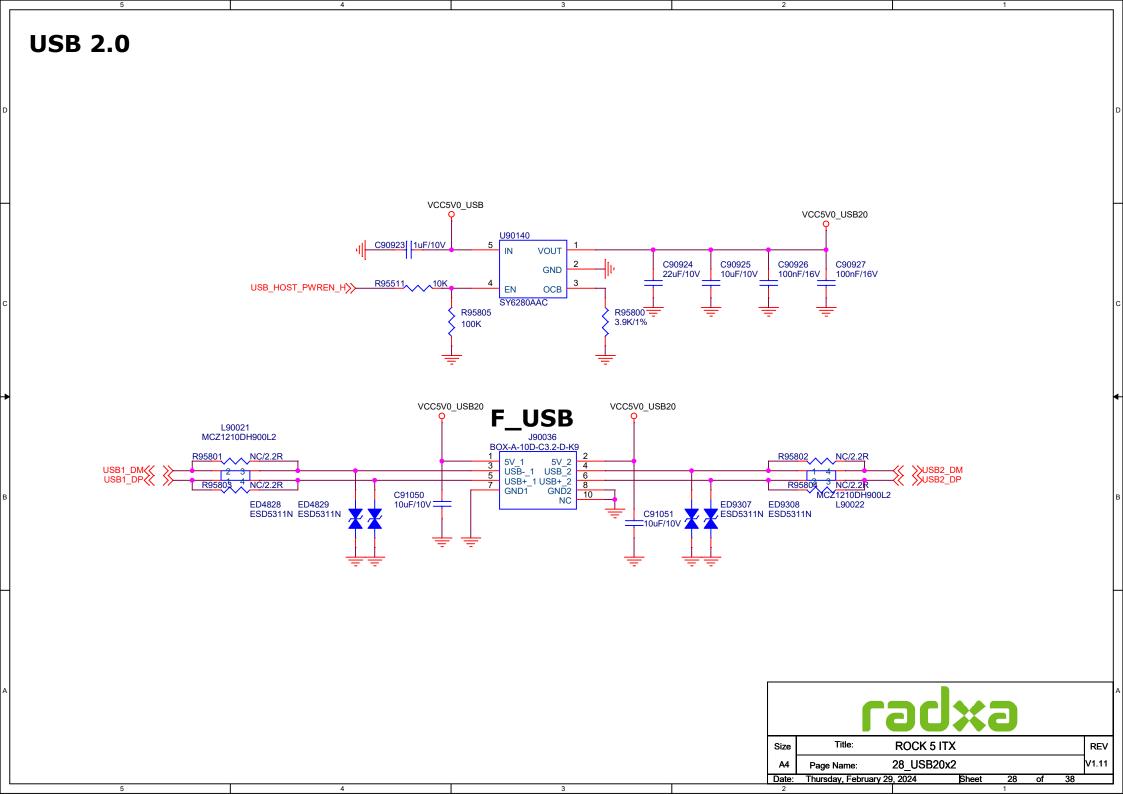


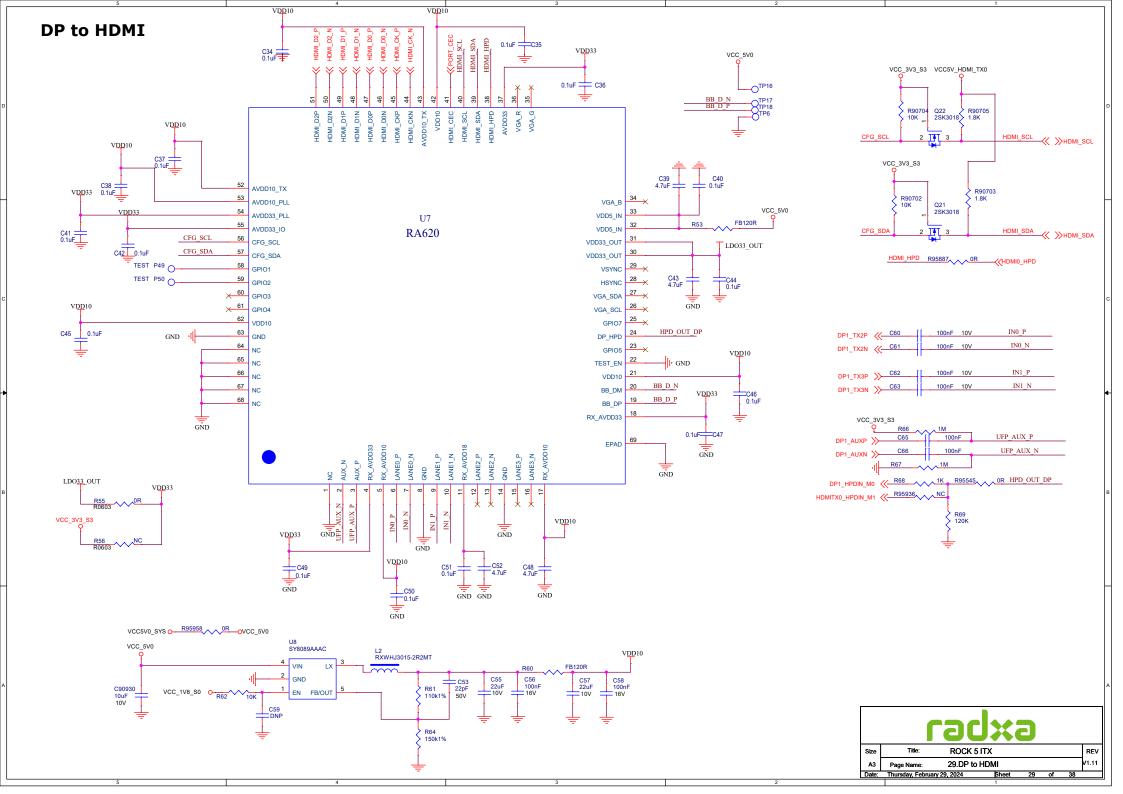
REV

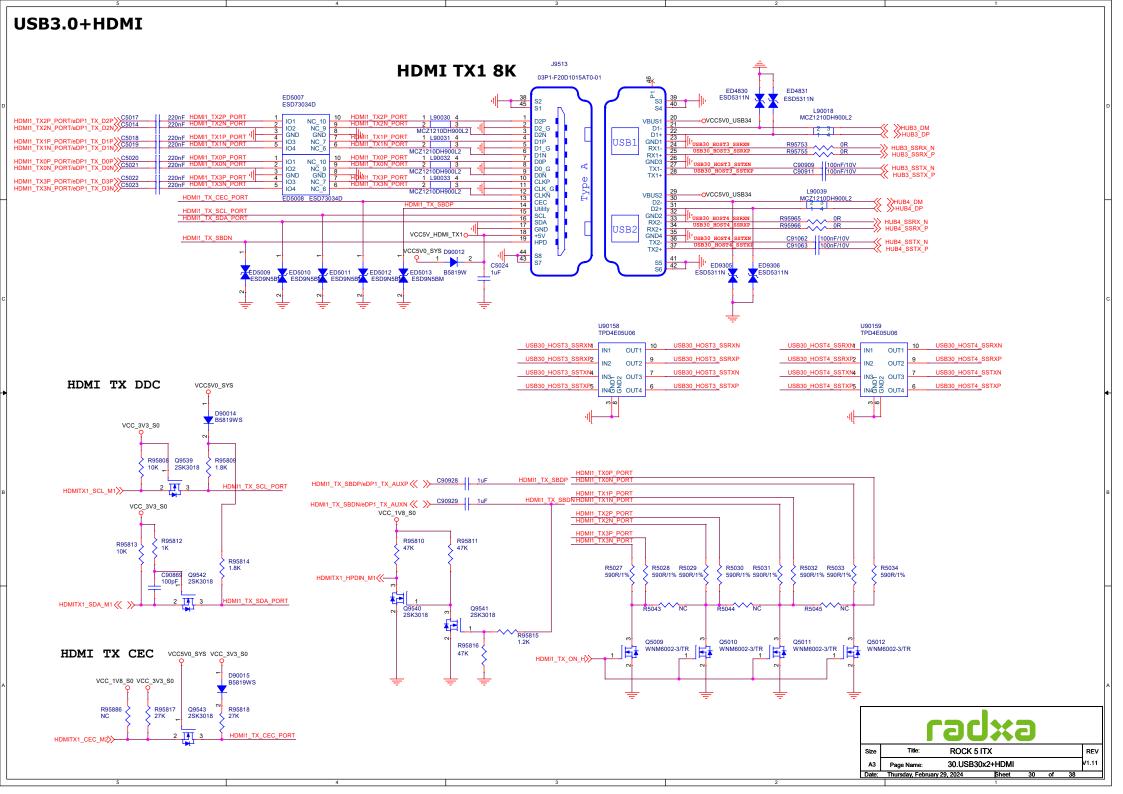


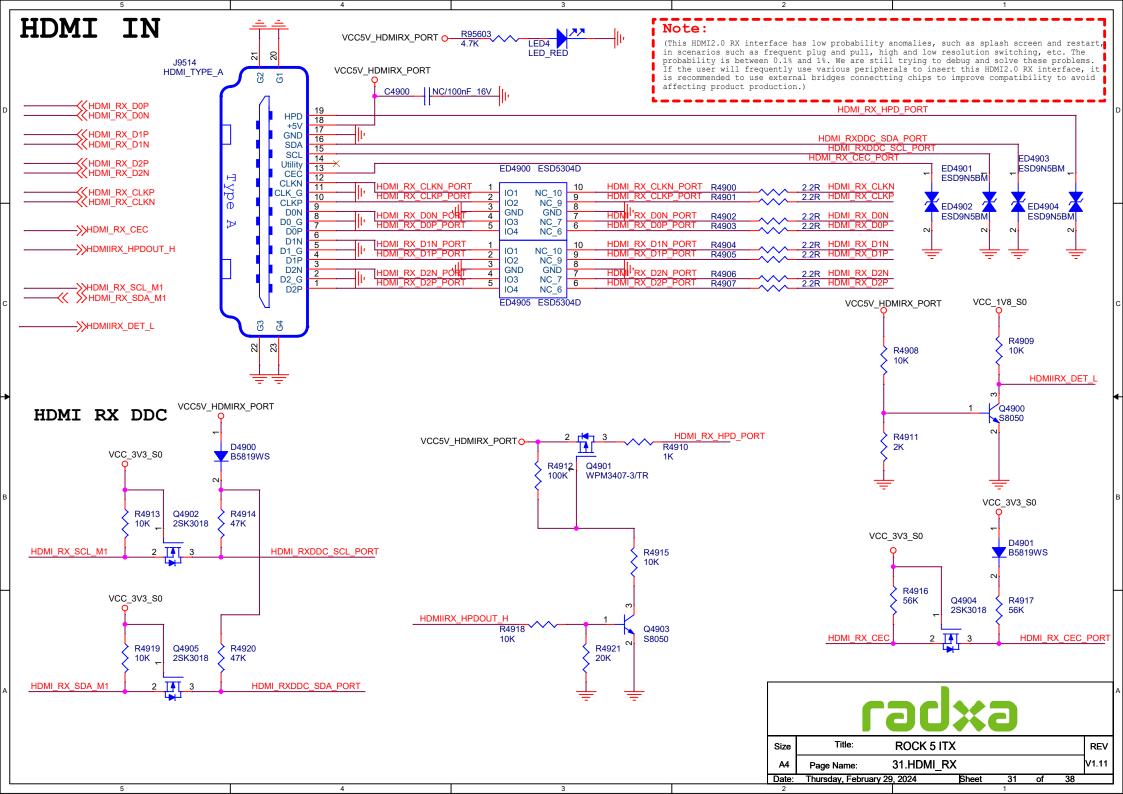


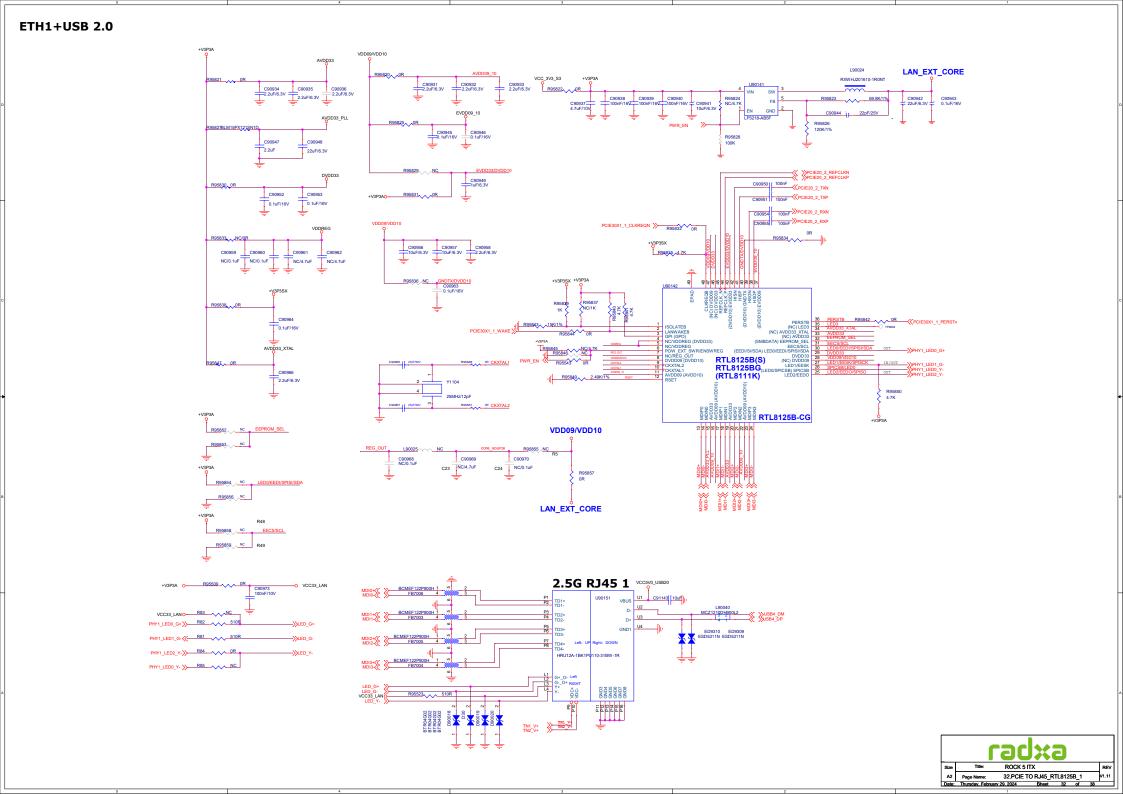












#### **ETH2+USB 2.0** VDD09/VDD10 PHY2 +V3P3A PHY2 AVDD33 PHY2 LAN\_EXT\_CORE\_PHY2 VCC\_3V3\_S3 C90979 C90960 2.2uF/6.3V 2.2uF/6.3V 2. R95862 OR EVDD09 10 PHY2 AVDD33 PLL PHY2 C90992 C90993 2.2uF DVDD33 PHY2 R95870\_0R C90998 PCIE20\_1\_2\_CLKREQn >> R95872 OR VDDREG PHY2 R95757 4.7K NC/0.1uF NC/0.1uF NC/4.7uF NC/4.7uF +V3P3SX\_PHY2 +V3P3A\_PHY2 R95762 . . . . OR R95764 OR CIE20X1\_2\_PERSTN C01000 0.1uF/16V PCIE20\_1\_2\_WAKEn AVDD33\_XTAL\_PHY2 R95769 OR R95770 . OR R95772 2.49K/1% C91011 2.2uF/6.3V R95773 4.7K ce CKXTAL2\_PHY2 ENIGW RTL8125B-CG +V3P3A PHY2 R95775 NC VDD09/VDD10\_PHY2 REG\_OUT\_PHY2 L90027 C91014 C91015 C23 NC/4.7uF +V3P3A PHY2 C24 NC/0.1uF R95779 NC PHY2 LAN EXT CORE PHY2 +V3P3A\_PHY2 R95782 NC 2.5G RJ45 2 Ų1 C91144 10µF L90041 MCZ1210DH900L2 WUSB20\_HOST1\_DM USB20\_HOST1\_DP D+ U3 R95785 NC Ų4 PHY2\_LED0\_G+>> R95784 510R PHY2\_LED2\_Y->> R95787 OR PHY2\_LED0\_Y- NC\_ GND3 GND4 GND6 GND6 GND6 GND7 R95788 510R

PCIE-PCIE2.0 Slot-Ekey VCC5V0\_SYS U90128 L90028 VIN LX OVCC3V3 Ekey C90794 C91024 1.7uH C91025 C91026 C91023 C91022 C90795 100nF 10uF 100nF R95875 10uF C90793 100nF **GND** BS 22pF 232K/1% 22uF/6.3V 0.1uF 0.1uF R95876 10K ΕN FB/OUT FB=0.6V SY8113B C91028 100nF EKEY EN R95877 49.9K/1% L90029 M2 NGFF KEY E MCZ1210DH900L2 **GND** USB3\_DP SUSB3\_DM NC OVCC3V3\_Ekey 3.3V 5 7 NC 3.3V 4 NC/2.2R R95791 **GND** GPIO LED 9 SDIO-CLK-M0 > ⟨I2S2 SCLK M0 BT SDIO CLK PCM-CLK SDIO-CMD-M0 | 12S2\_LRCK\_M0\_BT | 12S2\_SDI\_M0\_BT SDIO\_CMD PCM-SYNC 13 12 R90626 SDIO\_D0 PCM-IN 15 14 R90625 V/V OR SDIO-D1-M0 -{</a>( 12S2 SDO M0 BT SDIO D1 PCM-OUT 17 16 SDIO-D2-M0 SDIO D2 NC 19 18 SDIO D3 GND 21 20 WIFI\_WAKE\_HOST\_H) (BT WAKE HOST H WIFI HOST WAKE BT HOST 23 WIFI\_REG\_ON\_H ->>UART6-RX WIFI\_REG\_ON UARTO\_RXD M.2 NGFF E-KEY **(**UART6-TX GND UART0\_TXD C91029 II100nF/10V 35 37 **VUART6-CTSN** PCIE20 1 TXP/SATA30 1 TXP > TX-P UARTO CTS C91030 100nF/10V PCIE20\_1\_TXN/SATA30\_1\_TXN WART6-RTSN TX-N UARTO\_RTS 39 41 38 GND NC 40 PCIE20 1 RXP/SATA30\_1\_RXP RX-P NC 42 43 PCIE20\_1\_RXN/SATA30\_1\_RXN **(**BT\_REG\_ON\_H RX-N BT\_REG\_NO 45 47 44 GND NC PCIE20\_1\_REFCLKP CLK-P NC 49 48 PCIE20\_1\_REFCLKN CLK-N NC 51 50 GND 32KOUT WIFI RTC CLKO 53 CPCIE30x1\_0\_PERSTn\_M1\_L PCIE30x1\_0\_CLKREQn\_M1\_L CLKREQ0 PĒRSTO 55 57 54 56 R95932 0R PCIE30x1\_0\_WAKEn\_M1\_L PEWAKE0 BT WAKE L NC R95933 √ OR ₩-DĪSABLE GND NC 59 61 58 R95934 12C4 SDA E NC I2C DATA 60 R95935 NC 12C CLK 63 62 65 67 GND NC 64 66 NC NC NC NC 68 69 GND 71 70 R95931 NC 73 75 BT WAKE OVCC3V3\_Ekey NC 3.3V 74 **GND** 3.3V GND GND GND GND 81 79 82 1 92 გ ს HOLE1 Title: **ROCK 5 ITX** REV Size 34 PCIE-PCIE20 Slot-Ekey Page Name: Date: Thursday, February 29, 2024

