Intel Xeon Phi Architecture

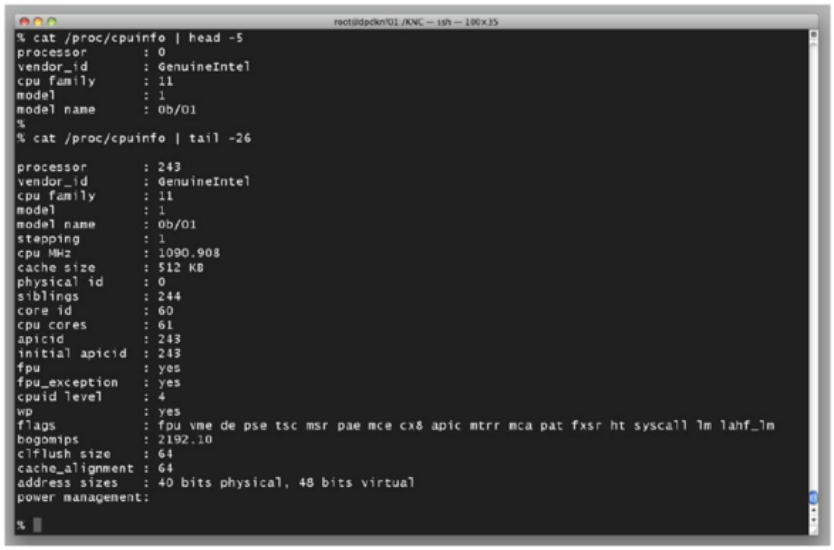
4:00 PM - November 12, 2012 by Patrick Kennedy

Intel has a vast portfolio of technology its engineers have developed, and Xeon Phi unquestionably taps some of that. However, the Many Integrated Core architecture is notably more than a bunch of modified Pentium processors manufactured at 22 nm. Some of its notable attributes include:

- An in-order, dual-issue x86 design with 64-bit support
- Four threads per core, and up to 61 cores per coprocessor
- 512-bit SIMD for wider vectors
- 512 KB of L2 cache per core (up to 30.5 MB per Xeon Phi)
- 22 nm tri-gate transistors
- Red Hat Enterprise Linux 6.x or SuSE Linux 12+ support
- 6 or 8 GB of GDDR5 per card

You'll notice that even the highest-end Xeon Phi wields far fewer cores than a typical GPU. However, you cannot compare an MIC core to a CUDA core, for example, on a 1:1 basis. Just *one* Phi core is quad-threaded with a 512-bit SIMD unit. A fair comparison requires getting past marketing's definition of a "core."

It's also interesting that the card runs Linux. This probably isn't a solution you'd want to run a LAMP package on, but I would also guess that someone will try to do it anyway. You can SSH into the Xeon Phi card, though, to find out more about the hardware. We were advised that the following screenshot came from a pre-production board.



```
% cat /proc/cpuinfo | head -5
processor       : 0
vendor_id       : GenuineIntel
cpu family      : 11
model           : 1
model name      : 0b/01
%
% cat /proc/cpuinfo | tail -26

processor       : 243
vendor_id       : GenuineIntel
cpu family      : 11
model           : 1
model name      : 0b/01
stepping        : 1
cpu MHz         : 1090.908
cache size      : 512 KB
physical id     : 0
siblings        : 244
core id         : 60
cpu cores       : 61
apicid          : 243
initial apicid  : 243
fpu             : yes
fpu_exception   : yes
cpuid level     : 4
wp              : yes
flags           : fpu vme de pse tsc msr pae mce cx8 apic mtrr mca pat fxsr ht syscall lm lahf_lm
bogomips        : 2192.10
clflush size    : 64
cache_alignment : 64
address sizes   : 40 bits physical, 48 bits virtual
power management:

%
```

Figure 3: Screenshot of an ssh session on a pre-production Intel Xeon Phi Coprocessor with the beginning and end of the 6100 lines of "cat /proc/cpuinfo"

In the following diagram of a MIC architecture core, Intel claims that less than two percent of the core and cache die area is x86-specific logic. Although the Xeon E5-2680 CPUs also found in the Stampede supercomputer are made up of 2.27 billion transistors each, the lineage of x86 comes from the 20 000- to 30 000-transistor 8086 processor.

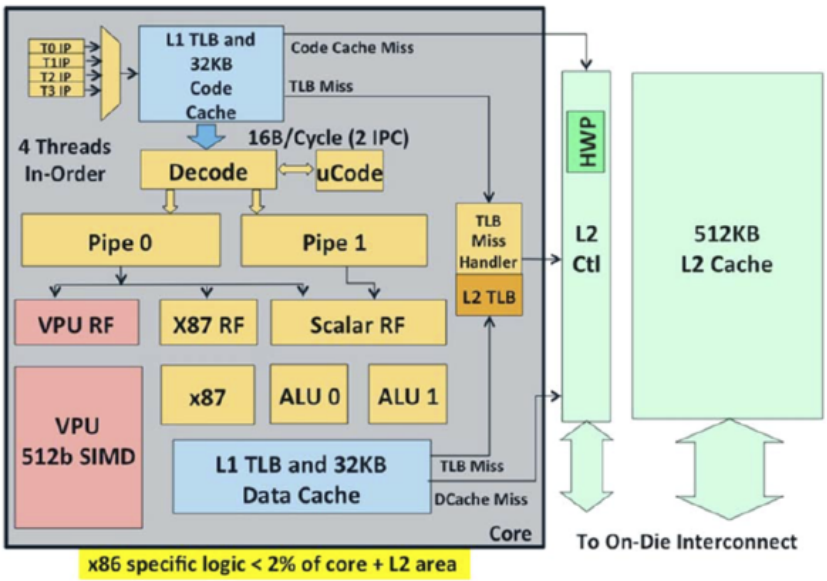


Figure 4: Knights Corner Core

Zoom

Of course, even today's desktop CPUs are incredibly complex, emphasizing the importance of getting data to and from where it needs to go as expediently as possible. Like the Sandy and Ivy Bridge-based CPUs, the prototype product code-named Knights Corner employs a ring bus interconnect to most effectively maximize throughput and available die area. By also giving each core lots of cache, the processor is able to avoid the performance hit it'd take if each core instead needed to be fed constantly from the GDDR memory controller stops.

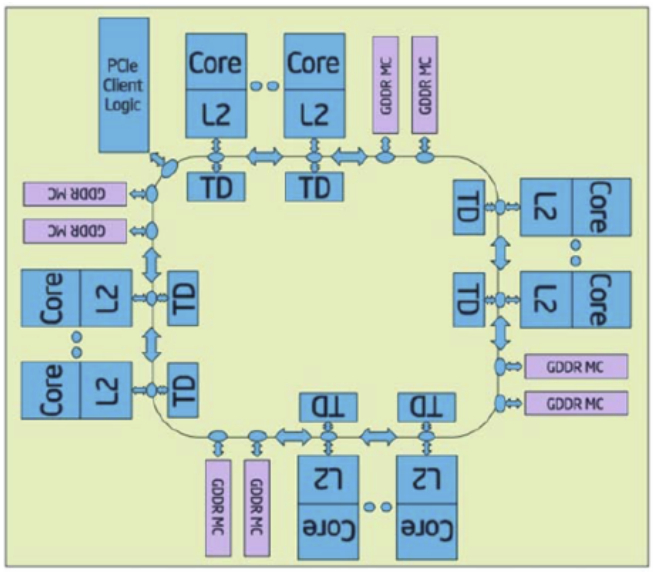


Figure 5: Knights Corner Microarchitecture

Zoom

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Intel Xeon Phi Hardware

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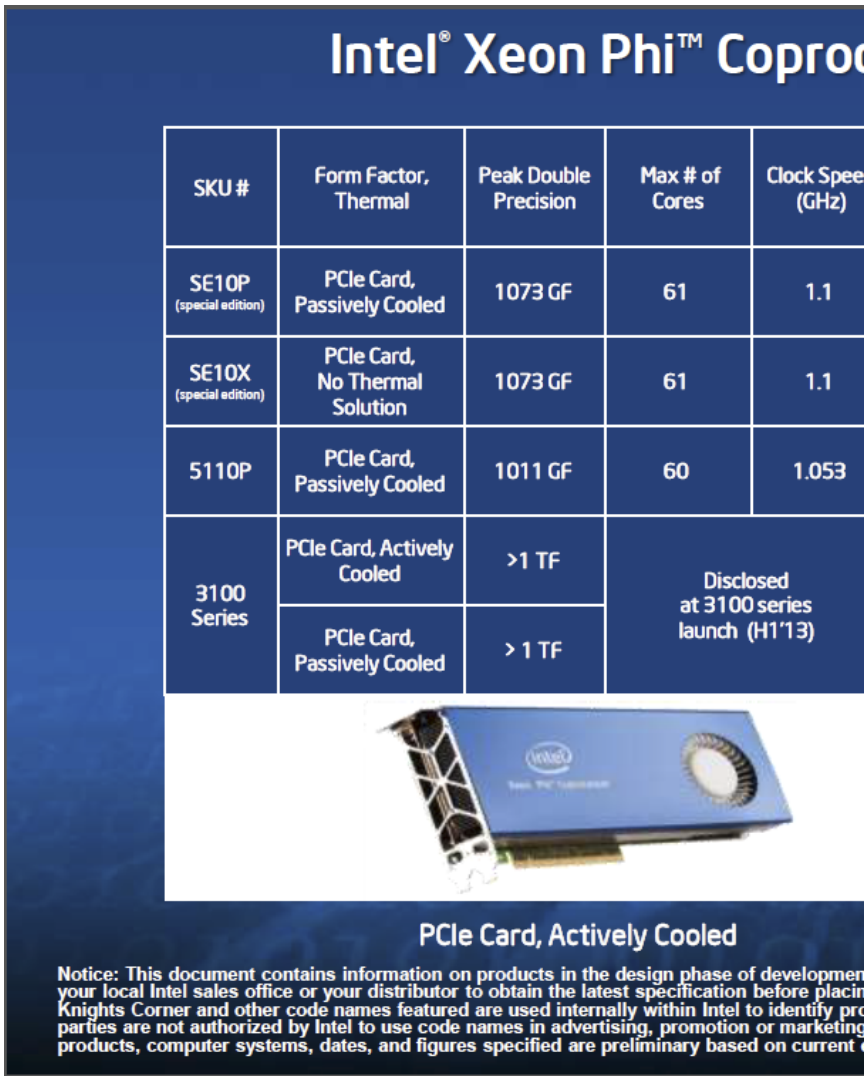
Intel is launching one Knights Corner-based product family today: the Xeon Phi Coprocessor 5110P. It's expected to see general availability in early January of next year, and it's expected to cost just under $2700. Later on in 2013, we'll see Intel's Xeon Phi Coprocessor 3100-series.

Confused by all of the code names with Knights in them? Intel's product team has taken some criticism for repeated use of the word in its technology roadmaps. Here's the run-down, though:

- Knights Ferry (pre-production hardware)
- Knights Corner (2012-2013 product, now known as Xeon Phi)
- Knights Landing (second-gen product)

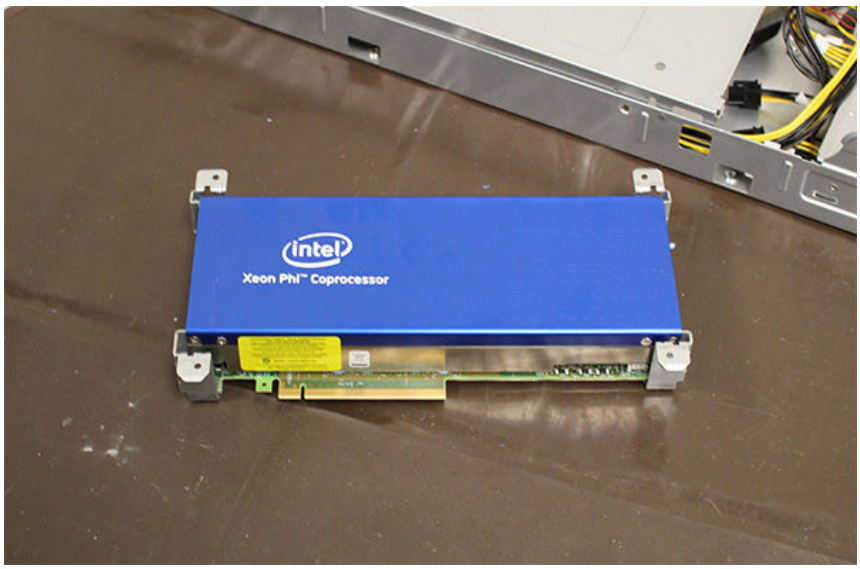


The Xeon Phi Coprocessor 5110P and 3100-series products are based on similar hardware, but wield specifications that more specifically target compute-bound applications. As you can see in the reference table above, Intel's two families employ different cooling solutions. The 5110P is passively-cooled, while the 3100-series will eventually ship in actively- and passively-cooled trims.

The 5110P includes more memory and greater peak bandwidth for workloads constrained by throughput. Add a 60-core processor running in excess of 1 GHz and you end up with a 225 W TDP. Although it doesn't feature active cooling, the 5110P still requires substantial airflow to dissipate all of that heat. As such, it's intended exclusively for rack-mounted servers with chassis fans able to force air through the card's heat sink and rear bracket.

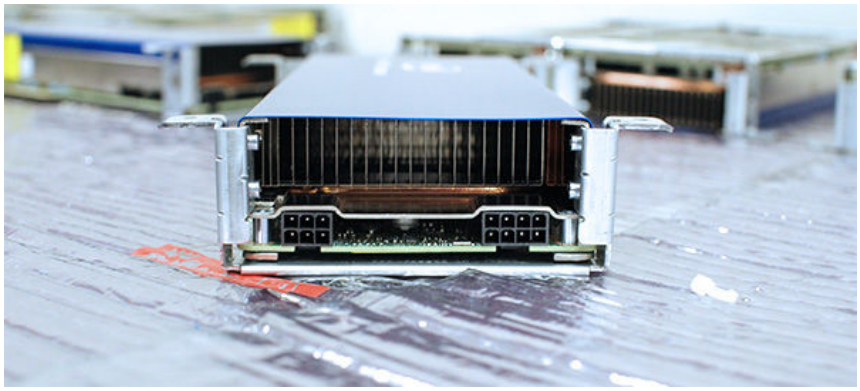
Meanwhile, the 3100-series cards are specified for 300 W thermal limits. They'll only come armed with 6 GB of GDDR5 memory. And although Intel does come right out and say it, we can work backwards to figure out that a chip with 28.5 MB of L2 cache is going to give us 57 cores. Why the higher TDP, then? We have to assume they'll be running at higher clock rates. Like the 5110P, a passively-cooled Xeon Phi 3100 would require a properly-validated server system. But a model with its own fan might exist as a workstation solution.

Because Intel hosted the Xeon Phi launch event at the TACC, we were able to snap some photos of the cards as they were being installed.



Zoom

To an enthusiast, the Xeon Phi looks a lot like two-slot graphics card with a 16-lane PCI Express interface. The two biggest differences, at least from this angle, are the lack of a cooling fan and the custom retention bracket. What you cannot see is the rear I/O panel, which is absent any display connectivity.



Zoom

The large and heavy heat sink under the card's shroud has fins that go straight back, allowing air to flow through and out the front. More familiar are the eight- and six-pin auxiliary connectors responsible for complementing the slot's 75 W power delivery.

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Intel Xeon Phi Performance

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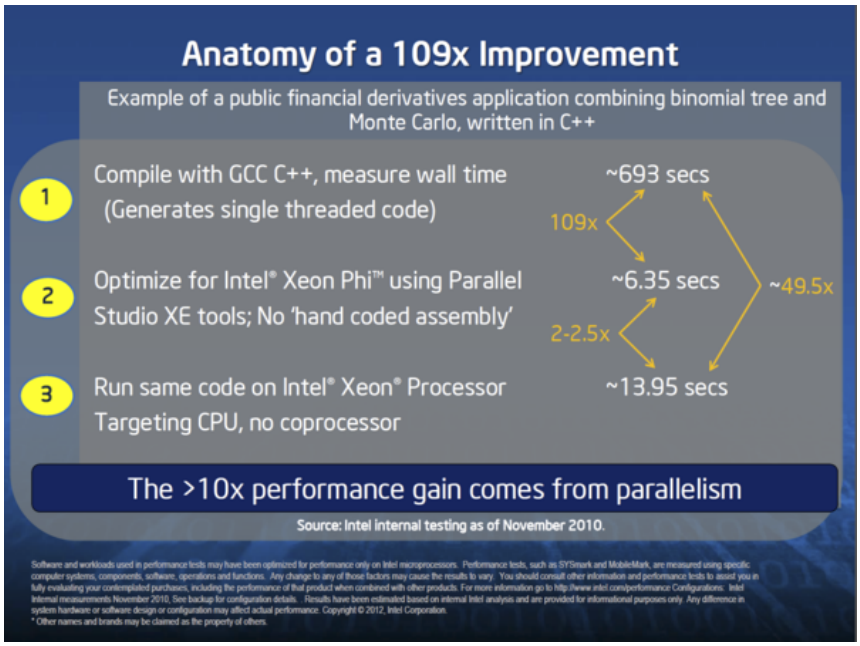
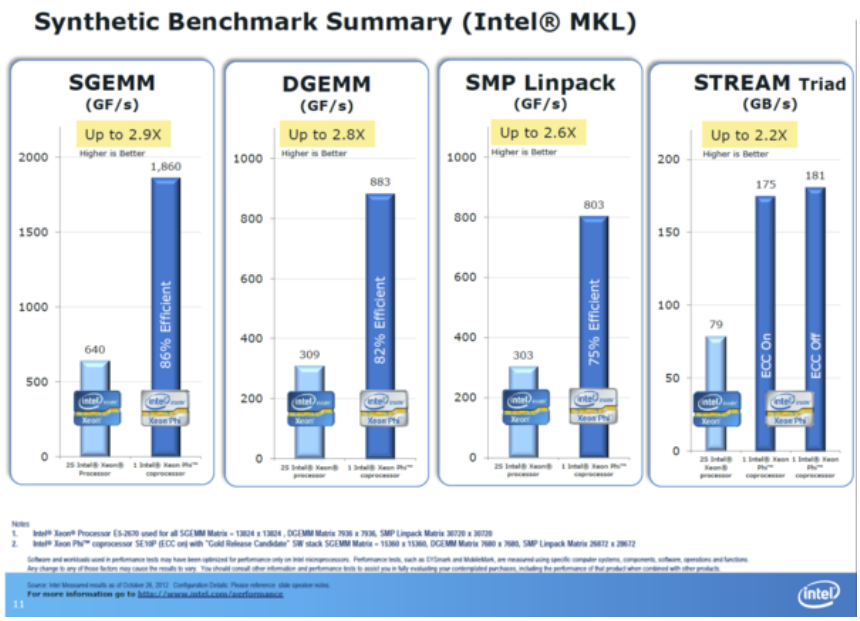
Throughout its press day, Intel repeated over and over the importance of optimized core when comparing the performance of a CPU to an accelerator. One of the company's first examples involved a bit of Fortran code. First, we saw results from the unoptimized single-threaded code, followed by a simple Xeon Phi port. The difference showed the Phi to be somewhere around 300x faster. Then, the Intel team demonstrated why its first comparison was flawed. When the same code was re-run on dual Xeon E5s, the Phi was only about twice as fast.



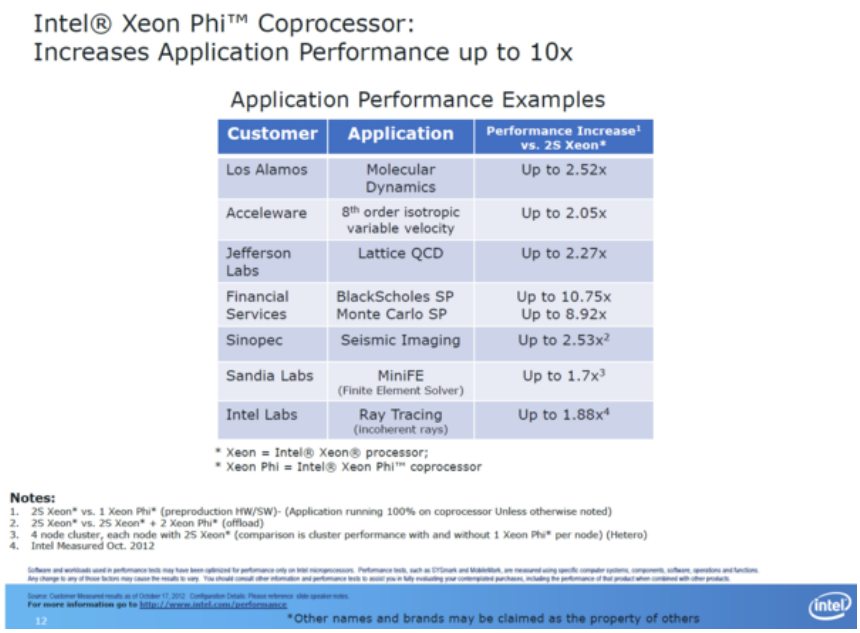
Zoom

The purpose of this exercise seemed to be expectation management. It's in the best interest of companies like Nvidia to run parallelized code in a single thread as a baseline, and then run the same code on a graphics processor to claim more than two orders of magnitude improvement. But if you allow optimized code to take advantage of a multi-core CPU's resources, the real delta between them is much smaller.



Zoom

Then, Intel shared some of the real-world performance improvements seen from comparisons between dual-socket Xeon-based machines and Xeon Phi.



Zoom

Financial services professionals are probably salivating at these numbers. Monte Carlo models are often used to solve problems using a bunch of unknown inputs and probability. I've personally used them to suggest the risk and financial impact of large projects and product programs. And, after the 2001 dot-com crash, Black-Scholes became a preferred option valuation method. This was a huge deal in the mid-2000s because Silicon Valley companies that gave employees options instead of higher salaries were under increased pressure to pin a value on those options.

Intel also brought in representatives from Altair, a software and technology provider, to suggest how easy it was for them to port code to the Xeon Phi architecture and show examples of workloads like crash test simulations, which generally saw a 2.5x performance improvement.

In lieu of hardware and software we can test ourselves, Intel's discussion of performance is plausible. Optimization can move the needle in one direction or the other, and certain applications are going to realize more gain from what Intel is doing with Xeon Phi than others. But, with that said, a 2-2.5x improvement seems reasonable in environments able to benefit from parallelized computing.

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The Value Proposition Of Xeon Phi: Optimization

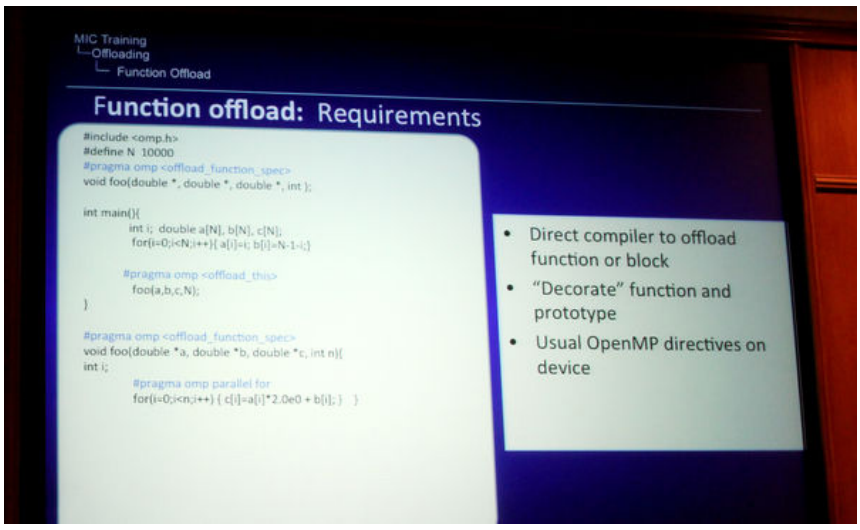
4:00 PM - November 12, 2012 by Patrick Kennedy

Intel came at us with a dual-pronged message during its presentation at the TACC:

1. With Xeon Phi, Intel is enabling a 2x or more performance-per-watt improvement in HPC apps compared to the Xeon E5 family.
2. Creating Xeon Phi-ready code happens through a similar approach developers use to exploit the Xeon's multiple cores.

The value in the first statement is both simple and powerful. Getting a greater-than 2x performance boost in optimized applications for somewhere between 225 and 300 W is not bad, particularly when you consider a pair of Xeon E5s is typically going to have a 190 to 300 W thermal ceiling, too. But because the Xeon Phi is a PCI Express-based card, you can also use more than one per pair of Xeon E5s. So long as the scaling is there, you can use two, three, or even four in a server with Xeon CPUs in it. The resulting combination can give you a lot more performance for a given amount of rack space, more performance under a defined power budget, or comparable performance using far less space, power, and cooling.

Then again, almost any step forward in manufacturing or architecture should yield gains in those same metrics. Xeon Phi's big advantage is tied to the development effort needed to harness the hardware's potential. Intel is hoping that programming for CUDA and OpenCL is still in its infancy, and that the idea of using familiar languages and tools is a compelling advantage able to generate support from the software community. Intel's position is strong, if it's able to maintain competitive performance. A unified programming model allows developers to exploit host processors and co-processors via x86, minimizing the time it takes to generate optimized code.



Zoom

One of the questions we put to Intel during the Xeon Phi Q&A was, "If you sell these accelerators for $2000 or more, how will the next generation of college students learn to write code able to exploit this hardware?" I received two responses. First, Xeon Phi will not be available at retail, so Intel is working to arm universities with hardware resources. The second answer was more intriguing. If a budding programmer has a Core i3 or better CPU, they can already learn the programming model. Remember, most of the gains you get from a many-core architecture come simply from optimizing code for parallelism.

Zoom

Intel doesn't care if you program for a Core i3, a Xeon E5, or a Xeon Phi. The company simply wants code written for multi-core x86 architectures. Back in the 1990s when I was doing computer science, we didn't have multi-core CPUs in our desktops. Nowadays, this is the model that will proliferate going forward.

I would also encourage Intel to get the Xeon Phi chips with manufacturing defects (resulting in lower usable core counts) into the hands of students. The name of the game is big data analytics, and that field is open to innovation from today's generation. For some at the University of Texas at Austin, they can look forward to access to the TACC and its Xeon Phi-equipped Stampede supercomputer.

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