Digital Design Project

agenda

SEMI CUSTOM

-VERILOG

-FPGA

FULL CUSTOM

-SPECS

-CADENCE

-LOGICSIM OR PAPER

TASKS DISTRIBUTION

REPORT

LINKS

Semi custom

Design Code

Testbench

Verilog Report
--RTL Code & Modeling
--Schematic
--Testbench
--waveform Screenshot of all possible ALU operations
--Displaying The Results
---PDF

https://github.com/amr10w/Digital-Design-Project

Verilog Team :
Amr wahidi – Hamza Bassem – Omar Theta

Verilog

Run Implementation

Targeting specific FPGA

FPGA Report

--Run Implementation

--Time Analysis Report

--FPGA Video

FPGA Team :
Ammar wahidi – Omar Ahmed
– Abderahman Essam

Full custom

Cadence Team :
Ammar wahidi – Omar Ahmed
– Abderahman Essam –
Ali Hany - Ammar Mohamed -
Youssef Emad - Mohamed
Elsayed - Anas Ayman

L= 130 nm,1.2 vcc, Free to choose any Family XOR

,

And …

--Lectures are important
You must Follow doctor every lecture weekly
--Hesham Omran Playlist
It's complicated for the project, but consider it all as a backup due to delay calculations

Specs

1- Transistor Level or Schematic : optimization required by Solving Boolean function ….

2- Symbolic

3-Testbench

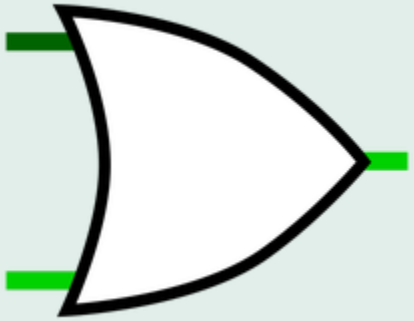
4-ScreenShot of output waveform

5-delivers these Screen shots

6- Report if your part demand reporting

----PDF File has All of that

Cadence



https://www.youtube.com/playlist?list=PLPCoEmG-V9tdE_LlyaMd4t2NA41_KQyUy

Logicsim or paper ?

Tasks distribution

Tasks Distribution

Design Units	Task by	Deadline
Logic gates (Not,Nand,Nor,…) **Sizing, delay** calcu,L=130….	Youssef Emad - Amr Ahmed (just calculations)	22/4
Logic Operations (One bit then four bit)	Ammar Mohammed	26/4
FlipFlop	Ammar -Omar Ahmed -Abderahman	30/4
Mux 2x1 Mux 8x1	Ammar Mohammed	26/4
Full Adder (2 xor , AOI) 4-bit Full adder (use full Adder as a Sympol)	Anas	26/4

Note : in Full adder we have xor from first task you are not required to design it again –use sympols- but you have to in case of AOI

Tasks Distribution

Design Units	Task by	Deadline
4-bit Full Subtractor (use full Adder as a Symbol)	Anas	26/4
Multiplication (Array Multiplier)	Ammar - Abderahman	29/4
Arithmetic Unit	Ali Hany	3/5
Whole ALU	Ammar – Ali Hany – Omar Ahmed	5/5
4-bit Register and 8-bit Register	Ammar -Omar Ahmed - Abderahman	30/4
Regeneration (Searching topic)	Mohammed Elsayed	28/4
Use a 2-pF load	Mohammed Elsayed	27/4

Use a 2-pF load capacitance at the output of your ALU not your flip-flops.

Tasks Distribution

Design Units	Task by	Deadline
Circuit-level simulations showing delay (at worst-case condition) and power consumption (at maximum possible frequency of operation) Max delay equation …	Ali Hany – Ammar – Omar Ahmed	6/5
power consumption	Ali Hany – Ammar – Omar Ahmed	6/5
Transient simulations with the flip-flops included at your maximum frequency of operation showing proper sampling of the inputs and outputs.	Ali Hany – Ammar – Omar Ahmed	6/5
Report		7/5

Design good pdf

Organized

All PDF files from the team will be sent to you—you just need to organize them.

Verilog Team :
Amr wahidi – Hamza Bassem –
Omar Theta –

Ammar Ahmed –
Ali Hany

Report

Links

[Arabic] Custom design of a 4-bit ALU (for Junior ECE students)
https://www.youtube.com/watch?v=D6mr9tTWkkI

Cadence Virtuoso Tutorial
Hesham Omran
https://www.youtube.com/playlist?list=PLMSBalys69yza1LVr3JNc6_pnYW4CvlEb

Logic sim 4-bit Alu
https://www.youtube.com/playlist?list=PLPCoEmG-V9tdE_LIyaMd4t2NA41_KQyUy

DR-Samih Lecturs
https://www.youtube.com/playlist?list=PLffO0PKa_AqF3fy9YwNoIJS6L2ihBfS2M

thank you

By : Ammar wahidi