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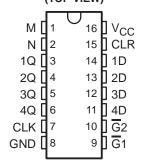
SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

- 3-State Outputs Interface Directly With **System Bus**
- Gated Output-Control Lines for Enabling or **Disabling the Outputs**
- **Fully Independent Clock Virtually Eliminates Restrictions for Operating in** One of Two Modes:
 - Parallel Load
 - Do Nothing (Hold)
- For Application as Bus Buffer Registers
- **Package Options Include Plastic** Small-Outline (D) Packages, Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) **DIPs**

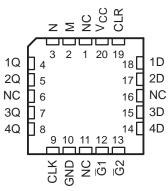
TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY
'173	23 ns	35 MHz
'LS173A	18 ns	50 MHz

description

The '173 and 'LS173A 4-bit registers include D-type flip-flops featuring totem-pole 3-state outputs capable of driving highly capacitive relatively low-impedance loads. high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and **SN54173, SN54LS173A...JOR W PACKAGE** SN74173 . . . N PACKAGE SN74LS173A . . . D or N PACKAGE (TOP VIEW)



SN54LS173A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs can be connected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable (G1, G2) inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output-control (M, N) inputs also are provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output-control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

The SN54173 and SN54LS173A are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74173 and SN74LS173A are characterized for operation from 0°C to 70°C.



testing of all parameters

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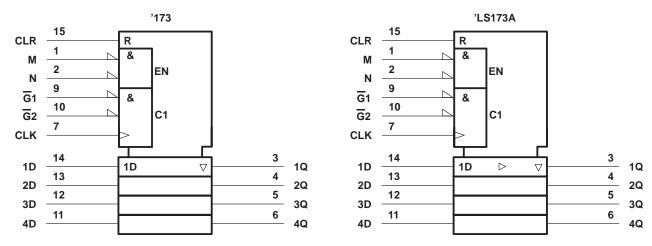


FUNCTION TABLE

		INPUTS	1		
CLR	CLK	DATA E	NABLE	DATA	OUTPUT Q
CLK	CLK	G1	G2	D	,
Н	Х	Х	Х	Χ	L
L	L	X	Χ	Χ	Q ₀
L	\uparrow	Н	Χ	Χ	Q ₀
L	\uparrow	X	Н	Χ	Q ₀
L	\uparrow	L	L	L	L
L	\uparrow	L	L	Н	Н

When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

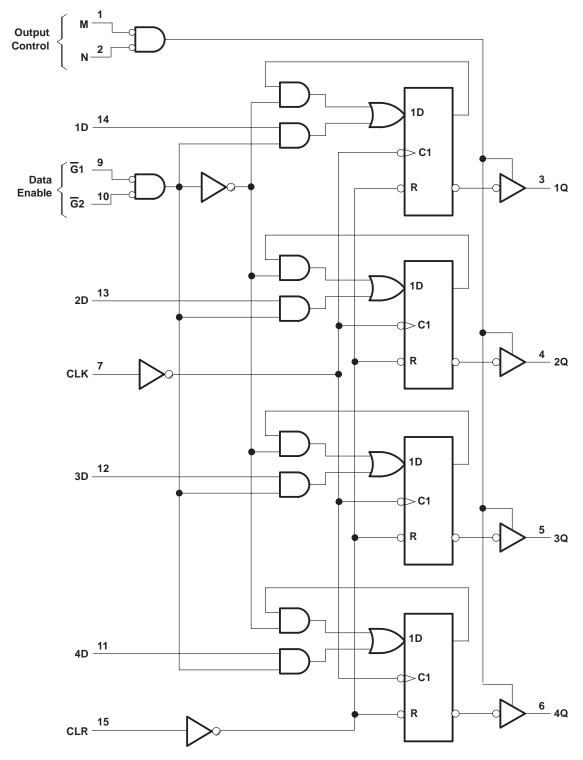
logic symbol†



[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.



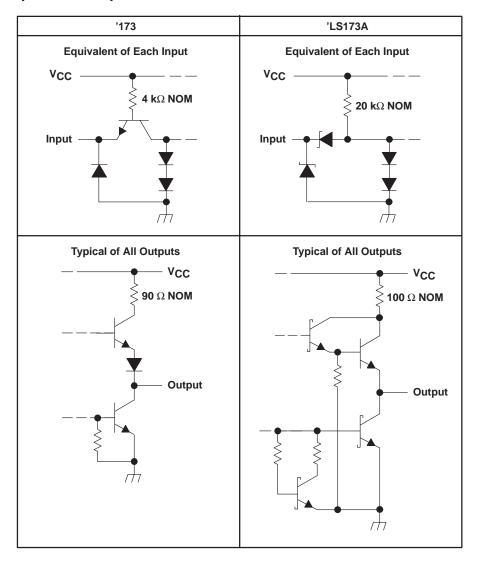
logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC} (see Note 1)	0.5 V to 7 V
Input voltage: '173	–0.5 V to 5.5 V
'LS173A	–0.5 V to 7 V
Off-state output voltage	–0.5 V to 5.5 V
Package thermal impedance, θ _{JA} (see Note 2): D package	113°C/W
N package	78°C/W
Storage temperature range, T _{sta}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{2.} The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



NOTES: 1. Voltage values are with respect to network ground terminal.

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recommended operating conditions (see Note 3)

		SN54173			5	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
ІОН	High-level output current			-2			-5.2	mA
loL	Low-level output current			16			16	mA
TA	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		NDITIONST	Ç	SN54173		•	SN74173		UNIT
	PARAMETER	TEST CO	NDITIONS†	MIN	TYP‡	MAX	MIN	TYP‡	MAX	Oitii
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
VIK	Input clamp voltage	$V_{CC} = MIN,$	$I_{ } = -12 \text{ mA}$			-1.5			-1.5	V
Vон	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = MAX	2.4			2.4			٧
VOL	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 16 mA			0.4			0.4	V
la con	Off-state (high-impedance state)	V _{CC} = MAX,	V _O = 2.4 V			150			40	^
IO(off)	output current	V _{IH} = 2 V	V _O = 0.4 V			-150			-40	μΑ
II	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
lн	High-level input current	$V_{CC} = MAX$,	V _I = 2.4 V			40			40	μΑ
I _{IL}	Low-level input current	$V_{CC} = MAX$,	V _I = 0.4 V			-1.6			-1.6	mA
los	Short-circuit output current§	$V_{CC} = MAX$		-30		-70	-30		-70	mA
ICC	Supply current	$V_{CC} = MAX$,	See Note 4		50	72		50	72	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

timing requirements over recommended operating conditions (unless otherwise noted)

			SN54	173	SN74	UNIT	
			MIN	MAX	MIN	MAX	UNII
fclock	Input clock frequency			25		25	MHz
t _W	Pulse duration	CLK or CLR	20		20		ns
		Data enable (G1, G2)	17		17		
t _{su}	Setup time	Data	10		10		ns
		CLR (inactive state)	10		10		
L	Hold time	Data enable (G1, G2)	2		2		20
th th	noid time	Data	10		10		ns



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 4: ICC is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, G1, G2, and all data inputs grounded; and CLK and M at 4.5 V.

SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω (see Figure 1)

	PARAMETER	TEST CONDITIONS	SN54173			S	UNIT		
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	ONIT
f _{max}	Maximum clock frequency		25	35		25	35		MHz
tPHL	Propagation delay time, high-to-low-level output from clear input	C _L = 50 pF		18	27		18	27	ns
tPLH	Propagation delay time, low-to-high-level output from clock input			28	43		28	43	
tPHL	Propagation delay time, high-to-low-level output from clock input			19	31		19	31	ns
tPZH	Output enable time to high level		7	16	30	7	16	30	
t _{PZL}	Output enable time to low level		7	21	30	7	21	30	ns
^t PHZ	Output disable time from high level	C 5 pE	3	5	14	3	5	14	nc
tPLZ	Output disable time from low level	C _L = 5 pF	3	11	20	3	11	20	ns



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recommended operating conditions

		SN54LS173A			SN	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
ІОН	High-level output current			-1			-2.6	mA
loL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		unizionist	SN	54LS173	BA	SN	74LS173	BA	UNIT
	PARAMETER	I EST CO	TEST CONDITIONS†		TYP [‡]	MAX	MIN	TYP [‡]	MAX	UNIT
VIH	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.7			0.8	V
VIK	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
VOH	High-level output voltage	$V_{CC} = MIN,$ $V_{IL} = V_{IL}max,$	$V_{IH} = 2 V$, $I_{OH} = MAX$	2.4	3.4		2.4	3.1		٧
V	Low lovel output voltage	V _{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	Low-level output voltage	$V_{IL} = 0.8 V,$	I _{OL} = 24 mA					0.35	0.5	V
10.40	Off-state (high-impedance state)	V _{CC} = MAX,	V _O = 2.7 V			20			20	V
IO(off)	output current	V _{IH} = 2 V	V _O = 0.4 V			-20			-20	V
II	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V			0.1			0.1	mA
lіН	High-level input current	$V_{CC} = MAX$,	V _I = 2.7 V			20			20	μΑ
Ι _Ι Γ	Low-level input current	$V_{CC} = MAX,$	V _I = 0.4 V			-0.4			-0.4	mA
los	Short-circuit output current§	V _{CC} = MAX		-30		-130	-30		-130	mA
ICC	Supply current	$V_{CC} = MAX$,	See Note 4		19	30		19	24	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, G1, G2, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

					SN74LS	UNIT	
			MIN	MAX	MIN	MAX	ONIT
fclock	f _{clock} Input clock frequency					25	MHz
t _W	Pulse duration	CLK or CLR	25		25		ns
		Data enable (G1, G2)	35		35		
t _{su}	Setup time	Data	17		17		ns
		CLR (inactive state)	10		10		
4.	Hold time	Data enable (G1, G2)	0		0		no
th	Data Data				3		ns



[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

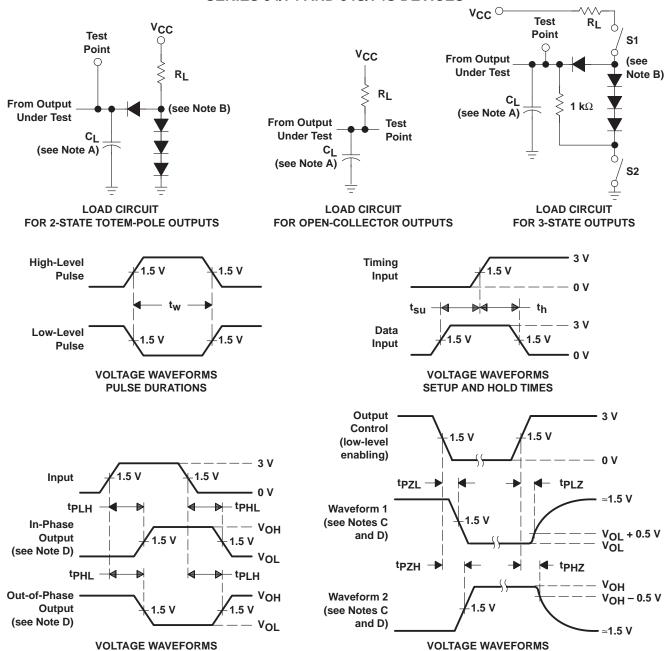
SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS SDLS067A - OCTOBER 1976 - REVISED JUNE 1999

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω (see Figure 2)

	PARAMETER	TEST CONDITIONS	SN	SN54LS173A			74LS173	3A	UNIT	
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	ONII	
f _{max}	Maximum clock frequency		30	50		30	50		MHz	
tPHL	Propagation delay time, high-to-low-level output from clear input	C _L = 45 pF		26	35		26	35	ns	
tPLH	Propagation delay time, low-to-high-level output from clock input			17	25		17	25	20	
tPHL	Propagation delay time, high-to-low-level output from clock input			22	30		22	30	ns	
^t PZH	Output enable time to high level			15	23		15	23	no	
tPZL	Output enable time to low level			18	27		18	27	ns	
tPHZ	Output disable time from high level	C 5 pE		11	20		11	20	ns	
tPLZ	Output disable time from low level	C _L = 5 pF		11	17		11	17	115	



PARAMETER MEASUREMENT INFORMATION SERIES 54/74 AND 54S/74S DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.

PROPAGATION DELAY TIMES

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.

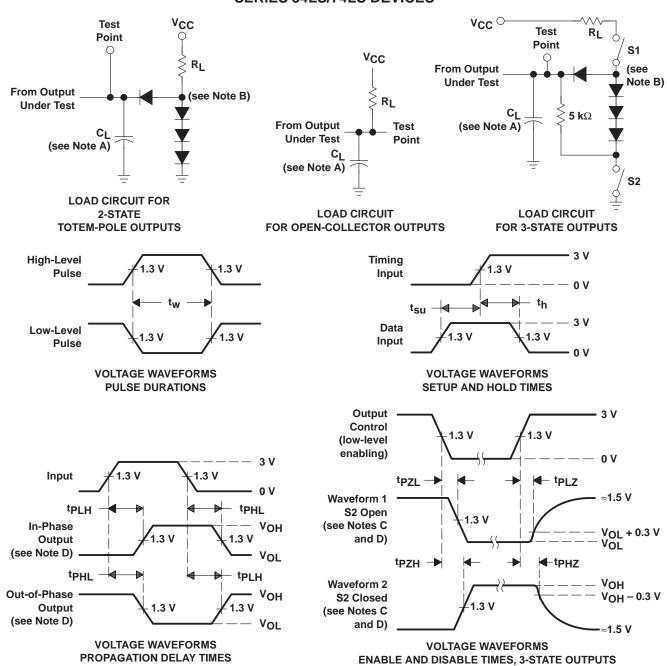
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \,\Omega$, t_r and $t_f \leq$ 7 ns for Series 54/74 devices and t_r and $t_f \leq$ 2.5 ns for Series 54S/74S devices.
- F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES



- NOTES: A. C_I includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. S1 and S2 are closed for tpLH, tpHZ, and tpLZ; S1 is open and S2 is closed for tpZH; S1 is closed and S2 is open for tpZL.
 - E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 - F. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{\Omega} \approx 50~\Omega$, $t_f \leq$ 15 ns, $t_f \leq$ 6 ns.
 - G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms



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