Modern Academy for Engineering & Technology

Computer Engineering and Information Technology Department

Course Specification

CMP 426: Logic Design-2

A- Affiliation

Relevant program: Computer Engineering and Information Technology BSc Program.
Department offering the program: Computer Engineering and Information Technology Department
Department offering the course: Computer Engineering and Information Technology Department
Date of specifications approval: September 2015

B - Basic information

Title: Logic Design-2 **Code**: CMP 426 **Level:** Junior, First Semester
Credit Hours: 3 **Lectures**: 2 **Tutorial/Exercise**: 1 **Practical**: 2
Pre-requisite: CMP 211

C - Professional information

1 – Course Learning Objectives:

By the end of this course the students should demonstrate the knowledge and understanding of the different logic modules, which are the main organs of a modern digital system. They should be able to design logic application by joining those modules in a complete operating system introducing the adequate performance analysis.

2 – Intended Learning Outcomes (ILOS)

a - Knowledge and understanding:

On successful completion of the course, the student should demonstrate knowledge and understanding of:

a1- Problems of digital nature and sequential behavior to a state diagram description in case of small numbers of states problems (A1, A5).
a2- Evaluation of the minimum cost circuit realization (A4, A5, A14).
a3- The state table for a given sequential circuit (A2, A5).
a4- Estimation the size of the problem to choose either flip-flop or modular realization circuitry (A2, A4, A5).
a5- The proper layout design of the data path that fits the allocated problem requirements (A3, A4, A9,A14).
a6- The control system of the given problem which secures the correct sequence of output signals, which control the transfer of data among path and registers (A4, A14).
a7- The verification of the overall design correctness (A1, A4, and A14).
a8- The memory circuit required to transfer data from and to data path under control of control unit, and the associated address, and data registers for exciting microinstructions if exist (A2, A4, A9, and A14).

b - Intellectual skills:

On successful completion of the course, the student should be able to:

b1- Create solutions for surrounding problems using the knowledge absorbed in this course (B3, B4, B12, and B14).
b2- Analyze any given system and extract the bugs in this system (B1, B4, B6, and B12).
b3- Create of revolutionary attempts to solve difficult sophisticated problems by logic approaches gained in course, giving rise up to simple and cheap solutions (B3, B4, B8, and B17).
b4- Measure procedure and self-correction means to proposed systems (B3, B6, B7, and B12).

c - Professional and practical skills:

On successful completion of the course, the student should be able to:

c1- Design a special-purpose computing system satisfying special requirements with cheaper price than normal computers (C1, C3, C4, and C5).

c2- Realize a digital system operating in real-time, which have computational time much less than that of normal PC (C1, C2, C3, and C5).

c3- Modify existing digital system to achieve either better performance or special application (C1, C2, C3, C6).

d - General and transferable skills:

On successful completion of the course, the student should be able to:

d1- Use internet, references and journals for searching information (D3, D7, D9).

d2- Write a technical report for a given task and prepare its presentation (D3, D4, D6, D7).

d3- Join with team work (D1, D2, D5).

Course Contribution in the Program ILO's

ILO's		Program ILO's
A	Knowledge and understanding	A1, A2, A3,A4, A5, A9, A14
B	Intellectual skills	B1, B3, B4, B6, B7,B8, B12, B14, B17
C	Professional and practical skills	C1, C2, C3, C4, C5, C6
D	General and transferable skills	D1, D2, D3, D4, D5, D6, D7, D9

3 – Contents

Topic	Lecture hours	Tutorial hours	Practical hours
➢ Introduction	3	1	3
• Aims realized through the topics of this subjects.			
• Logic gate types (RTL, DTL, TTL, ECL) and others.			
➢ Synthesis of sequential logic circuits	8	4	8
• State diagrams and state table representation.			
• The mealy and Moore models.			
• Synthesis procedure of completely specified sequential circuits.			
➢ Building state diagram (table)			
➢ Using state reduction techniques (state equivalent) and specially the implication chart method			
➢ State assignment techniques			
➢ Excitation functions derivation			
• Controllable counters as an example for a Moore model.			
➢ Analysis of sequential circuits			
➢ Modular design approaches using register transfers and data paths	6	3	6
• Digital systems subdivision (Data path and control).			
• Register transfer operations.			
• Arithmetic micro operations.			
• Logic micro operations.			
• Shift micro operations.			
• Multiplexer-based micro operations.			
• Trieste bus based transfers.			
• Memory based transfer.			

• A data path design proposed model. • Design of arithmetic logic unit (ALU). • Control word based design.			
➢ Sequencing control and algorithmic state machines (ASM) • The control unit. • The ASM chart construction. • An illustrative model (binary multiplier). • Hardwired control. • Realization of the sequencing part of the ASM chart using sequence register and decoder and using one flip-flop per state. • Micro programmed control.	7	4	7
➢ Memory system design • Static RAMs (RAM cell and RAM bit slice) • Coincident selection. • Dynamic RAMs (Basic cell, addressing and refreshing). • Memory system hierarchy. • Cache memory. • Design using ROM-RAM combination. • Design involving decoder implementation. • Design using memory array configuration. • Increasing the size of physical memory space.	6	3	6
Total hours	30	15	30

4 - Teaching and Learning and Assessment methods:

Course ILO's		Teaching Methods						Learning Methods		Assessment Method				
		Lecture	Presentations and Movies	Discussions and seminars	Tutorials	Problem solving	Laboratory & Experiments	Researches and Reports	Modeling and Simulation	Written Exam	Practical Exam	Quizzes	Term papers	Assignments
Knowledge & Understanding	a1	1			1			1		1				1
	a2	1			1			1		1		1		
	a3	1			1					1		1		1
	a4	1	1	1			1	1			1			1
	a5	1		1	1		1			1	1	1		
	a6	1			1		1			1	1			1
	a7	1	1			1		1						1
	a8	1			1		1			1	1	1		

Course ILO's		Teaching Methods						Learning Methods	Assessment Method					
		Lecture	Presentations and Movies	Discussions and seminars	Tutorials	Problem solving	Laboratory & Experiments	Researches and Reports	Modeling and Simulation	Written Exam	Practical Exam	Quizzes	Term papers	Assignments
Intellectual Skills	b1	1				1				1				1
	b2	1				1				1		1		
	b3			1		1		1				1		1
	b4			1		1		1						1
Applied Professional Skills	c1	1	1	1				1				1		1
	c2	1	1	1				1		1				1
	c3		1	1			1				1	1		1
General Tran. Skills	d1		1					1						
	d2		1			1		1				1		1
	d3		1					1						1

5- Assessment Timing and Grading:

Assessment Method	Timing	Grade (Degrees)
Semester Work: seminars, quizzes assignments and reports	Bi-Weekly	10
Mid-Term Exam	6-th Week	10
Practical Exam	Fifteenth week	20
Written Exam	Sixteenth week	60
Total		100

6- List of references:

6-1 Course notes: Digital logic circuit design (Theoritical + Practical).

6-2 Required books

- Mano, M.M, and Kime, C.R, Logic and Computer Design Fundamental, 2nd ed., Englewood cliffs, NJ: Prentice Hall, 2000.
- Nelson, V.P, Nagel, H.T., Carroll, B.D., and Irwin, J.D., Digital Logic Circuit Analysis and Design, NJ: Prentice Hall, 1995.

6-3 Recommended books:

- Warkely, J.F, Digital Design: Principles and Practices, 2nd ed. Englewood cliffs, NJ: Prentice Hall, 2000.
- Mano, M.M, Digital Design 2nd ed. Englewood cliffs, NJ: Prentice Hall, 1991.

6-4 Periodicals, Web sites, etc.

http://www.prenhall.com/mano

7- Facilities required for teaching and learning

- Logic lab. and Computers.
- Data show and Computer programs.

Course coordinator: Prof. Dr. Mohi-Eldin Rateb
Head of the Department: Prof. Dr. Mokhtar Abdelhalem
Date: September 2015