Assignment 1

By Amr Mohamed Ahmed Ebrahim

Question 1

Code

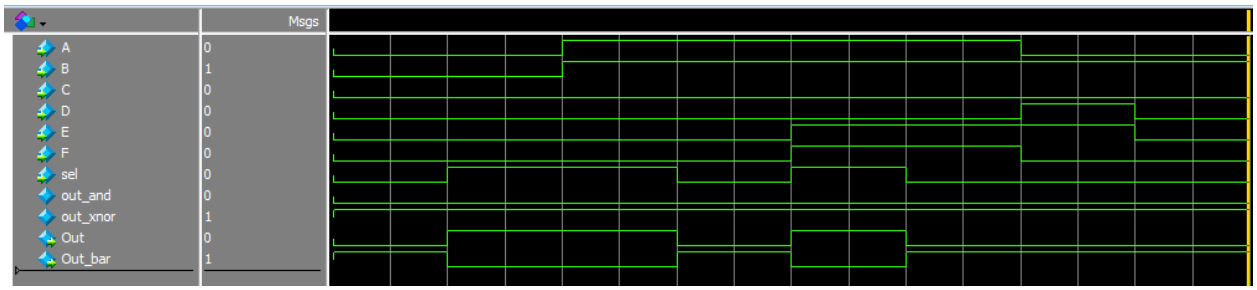
```
module q1
    (
     input A, B, C, D, E, F,
     input sel,
     output Out, Out_bar
    );

      wire out_and, out_xnor ;

      assign out_and = A & B & C ;              // describes the AND gate
      assign out_xnor = ~(D ^ E ^ F) ;         // describes the XNOR gate
      assign Out = sel ? out_xnor : out_and; //describes the Multiplexer
      assign Out_bar = ~Out ;                 // describes the inverter

endmodule
```

Simulation

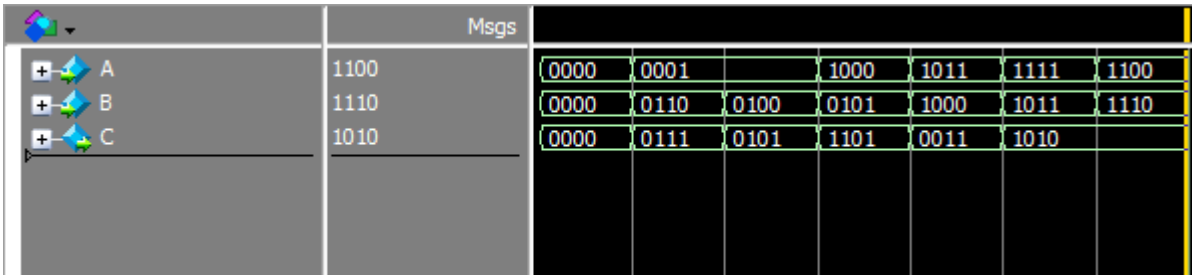


Question 2

Code

```
1  module q2
2      (
3       input  [3:0] A, B,
4       output [3:0] C
5      );
6
7          assign C = A + B;
8
9  endmodule
```

Simulation



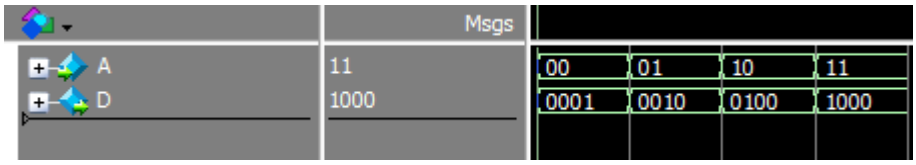
Question 3

Code

```
module q3
        (
         input [1:0] A,
         output [3:0] D
         );

          assign D = (A==2'b00) ? 4'b0001 :
                     (A==2'b01) ? 4'b0010 :
                     (A==2'b10) ? 4'b0100 : 4'b1000;
endmodule
```

Simulation

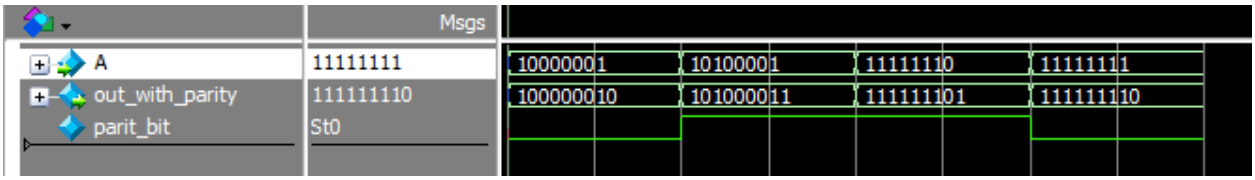


Question 4

Code

```
1   module q4
2           (
3             input [7:0] A,
4             output [8:0] out_with_parity
5             );
6
7              wire parit_bit ;
8              assign parit_bit = ^A;
9              assign out_with_parity = {A,parit_bit};
10
11  endmodule
```

Simulation



Question 5

Code

```
1   module q5
2           (
3               input [3:0] A, B,
4               output A_greaterthan_B,
5               output A_equals_B,
6               output A_lessthan_B
7               );
8           assign A_greaterthan_B = A>B ? 1'b1 : 1'b0 ;
9           assign A_equals_B = A==B ? 1'b1 : 1'b0 ;
10          assign A_lessthan_B = A<B ? 1'b1 : 1'b0 ;
11
12  endmodule
```

Simulation