Assignment 1 Extended

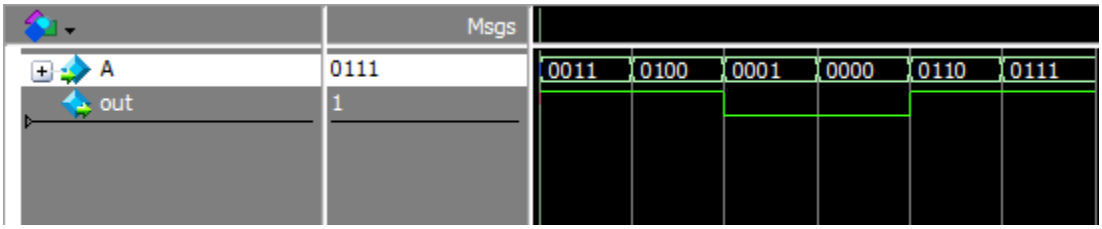
By Amr Mohamed Ahmed Ebrahim

Question 1

Code

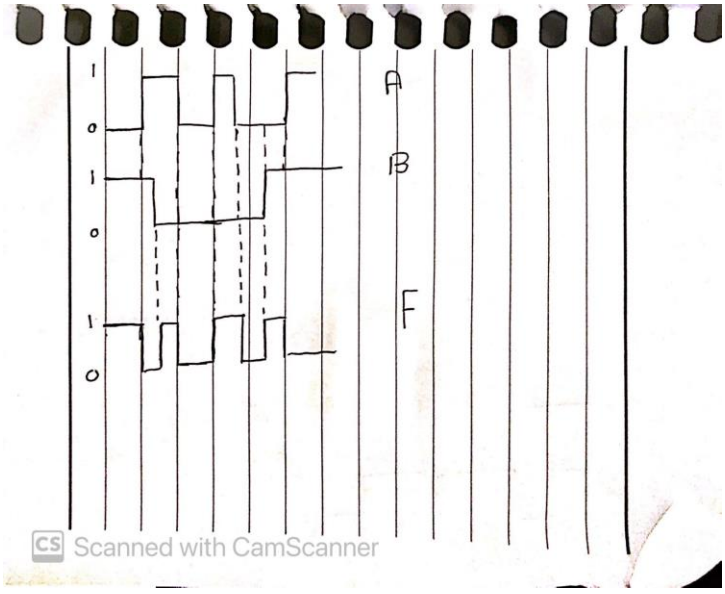
```
1  module q1
2          (
3                  input [3:0] A,
4                  output out
5                  );
6
7          assign out = ((A > 4'b0010) && (A < 4'b1000)) ? 1'b1 : 1'b0 ;
8
9  endmodule
```

Simulation

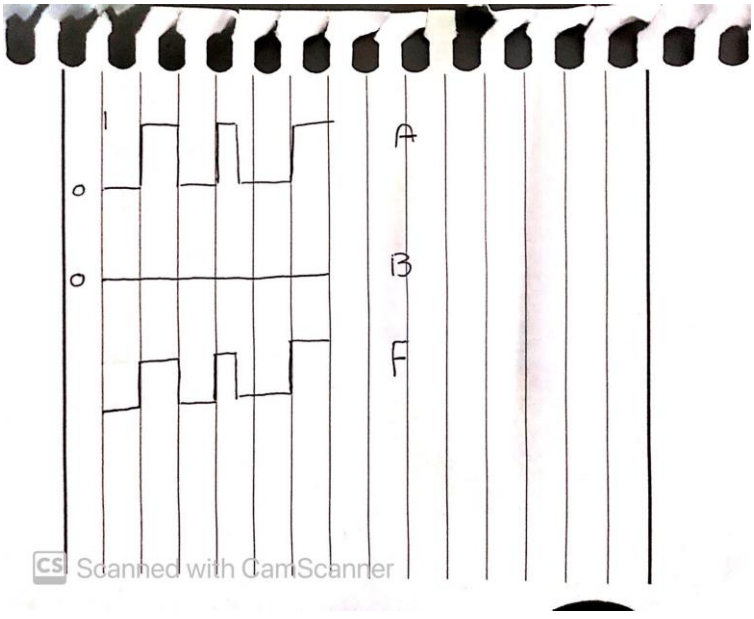


Question 2

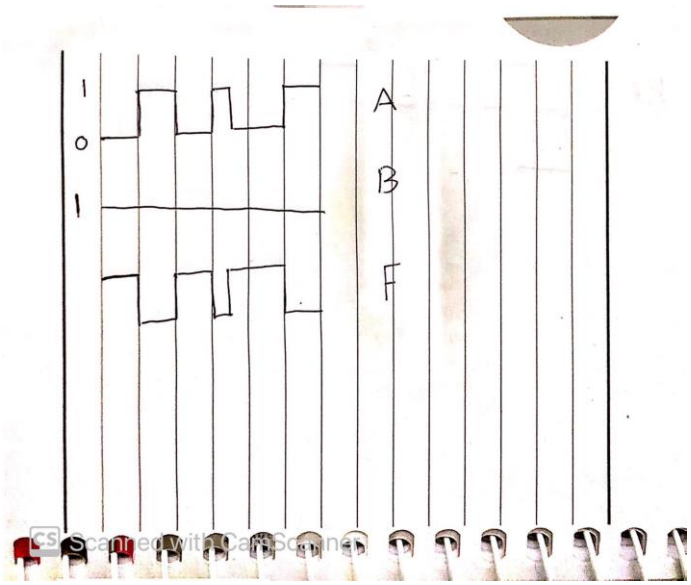
a)



b) Output F is the same as A



C) Output F is the inversion of A

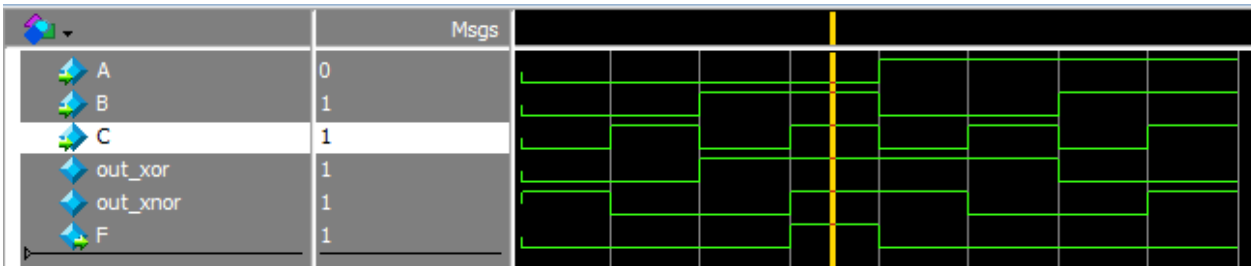


Question 3

Code

```
1  module q3 (
2      input A, B, C,
3      output F
4      );
5
6          wire out_xor, out_xnor;
7
8          assign out_xor = A ^ B;            //describes XOR Gate
9          assign out_xnor = B ~^ C;          //describes XNOR Gate
10         assign F = out_xor & out_xnor & C; //describes 3 inputs AND Gate
11 endmodule
```

Simulation



The Output is 1 when A=0, B=1, C=1.

Question 4

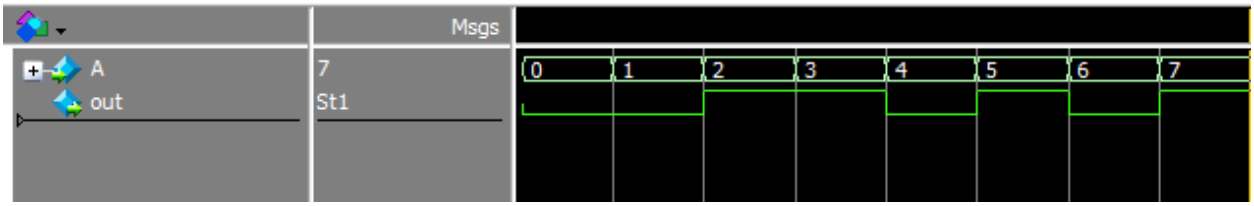
Code

```
module q4 (
    input [2:0] A,
    output out
    );

       assign out = A==4'b0010 || A==4'b0011 || A==4'b0101 || A==4'b111 ? 1'b1 : 1'b0 ;

endmodule
```

Simulation



Question 5

Code

```
module q5 (
    input A,B,
    input Ainvert, Binvert, CarryIn,
    input [1:0] Operation,
    output Carryout, Result
    );

        wire Amux, Bmux, ANDout, ORout, Adderout ;

        assign Amux = Ainvert ? ~A : A ;
        assign Bmux = Binvert ? ~B : B ;

        and (ANDout, Amux, Bmux) ;
        or  (ORout, Amux, Bmux) ;

        assign {Carryout, Adderout} = Amux + Bmux + CarryIn ;

        assign Result = Operation==2'b00 ? ANDout :
                        Operation==2'b01 ? ORout :
                        Operation==2'b10 ? Adderout : 1'bx ;

endmodule
```

Simulation