Assignment 4

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Design Code

```
module ALSU #(parameter INPUT_PRIORITY="A", FULL_ADDER="ON")
(
    input clk, rst,
    input [2:0] A, B,
    input [2:0] opcode,
    input cin, serial_in,
    input direction,
    input red_op_A, red_op_B,
    input bypass_A, bypass_B,
    output reg [5:0] out,
    output reg [15:0] leds
    );

    reg [2:0] A_reg, B_reg;
    reg [2:0] opcode_reg;
    reg cin_reg, serial_in_reg;
    reg direction_reg;
    reg red_op_A_reg, red_op_B_reg;
    reg bypass_A_reg, bypass_B_reg;
    reg [5:0] out_next;
    reg [15:0] leds_next;
```

```
    always@(posedge clk or posedge rst)
      if(rst) begin
        A_reg <= 0;
        B_reg <= 0;
        opcode_reg <= 0;
        cin_reg <= 0;
        serial_in_reg <= 0;
        direction_reg <= 0;
        red_op_A_reg <= 0;
        red_op_B_reg <= 0;
        bypass_A_reg <= 0;
        bypass_B_reg <= 0;
        out <= 0;
        leds <= 0;
      end
      else begin
        A_reg <= A;
        B_reg <= B;
        opcode_reg <= opcode;
        cin_reg <= cin;
        serial_in_reg <= serial_in;
        direction_reg <= direction;
        red_op_A_reg <= red_op_A;
        red_op_B_reg <= red_op_B;
        bypass_A_reg <= bypass_A;
        bypass_B_reg <= bypass_B;
        out <= out_next;
        leds <= leds_next;
      end
```

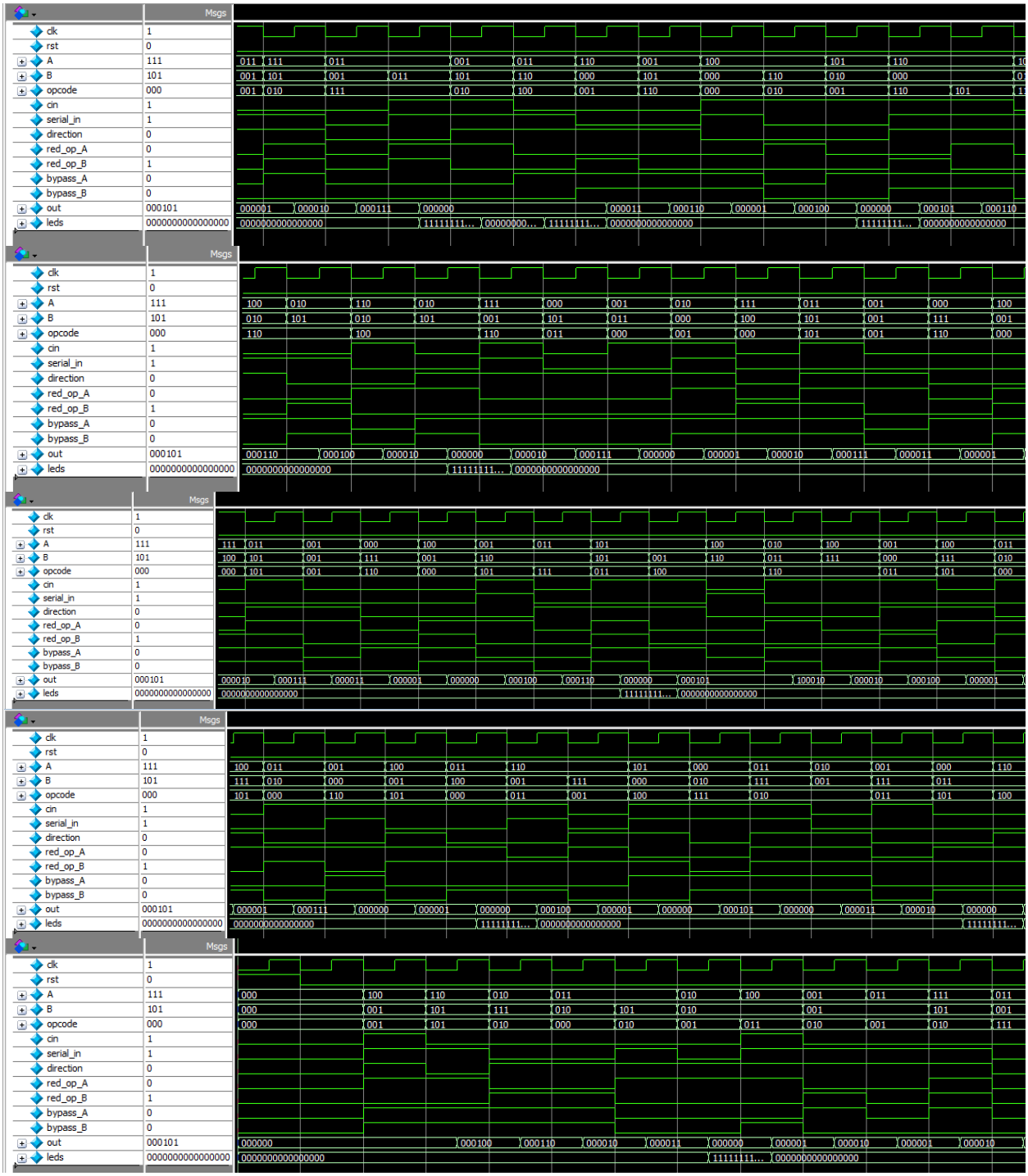
```
53          always @(*) begin
54          leds_next=0;
55           if(bypass_A_reg==1 && bypass_B_reg==1)
56              if(INPUT_PRIORITY=="A")
57                out_next=A_reg;
58              else if(INPUT_PRIORITY=="B")
59                out_next=B_reg;
60              else
61                out_next=out;
62           else if(bypass_A_reg==1)
63              out_next=A_reg;
64           else if(bypass_B_reg==1)
65              out_next=B_reg;
66            else
67                case(opcode_reg)
68                   0: if(red_op_A_reg==1 && red_op_B_reg==1)
69                         if(INPUT_PRIORITY=="A")
70                             out_next=&A_reg;
71                         else if(INPUT_PRIORITY=="B")
72                             out_next=&B_reg;
73                         else
74                             out_next=out;
75                      else if(red_op_A_reg==1)
76                         out_next=&A_reg;
77                      else if(bypass_B_reg==1)
78                         out_next=&B_reg;
79                      else
80                         out_next=A_reg&B_reg;
81
82                   1: if(red_op_A_reg==1 && red_op_B_reg==1)
83                         if(INPUT_PRIORITY=="A")
84                             out_next=^A_reg;
85                         else if(INPUT_PRIORITY=="B")
86                             out_next=^B_reg;
87                         else
88                             out_next=out;
89                      else if(red_op_A_reg==1)
90                         out_next=^A_reg;
91                      else if(bypass_B_reg==1)
92                         out_next=^B_reg;
93                      else
94                         out_next=A_reg^B_reg;
95
```

```
95
96                  2: if(red_op_A_reg==1 || red_op_B_reg==1) begin
97                       out_next=0;
98                       leds_next=~leds;
99                     end
100                    else if(FULL_ADDER=="ON")
101                      out_next=A_reg+B_reg+cin_reg;
102                    else if(FULL_ADDER=="OFF")
103                      out_next=A_reg+B_reg;
104                    else
105                      out_next=out;
106
107                 3: if(red_op_A_reg==1 || red_op_B_reg==1) begin
108                      out_next=0;
109                      leds_next=~leds;
110                    end
111                    else
112                      out_next=A_reg*B_reg;
113
114                 4: if(red_op_A_reg==1 || red_op_B_reg==1) begin
115                      out_next=0;
116                      leds_next=~leds;
117                    end
118                    else if(direction_reg)
119                      out_next={out[4:0],serial_in_reg};
120                    else
121                      out_next={serial_in_reg,out[5:1]};
122
123                 5: if(red_op_A_reg==1 || red_op_B_reg==1) begin
124                      out_next=0;
125                      leds_next=~leds;
126                    end
127                    else if(direction_reg)
128                      out_next={out[4:0],out[5]};
129                    else
130                      out_next={out[0],out[5:1]};
131
132                 6,7: begin
133                      out_next=0;
134                      leds_next=~leds;
135                    end
136           endcase
137         end
138 endmodule
```

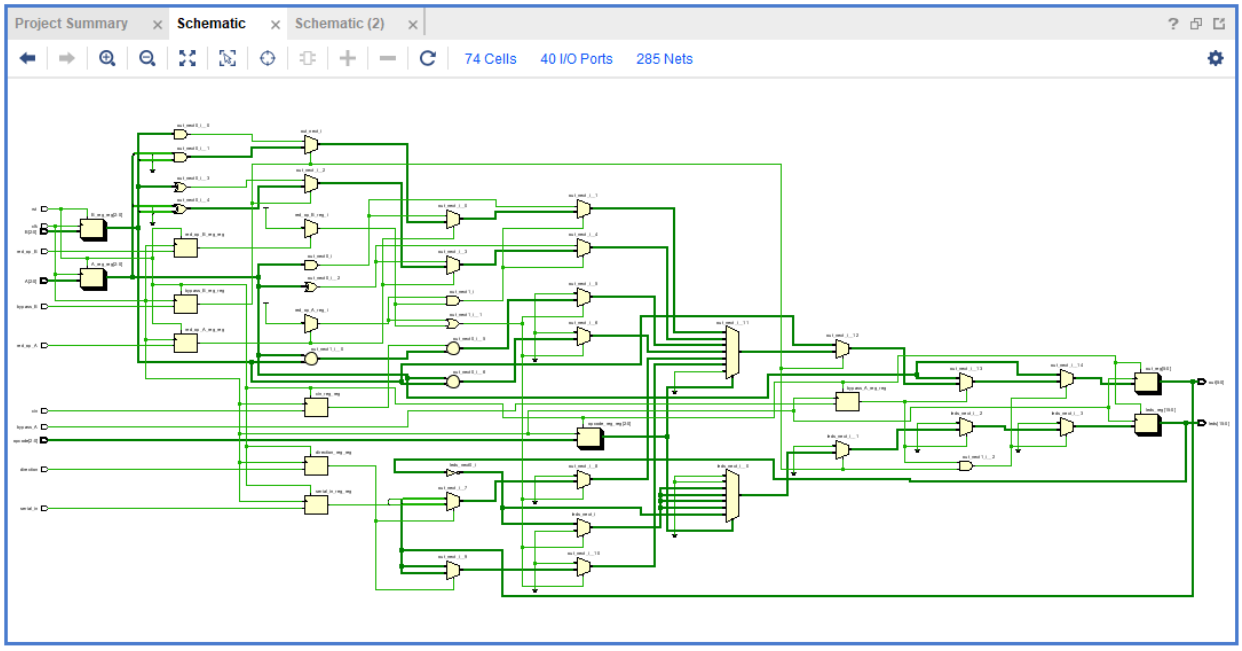
Testbench Code

```
module ALSU_tb ();
    reg clk, rst;
    reg [2:0] A, B;
    reg [2:0] opcode;
    reg cin, serial_in;
    reg direction;
    reg red_op_A, red_op_B;
    reg bypass_A, bypass_B;
    wire [5:0] out;
    wire [15:0] leds;
    ALSU #("A","ON") dut (clk, rst, A, B, opcode, cin, serial_in,
        direction, red_op_A, red_op_B, bypass_A, bypass_B, out, leds) ;
    initial begin
        clk=0;
        forever
          #10 clk=~clk;
    end
    initial begin
        rst=1;
        A = 0;
        B = 0;
        opcode= 0;
        cin= 0;
        serial_in= 0;
        direction= 0;
        red_op_A= 0;
        red_op_B= 0;
        bypass_A= 0;
        bypass_B= 0;
        @(negedge clk) ;
        rst=0;
        @(negedge clk);
        repeat(100) begin
         A = $random;
         B = $random;
         opcode= $random;
         cin= $random;
         serial_in= $random;
         direction= $random;
         red_op_A= $random;
         red_op_B= $random;
         bypass_A= $random;
         bypass_B= $random;
         #20;
        end
        $stop;
    end
endmodule
```

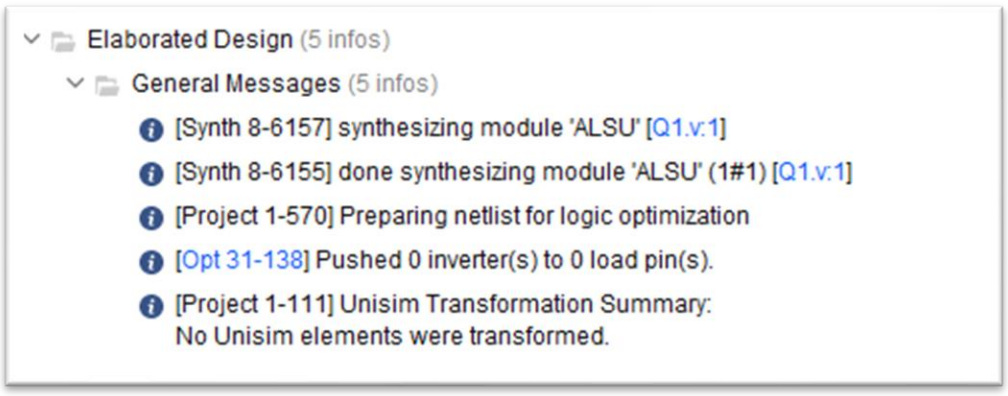
Waveform


Msgs
clk
rst
A
B
opcode
cin
serial_in
direction
red_op_A
red_op_B
bypass_A
bypass_B
out
leds

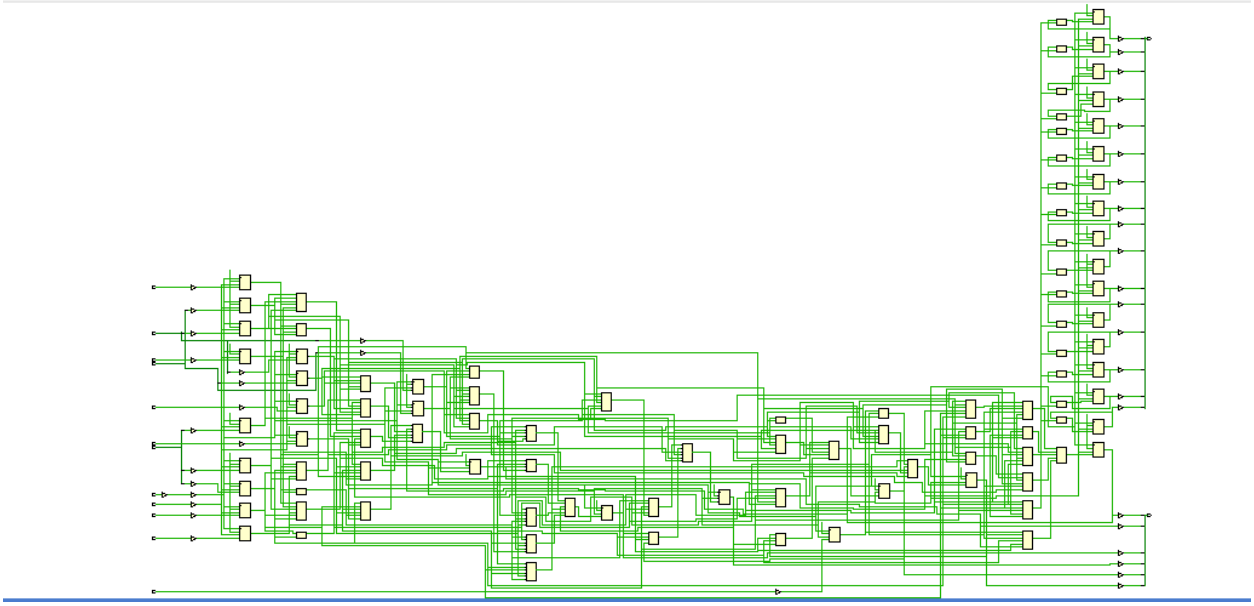
Elaboration Schematic



Elaboration Messages



Synthesis Schematic



Synthesis Message

Synthesis Utilization Report

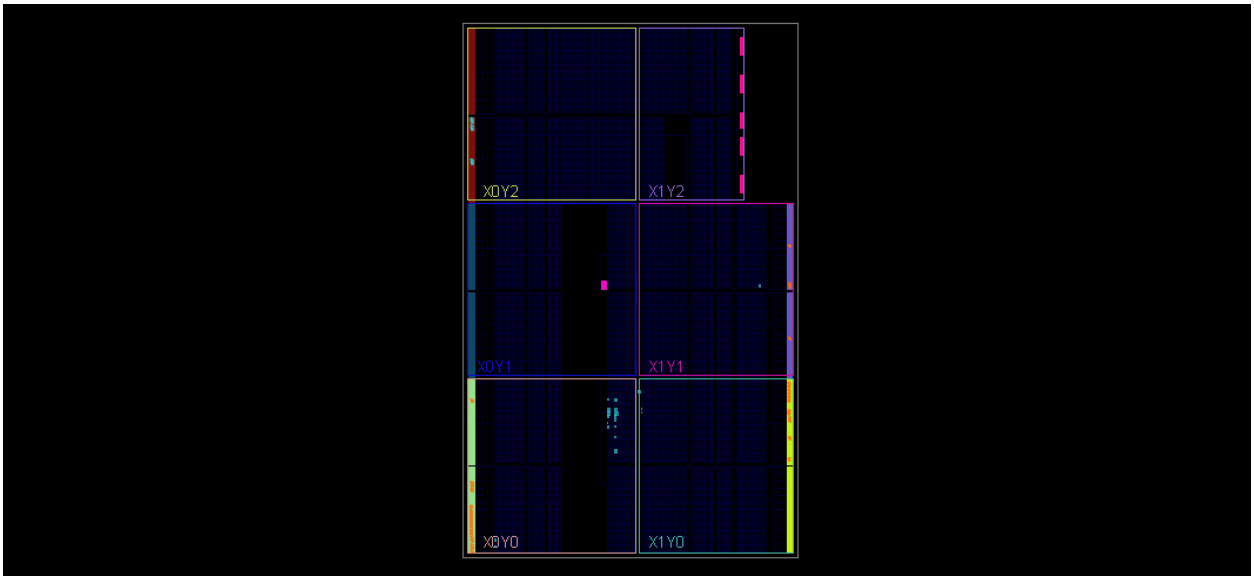
Name	Slice LUTs (20800)	Slice Registers (41600)	Bonded IOB (106)	BUFGCTRL (32)
ALSU	47	38	40	1

Synthesis Timing Report

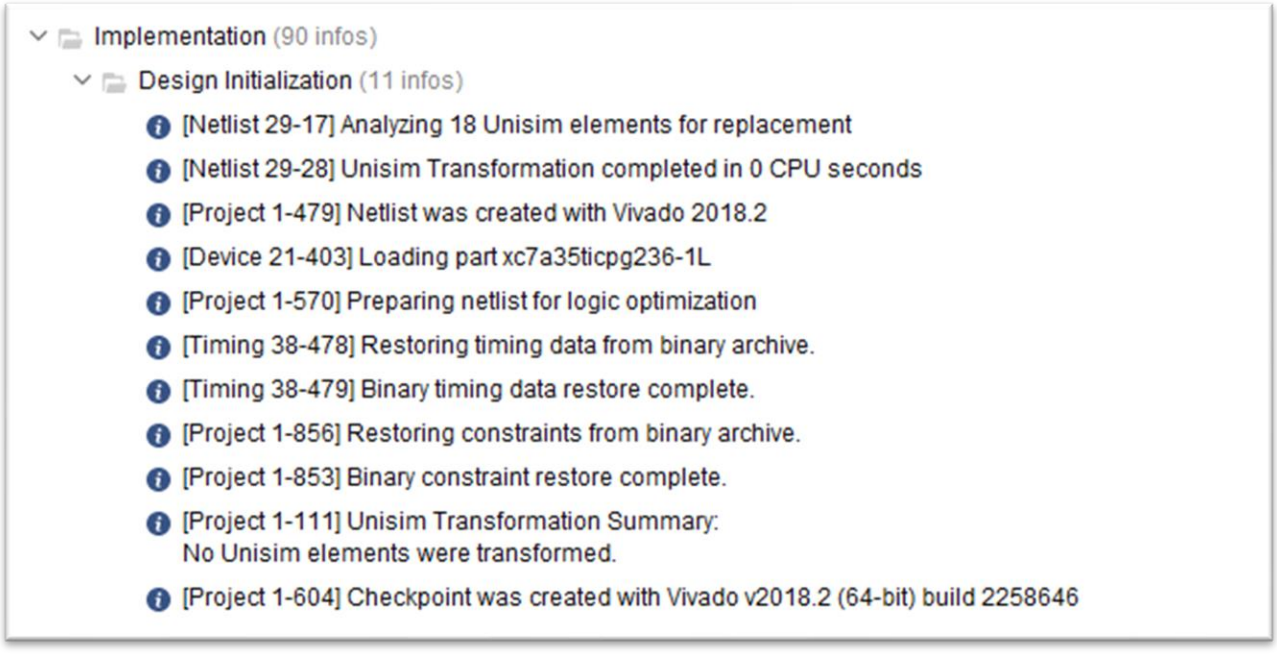
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.291 ns	Worst Hold Slack (WHS):	0.206 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	22	Total Number of Endpoints:	22	Total Number of Endpoints:	39

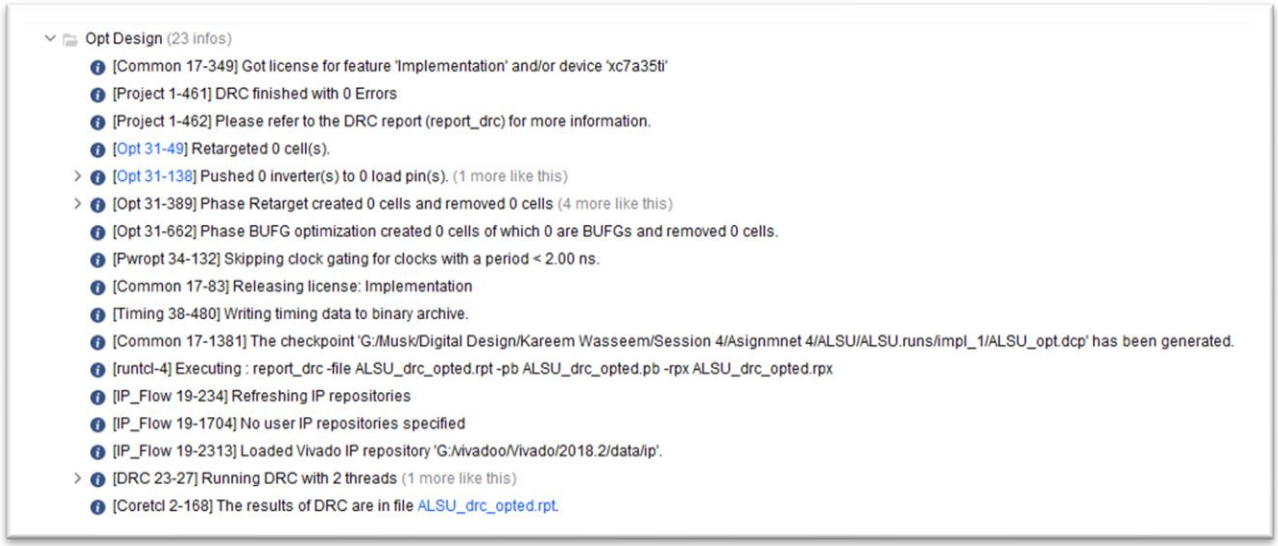
All user specified timing constraints are met.

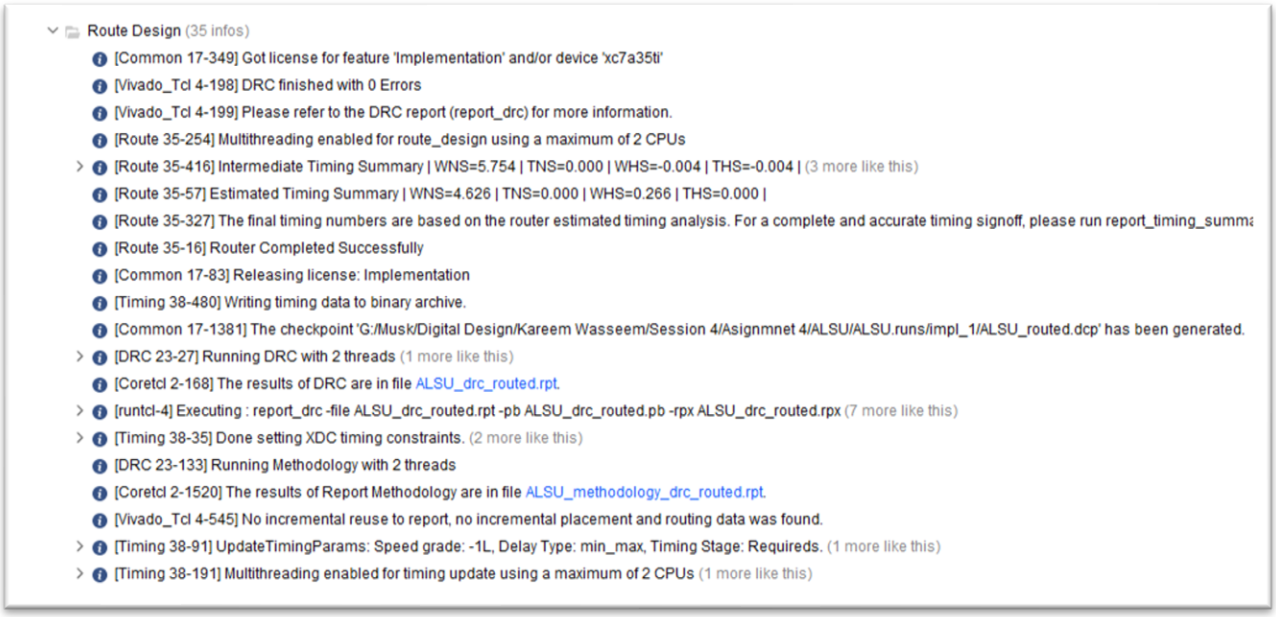
Implementation Device

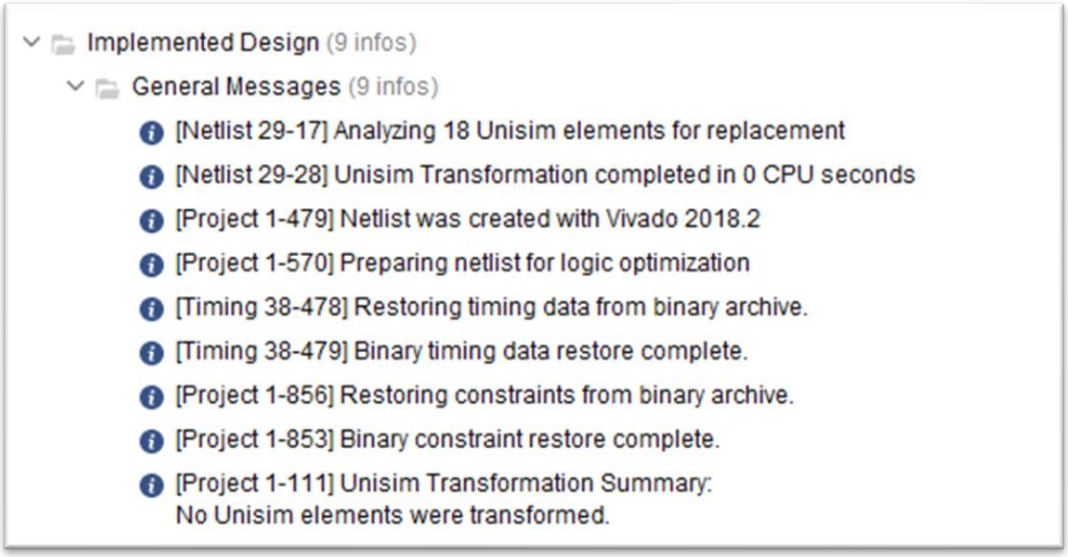


Implementation Messages




Opt Design (23 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
[Project 1-461] DRC finished with 0 Errors
[Project 1-462] Please refer to the DRC report (report_drc) for more information.
[Opt 31-49] Retargeted 0 cell(s).
[Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
[Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
[Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
[Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
[Common 17-83] Releasing license: Implementation
[Timing 38-480] Writing timing data to binary archive.
[Common 17-1381] The checkpoint 'G:/Musk/Digital Design/Kareem Wasseem/Session 4/Asignmnet 4/ALSU/ALSU.runs/impl_1/ALSU_opt.dcp' has been generated.
[runtcl-4] Executing : report_drc -file ALSU_drc_opted.rpt -pb ALSU_drc_opted.pb -rpx ALSU_drc_opted.rpx
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'G:/vivadoo/Vivado/2018.2/data/ip'.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file ALSU_drc_opted.rpt.


Route Design (35 infos)
[Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
[Vivado_Tcl 4-198] DRC finished with 0 Errors
[Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
[Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
[Route 35-416] Intermediate Timing Summary | WNS=5.754 | TNS=0.000 | WHS=-0.004 | THS=-0.004 | (3 more like this)
[Route 35-57] Estimated Timing Summary | WNS=4.626 | TNS=0.000 | WHS=0.266 | THS=0.000 |
[Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summa
[Route 35-16] Router Completed Successfully
[Common 17-83] Releasing license: Implementation
[Timing 38-480] Writing timing data to binary archive.
[Common 17-1381] The checkpoint 'G:/Musk/Digital Design/Kareem Wasseem/Session 4/Asignmnet 4/ALSU/ALSU.runs/impl_1/ALSU_routed.dcp' has been generated.
[DRC 23-27] Running DRC with 2 threads (1 more like this)
[Coretcl 2-168] The results of DRC are in file ALSU_drc_routed.rpt.
[runtcl-4] Executing : report_drc -file ALSU_drc_routed.rpt -pb ALSU_drc_routed.pb -rpx ALSU_drc_routed.rpx (7 more like this)
[Timing 38-35] Done setting XDC timing constraints. (2 more like this)
[DRC 23-133] Running Methodology with 2 threads
[Coretcl 2-1520] The results of Report Methodology are in file ALSU_methodology_drc_routed.rpt.
[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)


Implemented Design (9 infos)
General Messages (9 infos)
[Netlist 29-17] Analyzing 18 Unisim elements for replacement
[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
[Project 1-479] Netlist was created with Vivado 2018.2
[Project 1-570] Preparing netlist for logic optimization
[Timing 38-478] Restoring timing data from binary archive.
[Timing 38-479] Binary timing data restore complete.
[Project 1-856] Restoring constraints from binary archive.
[Project 1-853] Binary constraint restore complete.
[Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Implementation Utilization Report

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
N ALSU	47	44	26	47	10	40	1

Implementation Timing Report

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.628 ns	Worst Hold Slack (WHS):	0.287 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	28	Total Number of Endpoints:	28	Total Number of Endpoints:	45

All user specified timing constraints are met.

I Failed to generate the bitstream.

- Implementation (3 errors)
  - Write Bitstream (3 errors)
    - DRC (2 errors)
      - Pin Planning (2 errors)
        - [DRC NSTD-1] Unspecified I/O Standard: 6 out of 40 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical ports have a user specified I/O standard value defined. To allow bitstream creation with unspecified I/O standard values (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: out[5:0].
        - [DRC UCIO-1] Unconstrained Logical Port: 6 out of 40 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: out[5:0].
      - [Vivado 12-1345] Error(s) found during DRC. Bitgen not run.