National Institute Of Technology, Patna

(Department Of Electrical Engineering)

MINOR PROJECT REPORT ON

"Designing of radiation tolerant SRAM cell against single event upset (SEU)"

UNDER THE SUPERVISION OF

Prof. G.K. Choudhary

Department of Electrical Engineering

SUBMITTED BY

Amratansh Gupta (1402061)
Md. Ezaz Hussain (1401014)
Sujeet Kumar (1402028)

CERTIFICATE

This is to certify that Minor project report entitled "**Designing of radiation tolerant SRAM cell against single event upset (SEU)** " submitted by Amratansh Gupta (1402061), Md. Ezaz Hussain (1401016) and Sujeet Kumar (1402028) students of 6th semester B.Tech.(Electrical Engineering) of National Institute Of Technology Patna has completed the work under my supervision

Prof. G.K. Chaudhary

Project Supervisor

Professor, Department of Electrical Engineering

National Institute of Technology Patna

EXAMINERS SIGNUTURE

1.

2.

CANDIDATE'S DECLARATION

This is to certify that Minor Project report entitled "**Designing of radiation tolerant SRAM cell against single event upset (SEU)** " has been prepared by Amratansh Gupta (1402061), Md. Ezaz Hussain (1401016) and Sujeet Kumar (1402028) students of 6th semester B.Tech.(Electrical Engineering) under the supervision of Prof G.K. Choudhary professor of Electrical Engineering Department NIT,PATNA and has not been submitted elsewhere for award of any degree.

Amratansh Gupta (1402061)

Md. Ezaz Hussain (1401014)

Sujeet Kumar (1402028)

Prof G.K. Chaudhary

Supervisor

Professor

Department of Electrical Engineering

National Institute of Technology Patna

ACKNOWLEDGEMENT

We would like to acknowledge those who pitched in to push this seminar report over the finish line.

We are deeply indebted to **Prof. G.K. Chaudhary** for his supervision and guidance. He has helped us a lot by giving their precious time in upbringing the report. We also extend our gratitude to all our colleagues, **Dr. Gaurav Kaushal**, assistant professor Electronics & Communication Department and all the professor of Electrical Engineering Department, NIT Patna.

We express our sincere thanks **Prof. G.K. Chaudhary** to for making every possible arrangement for completing the seminar report

Dated:

Place: Patna

Amratansh Gupta (1402061)

Sujeet Kumar (1402028)

Md. Ezaz Hussain (1402016)

Static Read-Write Memory (SRAM) Circuits

Read-write (R/W) memory circuits are designed to permit the modification (writing) of data bits to be stored in the memory array, as well as their retrieval (reading) on demand. The memory circuit is said to be static if the stored data can be retained indefinitely (as long as a sufficient power supply voltage is provided), without any need for a periodic refresh operation, We will examine the circuit structure and the operation of simple SRAM cells. [1]

The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states). Depending on the preserved state of the two- inverter latch circuit, the data being held in the memory cell will be interpreted either as a logic 'O" or as a logic "1". To access (read and write) the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, i.e., the row address selection signal (Fig.1). Usually, two complementary access switches consisting of NMOS pass transistors are implemented to connect the 1-bit SRAM cell 10 the complementary bit lines (columns). This can be likened to turning the car steering wheel with both left and right hands in complementary directions. [1]

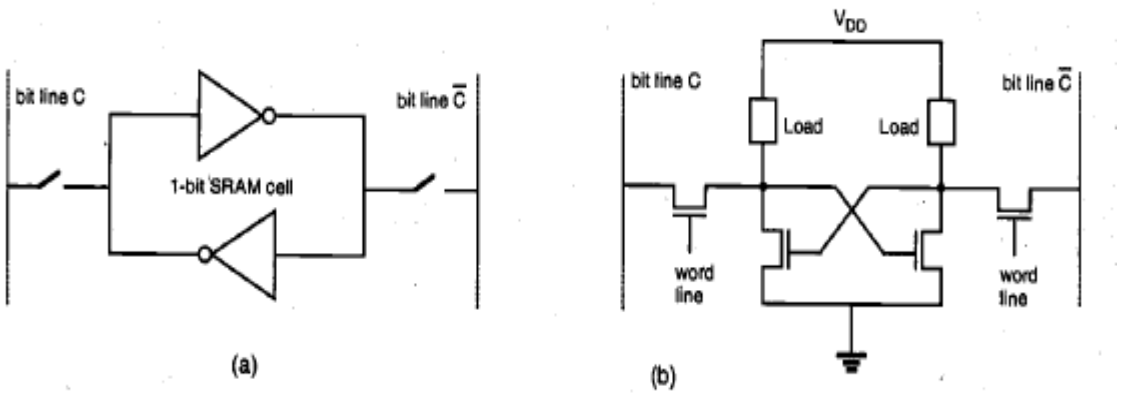


Fig 1: Basic Schematic of SRAM Cell

Full CMOS SRAM Cell

A low-power SRAM cell may be designed simply by using cross-coupled CMOS inverters instead of the resistive-load nMOS inverters. In the Full CMOS SRAM cell, the stand-by power consumption of the memory cell will be limited to the relatively small leakage currents of both CMOS inverters. The possible drawback of using CMOS SRAM cells, on the other hand, is that the cell area tends to increase in order to accommodate the n-well for the pMOS transistors and the polysilicon contacts.

The circuit structure of the full CMOS static RAM cell is shown in Fig. 2, along with the pMOS column pull-up transistors on the complementary bit lines. The most important advantage

of this circuit topology is that the static power dissipation is even smaller; essentially, it is limited by the leakage current of the pMOS transistors. A CMOS memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force for the increasing prominence of high-density CMOS SRAMs. Other advantages of CMOS SRAM cells include high noise immunity due to larger noise margins, and the ability to operate at lower power supply voltages than the resistive-load SRAM cells.

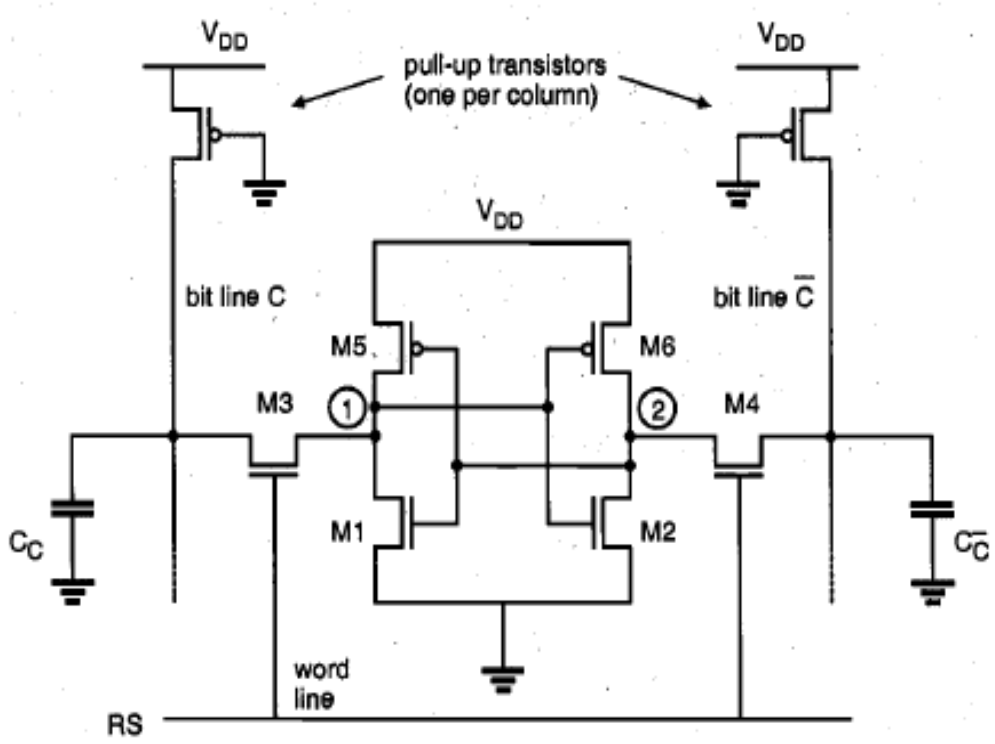


Fig 2: Six Transistor CMOS based SRAM circuit with bit lines [1]

The major disadvantages of CMOS memories historically were larger cell size, the added complexity of the CMOS process, and the tendency to exhibit 'latch-up" phenomena. With the widespread use of multi-layer polysilicon and multi-layer metal processes, however, the area disadvantage of the CMOS SRAM cell has been reduced significantly in recent years. Considering the undisputable advantages of CMOS for low-power and low-voltage operation, the added process complexity and the required latch-up prevention measures do not present a substantial barrier against the implementation of CMOS cells in high density SRAM arrays. [1]

Read / Write Operation

a) **Write '1' operation**: The voltage level of column is forced to logic-low by the data-write circuitry. The driver transistor Ml turns off. The voltage V1 attains a logic-high level, while V2 goes low.

b) **Read '1' operation**: The voltage of column C retains its precharge level while the voltage of column C is pulled down by M2 and M4. The data-read circuitry detects the small voltage difference (Vc> V)and amplifies it as a logic "1" data output.

c) **Write '0' operation**: The voltage level of column C is forced to logic-low by the data-write circuitry. The driver transistor M2 turns off. The voltage V2 attains a logic-high level, while V1 goes low.

d) **Read '0' operation**: The voltage of column retains its precharge level while the voltage of column C is pulled down by M1 and M3. The data-read circuitry detects the small voltage difference (Vc < VE) and amplifies it as a logic "0" data output.

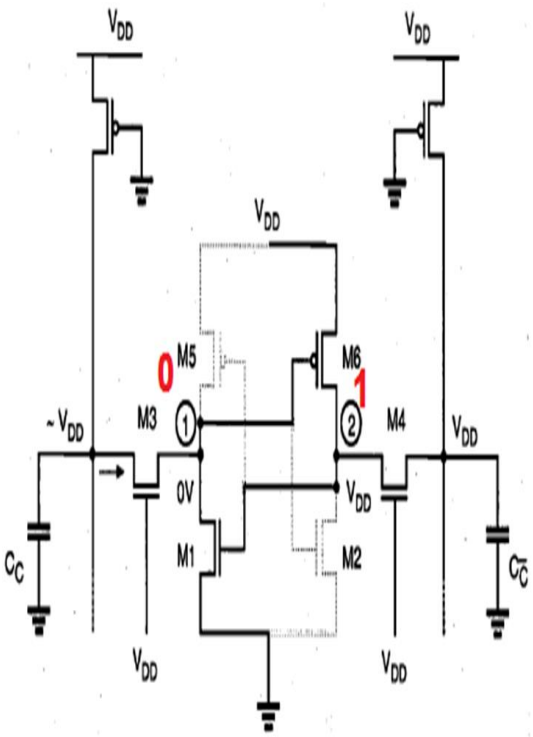


Fig 3: Read '0' operation [1]

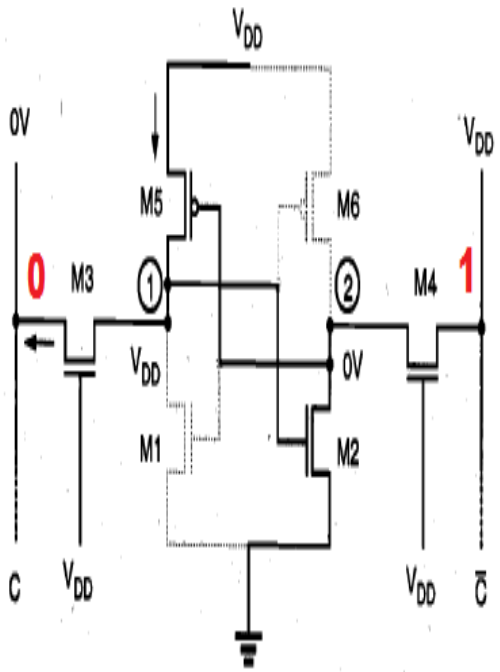
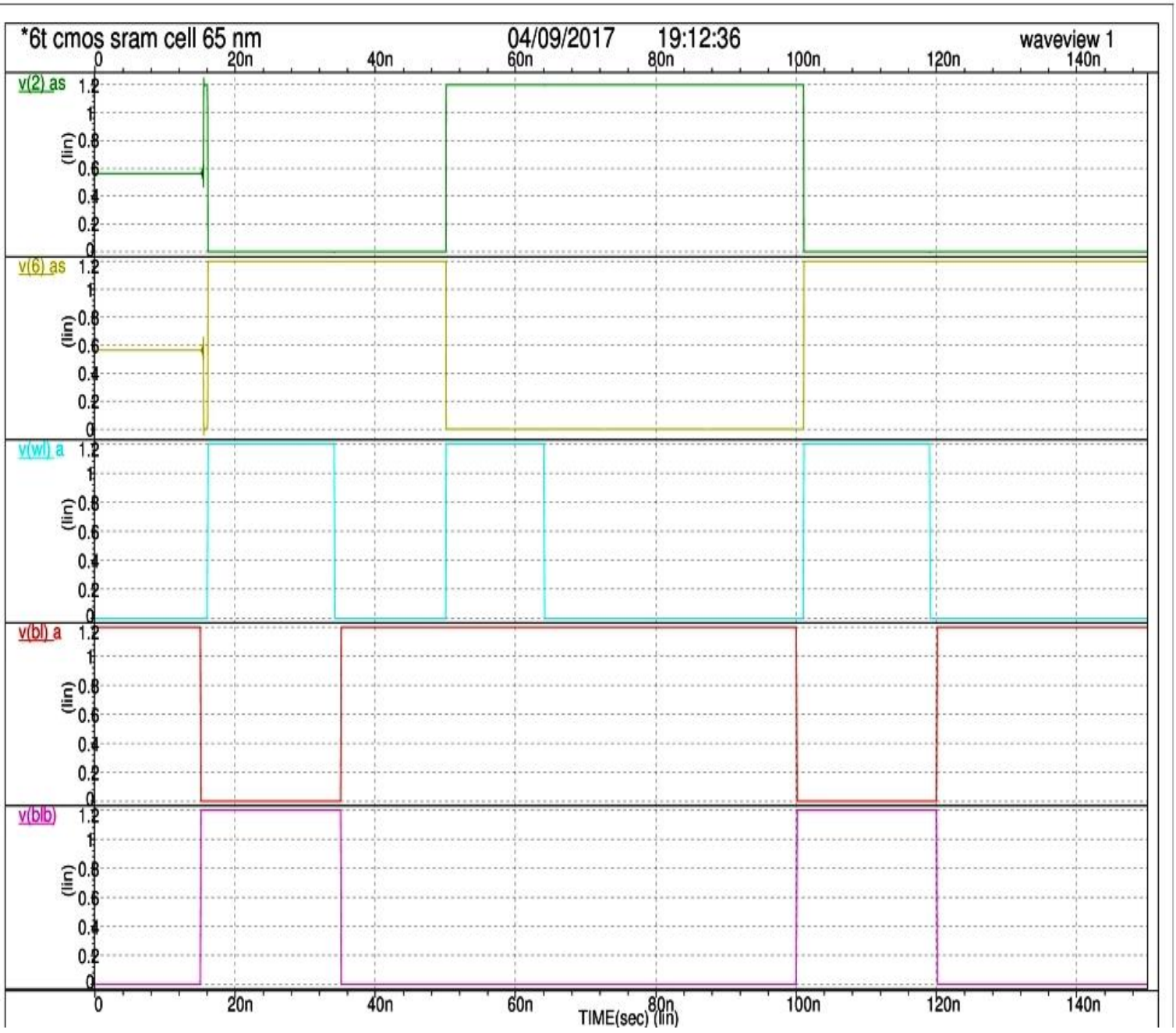


Fig 4: Write '0' operation [1]

After studying the standard literature of 6 transistors CMOS SRAM cell, we simulate the read and write operation of CMOS SRAM Cell using BSIM-SOI models for nMOS and pMOS for 65nm channel length. Simulations results are shown below:



Simulation 1: Simulation of read/write operation of 6 Transistor CMOS SRAM Cell

Single Event Upset (SEU) in semiconductor memory circuits

Single event upsets (SEUs) induced by particle radiation are becoming an increasing important threat to the reliability of memories fabricated in nanoscale CMOS technologies. SEUs are caused by particle-induced charge which is derived from direct ionization from heavy ions and indirect ionization from protons and neutrons [7]. A single event upset (SEU)

is a change of state caused by one single ionizing particle (ion, electron, α -particle) striking a sensitive node in a semiconductor device.

An energetic particle passes through the sensitive node of a semiconductor device it frees electron-hole pairs along its path as it loses energy. The electric field present in a reverse-biased junction depletion region can separate electron-hole pairs, so that the particle-induced charge is very efficiently collected through drift processes leading to an accumulation of extra charge at the sensitive node [7]. When the amplitude of the accumulated charge is enough and the time is long enough, it can generate a large voltage transient pulse which changes temporarily the value of the sensitive node (see Fig. (a))

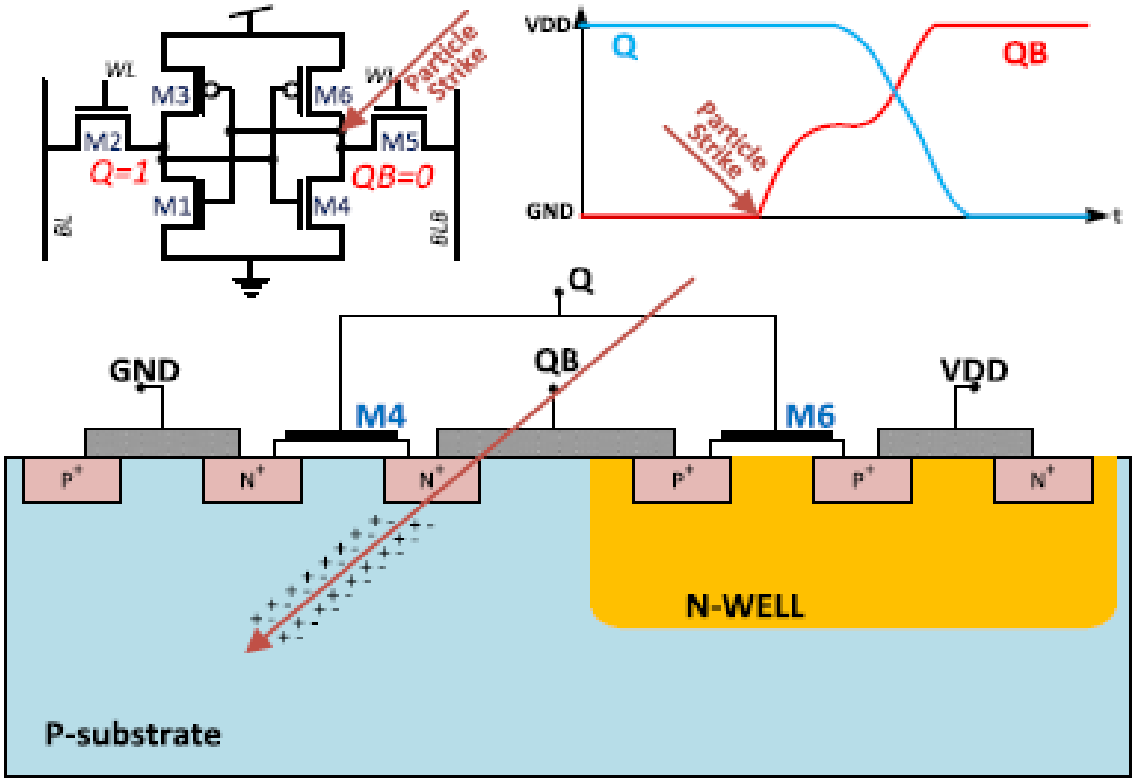


Fig 5: Particle strike hitting a silicon substrate junction, releasing electron–hole pairs, and causing a state flip in an SRAM cell

Modelling of Single Event

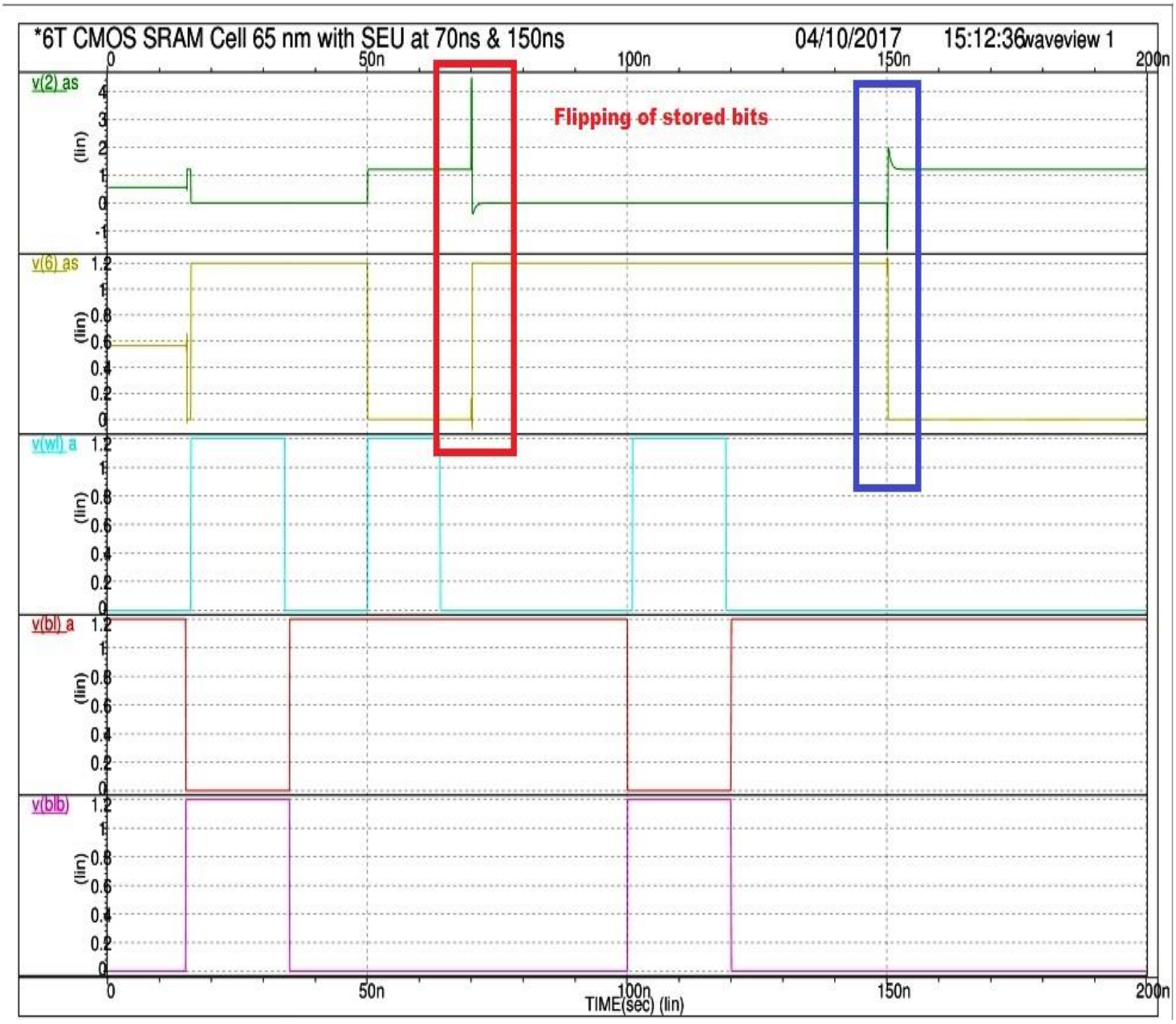
In a storage cell such as an SRAM cell, when deposited charge by a particle strike in the struck node is greater than the critical charge ($Q_{critical}$) of that node, an single event upset(SEU) will takes place.

$Q_{critical}$ for a node in a storage cell is defined as the minimum charge needed to alter the stored value of the storage cell when deposited in that node.

To model the injection of a particle strike and its associated deposited charge, we use the proposed model in [3] that is widely accepted by the researches [4],[5]. This model is a double exponential current source that is given by:

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2}(e^{-t/\tau_1} - e^{-t/\tau_2})$$

where, the Q_{inj} denotes the amount of injected charge in the struck region. Also, $\tau 1$ and $\tau 2$ are material dependent time constants ($\tau 1$ and $\tau 2$ are in range of 25 - 300 picosecond).



Simulation 2: Simulation of SEU on 6 Transistor CMOS SRAM Cell at 70ns and 150ns

Effects because of SEU on SRAM based circuits: [6]

- Modern *Field Programmable Gate Arrays* [FPGAs] provide a large number of Logic blocks and routing resources contains more than 50% SRAM cells [6].Hence, any error in stored data may affect the working of logic block.
- A particle strike on a SRAM cell (used to control routing switch) results in device failure or functional error.

Study of standard and reported radiation hard circuits

- **Dual Interlocked Cell [DICE] [2]**

As shown in Fig. 7, the DICE cell uses twice the number of transistors of a standard storage (6 T) cell. The DICE cell has two states, the **0 state (x1 = 0, x2 = 1, x3 = 0, x4 = 1)** and the **1 state (x1 = 1, x2 = 0, x3 = 1, x4 =0).** In any of these two states upon the occurrence of a single event as soft error (on a single node too), the state of the node is always driven back to its original value. For example, in the 0 state, if the node struck by a particle is x2, the state of x2 goes from 1 to 0. However, this strike does not propagate along the feedback loop due to the interlocked configuration. Meanwhile, the state 0 stored in x1 can restore the state of x2.

However, when a single event (strike) occurs on multiple nodes, the DICE cell is unable to drive back the original state. **In this case, due to the strike on x1, the state of x2 will not be restored and a soft error is said to occur**. **However, if there is a strike on x1, a very small amount of charge on x2 can change the state of the DICE.**

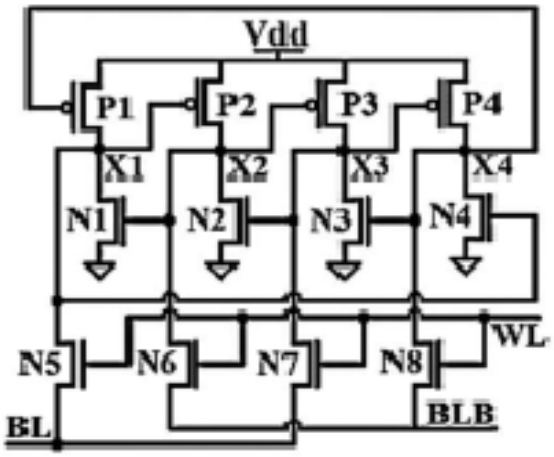


Fig 6: DICE Cell

- **DICE modified "TDICE" [2]**

This new cell design is a variant of DICE by adding NMOS transistors as (switching) resistive devices for tolerance to a single event with multiple-node upset. This design is shown in Fig. 8. The DICE cell circuit is modified by inserting four NMOS transistors into the feedback loops of the PMOS transistors of the inverters. These additional transistors are connected to WL such that they are turned on during the read and write operations.

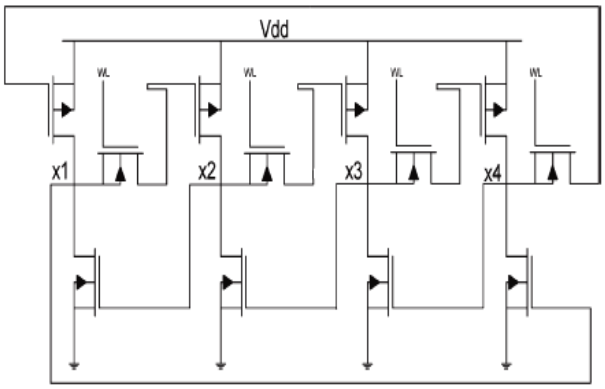


Fig 7: Modified DICE Cell mentioned as TDICE **[2]**

Comparison of DICE and TDICE:

PERFORMANCE COMPARISON

	Delay (psec)	Power (µW)	Normalized Area
6T 32nm	12.2 0	20.11	1
6T 45nm	16.72	23.73	1
DICE 32nm	21.19	43.67	2
DICE 45nm	25.34	61.11	2
TDICE 32nm	29.99	47.78	2.66
TDICE 45nm	34.48	68.14	2.66

Table 1

The critical charge (as measure of tolerance of a hardened cell) of TDICE is increased by more than 300% in compared to the critical charge of the DICE cell. **Hence, there is a trade-off between power-delay product and critical charge of memory cell.**

- **Quatro Cell [4]**

The SEU-tolerant storage cells with small area overhead are preferred by designers. Although Dual Interlock Storage Cell (DICE), a latch consisting of four interlocked inverters, has been widely used to mitigate SEU errors, the SEU hardness is achieved at the expense of doubled transistor counts compared with the 6T memory cell. This makes DICE design less attractive for applications where compact layout is critical such as SRAMs. Jahinuzzaman et al. introduced the 10 Transistor-Quatro cell,
which uses fewer transistors compared with DICE. This design reduces power by approx. 40% and layout area by 30% compared with those of DICE. However, the issue of Quatro is that it may still upset even if only one node is hit during the Hold mode in some cases. [13] The schematic of Quatro cell is shown below storing (Q2=1, iD2=1, Q1=0 & iD1=0).

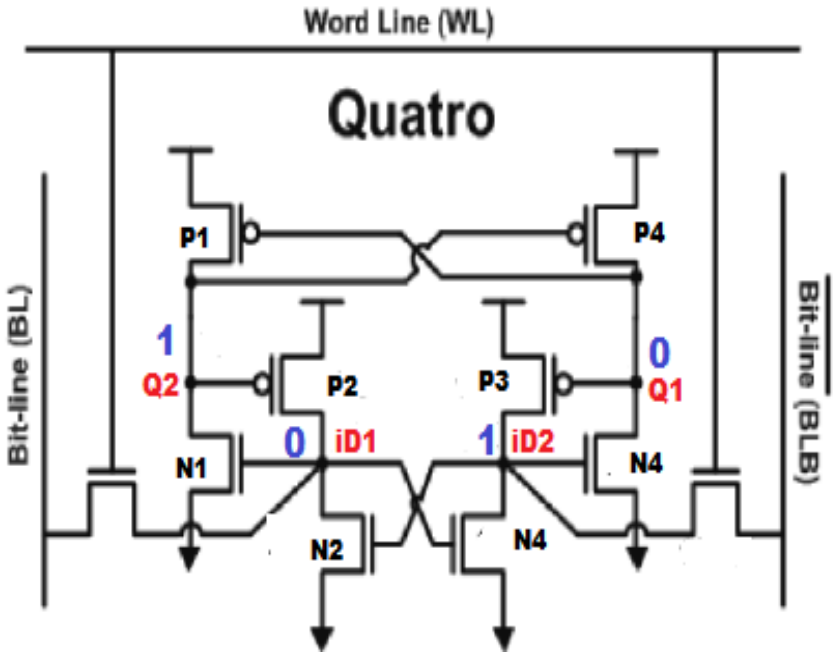
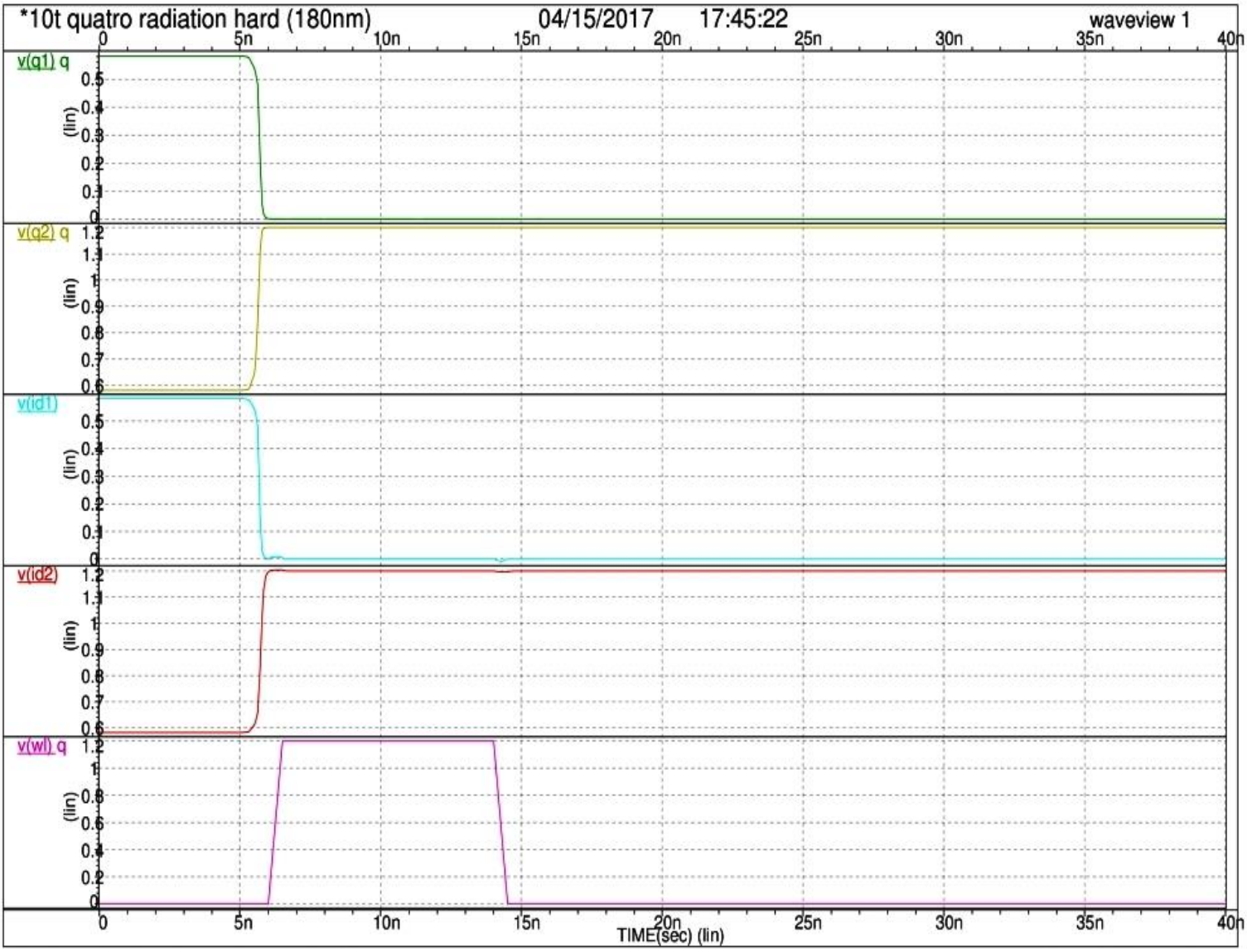


Fig 8: 10T- Quatro Cell

It is not immune to single node upsets in the Hold state. For instance, assume the logic values of nodes Q1, Q2, iD1 and iD2 are 0, 1,0 and 1, respectively, as shown in Fig.10. If the transistor P2 is struck by an ion particle, the voltage of its drain iD1 would rise, and as a result, the transistors N1 and N3 may be turned on.



Simulation 3: Simulation of write operation of 10T-Quatro Cell

▪ Modified Quatro (proposed in [4])

This design is same as original Quatro cell. However, it has two extra NMOS transistors; N12 and N34 are added in the feedback loops. N12 is placed between the gate of N1 (node iD1L) and node iD1, while N34 is placed between the gate of N4 (node iD2R) and node iD2. The gates of these extra NMOS transistors are connected to Clock'. The design has two internal storage nodes (iD1 and iD2) and two output nodes (Q1 and Q2).During a write operation, Clock is Low, Clock' is High, the blocking transistors N12 and N34 are turned on. The cell behaves like an original Quatro cell except for additional resistance added to the paths. During a Hold mode, Clock is High, Clock' is Low, the blocking transistors N12 and N34 are turned off, thus, iD1L and iD2R are left floating. However, the voltages of these two nodes are able to be maintained by using subthreshold leakage currents . For example, assume

that iD1L is logic High initially and left floating after N12 is turned off. As long as the subthreshold leakage of N12 is larger than the gate leakage of N1, iD1L can still maintain its voltage.

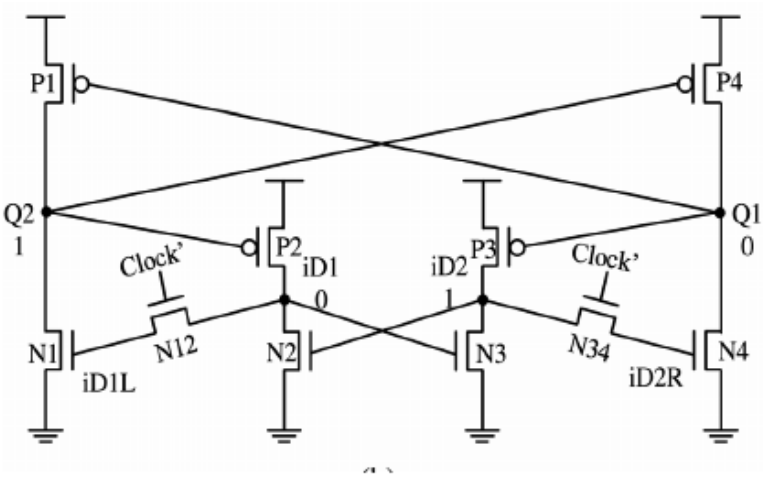


Fig 9: Modified Quatro with 2 extra nMOS

The radiation tolerance limit of the modified quarto is higher than original Quatro cell. The main idea behind this design is to control the feedback paths and subthreshold leakage currents.

RELATIVE PERFORMANCE COMPARISON

	Original Quatro	DICE	Proposed Design
Area	1	1.20	1.11
Delay	1	1.28	1.50
Power	1	1.31	1.50

Table 2: Values scaled with respect to original Quatro Cell [4]

This result shows there is a trade-off between area, power-delay product and radiation tolerant capability of memory cell.

Simulation 4: Simulation of SEU at node 'id1' at 25ns on 10T-Quatro Cell (using 180nm SOI BSIM models)

Results for 10T-Quatro (using HSPICE 180nm BSIM models):

SEU Strike Node	Operation	Critical Charge (in pC)
iD1	Write '1'	4.443
	Write '0'	0.2614
iD2	Write '1'	0.0694
	Write '0'	2497.2

Q1	**Write '1'**	**0.3612**
	Write '0'	**3782**
Q2	**Write '1'**	**3920**
	Write '0'	**0.36134**

Table 3

- ## RHD 11T- Cell:

In this circuit (that includes only11 transistors), access transistor of N6 is controlled by word line (WL). In the keeper part of the cell (consisting of all transistors except N6), transmission gates T1 and T2 are responsible for connecting/disconnecting the feedback loop from inverter (P1, N1) to the C-element (P3, P4, N3, N4). When refresh line (RL) is high (and consequently RLB is low) transmission gates T1 and T2 are ON. Therefore, they close the feedback loop. It should be noted that, RL goes high when WL goes high. When WL is low, RL should go high and low periodically to avoid losing the stored value. In fact, the proposed robust SRAM cell works like a DRAMwhen the RL is low. Now, suppose bit line (BL) is '1', when WL is high, node X1 takes a '1' and causes transistor N1 to turn ON. Consequently, X2 gets a logic value of '0'. As both transmission gates T1 and T2 are ON, nodes X3 and X4 both get logic values of '0' as well. As a result, P3 and P4 turn ON and X5 pulls up to VDD (logic '1').When WL goes low, RL goes low as well and the SRAM cell keeps its stored value. If the feedback loop is left open, i.e., RL remains at '0' until the read operation, the stored logic value might be lost.

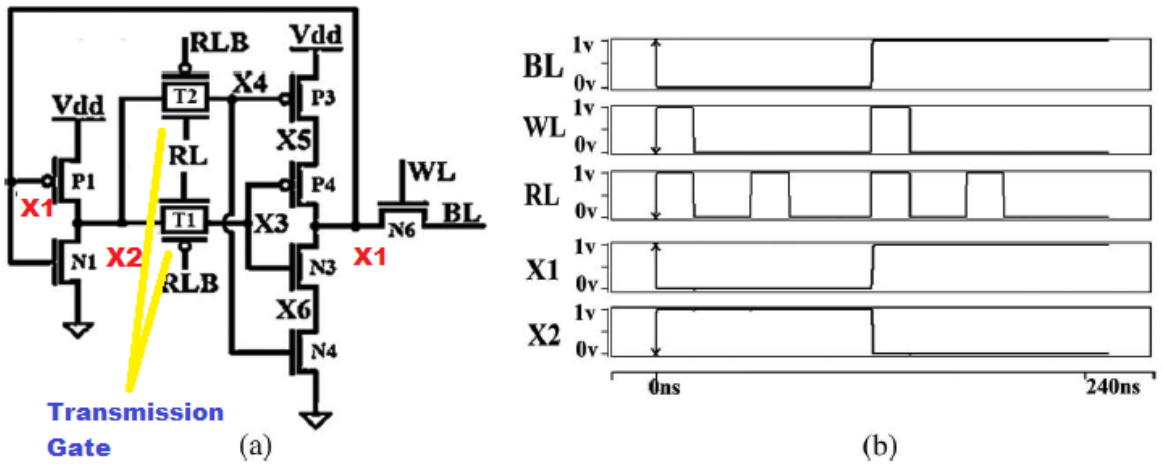
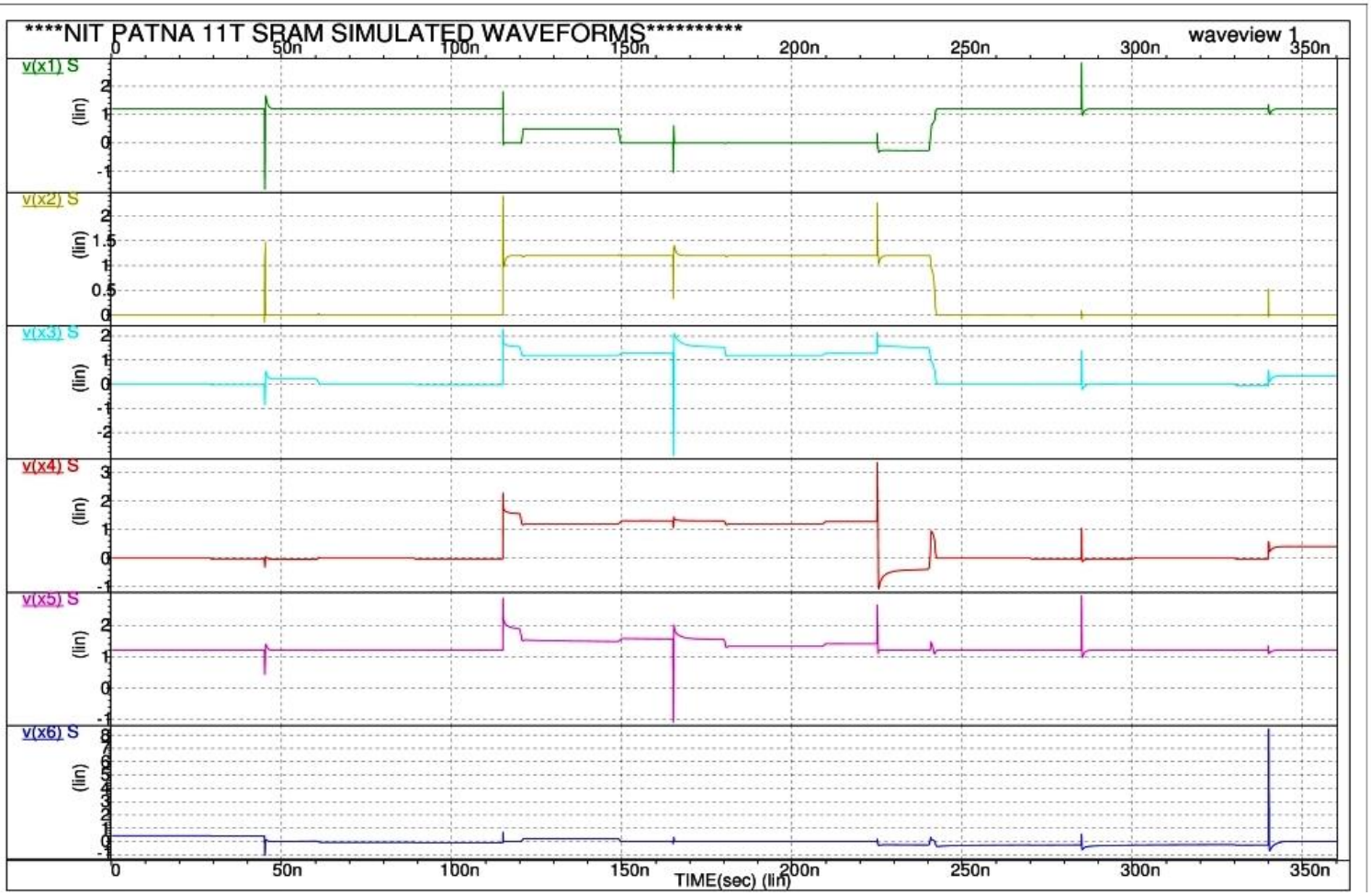


Fig 10: **a)** 11T transistor SRAM cell circuit proposed in [3] termed as RHD11 ;

b) Normal operation diagram



Simulation 5: Simulation of SEU at nodes 'x1', 'x2', 'x3', 'x4', 'x5' and 'x6'in sequence (using 180nm SOI BSIM models).

Observations and Results of study:

Basically, there are three principles to design a radiation tolerant latch:

1. **Block the feedback loop of the cell so that a transient pulse could not be propagated along this loop to reach back its creation point**.(Used in TDICE and Modified Quatro)

2. **Separate the gates of the nMOS and pMOS transistor of some inverter, to harden nodes unprotected by the first principle**. (shown in RHD 11T-Cell)

3. **Introduce a regeneration principle to avoid losing stored information in nodes that are electrically isolated due the first principle.**(Used in standard 6T SRAM)

Proposed Design 1:

In this proposed design, the circuit (that includes only 11 transistors), access transistor of N6 is controlled by word line (WL). In the keeper part of the cell (consisting of all transistors except N6), transmission gates T1 and T2 are responsible for connecting/disconnecting the feedback loop from inverter (P1, N1) to (P3, P4, N3, N4).In the circuit transistors P3 & P4 are connected in parallel, similarly N3 & N4 are in parallel. When refresh line (RL) is high (and consequently RLB is low) transmission gates T1 and T2 are ON. Therefore, they close the feedback loop. It should be noted that, RL goes high when WL goes high. When WL is low, RL should go high and low periodically to avoid losing the stored value. In fact, the proposed robust SRAM cell works like a DRAM when the RL is low. Now, suppose bit line (BL) is '1', when WL is high, node X1 takes a '1' and causes transistor N1 to turn ON. Consequently, X2 gets a logic value of '0'. As both transmission gates T1 and T2 are ON, nodes X3 and X4 both get logic values of '0' as well. As a result, P3 and P4 turn ON and X5 pulls up to VDD (logic '1').When WL goes low, RL goes low as well and the SRAM cell keeps its stored value. If the feedback loop is left open, i.e., RL remains at '0' until the read operation, the stored logic value might be lost. Having (P3 & P4) and (N3 & N4) in parallel will increase the charging and discharging paths at node X1,which leads to higher radiation tolerance level.

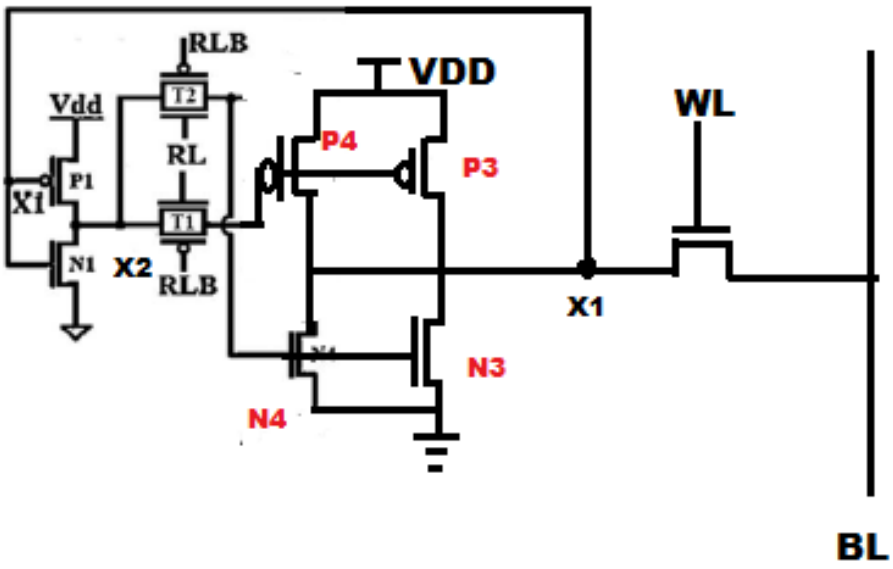
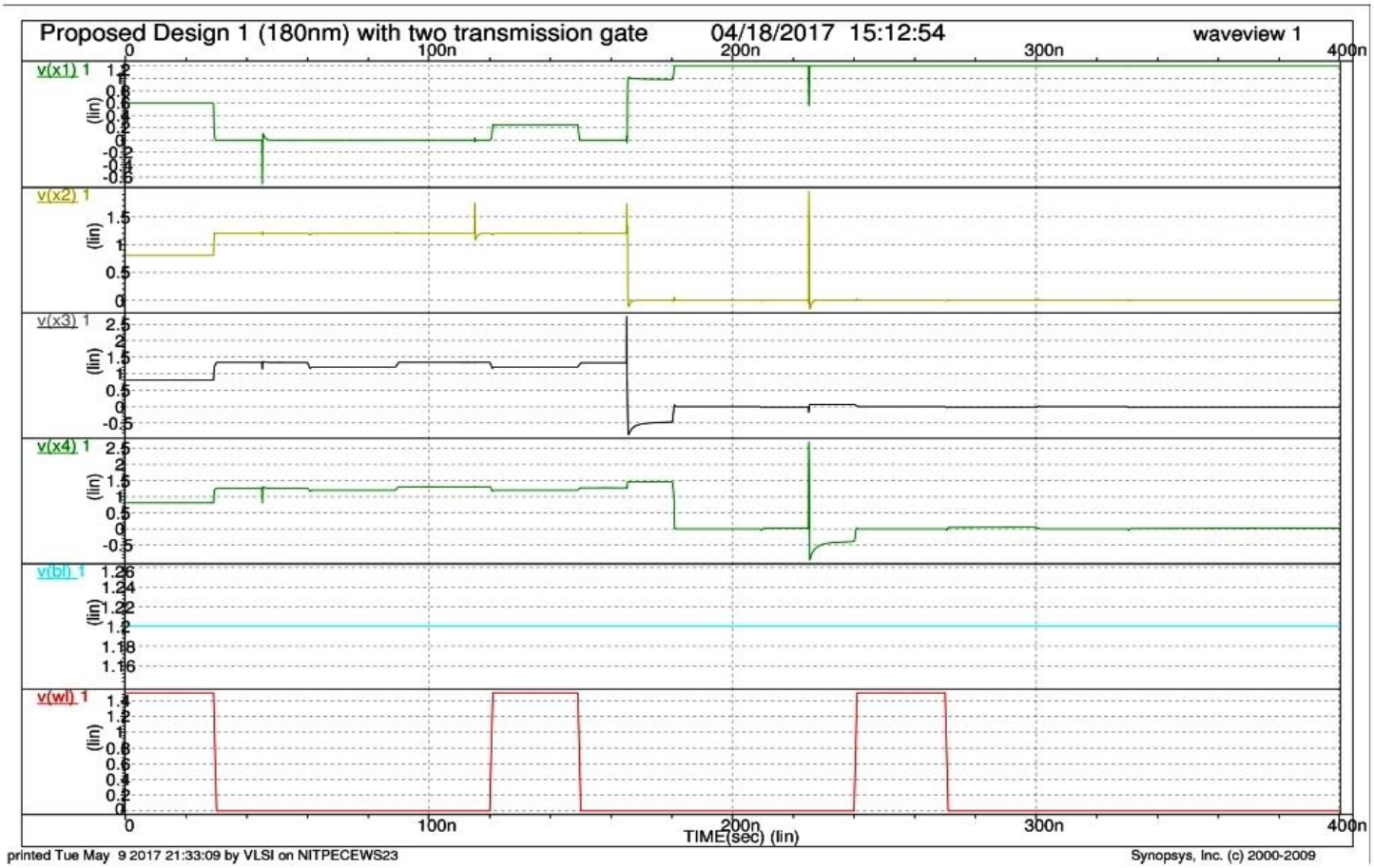


Fig 11: Proposed SRAM Cell 1

However, this design is not best suited because of transmission gates which are reducing the critical charge of the node X1 and X2.[8] However, use of transmission gates reduces the write and read delay. There is a trade-off between operation speed and critical charge of cell. Apart from these issues, a single ended SRAM cell (with 1 bit line) operates correctly when writing a '0' as data, but it encountered problem while writing '1' as data.



Simulation 5: Simulation of SEU at nodes ‘x1’, ‘x2’, ‘x3’ and ‘x4’in sequence (using 180nm SOI BSIM models).

Proposed Design 2 (improvement over design 1):

In this design, we eliminated the transmission gates T1 and T2 from the memory cell and add one more bitline in order to stabilize the write ‘1’ process. Inverter 1 consists of (P1,N1) and inverter 2 consists of (P2,N2) are connected back to back. However, there is one more additional inverter, inverter3, connected in parallel with inverter 2.

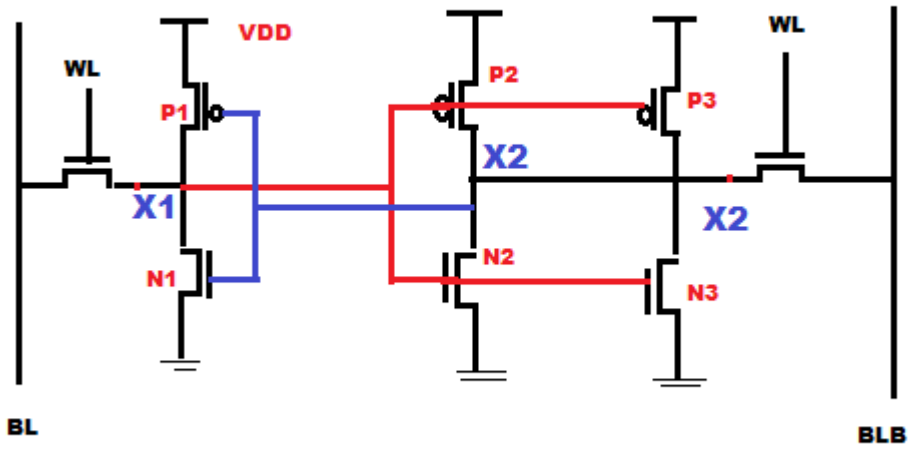


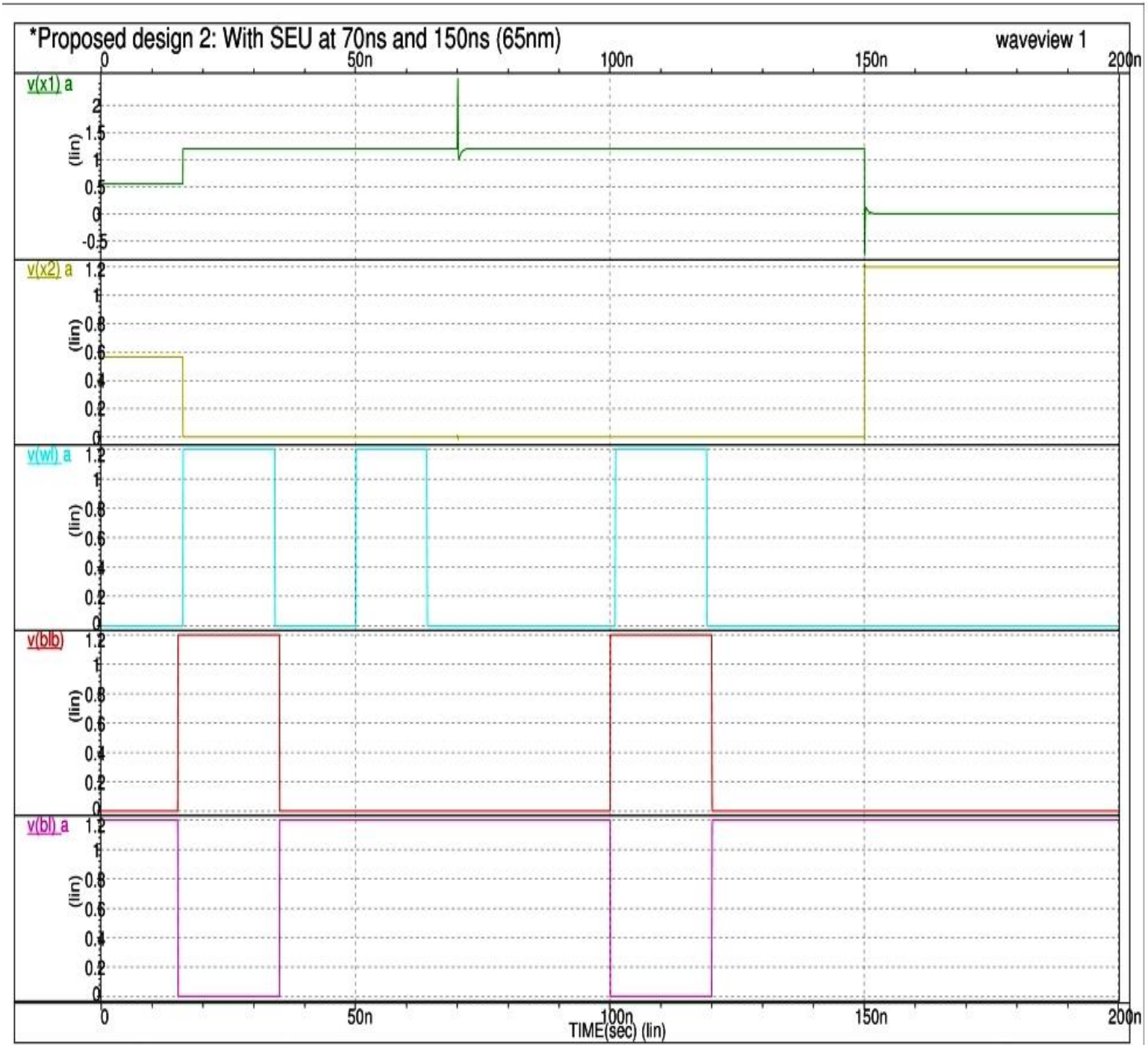
Fig 12: Proposed design 2

In this design, we overcome the issue of single bitline as explained above. However,we use only 10 transistor in place of 11 transistor in comparison of proposed design 1, it will lead to lower area on chip as compared to proposed design 1.The critical charge (measure of tolerance) is higher in case of proposed design 2 than proposed design 1.The increase in case of critical charge is because of elimination of transmission gates T1 and T2 in proposed design 2.

Observation and Results: (using BSIM SOI 65nm model cards)

SEU Strike Node	X1 store	Critical Charge (in fC)
X1	'1'	37.025
	'0'	85.377
X2	'1'	37.166
	'0'	37.179

Table 4: Critical charges for proposed design 2



Simulation 6: Simulation of SEU at node 'x2' of proposed design (using 65nm SOI BSIM model cards).

The above simulation clearly shows the radiation tolerant nature of proposed design. However, this design have higher read and writing delays than standard 6T SRAM. In comparison to DICE, it has lower area overhead, higher power-delay product and higher critical charge.

Conclusion:

In this project, we put a lot of emphasis on study research journals and principles to design radiation tolerant SRAM cell, which is supported by HSPICE simulations. We proposed two designs for radiation tolerant SRAM cell, in which proposed design 2 is superior and modified circuit of proposed design 1.Thus, improvements in proposed design 1 leads us to proposed design 2.In this designs, we put more focus on techniques to increase critical charges of critical nodes (more probable to undergo SEU).

References:

1. Textbook : **CMOS digital integrated circuits analysis & design by Sung-Mo(Steve) Kang and Yusuf Leblebici**, 3rd edition ISBN-13:978-0-07-053077-5
2. "***Design of a Nanometric CMOS Memory Cell for Hardening to a Single Event With a Multiple-Node Upset*** " by M. D'Alessio, M. Ottavi and F. Lombardi, in **IEEE Transactions on Device and Materials Reliability**, vol. 14, no. 1, pp. 127-132, March 2014.
3. "***Design of Robust SRAM Cells Against Single-Event Multiple Effects for Nanometer Technologies*** " by R. Rajaei, B. Asgari, M. Tabandeh and M. Fazeli, in **IEEE Transactions on Device and Materials Reliability**, vol. 15, no. 3, pp. 429-436, September 2015
4. "***An Area Efficient SEU-Tolerant Latch Design***," by H. B. Wang *et al*., in **IEEE Transactions on Nuclear Science**, vol. 61, no. 6, pp. 3660-3666, Dec. 2014.
5. "**A 32 kb Macro with 8T Soft Error Robust, SRAM Cell in 65-nm CMOS**," by J. S. Shah, D. Nairn and M. Sachdev, **in *IEEE Transactions on Nuclear Science***, vol. 62, no. 3, pp. 1367-1374, June 2015.
6. ***"*Consequences and categories of SRAM FGPA conguration SEUs** " by P. Graham, M. Caffrey, J. Zimmerman, and D. E. Johnson, **Proceedings of the Military and Aerospace Applications of Programmable Logic Devices (MAPLD)** Washington D.C., 2004
7. "**Novel Low-Power and Highly Reliable Radiation Hardened Memory Cell for 65 nm CMOS Technology**," by J. Guo, L. Xiao and Z. Mao, in ***IEEE Transactions on Circuits and Systems** I: Regular Papers*, vol. 61, no. 7, pp. 1994-2001, July 2014.
8. "**Single Event-Induced Error Propagation Through Nominally-off Transmission Gates**," by J. M. Hutson *et al*.,in ***IEEE Transactions on Nuclear Science***, vol. 53, no. 6, pp. 3558-3562, Dec. 2006.