

Amratansh Gupta

B.TECH IN ELECTRICAL ENGINEERING FROM NIT PATNA

WORK EXPERIENCE	Research Associate (under Prof. Nihar R. Mohapatra) Indian Institute of Technology(IIT) Gandhinagar, Gandhinagar, India <i>Jul' 18 - Present</i>
EDUCATION	National Institute of Technology(NIT) Patna, India <i>Bachelor of Technology</i> in Electrical Engineering, CGPA: 8.74/10* (Dept. Rank - 4 th out of 86) <i>Jul' 14 - June' 18</i> Maa Anjani Public School, CBSE, Shikohabad India <i>HighSchool</i> - Science Stream, Percentage: 86.6% (Class Rank - 1 st) <i>Jul' 11 - June' 13</i>
RESEARCH INTERESTS	Semiconductor Devices, Semiconductor Device Modeling, III-V Semiconductors
PUBLICATIONS	<p>Amratansh Gupta, Mohit D. Ganeriwala and Nihar R. Mohapatra, “An Unified Charge Centroid Model for Silicon and Low Effective Mass III-V Channel Double Gate MOS Transistor” presented at IEEE sponsored 32nd <i>International Conference on VLSI Design 2019</i> (VLSID), New Delhi, India (Nominated for Best Paper Award)</p> <p>Manish Kumar, Sanjeev Kumar, Amratansh Gupta and Arunangshu Ghosh, “Development of Electronic Interface for Sensing Applications with Voltammetric Electronic Tongue” presented at <i>IEEE Sensors 2018</i>, New Delhi, India (DOI:10.1109/ICSENS.2018.8589506)</p>
INTERNSHIP EXPERIENCE	<p>Investigation and Modelling of Charge Centroid in III-V Semiconductor based Double-Gate FETs IIT Gandhinagar, <i>Supervisor : Prof. Nihar R. Mohapatra</i> <i>Jan '18 - Apr '18</i></p> <ul style="list-style-type: none"> Investigated the application of the base centroid model of BSIM-CMG for modeling of charge centroid in III-V semiconductor based double-gate FETs Developed a unified charge centroid compact model for silicon and low effective mass III-V semiconductor based double-gate FETs <p>TCAD Simulations and Compact Modelling of Semiconductor Devices IIT Kanpur, <i>Supervisor : Prof. Yogesh Singh Chauhan</i> <i>May '17 - Jul '17</i></p> <ul style="list-style-type: none"> Worked on MOS transistor fabrication using SILVACO-TCAD environment Studied the effects of short channel effects and their modeling in BSIM3v3 Extracted BSIM3v3 parameters for the MOSFET TCAD-data using IC-CAP <p>Raspberry Pi based Automation of Diagnostic Device IIT Delhi, <i>Supervisor : Prof. Ravikrishnan Elangovan</i> <i>May '16 - Jul '16</i></p> <ul style="list-style-type: none"> Learned the Python based programming and Raspberry pi based automation techniques to automate a diagnostic device Automated the temperature controlling and sensing system, sample (fluid) flow system with precise flow rate, and stepper motor based movable platform of the diagnostic device

*(Evaluated on Absolute Grading Scale)

PROJECTS	Development of Low Current Measuring Device (ranging from 1nA to 100mA) Minor Project-II, <i>Supervisor : Prof. Arunangshu Ghosh</i> <i>Aug '17 - Nov '17</i> <ul style="list-style-type: none"> Developed a very precise current to voltage converter device for measuring currents ranging from nano-Ampere to milli-Ampere Voltage is fed to the input of a data acquisition system (NI-DAQ 6001) to obtain corresponding current values ranging from nano-Ampere to milli-Ampere
	Techniques to Design Radiation Tolerant SRAM Cell Reading Project, <i>Supervisor : Prof. Gaurav kaushal</i> <i>Feb '17 - Apr '17</i> <ul style="list-style-type: none"> Studied the literature based on Static Random Access Memory Cells (SRAM) and the effects arising due to Single Event Upset (SEU) Simulated the effects of radiation on data storing nodes against Single Event Upset (SEU) on SRAM cell using HSPICE(180nm, 65nm, 45nm)
	Implementation of Radiation Tolerant SRAM Cell Against Single Event Upset Minor Project-I, <i>Supervisor : Prof. Gaurav kaushal</i> <i>Feb '17 - Apr '17</i> <ul style="list-style-type: none"> Explored the various reported radiation tolerant SRAM cells and draw a performance comparison chart among various reported designs Proposed Single Event Upset(SEU) tolerant SRAM cell based on back to back connection of two inverters and an additional inverter feedback path Implemented the proposed design in HSPICE and improved the SEU tolerance of SRAM cell
	Sound Operated Lightening and Security Device Digital & Analog Electronics Lab Course - NIT Patna <i>Feb '16 - Apr '16</i> <ul style="list-style-type: none"> Designed a device capable of switching any other appliance ON or OFF with sound, equipped with facility to vary the sensitivity of detection of sound Device is based on the application of operational amplifier as comparator, J-K flip flops, bridge rectifiers and relays
AWARDS & ACHIEVEMENTS	Awarded the Merit based Scholarship for three consecutive years at NIT Patna Secured 3 rd Rank in Innovation category at Human Powered Vehicle Challenge 2016 Secured an All-India-Rank of 7329 in JEE Advanced 2014 amongst 121,000 candidates Secured 99.62 percentile in JEE Main 2014 amongst 1.4 million candidates Recognized as Regional Child Scientist at National Children Science Congress 2006
COMPUTER SKILLS	Programming: Python Python Packages: Matplotlib, Numpy, Scipy Software & Tools: Silvaco - TCAD, IC-CAP, MATLAB, HSPICE, Excel, LaTeX Automation Tools: Raspberry Pi, Arduino
POSITIONS OF RESPONSIBILITY	Served as Overall Coordinator (Highest Student Position) of Entrepreneurship Cell-NIT Patna Served as Joint Secretary of IEEE Student Chapter - NIT Patna Served as Member of Entrepreneurship Cell - NIT Patna
EXTRA INTERESTS	Hobbies: Microeconomics, EA-FIFA game, Quizzing