Project (1): “DSP48A1”
Team Name: Silicon Maestro
Team Member(solo): Amr Ayman Mohamed Abdo

1. RTL Code

registered.v | DSP48A1.v | DSP48A1_tb.v | run_dff.do | DSP.xdc

```
module DSP48A1 #(
    parameter A0REG = 0,
    parameter A1REG = 1,
    parameter B0REG = 0,
    parameter B1REG = 1,
    parameter CREG = 1,
    parameter DREG = 1,
    parameter MREG = 1,
    parameter PREG = 1,
    parameter CARRYINREG = 1,
    parameter CARRYOUTREG = 1,
    parameter OPMODEREG = 1,
    parameter CARRYINSEL = "OPMODE5",
    parameter B_INPUT = "DIRECT",
    parameter RSTTYPE = "SYNC"
    )(
    input [17:0] A, B, D,
    input [47:0] C,
    input [7:0] OPMODE,
    input [17:0] BCIN,
    input [47:0] PCIN,
    input CLK, CARRYIN,
    input RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP,
    input CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP,
    output [17:0] BCOUT,
    output [47:0] PCOUT, P,
    output [35:0] M,
    output CARRYOUT,
    output CARRYOUTF
    );

    wire [17:0] A0_reg, B0_reg, D_reg, A1_reg, B1_reg;
    wire [47:0] C_reg;
    wire [35:0] M_reg;
    wire [7:0] OPMODE_reg;
    wire [17:0] BINPUT;
    wire [35:0] M_mult;
    wire [17:0] B1_mux;
    wire [47:0] X, Z;
    wire [47:0] X_POST_Z;
    wire CIN, COUT, CARRYIN_mux;
    wire [47:0] M_to_mux;
    wire [17:0] Pre_AS;
    wire [47:0] DAB_concat;
    genvar i;

    assign BINPUT = (B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? BCIN : 0;
    assign CARRYIN_mux = (CARRYINSEL == "OPMODE5")? OPMODE_reg[5] : (CARRYINSEL == "CARRYIN")? CARRYIN : 0;
    assign Pre_AS = (OPMODE_reg[6])? D_reg - B0_reg : D_reg + B0_reg;
    assign B1_mux = (OPMODE_reg[4])? Pre_AS : B0_reg;
    assign M_mult = A1_reg * B1_reg;
    assign M_to_mux = {12'b0, M_reg};
    assign DAB_concat = {D[11:0], A1_reg, B1_reg};
    assign X = (OPMODE_reg[1:0] == 0)? 0 : (OPMODE_reg[1:0] == 1)? M_to_mux : (OPMODE_reg[1:0] == 2)? P : {D[11:0], A1_reg, B1_reg};
    assign Z = (OPMODE_reg[3:2] == 0)? 0 : (OPMODE_reg[3:2] == 1)? PCIN : (OPMODE_reg[3:2] == 2)? P : C_reg;
    assign {COUT, X_POST_Z} = (OPMODE_reg[7])? Z-(X+CIN) : Z+X+CIN;
    assign CARRYOUTF = CARRYOUT;
    assign BCOUT = B1_reg;
    assign PCOUT = P;

    generate
        for (i = 0; i < 36; i = i + 1)
        begin : buffer
            buf mbuf(M[i], M_reg[i]);
        end
    endgenerate
```

```
67
68      registered #(.REG(A0REG),
69                   .INWIDTH(18),
70                   .RSTTYPE(RSTTYPE)) A0_REG
71                   (.ce(CEA), .rst(RSTA), .clk(CLK), .in(A), .out(A0_reg));
72
73      registered #(.REG(B0REG),
74                   .INWIDTH(18),
75                   .RSTTYPE(RSTTYPE)) B0_REG
76                   (.ce(CEB), .rst(RSTB), .clk(CLK), .in(BINPUT), .out(B0_reg));
77
78      registered #(.REG(CREG),
79                   .INWIDTH(48),
80                   .RSTTYPE(RSTTYPE)) C_REG
81                   (.ce(CEC), .rst(RSTC), .clk(CLK), .in(C), .out(C_reg));
82
83      registered #(.REG(DREG),
84                   .INWIDTH(18),
85                   .RSTTYPE(RSTTYPE)) D_REG
86                   (.ce(CED), .rst(RSTD), .clk(CLK), .in(D), .out(D_reg));
87
88      registered #(.REG(MREG),
89                   .INWIDTH(36),
90                   .RSTTYPE(RSTTYPE)) M_REG
91                   (.ce(CEM), .rst(RSTM), .clk(CLK), .in(M_mult), .out(M_reg));
92
93      registered #(.REG(OPMODEREG),
94                   .INWIDTH(8),
95                   .RSTTYPE(RSTTYPE)) OPMODE_REG
96                   (.ce(CEOPMODE), .rst(RSTOPMODE), .clk(CLK), .in(OPMODE), .out(OPMODE_reg));
97
98      registered #(.REG(PREG),
99                   .INWIDTH(48),
100                  .RSTTYPE(RSTTYPE)) P_REG
101                  (.ce(CEP), .rst(RSTP), .clk(CLK), .in(X_POST_Z), .out(P));
102
103     registered #(.REG(A1REG),
104                  .INWIDTH(18),
105                  .RSTTYPE(RSTTYPE)) A1_REG
106                  (.ce(CEA), .rst(RSTA), .clk(CLK), .in(A0_reg), .out(A1_reg));
107
108     registered #(.REG(B1REG),
109                  .INWIDTH(18),
110                  .RSTTYPE(RSTTYPE)) B1_REG
111                  (.ce(CEB), .rst(RSTB), .clk(CLK), .in(B1_mux), .out(B1_reg));
112
113     registered #(.REG(CARRYINREG),
114                  .INWIDTH(1),
115                  .RSTTYPE(RSTTYPE)) CYI
116                  (.ce(CECARRYIN), .rst(RSTCARRYIN), .clk(CLK), .in(CARRYIN_mux), .out(CIN));
117
118     registered #(.REG(CARRYOUTREG),
119                  .INWIDTH(1),
120                  .RSTTYPE(RSTTYPE)) CYO
121                  (.ce(1), .rst(0), .clk(CLK), .in(COUT), .out(CARRYOUT));
122
123 endmodule
```

registered.v | DSP48A1.v | DSP48A1_tb.v | run_

```v
module registered #(
    parameter REG = 0,
    parameter INWIDTH = 18,
    parameter RSTTYPE = "SYNC"
    )(
    input ce, rst, clk,
    input [INWIDTH-1:0] in,
    output [INWIDTH-1:0] out
    );

    reg [INWIDTH-1:0] registered;

    assign out = (REG)? registered : in;

    generate
        if(RSTTYPE == "ASYNC") begin
            always @(posedge clk or posedge rst) begin
                if(rst)
                    registered <= 0;
                else if(ce)
                    registered <= in;
            end
        end

        else if(RSTTYPE == "SYNC") begin
            always @(posedge clk) begin
                if(ce) begin
                    if(rst)
                        registered <= 0;
                    else
                        registered <= in;
                end
            end
        end
    endgenerate

endmodule
```

2. Testbench code

registered.v | DSP48A1.v | DSP48A1_tb.v | run_dff.do | DSP.xdc

```
module DSP48A1_tb();
    reg [17:0] A, B, D;
    reg [47:0] C;
    reg [7:0] OPMODE;
    reg [17:0] BCIN;
    reg [47:0] PCIN;
    reg CLK, CARRYIN;
    reg RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP;
    reg CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP;
    wire [17:0] BCOUT;
    wire [47:0] PCOUT, P;
    wire [35:0] M;
    wire CARRYOUT;
    wire CARRYOUTF;

    //Inputs being operated on (forced inputs in the first clock cycle)
    reg [17:0] A_op, B_op, D_op, BCIN_op, BCOUT_op;
    reg [47:0] C_op, PCIN_op;
    reg [35:0] M_op;
    reg [7:0] OPMODE_op;
    reg CARRYIN_op;
    reg [47:0] DAB_concat_op;

    //Expected outputs
    reg [17:0] BCOUT_exp;
    reg [35:0] M_exp;
    reg [48:0] COUTandP_exp;
    reg [48:0] X_POST_Z;
    reg [47:0] P_exp;
    reg CARRYOUT_exp;

    //Instantiating the DUT module
    DSP48A1 DUT(A, B, D, C, OPMODE, BCIN, PCIN ,CLK, CARRYIN, RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE,
                RSTP, CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP, BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);

    //Implementing the clock
    initial begin
        CLK = 0;
        forever
            #10 CLK = ~CLK;
    end

    //Generating stimulus and comparing outputs and their corresponding expected outputs
    initial begin
        //Initializing the module by reseting everything
        {RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP} = 8'hFF;
        {CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP} = 0;
        repeat(2) @(negedge CLK);

        //Starting testing
        {RSTA, RSTB, RSTC, RSTCARRYIN, RSTD, RSTM, RSTOPMODE, RSTP} = 0;
        {CEA, CEB, CEC, CECARRYIN, CED, CEM, CEOPMODE, CEP} = 8'hFF;

        //Test case(1): the execution passes through 4 pipelines (4 clock cycles), where OPMODE[1:0] = 2'b01
        repeat(5000) begin
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = 8'b1111_1101;

```

```
            //operating inputs are the forced inputs in the first clock cycle to be operated on in the upcoming cycles
            A_op = A;
            B_op = B;
            C_op = C;
            D_op = D;
            PCIN_op = PCIN;
            BCIN_op = BCIN;
            CARRYIN_op = CARRYIN;
            OPMODE_op = OPMODE;

            @(posedge CLK);
            BCOUT_exp = D_op - B_op;
            repeat(2) @(negedge CLK);
            if(BCOUT != BCOUT_exp) begin
                $display("Error - Incorrect BCOUT, BCOUT_tb = %d, BCOUT_expected = %d", BCOUT, BCOUT_exp);
                $stop;
            end

            BCOUT_op = BCOUT;

            @(posedge CLK);
            M_exp = BCOUT_op * A_op;

            @(negedge CLK);
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = $random;

            if(M != M_exp) begin
                $display("Error - Incorrect M, M_tb = %d, M_expected = %d", M, M_exp);
                $stop;
            end

            M_op = M;

            @(posedge CLK);
            COUTandP_exp = C_op-(M_op+OPMODE_op[5]);
            P_exp = COUTandP_exp[47:0];
            CARRYOUT_exp = COUTandP_exp[48];

            @(negedge CLK);
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = $random;

            if(P != P_exp) begin
                $display("Error - Incorrect P, P_tb = %d, P_exp = %d", P, P_exp);
                $stop;
            end
            if(CARRYOUT != CARRYOUT_exp) begin
                $display("Error - Incorrect P, CARRYOUT_tb = %d, CARRYOUT_exp = %d", CARRYOUT, CARRYOUT_exp);
                $stop;
            end
        end
        $display("Test case (1) BCOUT after 2 clock cycles, M after 3 clock cycles, P after 4 clock cycles(X = M_reg)\n");
```

```
        //Test case(2): the execution passes through 3 pipelines (3 clock cycles), where OPMODE[1:0] = 2'b11
        repeat(5000) begin
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = 8'b1111_1111;

            //operating inputs are the forced inputs in the first clock cycle to be operated on in the upcoming cycles
            A_op = A;
            B_op = B;
            C_op = C;
            D_op = D;
            PCIN_op = PCIN;
            BCIN_op = BCIN;
            CARRYIN_op = CARRYIN;
            OPMODE_op = OPMODE;

            @(posedge CLK);
            BCOUT_exp = D_op - B_op;
            repeat(2) @(negedge CLK);
            if(BCOUT != BCOUT_exp) begin
                $display("Error - Incorrect BCOUT, BCOUT_tb = %d, BCOUT_expected = %d", BCOUT, BCOUT_exp);
                $stop;
            end

            BCOUT_op = BCOUT;
            DAB_concat_op = {D_op[11:0], A_op, BCOUT_op};

            @(posedge CLK);
            M_exp = BCOUT_op * A_op;
            COUTandP_exp = C_op-(DAB_concat_op+OPMODE_op[5]);
            P_exp = COUTandP_exp[47:0];
            CARRYOUT_exp = COUTandP_exp[48];

            @(negedge CLK);
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = $random;

            if(M != M_exp) begin
                $display("Error - Incorrect M, M_tb = %d, M_expected = %d", M, M_exp);
                $stop;
            end
            if(P != P_exp) begin
                $display("Error - Incorrect P, P_tb = %d, P_exp = %d", P, P_exp);
                $stop;
            end
            if(CARRYOUT != CARRYOUT_exp) begin
                $display("Error - Incorrect P, CARRYOUT_tb = %d, CARRYOUT_exp = %d", CARRYOUT, CARRYOUT_exp);
                $stop;
            end
        end
        $display("Test case (2) BCOUT after 2 clock cycles, M after 3 clock cycles, P after 3 clock cycles(X = D:A:B)\n");

```

```
        //Test case(3): P gets an initial value after the first 3 cycles and then gets updated every clock cycle(X = P)
        repeat(5000) begin
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = 8'b1111_1110;

            //operating inputs are the forced inputs in the first clock cycle to be operated on in the upcoming cycles
            A_op = A;
            B_op = B;
            C_op = C;
            D_op = D;
            PCIN_op = PCIN;
            BCIN_op = BCIN;
            CARRYIN_op = CARRYIN;
            OPMODE_op = OPMODE;

            @(posedge CLK);
            BCOUT_exp = D_op - B_op;
            repeat(2) @(negedge CLK);
            if(BCOUT != BCOUT_exp) begin
                $display("Error - Incorrect BCOUT, BCOUT_tb = %d, BCOUT_expected = %d", BCOUT, BCOUT_exp);
                $stop;
            end

            BCOUT_op = BCOUT;
            DAB_concat_op = {D_op[11:0], A_op, BCOUT_op};
            X_POST_Z = C_op-(P+OPMODE_op[5]);

            @(posedge CLK);
            M_exp = BCOUT_op * A_op;
            COUTandP_exp = X_POST_Z;
            P_exp = COUTandP_exp[47:0];
            CARRYOUT_exp = COUTandP_exp[48];


            @(negedge CLK);
            A = $random;
            B = $random;
            C = $random;
            D = $random;
            PCIN = $random;
            BCIN = $random;
            CARRYIN = $random;
            OPMODE = $random;

            if(M != M_exp) begin
                $display("Error - Incorrect M, M_tb = %d, M_expected = %d", M, M_exp);
                $stop;
            end
            if(P != P_exp) begin
                $display("Error - Incorrect P, P_tb = %d, P_exp = %d", P, P_exp);
                $stop;
            end
            if(CARRYOUT != CARRYOUT_exp) begin
                $display("Error - Incorrect P, CARRYOUT_tb = %d, CARRYOUT_exp = %d", CARRYOUT, CARRYOUT_exp);
                $stop;
            end
        end
        $display("Test case (3) P gets an initial value after the first 3 cycles and then gets updated every clock cycle(X = P)\n");

        $display("DSP48A1 is successfully verified");
        $stop;
    end
endmodule
```

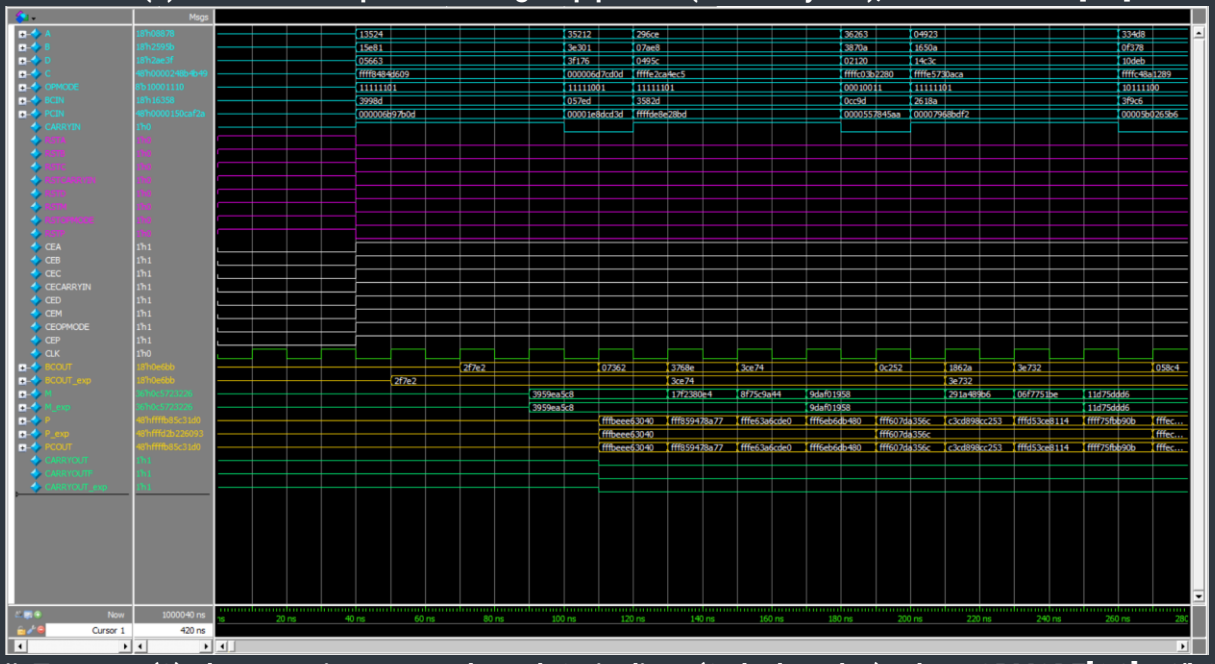
3. Do file

registered.v | DSP48A1.v | DSP48A1_tb.v | run_DSP48A1.do

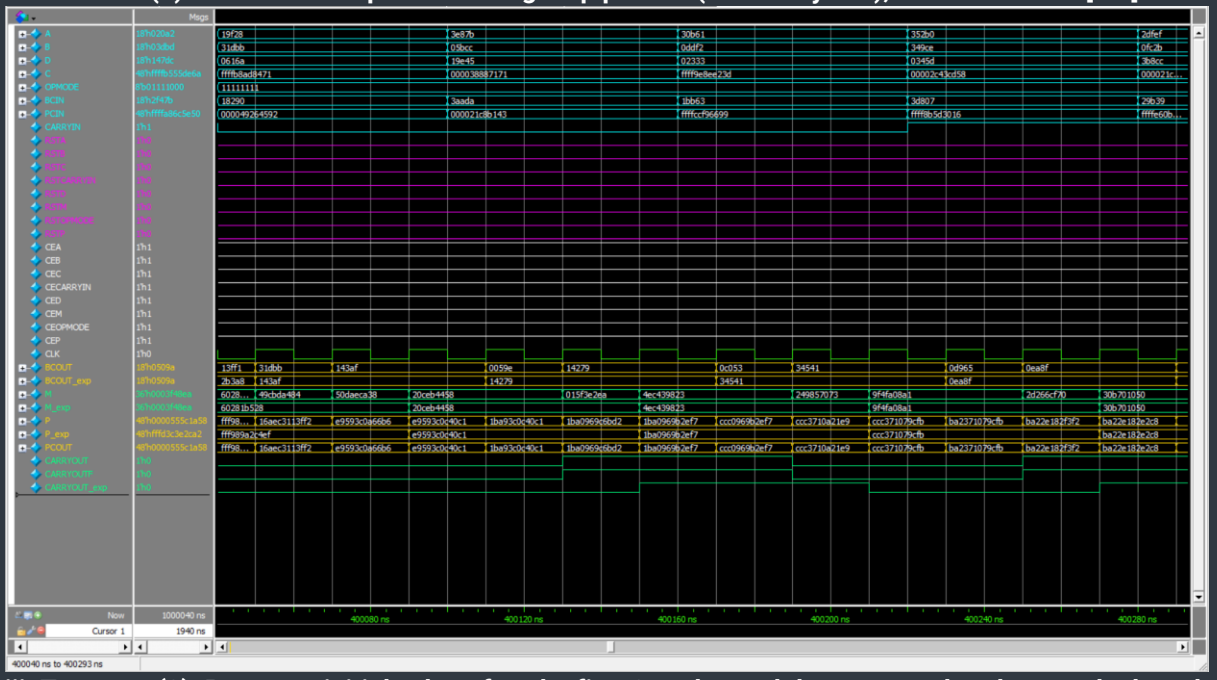
```
vlib work
vlog registered.v DSP48A1.v DSP48A1_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -sim
```

4. QuestaSim Snippets

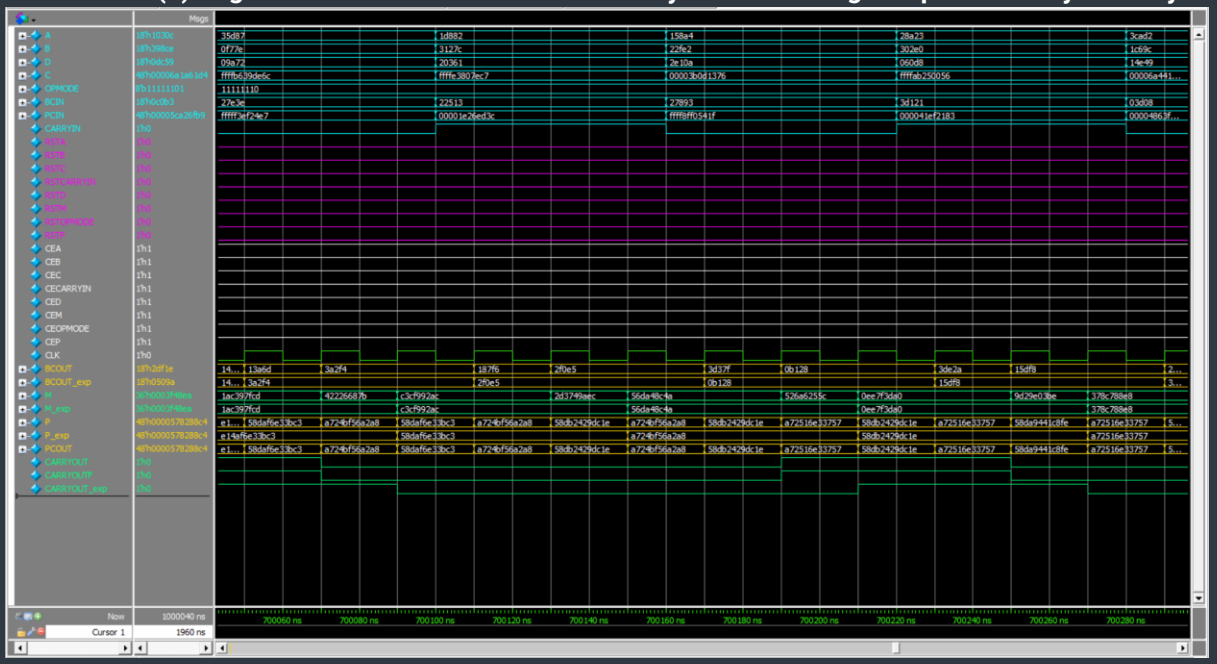
i. Test case(1): the execution passes through 4 pipelines (4 clock cycles), where OPMODE[1:0] = 2'b01



ii. Test case(2): the execution passes through 3 pipelines (3 clock cycles), where OPMODE[1:0] = 2'b11



iii. Test case(3): P gets an initial value after the first 3 cycles and then gets updated every clock cycle(X = P)



5. Constraint File

registered.v | DSP48A1.v | DSP48A1_tb.v | run_DSP48A1.do | DSP.xdc

```
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]

## Clock signal
set_property -dict {PACKAGE_PIN AL30 IOSTANDARD LVCMOS33} [get_ports CLK]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports CLK]

##I/O Ports
set_property IOSTANDARD LVCMOS33 [get_ports *]
set_property PACKAGE_PIN AG7 [get_ports {D[6]}]
set_property PACKAGE_PIN AB4 [get_ports {B[3]}]
set_property PACKAGE_PIN V4 [get_ports {B[10]}]
set_property PACKAGE_PIN W28 [get_ports {M[28]}]
set_property PACKAGE_PIN N2 [get_ports {C[29]}]
set_property PACKAGE_PIN U7 [get_ports {C[6]}]
set_property PACKAGE_PIN Y25 [get_ports {M[25]}]
set_property PACKAGE_PIN AG5 [get_ports {D[12]}]
set_property PACKAGE_PIN V26 [get_ports {M[32]}]
set_property PACKAGE_PIN AH28 [get_ports {P[25]}]
set_property PACKAGE_PIN AG34 [get_ports {P[47]}]
set_property PACKAGE_PIN AE32 [get_ports {P[38]}]
set_property PACKAGE_PIN V34 [get_ports {M[17]}]
set_property PACKAGE_PIN AF33 [get_ports {P[41]}]
set_property PACKAGE_PIN L25 [get_ports {PCIN[41]}]
set_property PACKAGE_PIN AB32 [get_ports {M[7]}]
set_property PACKAGE_PIN AD29 [get_ports {P[31]}]
set_property PACKAGE_PIN AB31 [get_ports {M[8]}]
set_property PACKAGE_PIN V24 [get_ports {M[35]}]
set_property PACKAGE_PIN W10 [get_ports {BCOUT[16]}]
set_property PACKAGE_PIN W8 [get_ports {BCOUT[11]}]
set_property PACKAGE_PIN M6 [get_ports {BCOUT[4]}]
set_property PACKAGE_PIN AD25 [get_ports {C[45]}]
set_property PACKAGE_PIN M5 [get_ports {C[34]}]
set_property PACKAGE_PIN K28 [get_ports {PCIN[27]}]
set_property PACKAGE_PIN H24 [get_ports {PCIN[37]}]
set_property PACKAGE_PIN H27 [get_ports {PCIN[36]}]
set_property PACKAGE_PIN J29 [get_ports {PCIN[24]}]
set_property PACKAGE_PIN G29 [get_ports {PCIN[20]}]
set_property PACKAGE_PIN H32 [get_ports {PCIN[12]}]
set_property PACKAGE_PIN G34 [get_ports {PCIN[7]}]
set_property PACKAGE_PIN M34 [get_ports {PCOUT[3]}]
set_property PACKAGE_PIN M26 [get_ports {PCIN[0]}]
set_property PACKAGE_PIN T24 [get_ports {PCOUT[47]}]
set_property PACKAGE_PIN N28 [get_ports {PCOUT[31]}]
set_property PACKAGE_PIN N34 [get_ports {PCOUT[4]}]
set_property PACKAGE_PIN R28 [get_ports {PCOUT[29]}]
set_property PACKAGE_PIN P30 [get_ports {PCOUT[21]}]
set_property PACKAGE_PIN AD23 [get_ports CARRYOUTF]
set_property PACKAGE_PIN AD1 [get_ports RSTD]
set_property PACKAGE_PIN AJ3 [get_ports CECARRYIN]
set_property PACKAGE_PIN AF4 [get_ports CEC]
set_property PACKAGE_PIN AH1 [get_ports RSTM]
set_property PACKAGE_PIN AC11 [get_ports RSTP]
set_property PACKAGE_PIN AF2 [get_ports CEP]
set_property PACKAGE_PIN R5 [get_ports {C[23]}]
set_property PACKAGE_PIN R11 [get_ports {BCOUT[6]}]
set_property PACKAGE_PIN AB2 [get_ports {B[2]}]
set_property PACKAGE_PIN AC2 [get_ports {A[16]}]
set_property PACKAGE_PIN W26 [get_ports {M[30]}]
set_property PACKAGE_PIN T3 [get_ports {C[16]}]
set_property PACKAGE_PIN Y27 [get_ports {M[24]}]
set_property PACKAGE_PIN P1 [get_ports {C[31]}]
```

```
set_property PACKAGE_PIN AJ4 [get_ports {D[16]}]
set_property PACKAGE_PIN AF5 [get_ports {D[10]}]
set_property PACKAGE_PIN AC27 [get_ports {P[18]}]
set_property PACKAGE_PIN V27 [get_ports {M[31]}]
set_property PACKAGE_PIN W34 [get_ports {M[19]}]
set_property PACKAGE_PIN AD31 [get_ports {P[36]}]
set_property PACKAGE_PIN AE33 [get_ports {P[42]}]
set_property PACKAGE_PIN AE30 [get_ports {P[33]}]
set_property PACKAGE_PIN V33 [get_ports {M[18]}]
set_property PACKAGE_PIN AD28 [get_ports {P[32]}]
set_property PACKAGE_PIN H34 [get_ports {PCIN[3]}]
set_property PACKAGE_PIN AB25 [get_ports {OPMODE[1]}]
set_property PACKAGE_PIN V8 [get_ports {BCOUT[13]}]
set_property PACKAGE_PIN AF25 [get_ports {C[47]}]
set_property PACKAGE_PIN AE25 [get_ports {C[44]}]
set_property PACKAGE_PIN M4 [get_ports {C[33]}]
set_property PACKAGE_PIN AG27 [get_ports {P[17]}]
set_property PACKAGE_PIN AC28 [get_ports {P[4]}]
set_property PACKAGE_PIN AB26 [get_ports {P[0]}]
set_property PACKAGE_PIN P34 [get_ports {PCIN[40]}]
set_property PACKAGE_PIN G30 [get_ports {PCIN[19]}]
set_property PACKAGE_PIN K31 [get_ports {PCIN[18]}]
set_property PACKAGE_PIN L32 [get_ports {PCIN[6]}]
set_property PACKAGE_PIN T27 [get_ports {PCOUT[34]}]
set_property PACKAGE_PIN T34 [get_ports {PCOUT[1]}]
set_property PACKAGE_PIN T30 [get_ports {PCOUT[19]}]
set_property PACKAGE_PIN P28 [get_ports {PCOUT[24]}]
set_property PACKAGE_PIN P29 [get_ports {PCOUT[23]}]
set_property PACKAGE_PIN W5 [get_ports {B[8]}]
set_property PACKAGE_PIN Y2 [get_ports {B[13]}]
set_property PACKAGE_PIN AC1 [get_ports {A[15]}]
set_property PACKAGE_PIN AC4 [get_ports {A[14]}]
set_property PACKAGE_PIN Y3 [get_ports {B[14]}]
set_property PACKAGE_PIN V3 [get_ports {B[12]}]
set_property PACKAGE_PIN AA4 [get_ports {B[5]}]
set_property PACKAGE_PIN R3 [get_ports {C[20]}]
set_property PACKAGE_PIN N3 [get_ports {C[30]}]
set_property PACKAGE_PIN R6 [get_ports {C[24]}]
set_property PACKAGE_PIN T7 [get_ports {C[3]}]
set_property PACKAGE_PIN R8 [get_ports {C[12]}]
set_property PACKAGE_PIN U6 [get_ports {C[5]}]
set_property PACKAGE_PIN AD6 [get_ports {D[9]}]
set_property PACKAGE_PIN V32 [get_ports {M[21]}]
set_property PACKAGE_PIN AD26 [get_ports {P[21]}]
set_property PACKAGE_PIN AA34 [get_ports {M[0]}]
set_property PACKAGE_PIN L29 [get_ports {PCIN[14]}]
set_property PACKAGE_PIN AH29 [get_ports {P[24]}]
set_property PACKAGE_PIN AH32 [get_ports {P[39]}]
set_property PACKAGE_PIN AH31 [get_ports {P[29]}]
set_property PACKAGE_PIN AA29 [get_ports {OPMODE[6]}]
set_property PACKAGE_PIN Y32 [get_ports {M[16]}]
set_property PACKAGE_PIN AE6 [get_ports {D[8]}]
set_property PACKAGE_PIN AB1 [get_ports {B[1]}]
set_property PACKAGE_PIN N8 [get_ports {BCOUT[1]}]
set_property PACKAGE_PIN N7 [get_ports {BCOUT[0]}]
set_property PACKAGE_PIN V7 [get_ports {BCOUT[10]}]
set_property PACKAGE_PIN H28 [get_ports {PCIN[25]}]
set_property PACKAGE_PIN AG26 [get_ports {P[13]}]
set_property PACKAGE_PIN AH24 [get_ports {P[8]}]
set_property PACKAGE_PIN AA27 [get_ports {P[2]}]
set_property PACKAGE_PIN H26 [get_ports {PCIN[34]}]
set_property PACKAGE_PIN J31 [get_ports {PCIN[17]}]
set_property PACKAGE_PIN R27 [get_ports {PCOUT[33]}]
set_property PACKAGE_PIN M29 [get_ports {PCOUT[27]}]
set_property PACKAGE_PIN M30 [get_ports {PCOUT[18]}]
set_property PACKAGE_PIN R32 [get_ports {PCOUT[9]}]
set_property PACKAGE_PIN T33 [get_ports {PCOUT[6]}]
```

```
set_property PACKAGE_PIN U32 [get_ports {PCOUT[11]}]
set_property PACKAGE_PIN AF3 [get_ports CEOPMODE]
set_property PACKAGE_PIN Y5 [get_ports {B[7]}]
set_property PACKAGE_PIN AC3 [get_ports {A[13]}]
set_property PACKAGE_PIN AA7 [get_ports {A[11]}]
set_property PACKAGE_PIN AC7 [get_ports {A[10]}]
set_property PACKAGE_PIN AD10 [get_ports {B[17]}]
set_property PACKAGE_PIN AE10 [get_ports {B[16]}]
set_property PACKAGE_PIN AA5 [get_ports {B[6]}]
set_property PACKAGE_PIN W9 [get_ports {BCOUT[12]}]
set_property PACKAGE_PIN P6 [get_ports {C[38]}]
set_property PACKAGE_PIN R2 [get_ports {C[19]}]
set_property PACKAGE_PIN Y6 [get_ports {D[4]}]
set_property PACKAGE_PIN W31 [get_ports {M[13]}]
set_property PACKAGE_PIN AA25 [get_ports {OPMODE[3]}]
set_property PACKAGE_PIN AB24 [get_ports {OPMODE[2]}]
set_property PACKAGE_PIN W33 [get_ports {M[20]}]
set_property PACKAGE_PIN Y33 [get_ports {M[15]}]
set_property PACKAGE_PIN AF30 [get_ports {P[28]}]
set_property PACKAGE_PIN G25 [get_ports {PCIN[45]}]
set_property PACKAGE_PIN J28 [get_ports {PCIN[26]}]
set_property PACKAGE_PIN AC34 [get_ports {M[5]}]
set_property PACKAGE_PIN AA24 [get_ports {OPMODE[4]}]
set_property PACKAGE_PIN W1 [get_ports {D[3]}]
set_property PACKAGE_PIN U4 [get_ports {C[13]}]
set_property PACKAGE_PIN T9 [get_ports {C[1]}]
set_property PACKAGE_PIN V28 [get_ports {M[34]}]
set_property PACKAGE_PIN T8 [get_ports {C[4]}]
set_property PACKAGE_PIN M11 [get_ports {C[42]}]
set_property PACKAGE_PIN AF27 [get_ports {P[14]}]
set_property PACKAGE_PIN J23 [get_ports {PCIN[47]}]
set_property PACKAGE_PIN AA28 [get_ports {P[1]}]
set_property PACKAGE_PIN K25 [get_ports {PCIN[44]}]
set_property PACKAGE_PIN G27 [get_ports {PCIN[35]}]
set_property PACKAGE_PIN H29 [get_ports {PCIN[23]}]
set_property PACKAGE_PIN L33 [get_ports {PCIN[2]}]
set_property PACKAGE_PIN N33 [get_ports {PCOUT[7]}]
set_property PACKAGE_PIN R33 [get_ports {PCOUT[5]}]
set_property PACKAGE_PIN R26 [get_ports {PCOUT[46]}]
set_property PACKAGE_PIN U25 [get_ports {PCOUT[42]}]
set_property PACKAGE_PIN AG2 [get_ports CEM]
set_property PACKAGE_PIN AH2 [get_ports RSTC]
set_property PACKAGE_PIN P9 [get_ports {C[40]}]
set_property PACKAGE_PIN AA2 [get_ports {A[17]}]
set_property PACKAGE_PIN AB6 [get_ports {A[7]}]
set_property PACKAGE_PIN AB10 [get_ports {A[2]}]
set_property PACKAGE_PIN AF10 [get_ports {B[15]}]
set_property PACKAGE_PIN W3 [get_ports {B[11]}]
set_property PACKAGE_PIN AB5 [get_ports {B[4]}]
set_property PACKAGE_PIN AA3 [get_ports {B[0]}]
set_property PACKAGE_PIN N9 [get_ports {BCOUT[3]}]
set_property PACKAGE_PIN N6 [get_ports {C[37]}]
set_property PACKAGE_PIN U2 [get_ports {C[18]}]
set_property PACKAGE_PIN U5 [get_ports {C[14]}]
set_property PACKAGE_PIN T2 [get_ports {C[15]}]
set_property PACKAGE_PIN U11 [get_ports {C[0]}]
set_property PACKAGE_PIN V29 [get_ports {M[33]}]
set_property PACKAGE_PIN R7 [get_ports {C[11]}]
set_property PACKAGE_PIN R10 [get_ports {C[10]}]
set_property PACKAGE_PIN Y28 [get_ports {M[23]}]
set_property PACKAGE_PIN AD33 [get_ports {P[46]}]
set_property PACKAGE_PIN AE26 [get_ports {P[20]}]
set_property PACKAGE_PIN V31 [get_ports {M[22]}]
set_property PACKAGE_PIN AC32 [get_ports {M[1]}]
set_property PACKAGE_PIN AG31 [get_ports {P[30]}]
set_property PACKAGE_PIN AG29 [get_ports {P[27]}]
set_property PACKAGE_PIN AC29 [get_ports {P[3]}]
```

```
set_property PACKAGE_PIN M25 [get_ports {PCIN[42]}]
set_property PACKAGE_PIN AG30 [get_ports {P[26]}]
set_property PACKAGE_PIN U10 [get_ports {C[8]}]
set_property PACKAGE_PIN Y11 [get_ports {BCOUT[17]}]
set_property PACKAGE_PIN G31 [get_ports {PCIN[15]}]
set_property PACKAGE_PIN AH27 [get_ports {P[16]}]
set_property PACKAGE_PIN G26 [get_ports {PCIN[33]}]
set_property PACKAGE_PIN L27 [get_ports {PCIN[32]}]
set_property PACKAGE_PIN K33 [get_ports {PCIN[10]}]
set_property PACKAGE_PIN K32 [get_ports {PCIN[5]}]
set_property PACKAGE_PIN P26 [get_ports {PCOUT[45]}]
set_property PACKAGE_PIN R31 [get_ports {PCOUT[16]}]
set_property PACKAGE_PIN M31 [get_ports {PCOUT[17]}]
set_property PACKAGE_PIN U34 [get_ports {PCOUT[2]}]
set_property PACKAGE_PIN M27 [get_ports {PCOUT[43]}]
set_property PACKAGE_PIN P24 [get_ports {PCOUT[40]}]
set_property PACKAGE_PIN N24 [get_ports {PCOUT[39]}]
set_property PACKAGE_PIN N27 [get_ports {PCOUT[32]}]
set_property PACKAGE_PIN AE1 [get_ports RSTCARRYIN]
set_property PACKAGE_PIN T4 [get_ports {C[21]}]
set_property PACKAGE_PIN AC6 [get_ports {A[9]}]
set_property PACKAGE_PIN AC8 [get_ports {A[5]}]
set_property PACKAGE_PIN AE5 [get_ports {D[11]}]
set_property PACKAGE_PIN Y1 [get_ports {D[2]}]
set_property PACKAGE_PIN P4 [get_ports {C[28]}]
set_property PACKAGE_PIN W30 [get_ports {M[14]}]
set_property PACKAGE_PIN W24 [get_ports {OPMODE[0]}]
set_property PACKAGE_PIN AC26 [get_ports {P[19]}]
set_property PACKAGE_PIN Y30 [get_ports {M[12]}]
set_property PACKAGE_PIN AC33 [get_ports {M[6]}]
set_property PACKAGE_PIN AA30 [get_ports {M[10]}]
set_property PACKAGE_PIN AF23 [get_ports {P[10]}]
set_property PACKAGE_PIN L28 [get_ports {PCIN[28]}]
set_property PACKAGE_PIN AE28 [get_ports {P[23]}]
set_property PACKAGE_PIN Y31 [get_ports {M[11]}]
set_property PACKAGE_PIN V2 [get_ports {D[1]}]
set_property PACKAGE_PIN T10 [get_ports {C[7]}]
set_property PACKAGE_PIN U9 [get_ports {C[2]}]
set_property PACKAGE_PIN AH4 [get_ports {D[17]}]
set_property PACKAGE_PIN V6 [get_ports {BCOUT[9]}]
set_property PACKAGE_PIN Y8 [get_ports {BCOUT[8]}]
set_property PACKAGE_PIN M9 [get_ports {BCOUT[2]}]
set_property PACKAGE_PIN H33 [get_ports {PCIN[8]}]
set_property PACKAGE_PIN AG24 [get_ports {P[9]}]
set_property PACKAGE_PIN J25 [get_ports {PCIN[43]}]
set_property PACKAGE_PIN N29 [get_ports {PCOUT[28]}]
set_property PACKAGE_PIN N32 [get_ports {PCOUT[8]}]
set_property PACKAGE_PIN M32 [get_ports {PCOUT[13]}]
set_property PACKAGE_PIN J24 [get_ports {PCIN[38]}]
set_property PACKAGE_PIN K27 [get_ports {PCIN[31]}]
set_property PACKAGE_PIN J30 [get_ports {PCIN[21]}]
set_property PACKAGE_PIN N26 [get_ports {PCOUT[44]}]
set_property PACKAGE_PIN T25 [get_ports {PCOUT[41]}]
set_property PACKAGE_PIN U27 [get_ports {PCOUT[37]}]
set_property PACKAGE_PIN T29 [get_ports {PCOUT[25]}]
set_property PACKAGE_PIN AF24 [get_ports {C[43]}]
set_property PACKAGE_PIN Y10 [get_ports {BCOUT[15]}]
set_property PACKAGE_PIN AA10 [get_ports {A[4]}]
set_property PACKAGE_PIN AA8 [get_ports {A[12]}]
set_property PACKAGE_PIN AC9 [get_ports {A[6]}]
set_property PACKAGE_PIN N1 [get_ports {C[36]}]
set_property PACKAGE_PIN R1 [get_ports {C[32]}]
set_property PACKAGE_PIN T5 [get_ports {C[22]}]
set_property PACKAGE_PIN W29 [get_ports {M[27]}]
set_property PACKAGE_PIN Y26 [get_ports {M[29]}]
set_property PACKAGE_PIN P10 [get_ports {C[9]}]
set_property PACKAGE_PIN AE3 [get_ports {D[14]}]
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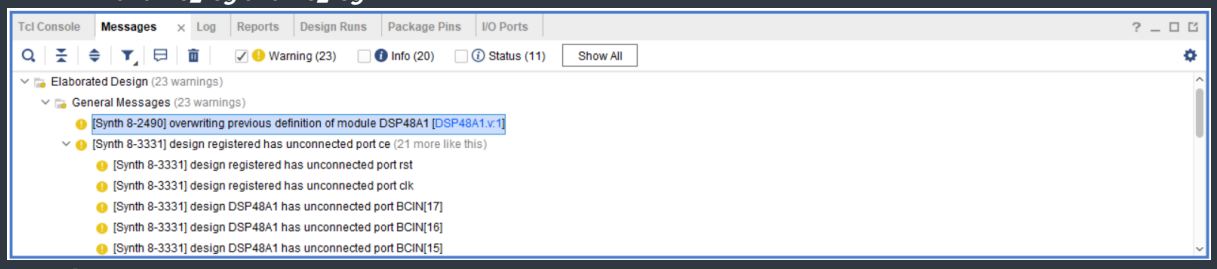
```
set_property PACKAGE_PIN AE3 [get_ports {D[14]}]
set_property PACKAGE_PIN P3 [get_ports {C[27]}]
set_property PACKAGE_PIN AB30 [get_ports {M[9]}]
set_property PACKAGE_PIN AC31 [get_ports {M[2]}]
set_property PACKAGE_PIN AB27 [get_ports {OPMODE[7]}]
set_property PACKAGE_PIN AB29 [get_ports {OPMODE[5]}]
set_property PACKAGE_PIN K30 [get_ports {PCIN[22]}]
set_property PACKAGE_PIN J34 [get_ports {PCIN[9]}]
set_property PACKAGE_PIN AH33 [get_ports {P[44]}]
set_property PACKAGE_PIN AA32 [get_ports {M[4]}]
set_property PACKAGE_PIN AG6 [get_ports {D[13]}]
set_property PACKAGE_PIN V9 [get_ports {BCOUT[14]}]
set_property PACKAGE_PIN P8 [get_ports {C[39]}]
set_property PACKAGE_PIN Y7 [get_ports {BCOUT[7]}]
set_property PACKAGE_PIN AE27 [get_ports {P[15]}]
set_property PACKAGE_PIN AH26 [get_ports {P[12]}]
set_property PACKAGE_PIN R30 [get_ports {PCOUT[22]}]
set_property PACKAGE_PIN AE23 [get_ports {P[11]}]
set_property PACKAGE_PIN U24 [get_ports {PCIN[39]}]
set_property PACKAGE_PIN K26 [get_ports {PCIN[30]}]
set_property PACKAGE_PIN H31 [get_ports {PCIN[16]}]
set_property PACKAGE_PIN U26 [get_ports {PCOUT[38]}]
set_property PACKAGE_PIN R25 [get_ports {PCOUT[36]}]
set_property PACKAGE_PIN P25 [get_ports {PCOUT[35]}]
set_property PACKAGE_PIN U29 [get_ports {PCOUT[26]}]
set_property PACKAGE_PIN U30 [get_ports {PCOUT[20]}]
set_property PACKAGE_PIN AG1 [get_ports RSTOPMODE]
set_property PACKAGE_PIN AE2 [get_ports RSTA]
set_property PACKAGE_PIN AH3 [get_ports CED]
set_property PACKAGE_PIN AD5 [get_ports CEA]
set_property PACKAGE_PIN AB9 [get_ports {A[1]}]
set_property PACKAGE_PIN AB7 [get_ports {A[8]}]
set_property PACKAGE_PIN AA9 [get_ports {A[3]}]
set_property PACKAGE_PIN AB11 [get_ports {A[0]}]
set_property PACKAGE_PIN W4 [get_ports {B[9]}]
set_property PACKAGE_PIN M1 [get_ports {C[35]}]
set_property PACKAGE_PIN W25 [get_ports {M[26]}]
set_property PACKAGE_PIN P5 [get_ports {C[26]}]
set_property PACKAGE_PIN AA33 [get_ports {M[3]}]
set_property PACKAGE_PIN AG32 [get_ports {P[40]}]
set_property PACKAGE_PIN AD30 [get_ports {P[34]}]
set_property PACKAGE_PIN AD34 [get_ports {P[45]}]
set_property PACKAGE_PIN AE31 [get_ports {P[35]}]
set_property PACKAGE_PIN AF32 [get_ports {P[37]}]
set_property PACKAGE_PIN AC24 [get_ports {P[7]}]
set_property PACKAGE_PIN J33 [get_ports {PCIN[4]}]
set_property PACKAGE_PIN AF28 [get_ports {P[22]}]
set_property PACKAGE_PIN AH34 [get_ports {P[43]}]
set_property PACKAGE_PIN V1 [get_ports {D[0]}]
set_property PACKAGE_PIN U1 [get_ports {C[17]}]
set_property PACKAGE_PIN AF7 [get_ports {D[7]}]
set_property PACKAGE_PIN W6 [get_ports {D[5]}]
set_property PACKAGE_PIN AD3 [get_ports {D[15]}]
set_property PACKAGE_PIN N4 [get_ports {C[25]}]
set_property PACKAGE_PIN AG25 [get_ports {C[46]}]
set_property PACKAGE_PIN M7 [get_ports {BCOUT[5]}]
set_property PACKAGE_PIN M10 [get_ports {C[41]}]
set_property PACKAGE_PIN AB34 [get_ports {P[5]}]
set_property PACKAGE_PIN AD24 [get_ports {P[6]}]
set_property PACKAGE_PIN G24 [get_ports {PCIN[46]}]
set_property PACKAGE_PIN N31 [get_ports {PCOUT[14]}]
set_property PACKAGE_PIN U31 [get_ports {PCOUT[12]}]
set_property PACKAGE_PIN T32 [get_ports {PCOUT[10]}]
set_property PACKAGE_PIN P33 [get_ports {PCOUT[0]}]
set_property PACKAGE_PIN J26 [get_ports {PCIN[29]}]
set_property PACKAGE_PIN L30 [get_ports {PCIN[13]}]
set_property PACKAGE_PIN G32 [get_ports {PCIN[11]}]
set_property PACKAGE_PIN L34 [get_ports {PCIN[1]}]
set_property PACKAGE_PIN T28 [get_ports {PCOUT[30]}]
set_property PACKAGE_PIN P31 [get_ports {PCOUT[15]}]
set_property PACKAGE_PIN AF34 [get_ports CARRYOUT]
set_property PACKAGE_PIN AG4 [get_ports CEB]
set_property PACKAGE_PIN AJ1 [get_ports RSTB]
set_property PACKAGE_PIN AG9 [get_ports {BCIN[4]}]
set_property PACKAGE_PIN AH7 [get_ports {BCIN[13]}]
set_property PACKAGE_PIN AF8 [get_ports {BCIN[10]}]
set_property PACKAGE_PIN AG10 [get_ports {BCIN[5]}]
set_property PACKAGE_PIN AF12 [get_ports {BCIN[7]}]
set_property PACKAGE_PIN AH11 [get_ports {BCIN[0]}]
set_property PACKAGE_PIN AD9 [get_ports {BCIN[17]}]
set_property PACKAGE_PIN AD8 [get_ports {BCIN[16]}]
set_property PACKAGE_PIN AE7 [get_ports {BCIN[14]}]
set_property PACKAGE_PIN AH6 [get_ports {BCIN[12]}]
set_property PACKAGE_PIN AE8 [get_ports {BCIN[15]}]
set_property PACKAGE_PIN AG12 [get_ports {BCIN[6]}]
set_property PACKAGE_PIN AD11 [get_ports {BCIN[3]}]
set_property PACKAGE_PIN AD4 [get_ports CARRYIN]
set_property PACKAGE_PIN AF9 [get_ports {BCIN[11]}]
set_property PACKAGE_PIN AE11 [get_ports {BCIN[2]}]
set_property PACKAGE_PIN AH8 [get_ports {BCIN[8]}]
set_property PACKAGE_PIN AH9 [get_ports {BCIN[9]}]
set_property PACKAGE_PIN AG11 [get_ports {BCIN[1]}]
```

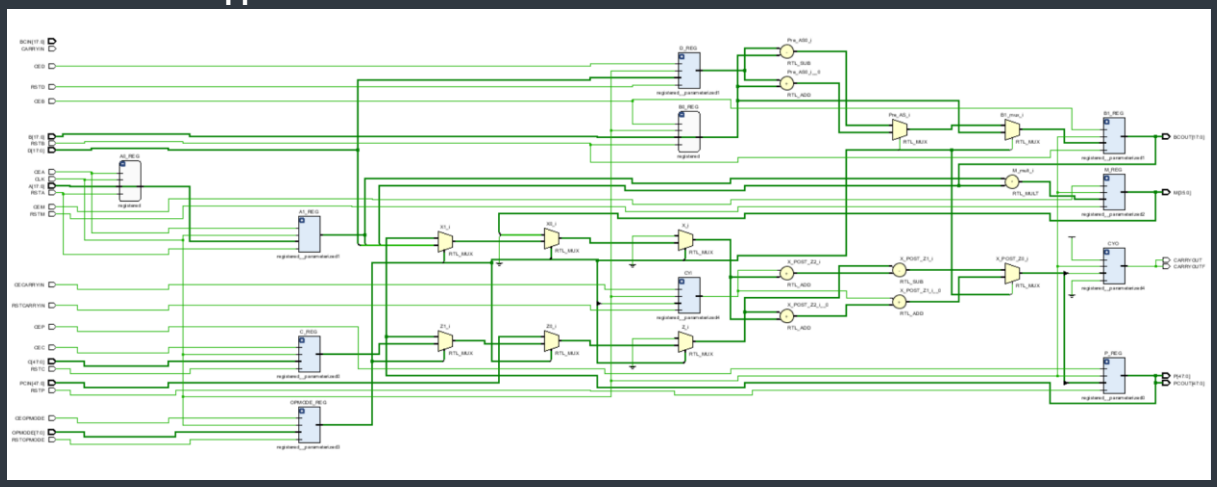
6. Elaboration

i. “Messages” tab

a. [Synth 8-2490] is because I have chosen the module name similar to another module in the FPGA (DSP48A1)
b. [Synth 8-3331] the unconnected ports are because based on the parameter B_INPUT B is passed into the module while BCIN is held unconnected. Subsequently BCIN [17:0] is held unconnected. Same for CARRYIN and A0_reg and B0_reg.



ii. Schematic snippets

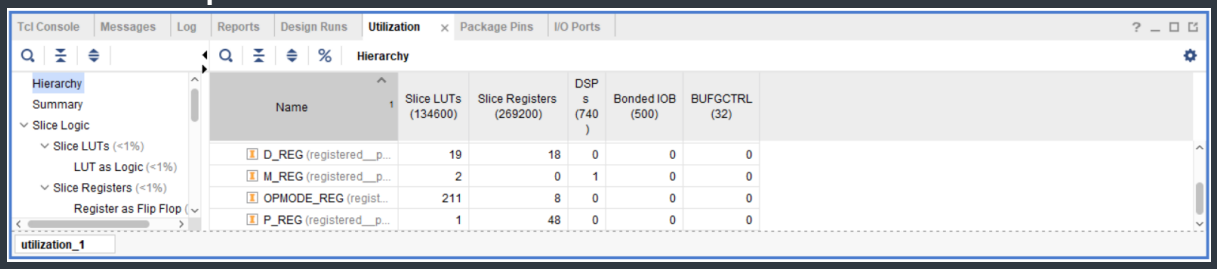


7. Synthesis

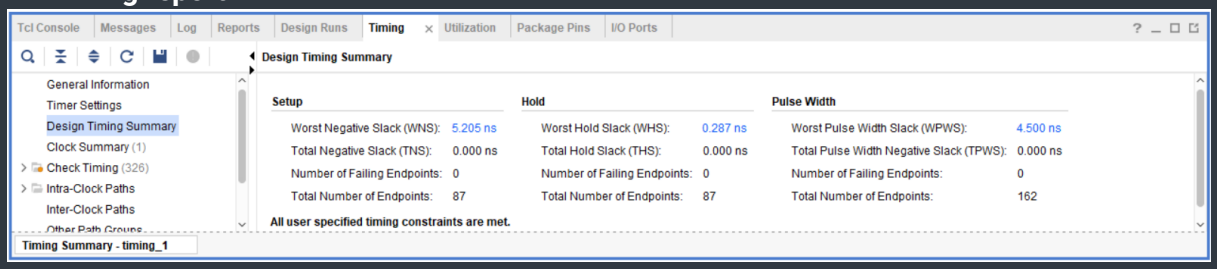
i. “Messages” tab

[Constraints 18-5210] This message is found in Vivado versions 2018.2 through 2019.2.
This message has been removed from the 2020.1 version of Vivado as it was found to be contusing.

ii. Utilization report

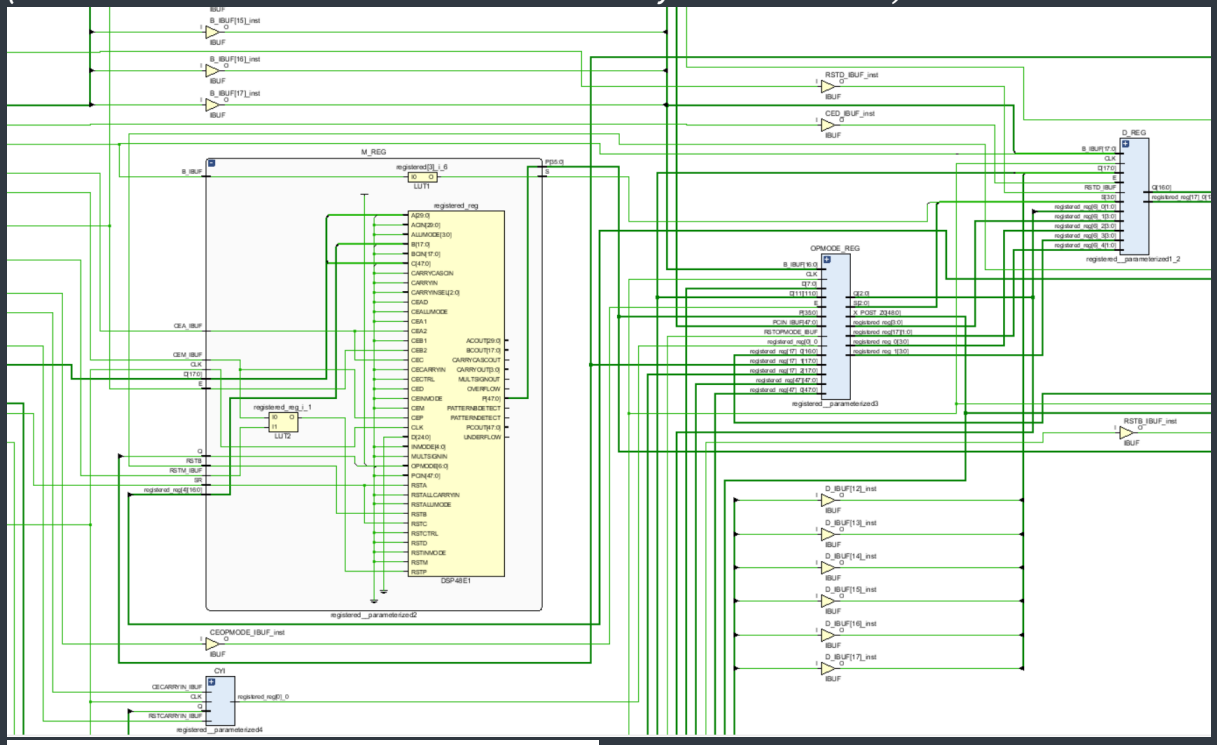


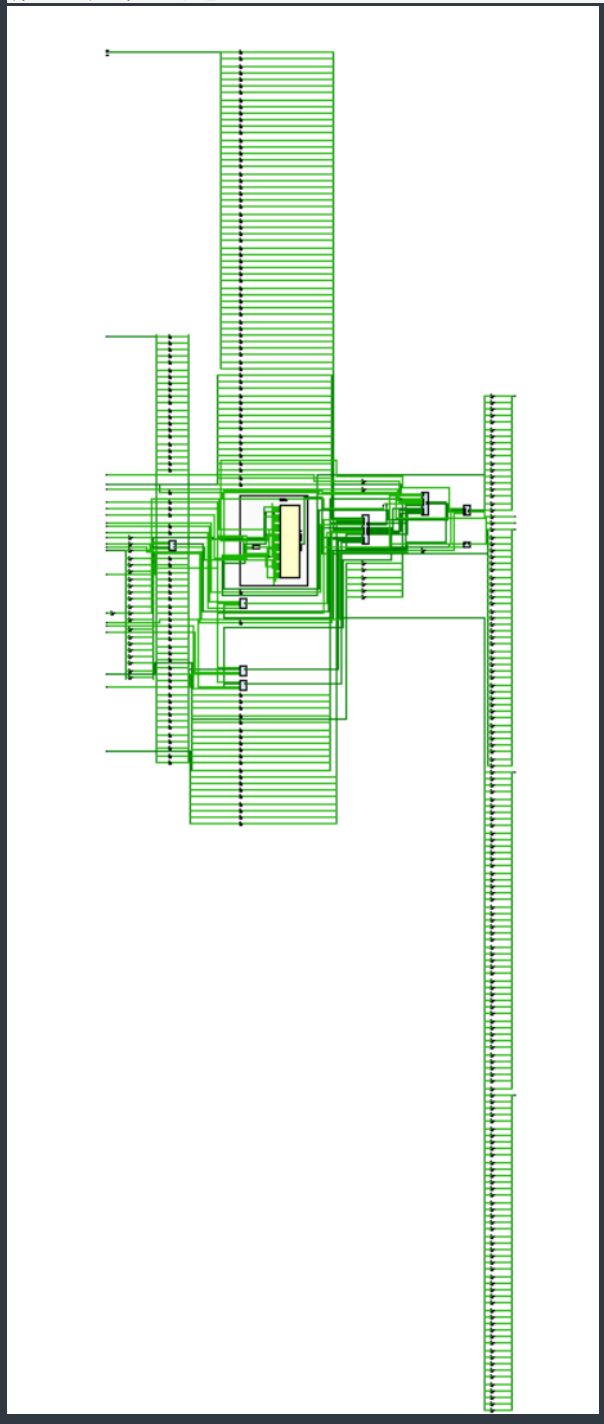
iii. Timing report



iv. Schematic snippets

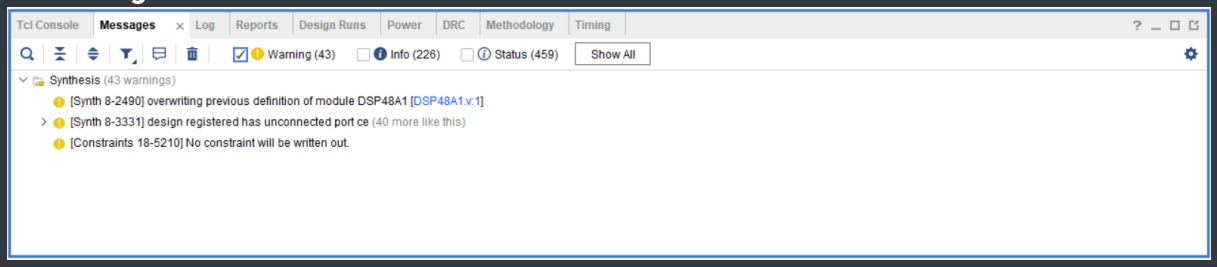
(DSP block with other cells from the FPGA should be in the synthesized schematic)



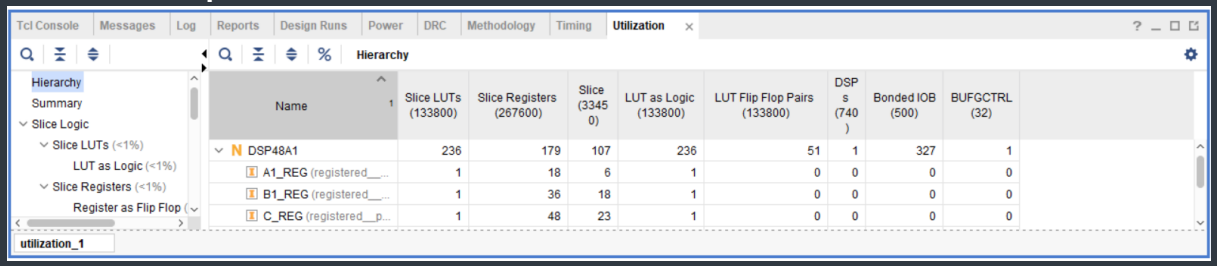


8. Implementation

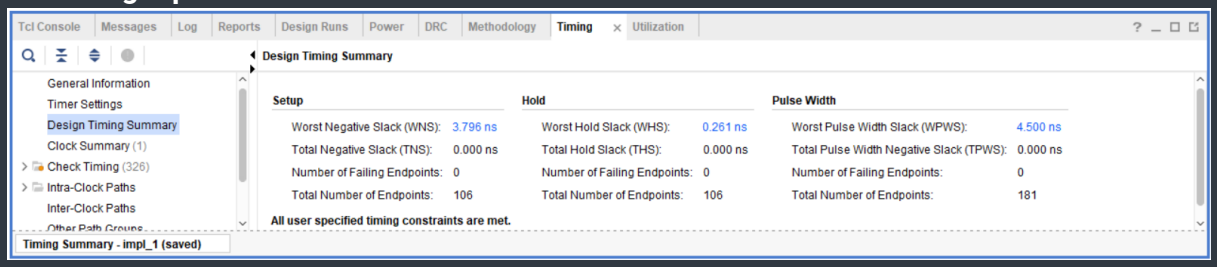
i. “Messages” tab



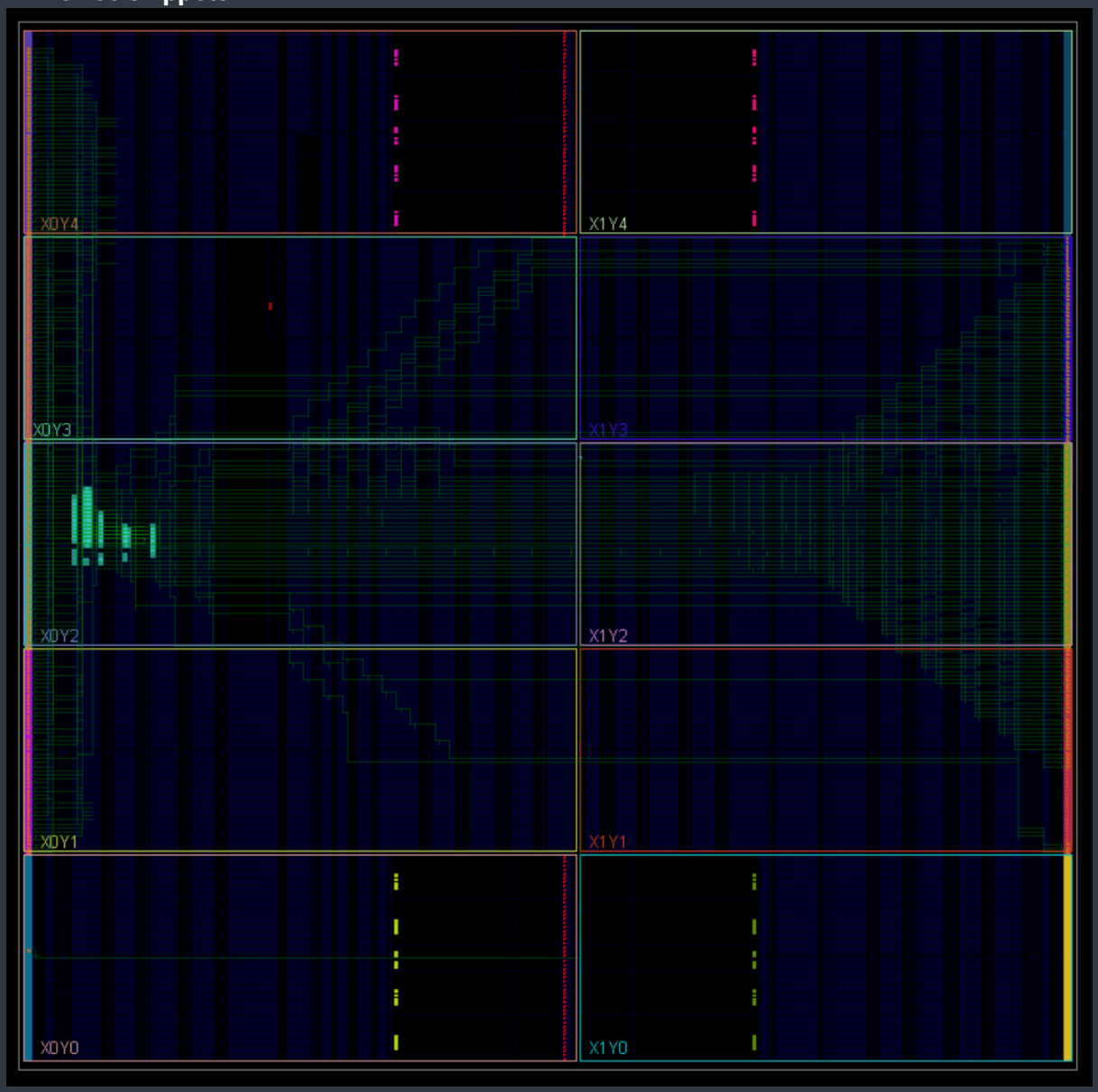
ii. Utilization report



iii. Timing report



iv. Device snippets



DSP Slice