

**Project(2): SPI Slave with Single Port RAM**

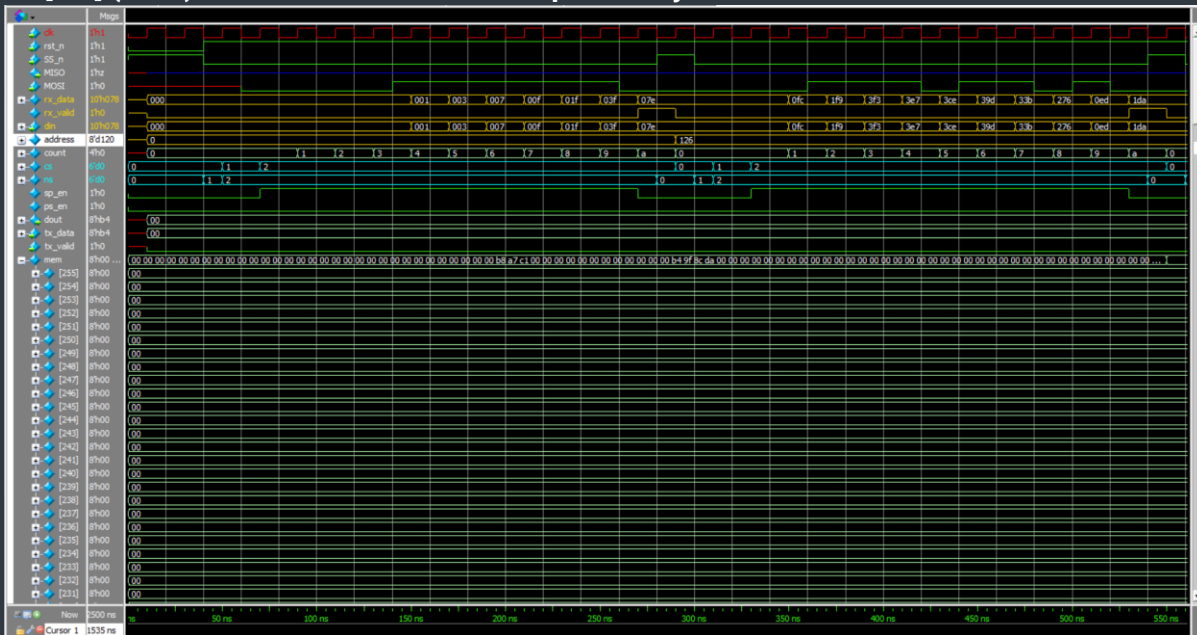
**Team Name: Silicon Maestro**

**Team Member(solo): Amr Ayman Mohamed Abdo**

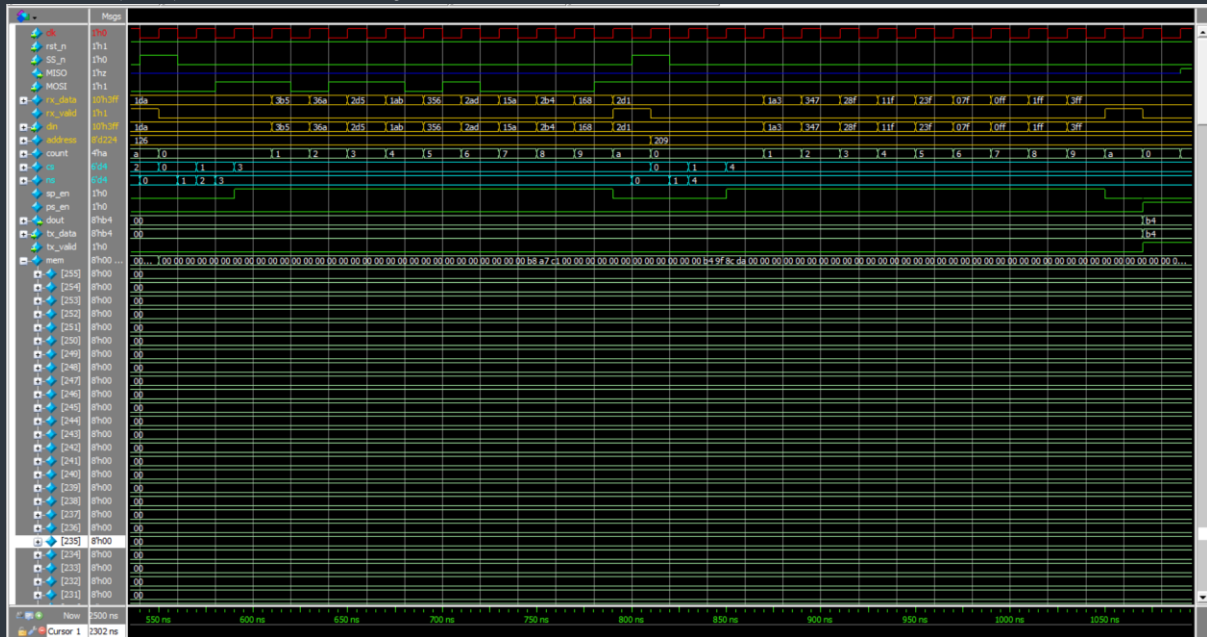
# 1. QuestaSim Snippets

i. First Communication Cycle (cs = WRITE, din[9:8] = 00): MOSI is converted from serial to parallel and after 10 clock cycles rx\_data (din) gets the parallel data, rx\_valid is asserted and din[7:0] (126) is held internally in the RAM as a write address.

ii. Second Communication Cycle (cs = WRITE, din[9:8] = 01): MOSI is converted from serial to parallel and after 10 clock cycles rx\_data (din) gets the parallel data, rx\_valid is asserted and din[7:0] (0xda) is written into the address previously held in the address bus.

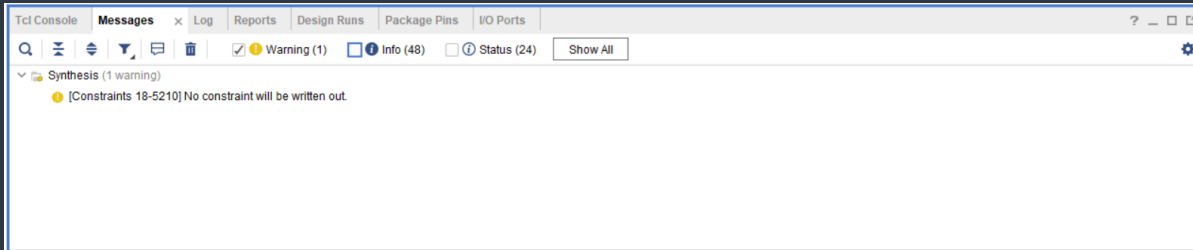


iii. Third Communication Cycle (cs = READ\_ADD, din[9:8] = 10): MOSI is converted from serial to parallel and after 10 clock cycles rx\_data (din) gets the parallel data, rx\_valid is asserted and din[7:0] (209) is held internally in the RAM as a read address.

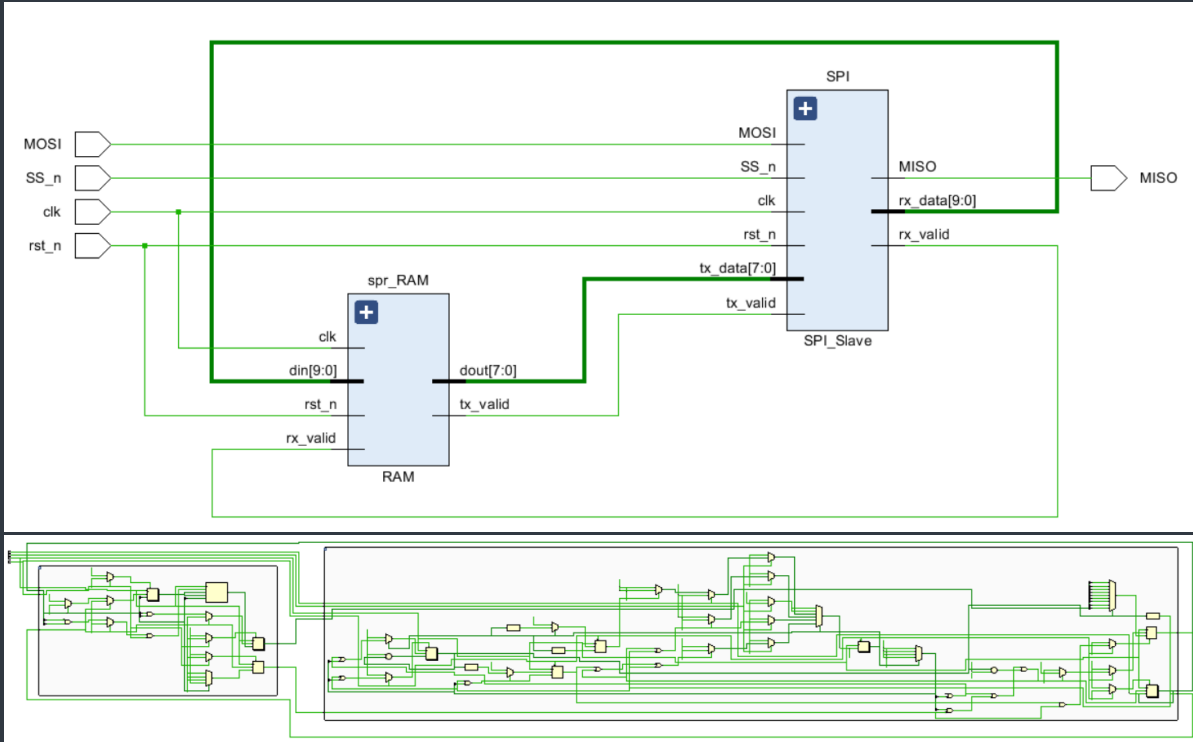


## 2. Elaboration

### i. "Messages" tab

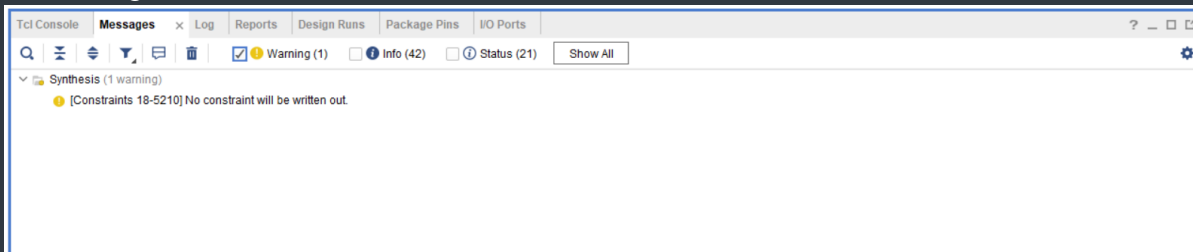


### ii. Schematic snippets



## 3. Synthesis

### i. "Messages" tab



### ii. Utilization report

#### a. (\*fsm\_encoding = "gray"\*)

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_spr_ram	27	30	0.5	5	1
SPI (SPI_Slave)	25	20	0	0	0
spr_RAM (RAM)	1	9	0.5	0	0

#### b. (\*fsm\_encoding = "one\_hot"\*)

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_spr_ram	28	32	0.5	5	1
SPI (SPI_Slave)	24	22	0	0	0
spr_RAM (RAM)	3	9	0.5	0	0

c. (\*fsm\_encoding = "sequential"\*)

Utilization						
Hierarchy						
Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFCTRL (32)	
SPI_spr_ram	31	30	0.5	5	1	
SPI (SPI_Slave)	30	20	0	0	0	
spr_RAM (RAM)	0	9	0.5	0	0	

iii. Timing report

a. (\*fsm\_encoding = "gray"\*)

Design Timing Summary						
Setup			Hold		Pulse Width	
Worst Negative Slack (WNS):	5.236 ns		Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	81		Total Number of Endpoints:	81	Total Number of Endpoints:	33
All user specified timing constraints are met.						

b. (\*fsm\_encoding = "one\_hot"\*)

Design Timing Summary						
Setup			Hold		Pulse Width	
Worst Negative Slack (WNS):	5.355 ns		Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	83		Total Number of Endpoints:	83	Total Number of Endpoints:	35
All user specified timing constraints are met.						

c. (\*fsm\_encoding = "sequential"\*)

Design Timing Summary						
Setup			Hold		Pulse Width	
Worst Negative Slack (WNS):	5.236 ns		Worst Hold Slack (WHS):	0.153 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns		Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0		Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	81		Total Number of Endpoints:	81	Total Number of Endpoints:	33

All of them are almost the same. We will proceed with sequential encoding.

iv. Synthesis report showing the encoding used

a. (\*fsm\_encoding = "gray"\*)

INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [C:/Digital_Electronics/Kareem_Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:15]			
INFO: [Synth 8-6155] done synthesizing module 'SPI_Slave' (i#1) [C:/Digital_Electronics/Kareem_Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:1]			
INFO: [Synth 8-6157] synthesizing module 'RAM' [C:/Digital_Electronics/Kareem_Waseem_Digital_Design_Diploma/Project2_SPI_Slave/RAM.v:1]			
State		New Encoding	Previous Encoding
IDLE		001	000000
CHK_CMD		000	000001
READ_DATA		011	000100
READ_ADD		010	000011
WRITE		111	000010

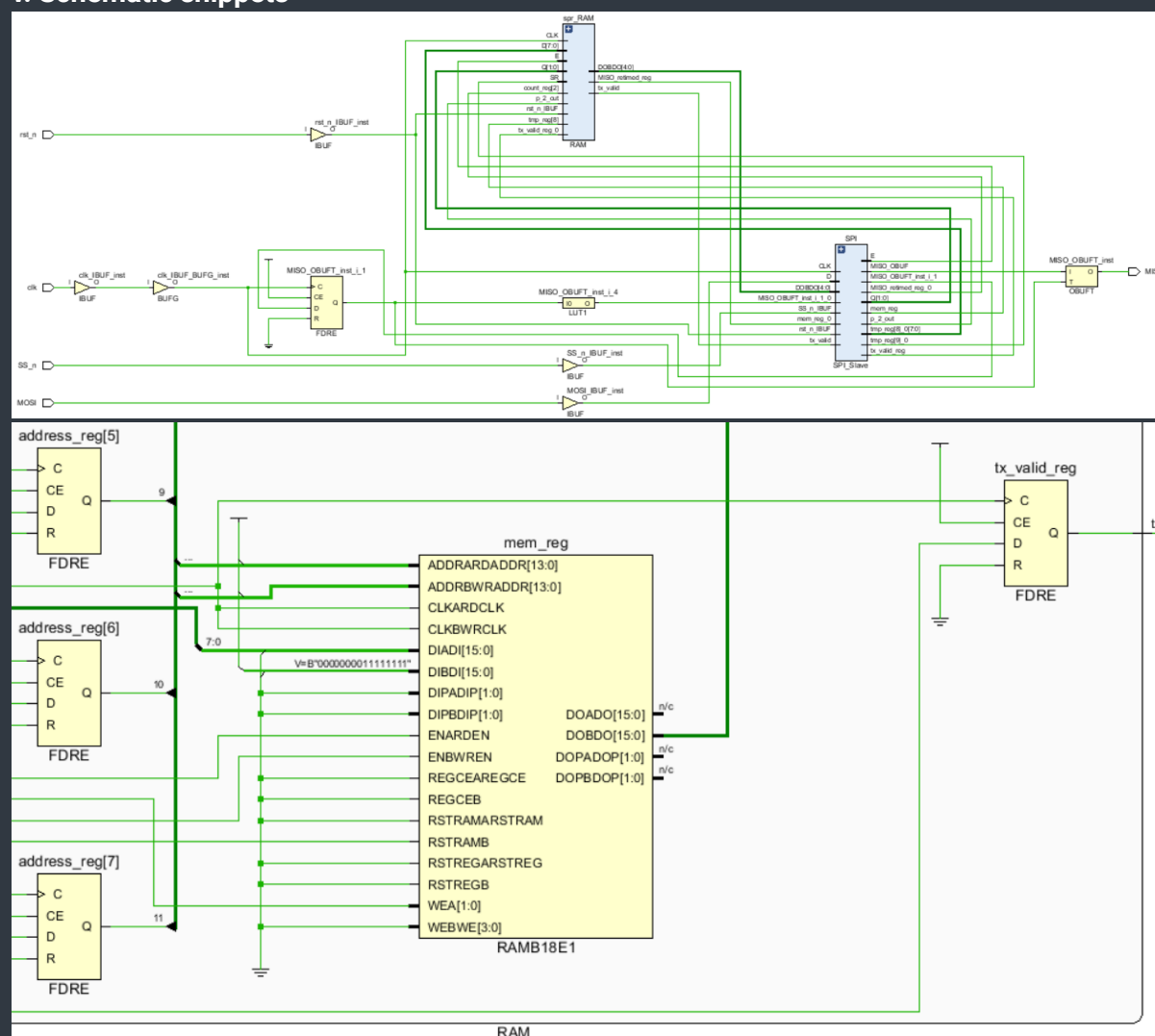
b. (\*fsm\_encoding = "one\_hot"\*)

INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "one_hot" *) [C:/Digital_Electronics/Kareem_Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:15]			
INFO: [Synth 8-6155] done synthesizing module 'SPI_Slave' (i#1) [C:/Digital_Electronics/Kareem_Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:1]			
State		New Encoding	Previous Encoding
IDLE		00010	000000
CHK_CMD		00001	000001
READ_DATA		00100	000100
READ_ADD		01000	000011
WRITE		10000	000010

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INFO: [Synth 8-5534] Detected attribute (* fsm_encoding = "sequential" *) [C:/Digital_Electronics/Kareem Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:15]
INFO: [Synth 8-6155] done synthesizing module 'SPI Slave' (1#1) [C:/Digital_Electronics/Kareem Waseem_Digital_Design_Diploma/Project2_SPI_Slave/SPI_Slave.v:1]
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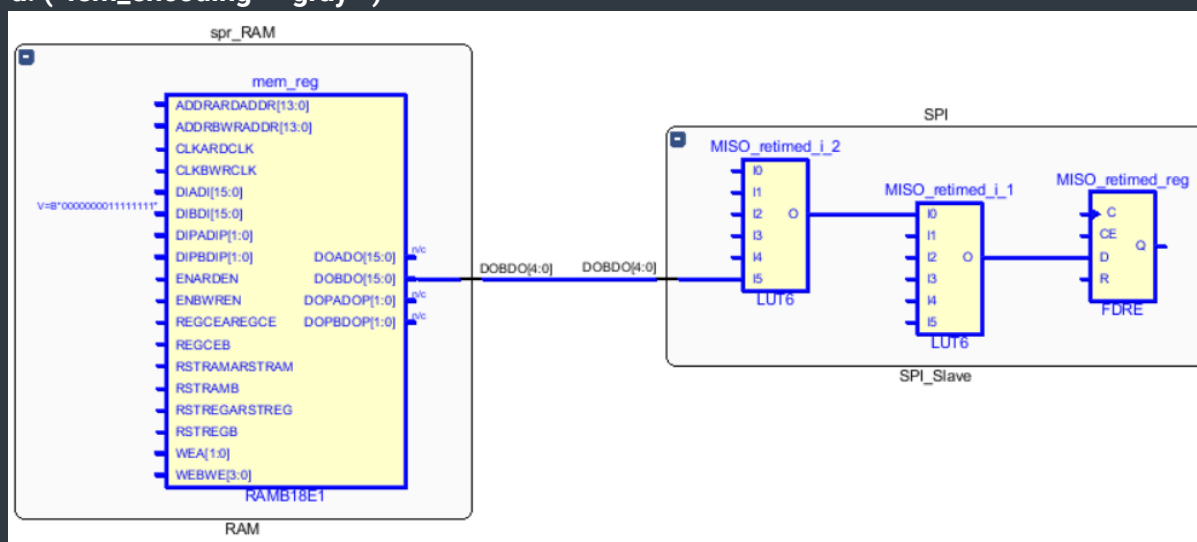
State	New Encoding	Previous Encoding
IDLE	001	000000
CHK_CMD	000	000001
READ_DATA	010	000100
READ_ADD	011	000011
WRITE	100	000010

## v. Schematic snippets

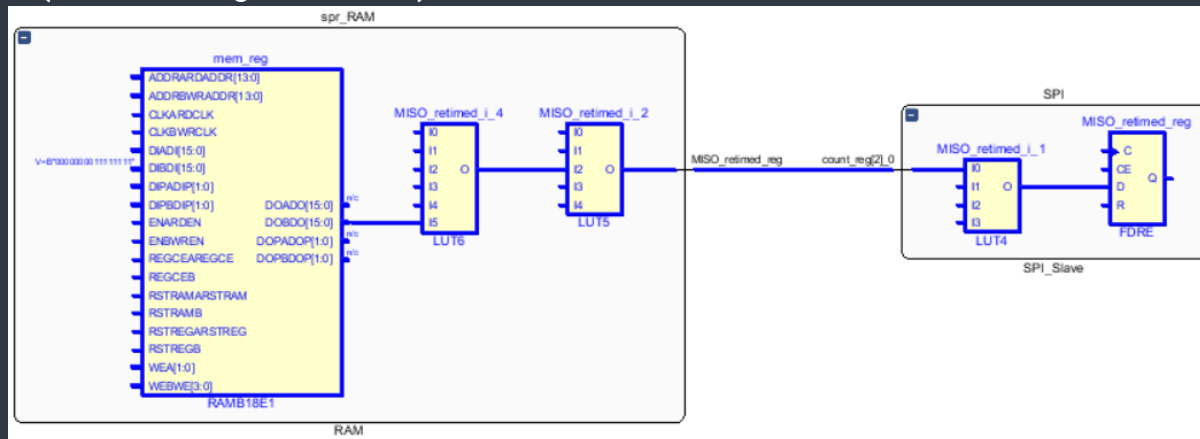


## vi. Critical path snippets

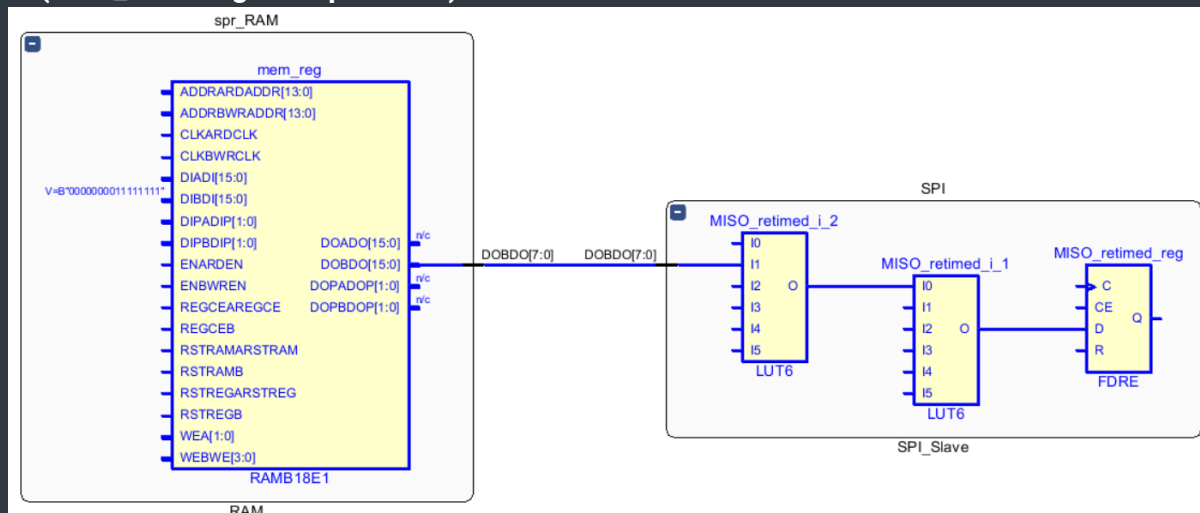
a. (\*fsm\_encoding = "gray"\*)



b. (\*fsm\_encoding = "one\_hot"\*)

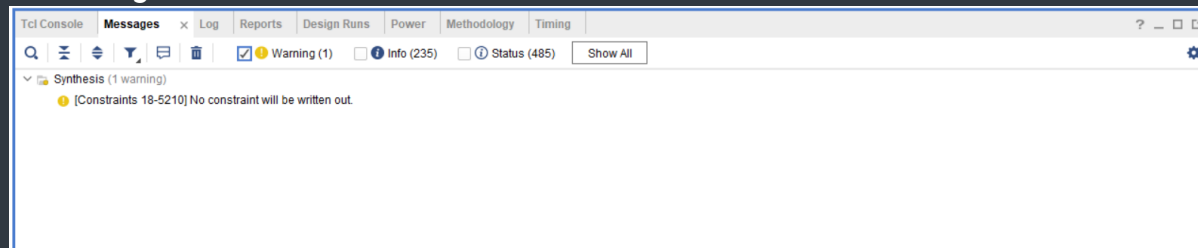


c. (\*fsm\_encoding = "sequential"\*)



## 4. Implementation

i. "Messages" tab



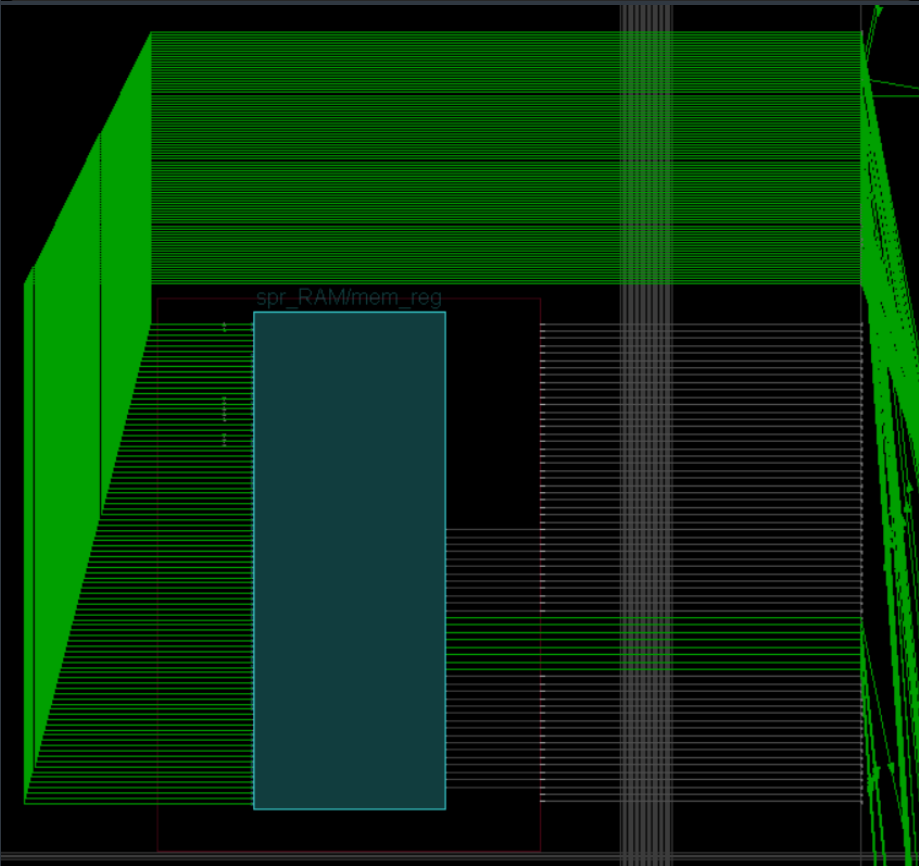
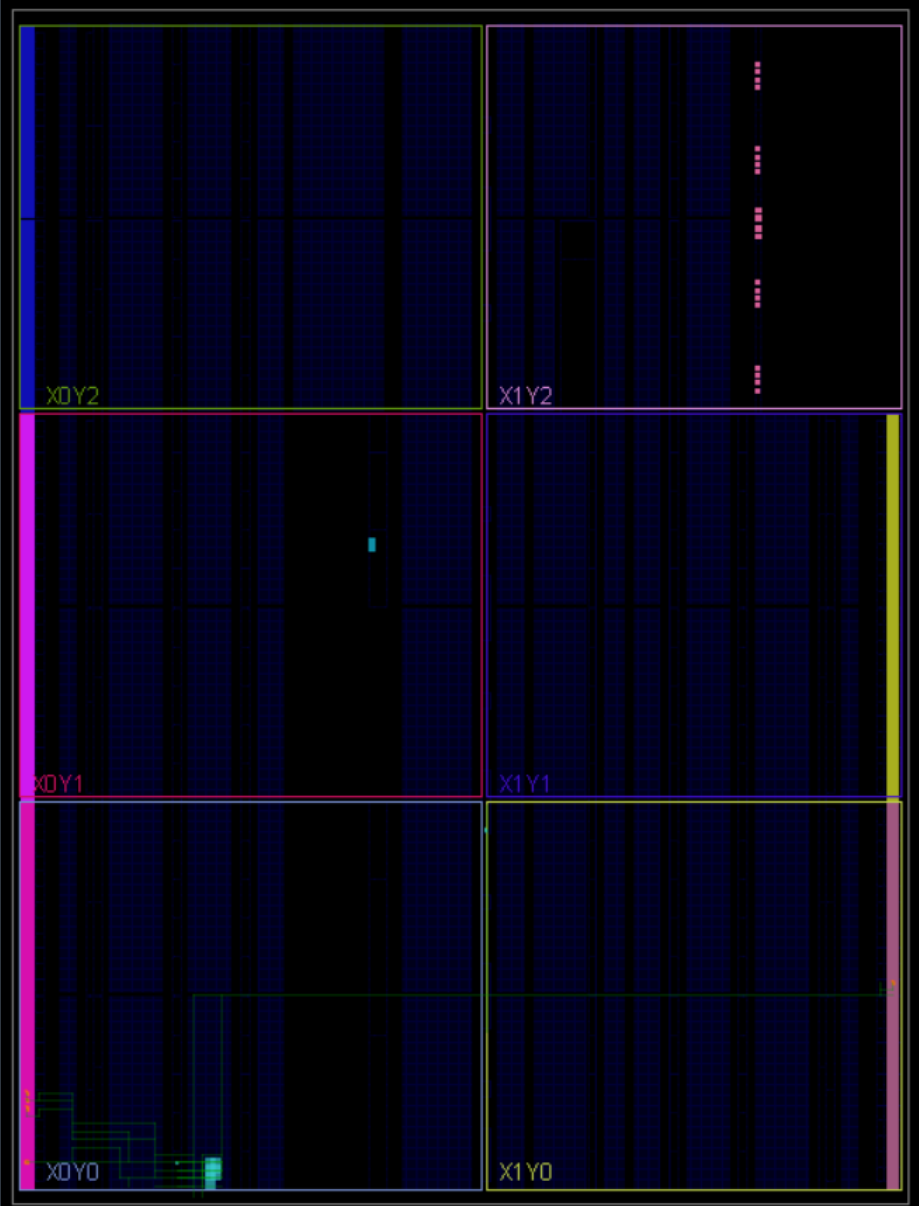
ii. Utilization report

Utilization									
Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
SPI_spr_ram	29	30	9	29	14	0.5	5	1	
SPI (SPI_Slave)	29	20	9	29	12	0	0	0	
spr_RAM (RAM)	0	9	2	0	0	0.5	0	0	

iii. Timing report

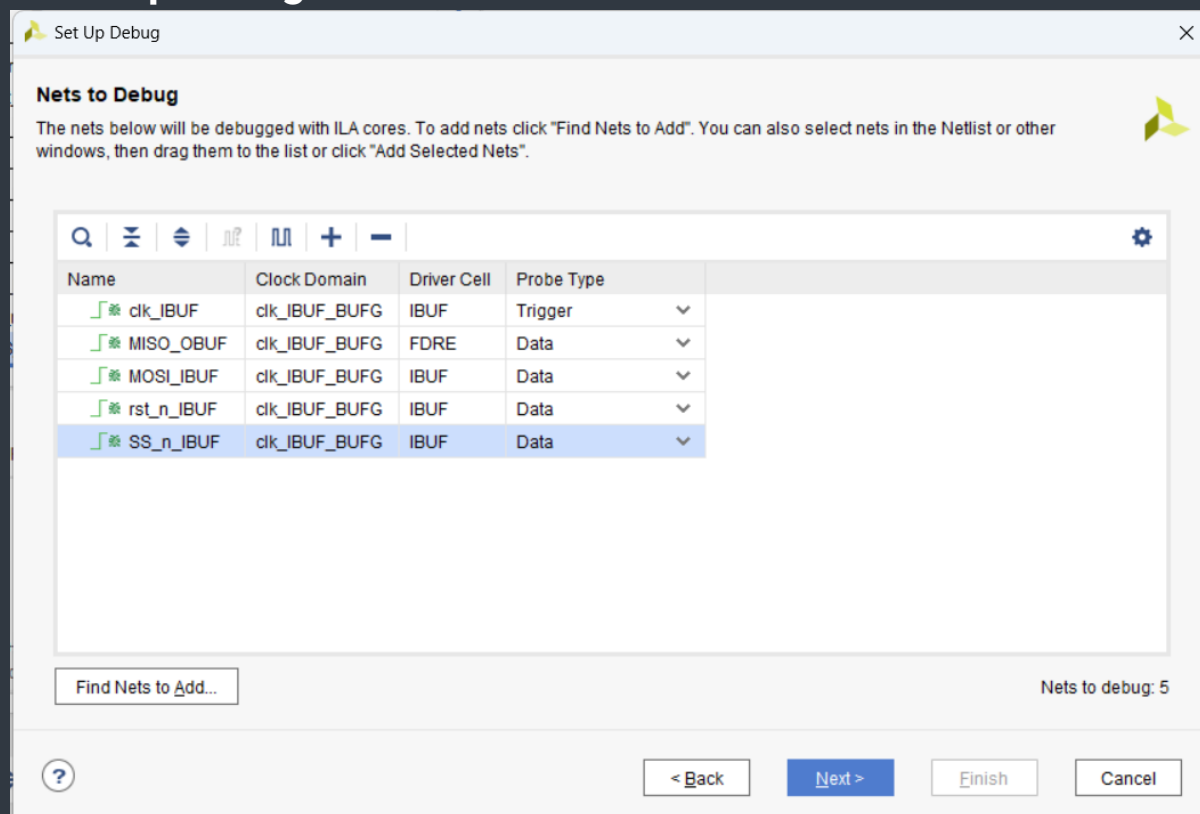
Design Timing Summary			
General Information	Setup	Hold	Pulse Width
Timer Settings			
Design Timing Summary			
Clock Summary (1)			
Check Timing (4)			
Intra-Clock Paths			
Inter-Clock Paths			
Other Path Groups			
Timing Summary - impl_1 (saved)			
Timing Summary - timing_1			

iv. Device snippets





## 5. Set Up Debug



## 6. Bitstream file

