ALU Design and Verification Using Cocotb

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Overview

This document provides an overview of the design and verification of an Arithmetic Logic Unit (ALU) using CoCotb. The verification process includes are based on the verification plan used before. The results from these tests are compared against a golden reference.

Design Description

The ALU design is implemented in Verilog and includes the following features:

- **Inputs:**
  - `A`: 4-bit operand
  - `B`: 4-bit operand
  - `ALU_FUN`: 2-bit function select signal
  - `CLK`: Clock signal
- **Output:**
  - `ALU_OUT`: 8-bit result of the ALU operation

The ALU supports four operations based on the `ALU_FUN` input:

- `2'b00`: Addition (`ALU_OUT = A + B`)
- `2'b01`: Subtraction (`ALU_OUT = A - B`)
- `2'b10`: Multiplication (`ALU_OUT = A * B`)
- `2'b11`: Division (`ALU_OUT = A / B`)

Verification Methodology

Tests were conducted by entering predefined inputs into the ALU and observing the output. The results were then compared to the expected values to validate correctness.

Verification Plan and Results:

```
PASSED: A = 1, B = 2, ALU_FUN = 0 -> 3
PASSED: A = 15, B = 1, ALU_FUN = 0 -> 16
PASSED: A = 4, B = 3, ALU_FUN = 1 -> 1
PASSED: A = 1, B = 4, ALU_FUN = 1 -> -3
PASSED: A = 2, B = 3, ALU_FUN = 2 -> 6
PASSED: A = 15, B = 2, ALU_FUN = 2 -> 30
PASSED: A = 4, B = 2, ALU_FUN = 3 -> 2
PASSED: A = 15, B = 1, ALU_FUN = 3 -> 15
PASSED: A = 15, B = 15, ALU_FUN = 0 -> 30
PASSED: A = 15, B = 15, ALU_FUN = 1 -> 0
PASSED: A = 15, B = 15, ALU_FUN = 2 -> 225
PASSED: A = 15, B = 15, ALU_FUN = 3 -> 1
After Driving Stimulus
tb_top passed
```

Comparison with Golden Reference

The outputs were compared to a golden reference. This comparison helps ensure that the ALU operates as expected and meets the design specifications.