

BIPOLAR JUNCTION TRANSISTOR

[Unit 2]

- A Bipolar junction transistor has 3 layers of semiconductor material.
- These are arranged either in npn sequence or pnp sequence and each of the 3 layers has terminal.
- The amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name Transfer - Resistor ie TRANSISTOR.

⇒ PNP Transistor :

- A BJT is simply a sandwich of one type of semiconductor material (p type or n type) between 2 layers of the opposite type.

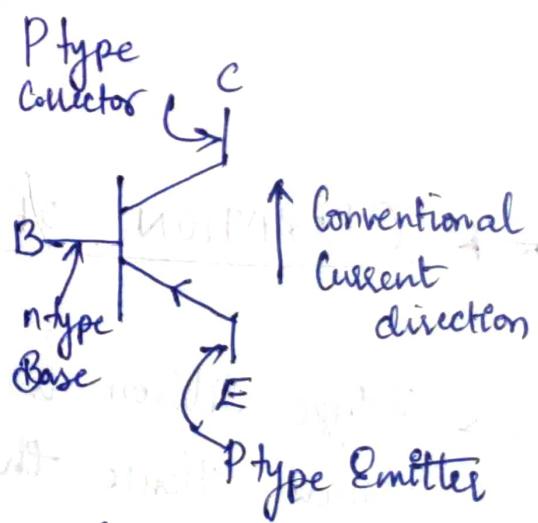
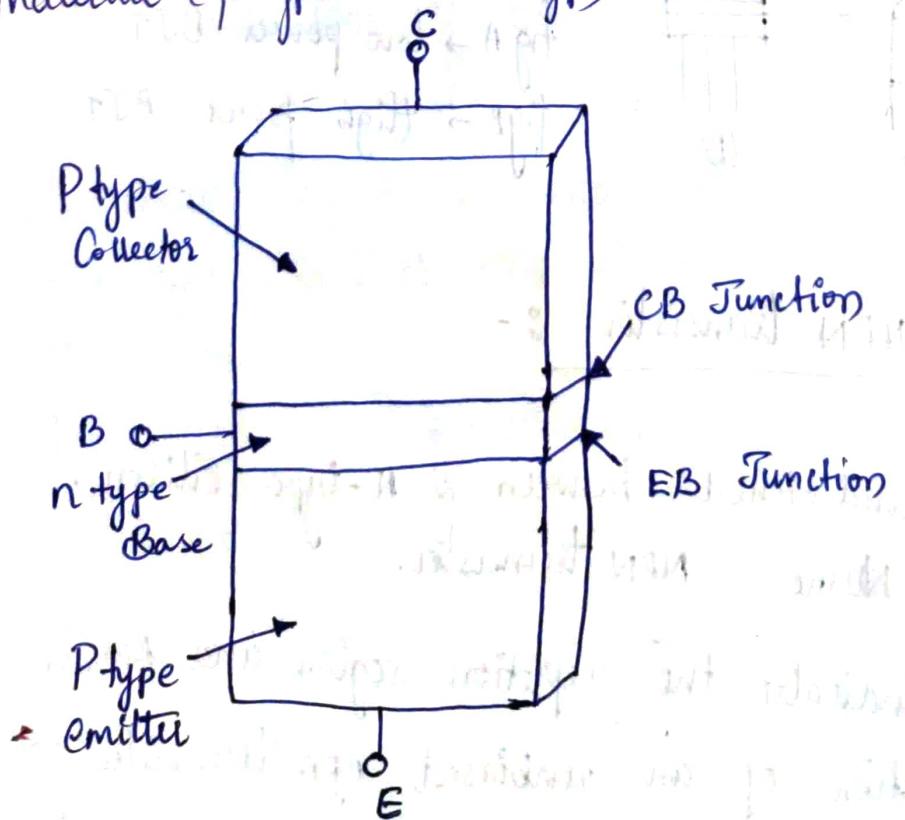


FIG : SYMBOL OF PNP Transistor

NPN Transistor

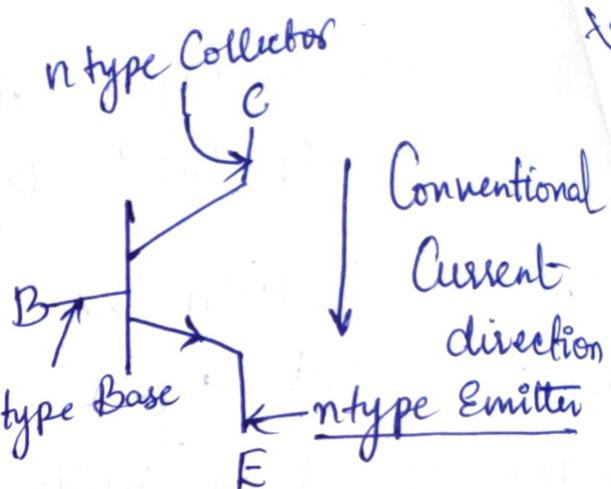
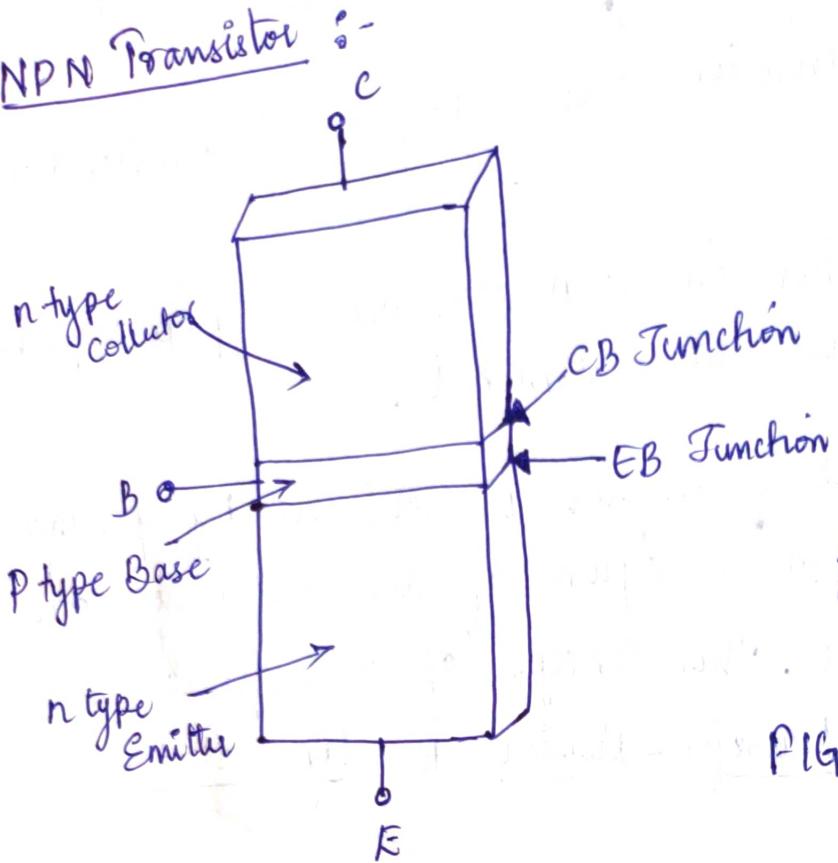


FIG: Symbol of npn transistor

- In low power BJT, the current levels are between 1mA to 20mA
- In high power BJT, the current levels are about 100mA to several amps.

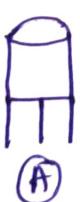


fig A → low power BJT

fig B → high power BJT.

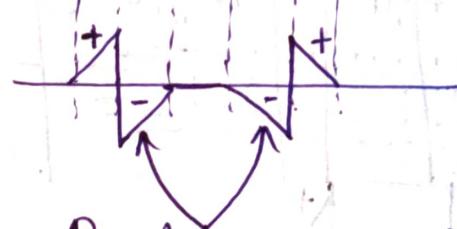
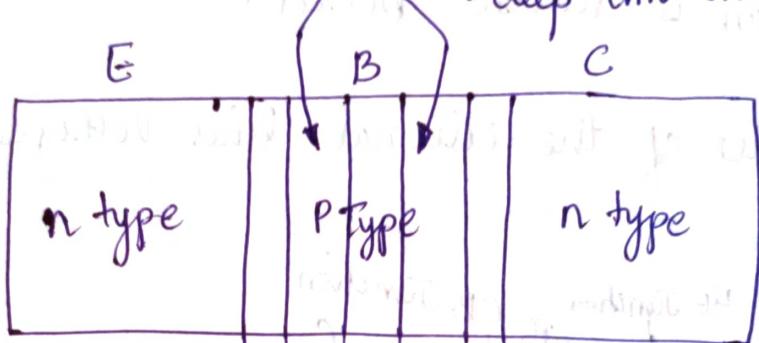
OPERATION OF NPN transistor :-

- P type silicon is sandwiched between 2 N-type silicon layers. Hence the name NPN transistor.
- The below figure indicates the depletion region and Barrier Voltages at the Junction of an unbiased npn transistor.

Unbiased transistor means a transistor with no external voltage is applied.

- ie there will be no current flowing from any of the transistor leads.

Depletion regions penetrate deep into the base.



Barrier voltages positive on n-type and -ve on p-type

- The centre layer of the transistor is very much narrower than the 2 outer layers.
- The outer layers are much more heavily doped than the centre layer, so that the depletion region penetrate deep into the base.
- Because of this penetration the distance between the 2 depletion regions is very short (within the base).

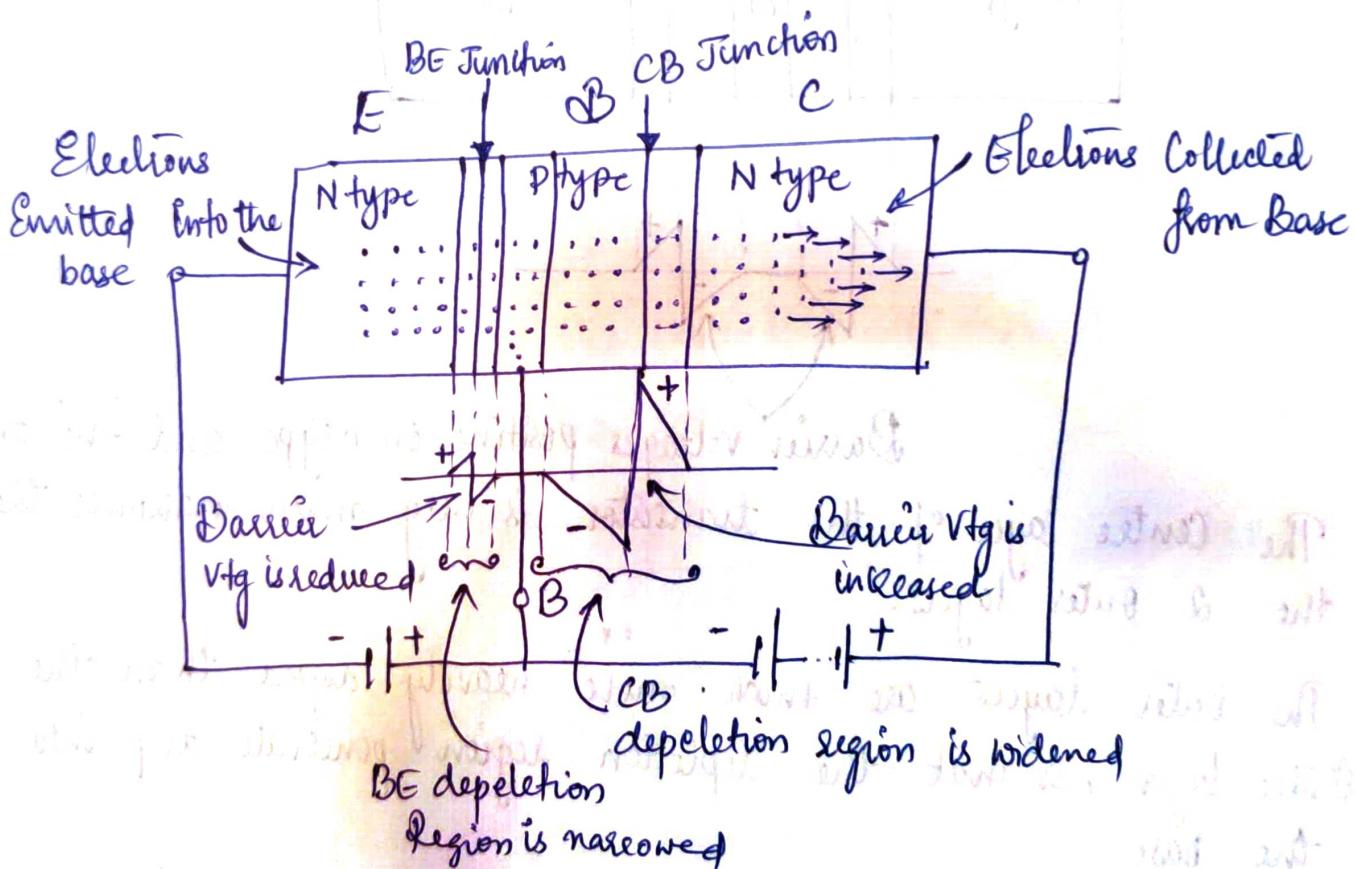
→ Consider the figure below, which shows npn transistor with external bias voltage.

→ For normal operation of the transistor,

→ BE junction is forward biased.

→ CB junction is reverse biased.

→ Note the polarities of the external bias voltages.



→ The forward bias at the BE Junction reduces the barrier voltage and causes electrons to flow from n type emitter to p type base.

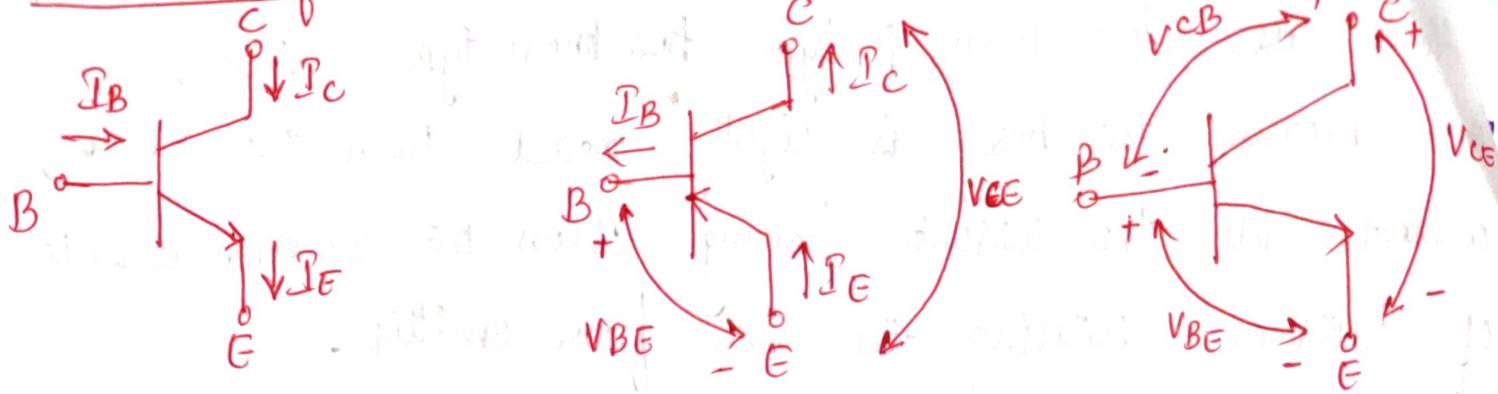
→ The electrons are emitted into the base region. hence the name emitter.

(3)

Holes also flow from P type base to n type emitter, But because the base is lightly doped than the collector, almost all the current flowing across BE Junction consists of electrons entering the base from emitter.

- Thus electrons are the majority charge carriers in npn device.
- The reverse bias at the CB junction cause the CB depletion region to penetrate deep into the base than when the junction was unbiased.
- The electrons crossed from emitter to the base, arrive quite close to the large negative-positive electric field at the CB depletion region.
- Because electrons have -ve charge, they are drawn across the CB Junction by the biased voltage.
- Hence they are said to be collected.
- Some of the charge carriers entering the base from the emitter do not reach the collector but flow out through the base connection.

Directions of Current



Note: The directions of I_B and I_C are always opposite to the direction of I_E in BJT.

Transistor Current gains :-

① Emitter to Collector Current gain:

→ It is given by the ratio of dc collector current to dc emitter current.

→ It is denoted by α_{dc} and given by,

$$\alpha_{dc} = \frac{I_C}{I_E}$$

→ α_{dc} is also called as Common base current gain.

② Base to Collector Current.

→ It is given by the ratio of dc collector current to dc base current.

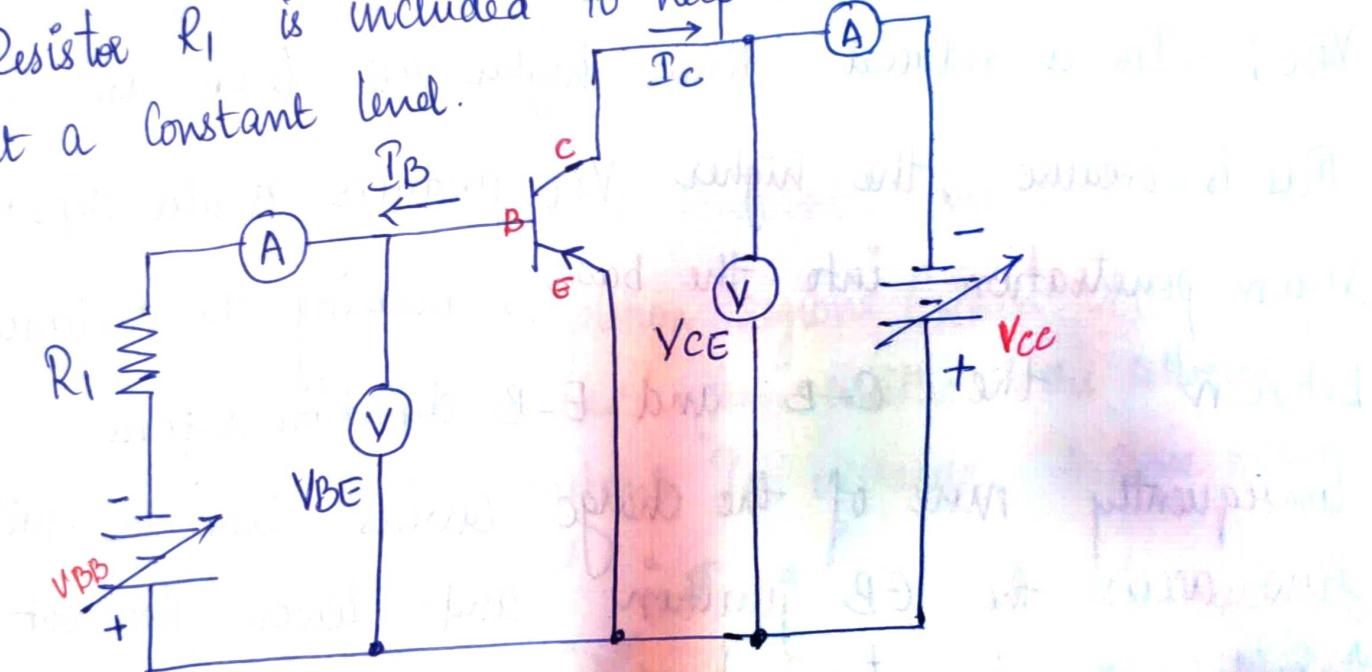
$$\beta_{dc} = \frac{I_C}{I_B}$$

→ β_{dc} is also called as common emitter current gain.

COMMON Emitter CHARACTERISTICS :

Common Emitter circuit :-

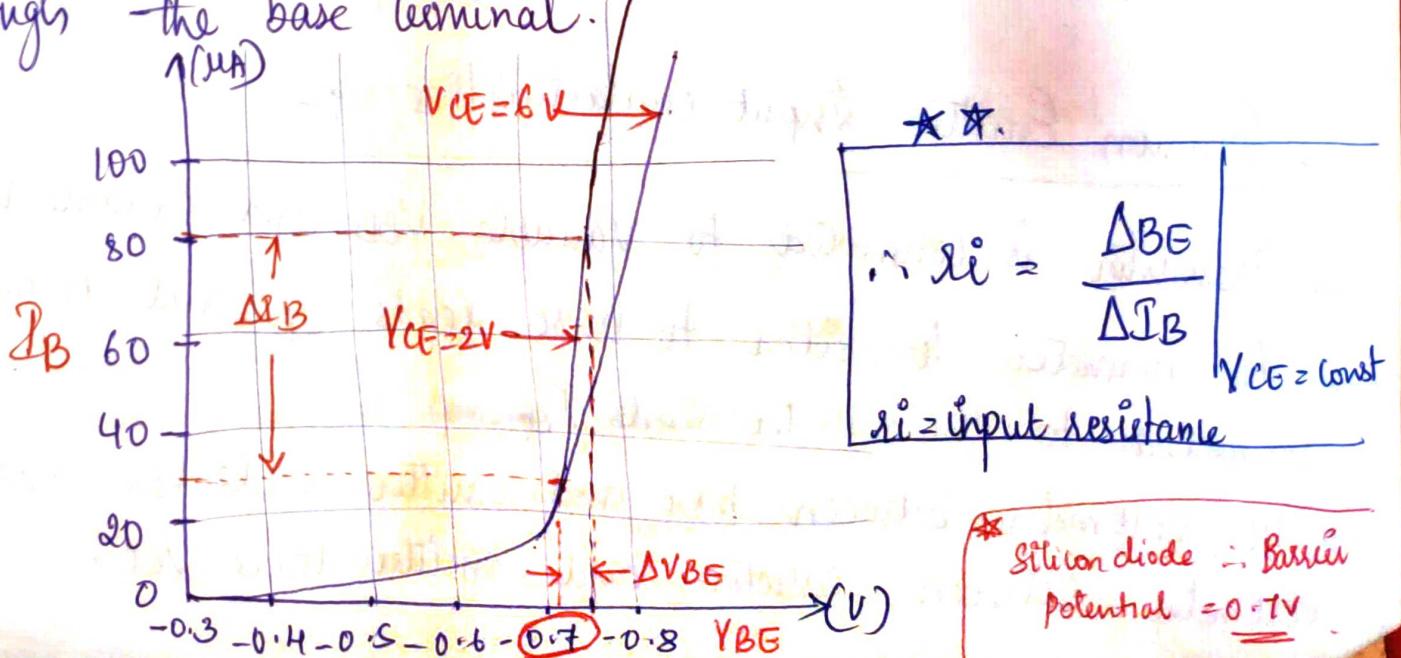
- The figure shows a ckt for determining BJT Common emitter characteristics.
- The input is applied between the base and emitter terminals, and the output is taken at the collector and emitter terminals, so that the emitter terminal is common to both input and O/p.
- Resistor R_1 is included to help maintain the base current at a constant level.



Common Emitter Input characteristics :-

- Transistor is connected to variable V_{BB} and variable V_{CC} Supply.
- A Ammeter connected to base reads I_B and Ammeter connected to the collector reads I_C .
- DC voltmeter between base and emitter reads V_{BE} and dc voltmeter between collector and emitter reads V_{CE} .

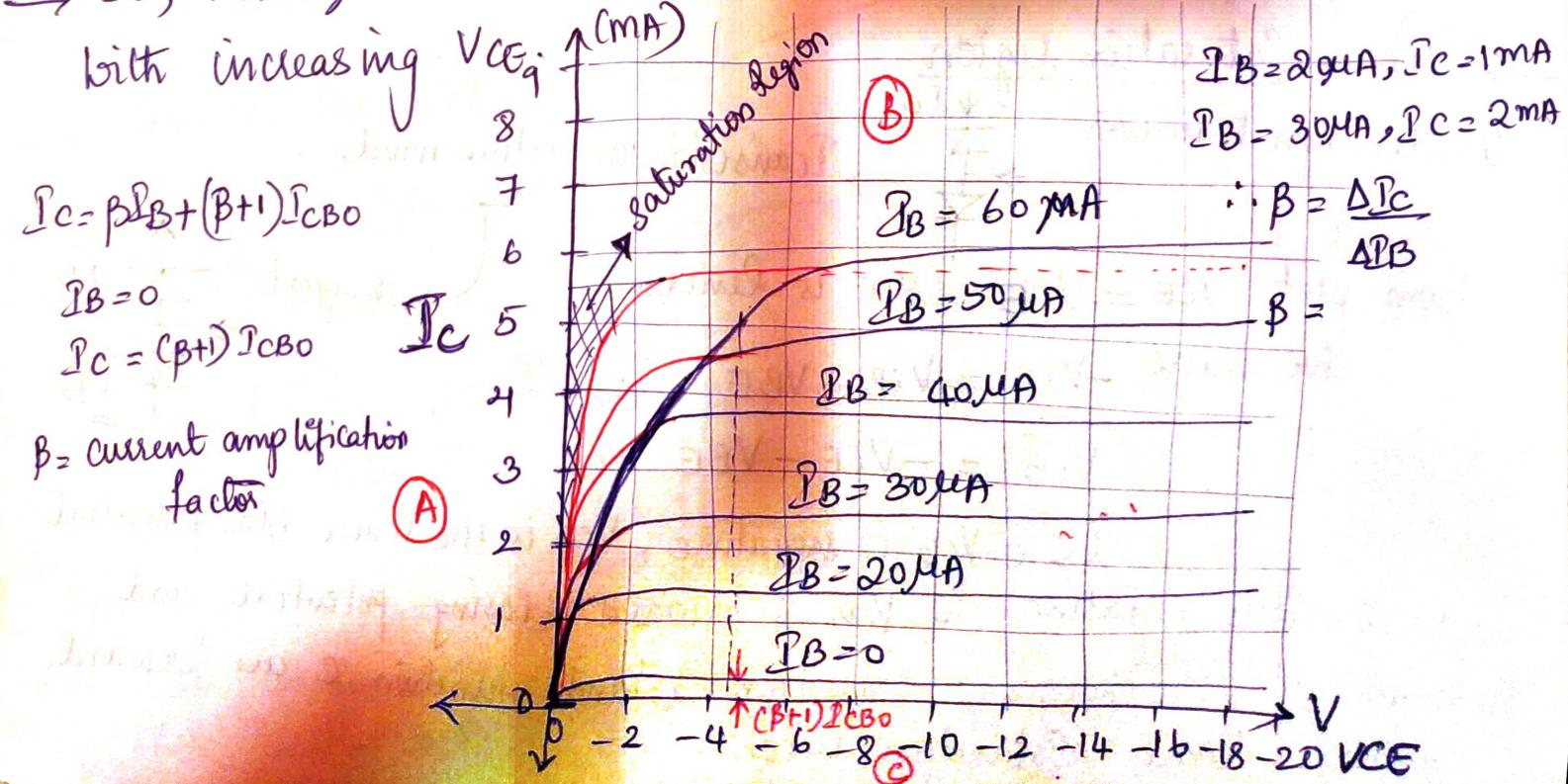
- Procedure for plotting input characteristics is as follows
- V_{CE} is held constant, V_{BE} is set at convenient levels and the corresponding I_B levels are recorded.
- I_B is then plotted Verses V_{BE} , as shown in figure.
- It is seen that common emitter input characteristics are those of a forward biased pn junction diode.
- In the plot, it is observed that, for a given level of V_{BE} , I_B is reduced when higher V_{CE} levels are employed.
- This is because, the higher V_{CE} produces greater depletion region penetration into the base, reducing the distance between the C-B and E-B depletion regions.
- Consequently more of the charge carriers from the emitter flow across the CB junction and fewer flow out through the base terminal.



Common Emitter Output characteristics

To plot the off characteristics, the following procedure is followed.

- Adjust V_{BB} , to set I_B to a fixed value
- At each I_B level, V_{CE} is adjusted in steps and I_C is recorded at each V_{CE} step.
- The I_C values are plotted versus V_{CE} for each I_B level, to create the kind of off characteristics.
- Note that V_{BE} and V_{CG} polarities are negative in the graph. This is because pnp transistor is been used ★
- Because I_E is not held constant, the shortening of the distance b/n the depletion regions (when V_{CB} is increased) draws more charge carriers from emitter to the collector
- So, although I_B is constant I_C increases to some extent with increasing V_{CE} .



β = current amplification factor

$$I_B = 0$$

$$I_C = (\beta + 1)I_{CBO}$$

$\rightarrow V_{CE} \neq 0$ due to Early effect (EE)

$$V_{CE} = V_{CB} + V_{BE}$$

If we increase V_{CE} , V_{CB} also increases.

i.e. The effective width of the base decreases, decreasing the base current. When Base current I_B decreases, I_C increases

$$N_{eff} \downarrow = I_B \downarrow \Rightarrow I_C \uparrow$$

i.e. The Collector current not only depends on the input current I_C , but also depends upon the o/p v/tg V_{CE}

★★(This is because the electrons emitted by the emitter will get collected by the collector, so I_C increase and I_B decrease on increasing the o/p voltage V_{CG})★★

\rightarrow In the plot, B \rightarrow Active region because there is amplification in the current, i.e. Junction E is forward biased and Junction C is reverse biased.

\rightarrow A \rightarrow Saturation region

Consider n/pn transistor



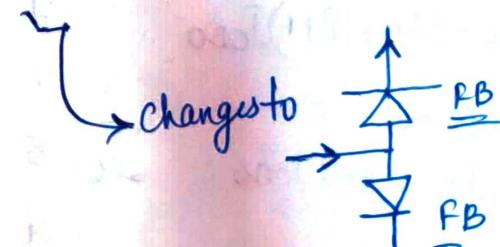
Transistor in active mode.

From plot $V_{CE} = -V_{CB}$ (V_{CE} is reversed)

$$\text{we have } -V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = -V_{CE} - V_{BE}$$

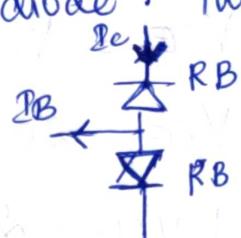
\hookrightarrow i.e. V_{CB} is negative, V_{CB} is the reverse bias potential and now it is negative. i.e. $V_{CB} \rightarrow$ forward biasing potential and direction of I_C changes. i.e. Junction E and Junction C are forward biased. Hence Saturation region.



⑥ C. \rightarrow Cut off region

i.e. $I_B < 0$, so the direction of base current will change. Both the diodes are reverse biased because $V_{CE} \gg 0$,

$\rightarrow V_{CB}$ can easily reverse bias the diode. This happens in cut off region.



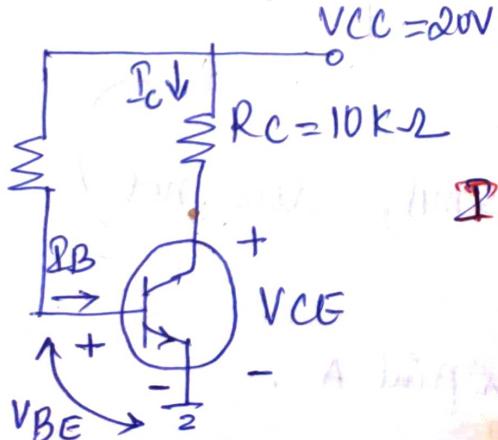
DC LOAD LINE and BIAS POINT

\rightarrow DC load line :-

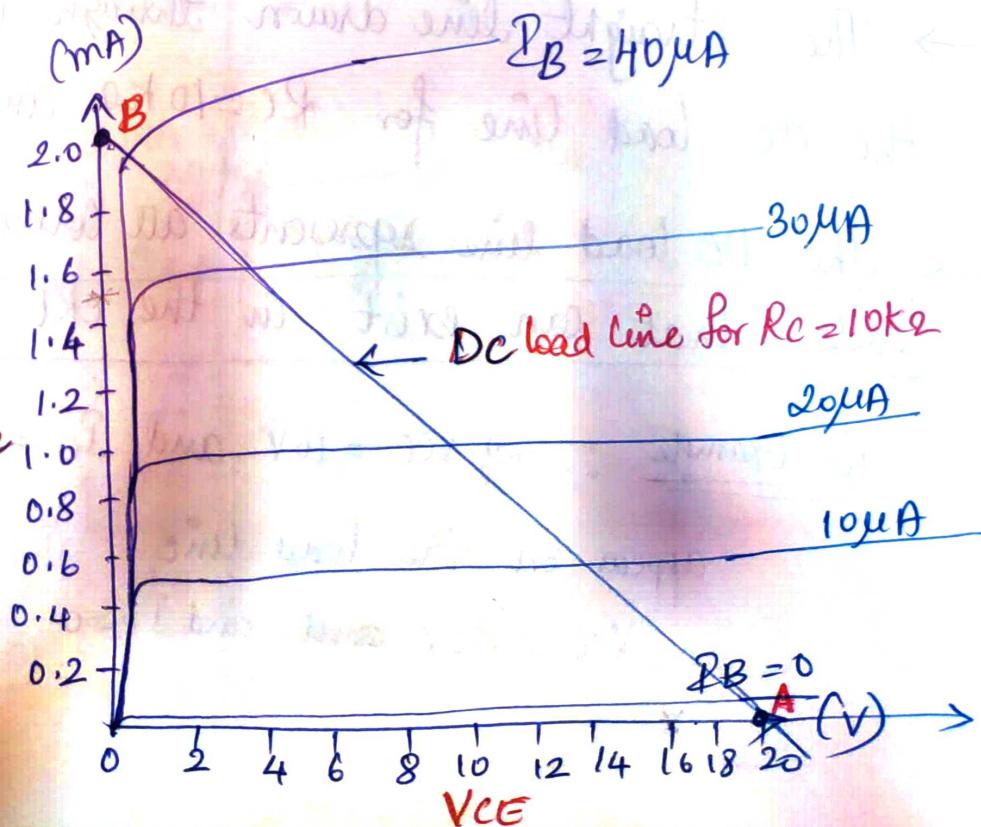
\rightarrow The DC load line for a transistor circuit is a straight line drawn on the transistor output characteristics.

\rightarrow For a common emitter (CE) ckt, the load line is a graph of I_C v/s V_{CE} , for a given value of R_C , and supply voltage V_{CC} .

\rightarrow Consider the ckt,



Here, BE Junction \Rightarrow FB
CB Junction \Rightarrow RB



from the Ckt,

$$V_{CE} = V_{CC} - I_C R_C$$

If $V_{BE} = 0$, then transistor is not conducting and $I_C = 0$.

$$\therefore V_{CE} = V_{CC} - (0 \times R_C)$$

$$\therefore V_{CE} = 20 - 10 \times 0$$

$$\boxed{V_{CE} = 20V} \rightarrow \text{Point A}$$

→ Plot point A on CE characteristics @ $I_C = 0$ and $V_{CE} = 20V$

→ Now assume $I_C = 2mA$

$$V_{CE} = 20V - (2mA \times 10k\Omega)$$

$$\boxed{V_{CE} = 0V} \rightarrow \text{point B}$$

→ Plot point B on the graph @ $V_{CE} = 0$ and $I_C = 2mA$.

→ The straight line drawn through points A and B is the dc load line for $R_L = 10k\Omega$ and $V_{CE} = 20V$.

→ The DC load line represents all corresponding I_C and V_{CE} levels that can exist in the ckt.

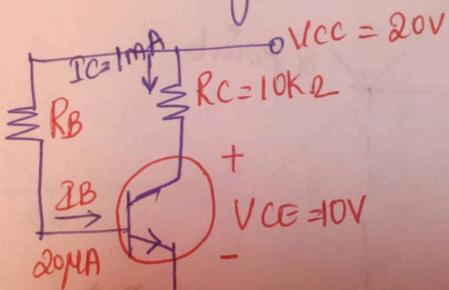
for example : If $V_{CE} = 16V$ and $I_C = 1.5mA$, does not appear on the load line.

$\therefore V_{CC} = 20V$ and $I_C = 0$ for point A.

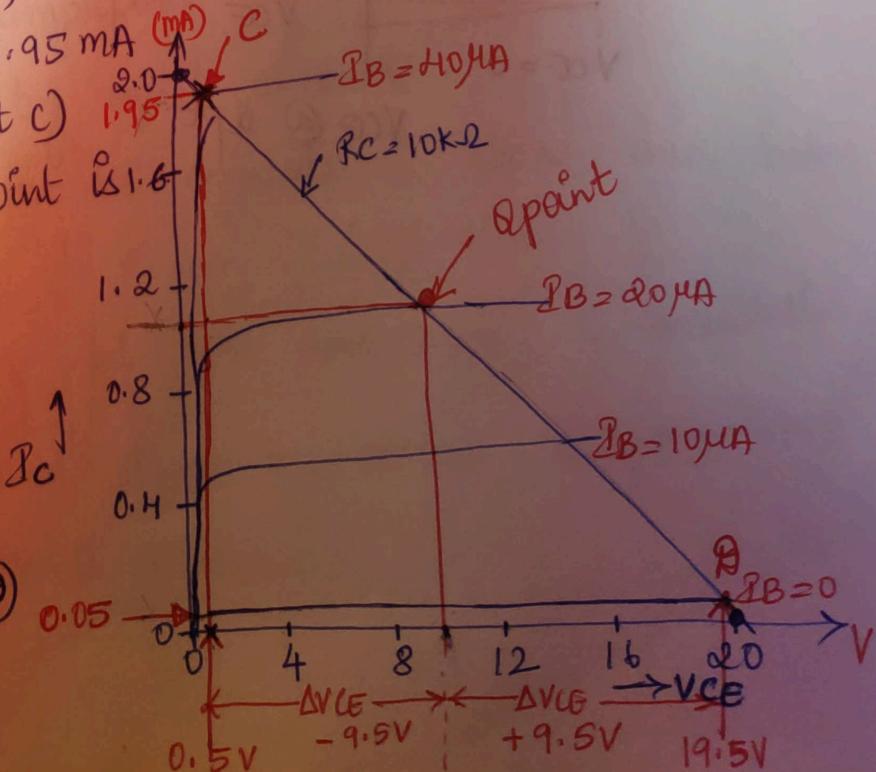
(7)

dc Bias point (Q point) :

- The dc bias point or quiescent point (Q point) also known as the dc operating point identifies the transistor collector current (I_C) and collector-emitter voltage (V_{CE}) when there is no input signal at the base terminal.
- Thus it defines the dc conditions in the circuit.
- When a signal is applied to the transistor base, I_B varies causing I_C to vary and produces a variation in V_{CE} .
- Consider the Ckt,



- When I_B is increased from 20μA to 40μA, I_C becomes ≈ 1.95 mA (Point C) and V_{CE} becomes 0.5V (Point D).
- The V_{CE} change from Q point is 1.5V.
- When I_B is reduced from 20μA to 0, I_C goes ≈ 0.05 mA, and V_{CE} goes up to 19.5V (Point E).
- ∴ $\Delta V_{CE} = 19.5V - 10V = 9.5V$.



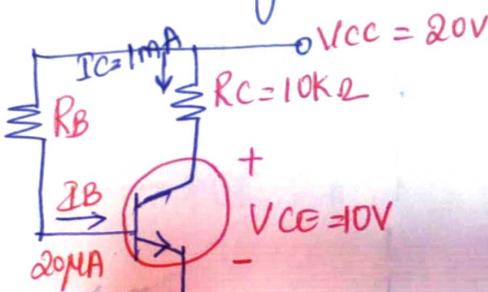
DC Bias point (α point) :

→ The dc bias point or quiescent point (α point) also known as the dc operating point identifies the transistor collector current (I_C) and Collector-emitter V_{CE} (V_{CE}) when there is no input signal at the base terminal.

→ Thus it defines the dc conditions in the circuit.

→ When a signal is applied to the transistor base, I_B varies causing I_C to vary and produces a variation in V_{CE} .

→ Consider the Ckt,



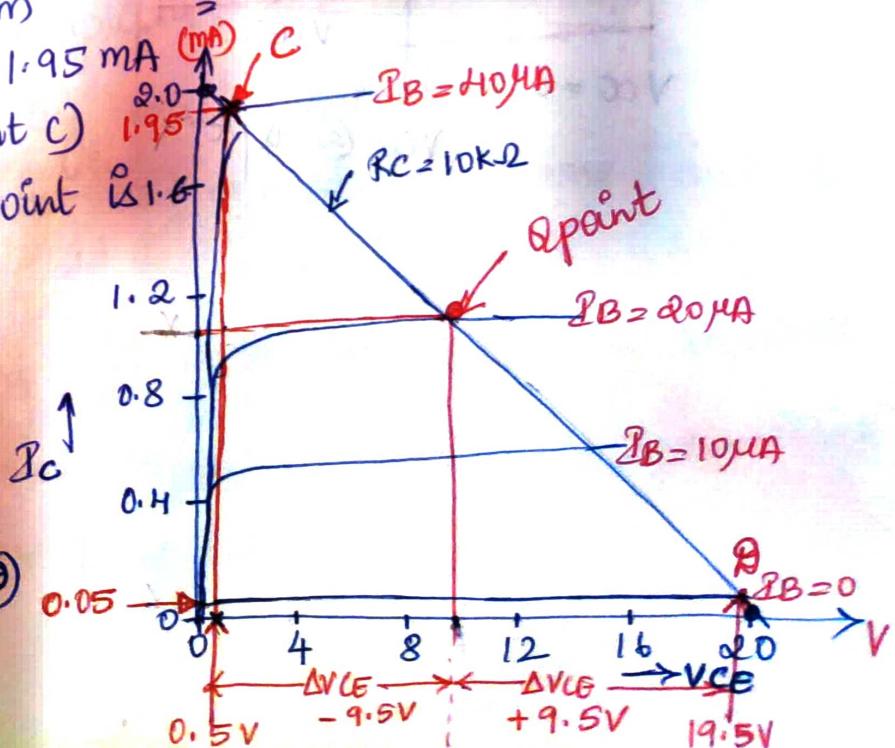
→ When I_B is increased from 20μA to 40μA, I_C becomes ≈ 1.95 mA (point C) and V_{CE} becomes 0.5V (point C)

→ The V_{CE} change from α point is 1.6

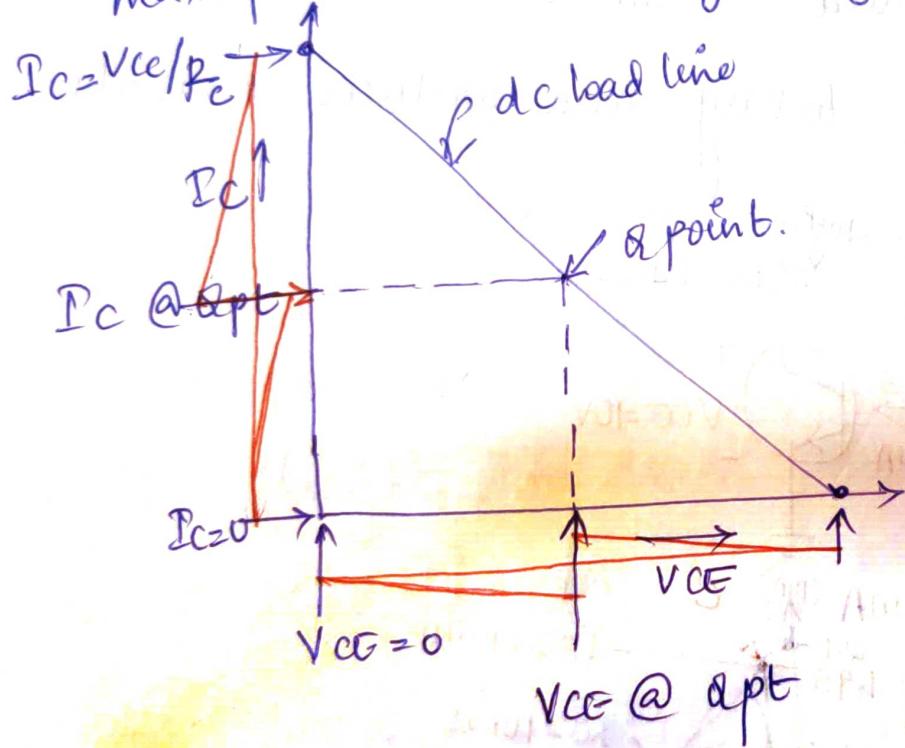
$$\Delta V_{CE} = 10V - 0.5V \\ = \underline{\underline{9.5V}}$$

→ When I_B is reduced from 20μA to 0, I_C goes ≈ 0.05 mA, and V_{CE} goes up to 19.5V (point D)

$$\therefore \Delta V_{CE} = 19.5V - 10V \\ = \underline{\underline{9.5V}}$$



- ie It produces a collector voltage swing of 9.5V.
- The maximum possible transistor collector emitter vtg swing for a circuit can be determined without using the transistor characteristics.
- For convenience it may be assumed that I_C can be driven to zero at one extreme and V_{CE} at the other extreme.
- This changes the V_{CE} from $V_{CE} = V_{CC}$ to $V_{CE} = 0$.
- Thus the Q pt at the center of the load line, the max. possible collector vtg swing is to be $\approx \frac{V_{CC}}{2}$.



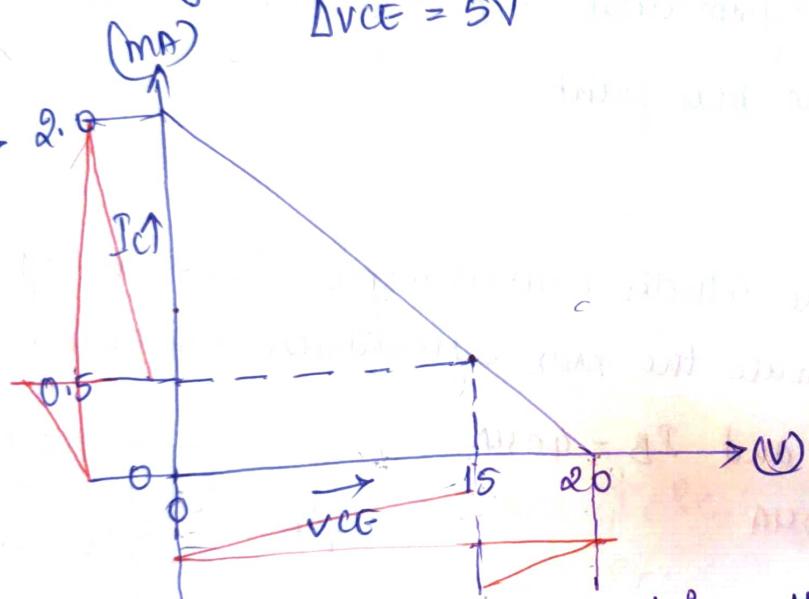
(8)

Selection of Q point

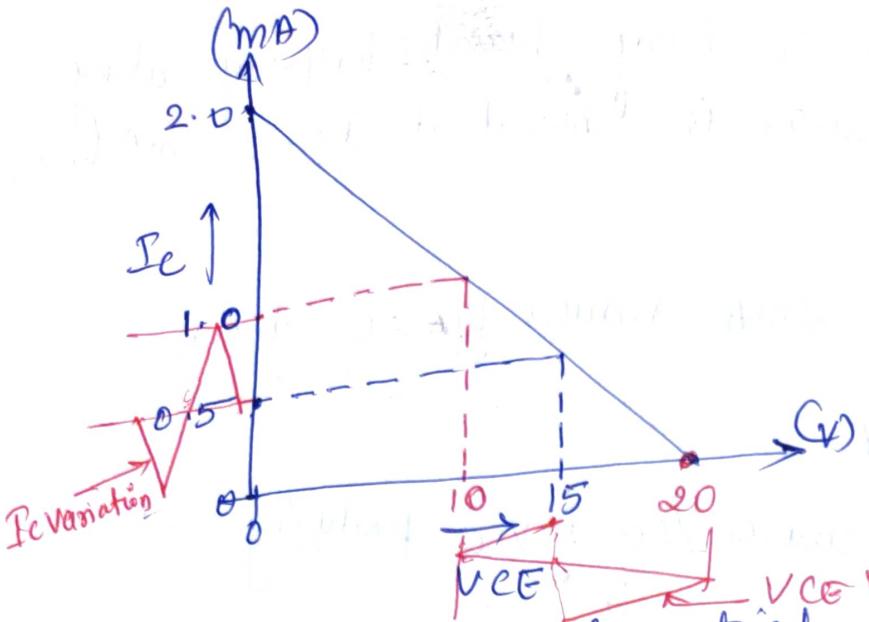
Suppose that instead of being biased halfway along the load line, the transistor is biased at $I_C = 0.5 \text{ mA}$ and $V_{CE} = 15V$

→ Increasing the I_C to 2mA reduces $V_{CE} = 0$ giving $\Delta V_{CE} = -15V$

→ Reducing $I_C \rightarrow 0$ increases V_{CE} to V_{CE} producing $\Delta V_{CE} = 5V$



- When used as an amplifier, the transistor off V_{CE} must swing up and down by equal amounts
- ie the off V_{CE} swing must be symmetrical above and below the bias point.
- So asymmetrical swing of $-15V$ and $+5V$ is unsuitable.
- If I_C is driven up and down by $\pm 0.5 \text{ mA}$, a symmetrical off V_{CE} swing of $\pm 5V$ is obtained.

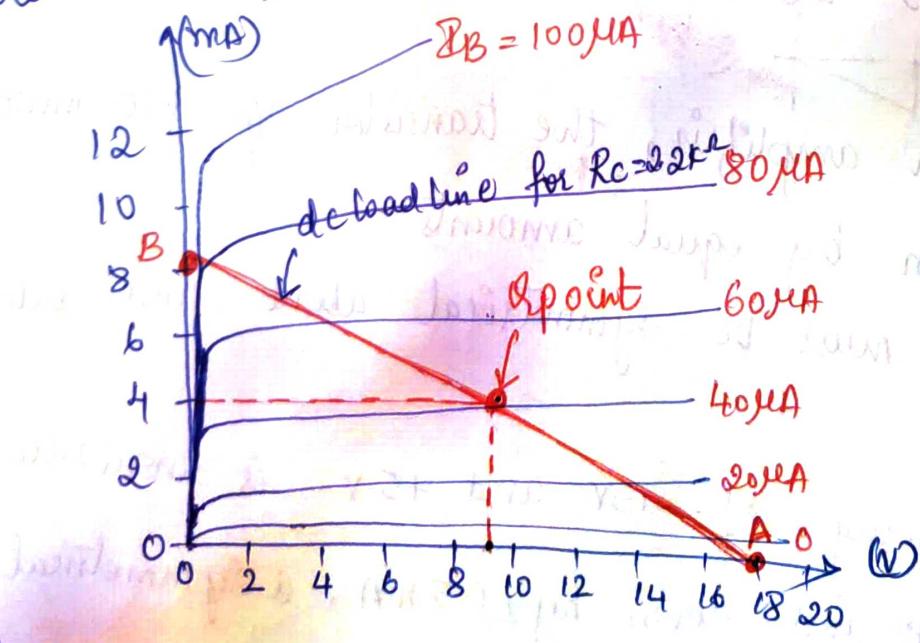


→ This is the maximum symmetrical o/p voltage swing that can be achieved with the bias point

Numericals

① The transistor ekt has the collector characteristics shown in fig. Determine the Qpt and estimate the max symmetrical o/p swing.

Note $V_{cc} = 18V$, $R_c = 2.2k\Omega$ and $I_B = 40\mu A$

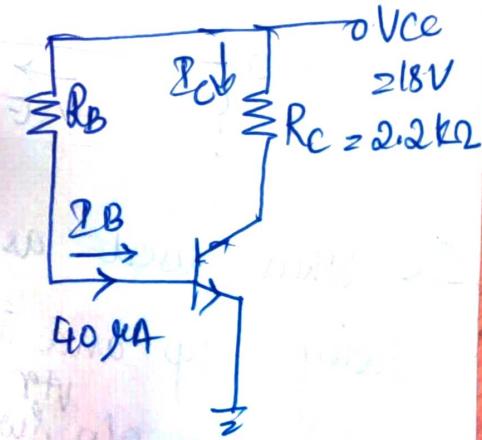


$$\text{Soln: } V_{CE} = V_{CC} - I_C R_C$$

When $I_C = 0$,

$$V_{CE} = V_{CC} \Rightarrow 18V$$

→ Draw the de-load line through A and B. The Qpt at the intersection of load line and $I_B = 40\mu A$. ∴ $I_C \approx 4.1mA$ and $V_{CE} \approx 9V$, $\Delta V_{CE} \approx \pm 9V$



When $V_{CE} = 0$,

$$0 = V_{CE} - I_C R_C$$

$$V_{CE} = I_C R_C$$

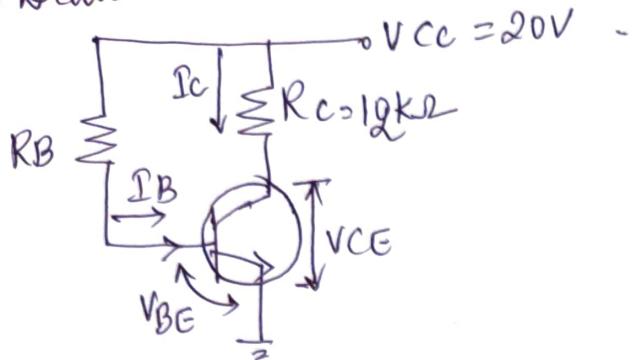
$$I_C = \frac{V_{CC}}{R_C}$$

$$I_C = \approx 8.2 \text{ mA}$$

load line and Q point numericals

8-a

Draw the dc load line for the circuit below when $R_C = 12k\Omega$



Soln When $I_B = 0$, $I_C = 0$.

$$\text{we have } V_{CC} = I_C R_C + V_{CE} \quad \rightarrow \quad (1)$$

$$V_{CE} = V_{CC} - I_C R_C \quad \rightarrow \quad (2)$$

$$V_{CE} = V_{CC} - 0$$

$$\boxed{V_{CE} = 20V}$$

Now fix a point 'A' on $I_C = 0$ and $V_{CE} = 20$.

→ When $V_{CE} = 0$.

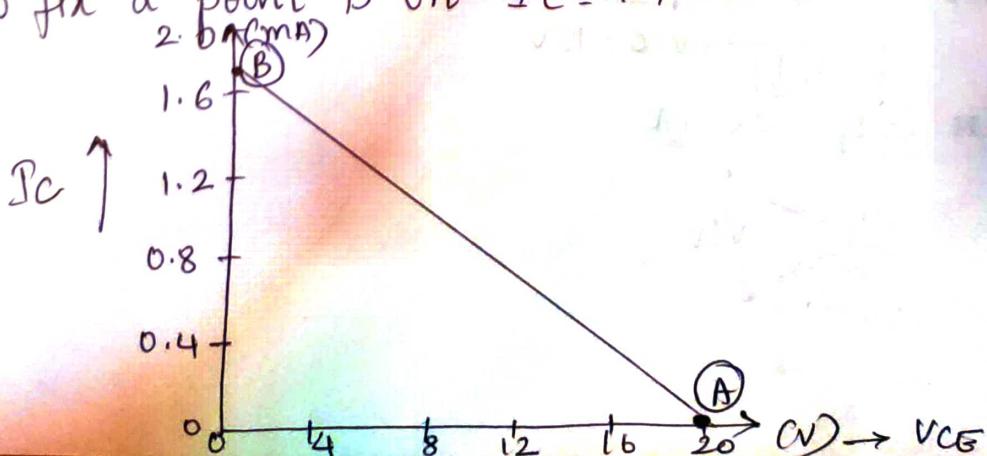
$$\text{from Eqn (1)} \rightarrow 0 = V_{CC} - I_C R_C$$

$$V_{CC} = I_C R_C$$

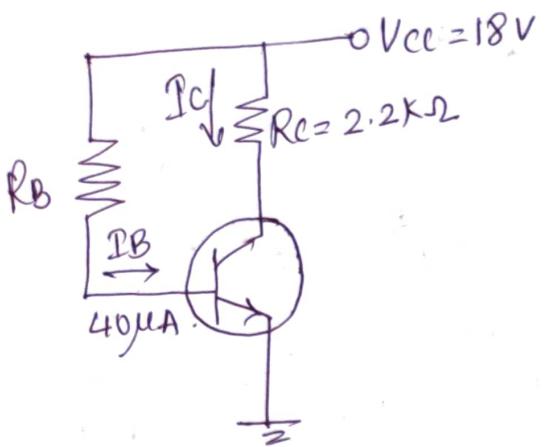
$$I_C = \frac{V_{CC}}{R_C} = \frac{20}{12000}$$

$$\boxed{I_C = 1.7 \text{ mA}}$$

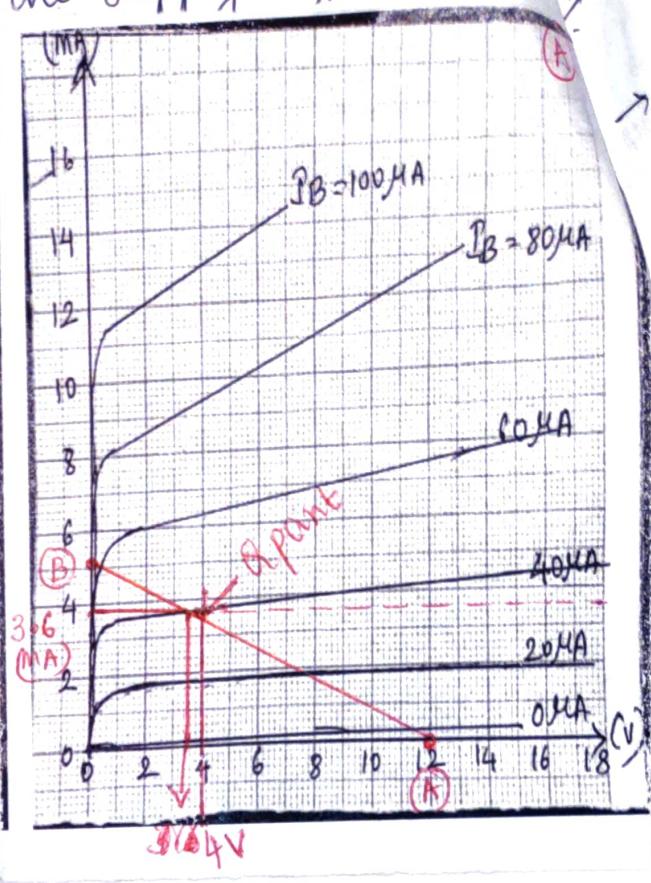
→ Now fix a point 'B' on $I_C = 1.7 \text{ mA}$ and $V_{CE} = 0$.



② Draw the dc load line and determine the Q point
the ckt shown below, when the supply V_{CC} is 12V.



(Graph)



$$\text{Soln : } V_{CC} = V_{CE} - I_C R_C \quad \text{(1)}$$

since $I_C = 0$, $V_{CE} = V_{CC}$ and Q-point

$$V_{CE} = 12V$$

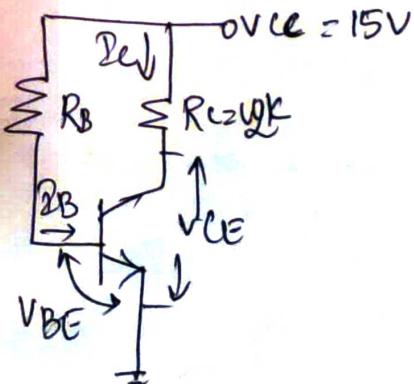
→ Now Consider $V_{CE} = 0$. in (1)

$$\therefore I_C = \frac{V_{CC}}{R_C}, I_C = 5mA$$

\therefore Q point @ $40\mu A \rightarrow 4V$ and $I_C = 3.6mA$

③ A Common emitter shown in fig has $R_C = 12k\Omega$ and $V_{CC} = 15V$
Draw DC load line on the characteristics below. Specify the
Q point and determine the max dyn off V_{TG} swing if the
base current is $10\mu A$. [Graph B]

④ transistor



$\rightarrow g_f @ I_C = 0$

$$V_{CC} = V_{CE}$$

$$V_{CE} = 15V$$

Pt A

$\rightarrow @ V_{CE} = 0$

$$V_{CE} = V_{cc} - I_c R_e$$

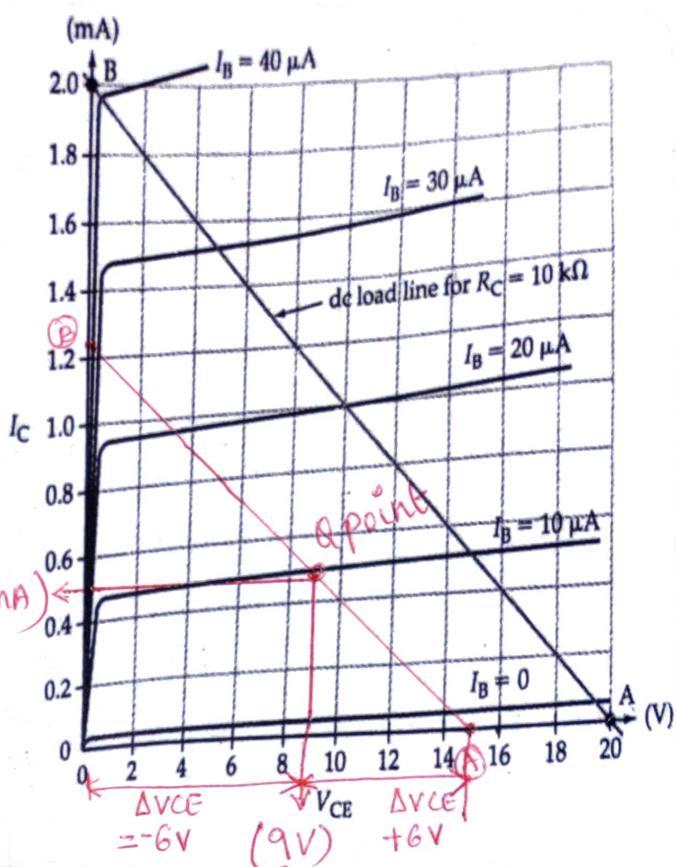
$$0 = V_{cc} - I_c R_e$$

$$I_c = \frac{V_{CC}}{R_e}$$

$$I_c = 1.25 \text{ mA}$$

(0.5mA)

Q point



from the graph, we get, @ Qpoint for

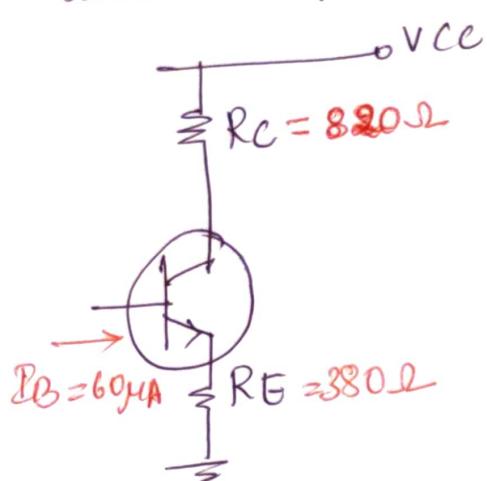
$$I_B = 10 \mu\text{A}, I_C = 0.5 \text{ mA} \text{ and } V_{CE} = 9V$$

$$\Delta V_O \Rightarrow 9 - 15 = -6V \quad \text{and} \quad 15 - 9 = +6V$$

$$\therefore V_O \approx \pm 6V$$

Cletana Gosai S
Asst Prof, ECE

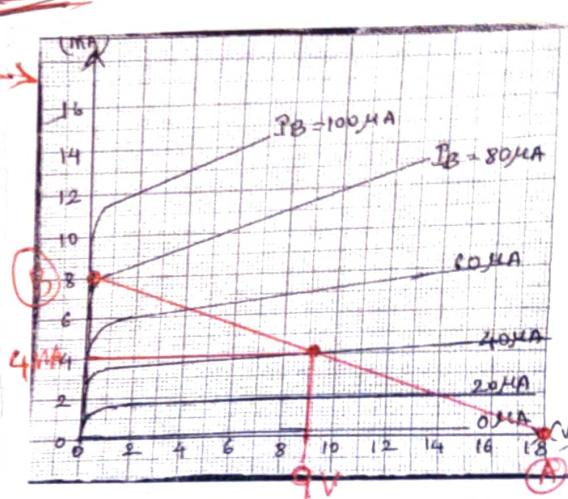
④ A transistor ckt as shown has $V_{CE} = 12V$, $R_C = 820\Omega$ and $R_E = 380\Omega$ and $I_B = 60\mu A$. Draw AC load line and determine symmetrical Q-point voltage. (graph A)



(Initially consider Q-point is at $I_B = 40\mu A$)

* When $I_B = 40\mu A$, $P_{TA} = 18V$ and
* $P_{TB} = 8mA$, @ Qpt = $40\mu A$,
 $V_{CE} = 9V$ and $I_C = 4mA$.

Initial graph



Soln for Convenience P_E is taken $P_C \rightarrow *$

$$\text{we have } V_{CC} = I_C R_E + V_{CE} + I_E R_E$$

$$V_{CC} = I_C R_E + V_{CE} + I_C R_E$$

$$V_{CC} = I_C [R_E + R_C] + V_{CE}$$

$$V_{CE} = V_{CC} - I_C [R_E + R_C]$$

①

A (Soln for given Specification)

② $I_C = 0$

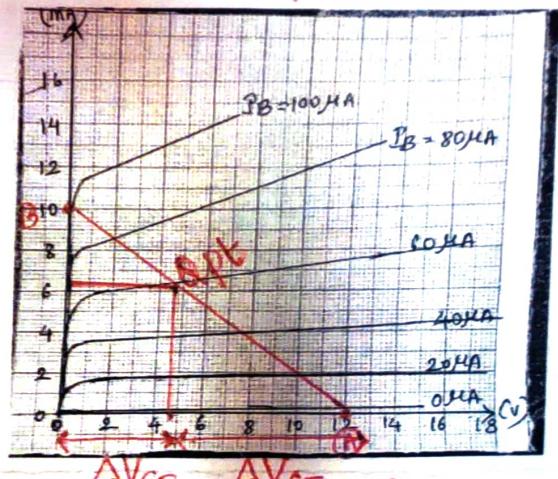
$$V_{CG} = V_{CC}$$

$$\boxed{V_{CE} = 12V} \quad \text{PT A}$$

③ $V_{CE} = 0 \Rightarrow V_{CC} = I_C [R_E + R_C]$

$$I_C = \frac{V_{CC}}{(R_E + R_C)}$$

$$\boxed{I_C = 10mA} \quad \text{PT B}$$



obtained from $I_B = 40\mu A$.

→ Q-point = 6.25mA and 4.5V.

$$\Delta V_o \approx \pm 4.5V \quad \therefore \Delta V_o = 4.5 - 9V = -4.5V$$

$$\text{and } 9V - 4.5 = +4.5V$$

BASE BIAS

8-c

→ Circuit operation and Analysis :

→ The transistor bias arrangements are as shown.

→ It is known as base bias or fixed current bias.

→ The base current is a constant quantity determined by supply vtg V_{CC} and base resistor R_B .

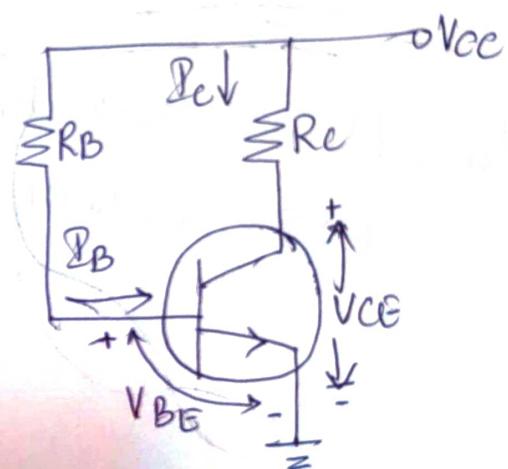
→ Because V_{CE} and R_B are constant quantities, I_B remain fixed at particular level.

→ From figure,

$$V_{CC} = I_B R_B + V_{BE} \quad \text{--- (1)}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{--- (2)}$$



where V_{BE} → base emitter vtg (0.7V for silicon and 0.3V for germanium)

→ The transistor Collector Current is calculated as,

$$I_C = \beta I_B \quad \text{--- (3)} \quad \boxed{I_C = h_{FE} I_B}$$

where, where h_{FE} is the another symbol of β [collector current gain] used in transistor data sheets.

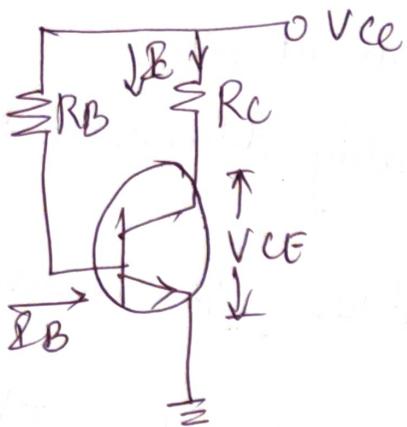
→ We have, $V_{CC} = I_C R_C + V_{CE}$ (from fig)

$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- (4)}$$

→ thus when the supply vtg and component values are known a base bias circuit is easily analysed to determine the circuit current and voltage levels.

⑤ Plot the dc load line for the fig and characteristics curve when $V_{CC} = 15V$, $R_C = 7.5k\Omega$, (b) when $V_{CC} = 12V$ and $R_C = 8k\Omega$. Specify Q point in each case if $I_B = 20\mu A$ and maximum symmetrical o/p voltage for each.

(Graph c)



A Case(i) @ $I_C = 0$

$$V_{CC} = V_{CE} + I_C R_C \rightarrow 0$$

$$V_{CC} = V_{CE} = 15V \rightarrow \text{pt(A)}$$

$$\text{Case(ii)} V_{CE} = V_{CC} - I_C R_C$$

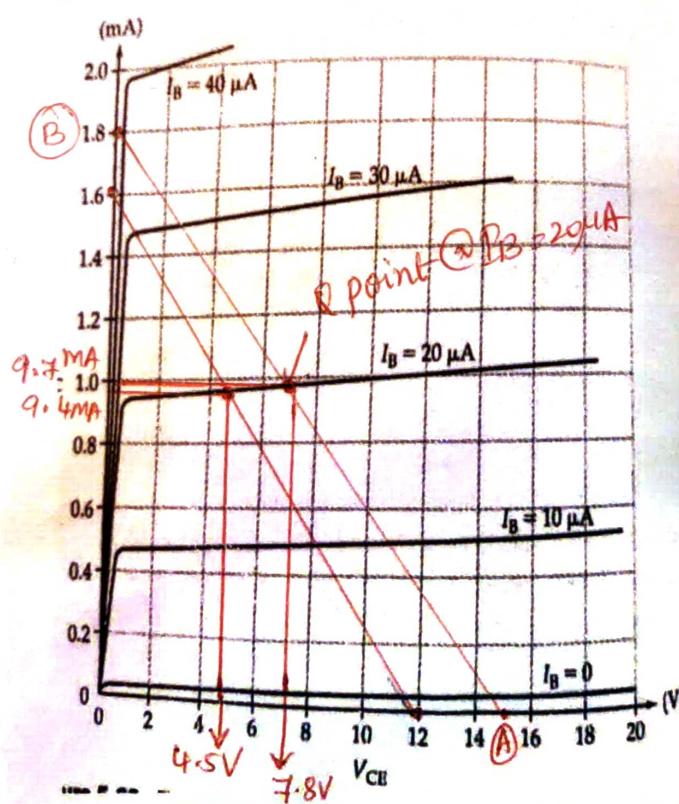
$$0 = V_{CC} - I_C R_C$$

$$V_{CC} = I_C R_C$$

$$I_C = \frac{15}{8K} = 1.8mA \downarrow \text{pt(B)}$$

Soln : (a) $I_C = 0.97mA$ and $V_{CE} = 7.8V$.

(b) $I_C = 0.94mA$ and $V_{CE} = 4.5V$.



C (b) @ $I_C = 0$

$$V_{CE} = V_{CC} = 12V$$

@ $V_{CE} = 0$

$$V_{CC} = I_C R_C$$

$$I_C = \frac{12}{7.5K} = 1.6mA$$

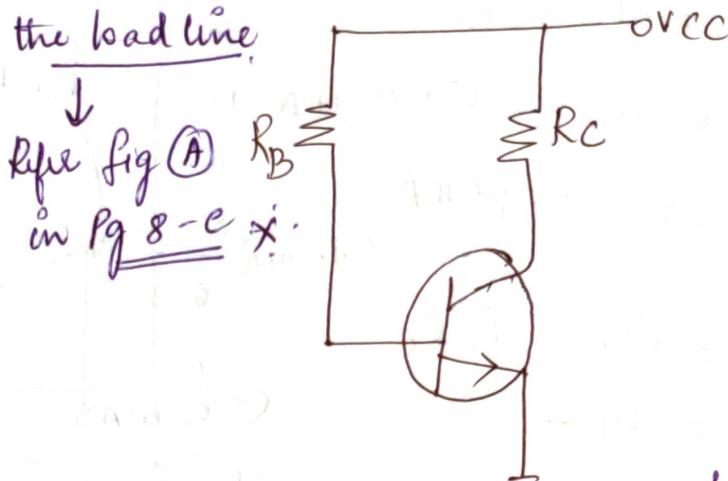
Numericals *

The base bias ckt in fig has $R_B = 470 \text{ k}\Omega$, $R_C = 2.2 \text{ k}\Omega$ and $V_{CC} = 18V$ and transistor has $hFE = 100$. Determine I_B , I_C and V_{CE} . Draw the load line.

$$\text{Soln } I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{18 - 0.7}{470}$$

$$I_B = 36.8 \mu\text{A}$$



→ Calculate the max & min levels of I_C and V_{CE} for the base bias circuit when $hFE(\min) = 50$ and $hFE(\max) = 200$.

$$\rightarrow I_C = hFE \times I_B$$

$$= 100 \times 36.8 \mu\text{A}$$

$$I_C = 3.68 \text{ mA}$$

$$\rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$= 18 - [3.68 \text{ mA} \times 2.2 \text{ k}\Omega]$$

$$V_{CE} = 9.9 \text{ V}$$

NOTE : Transistors of a given type always have a wide range of hFE values. So, $hFE(\max)$ and $hFE(\min)$ should be always used for practical ckt analysis.

② A base bias circuit has $V_{CC} = 24V$, $R_B = 390 \text{ k}\Omega$, $R_C = 3.3 \text{ k}\Omega$ and $V_{CE} = 10V$. Calculate hFE . Determine the new V_{CE} if $hFE = 100$.

$$\text{Soln } I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B = \frac{24 - 0.7}{390 \text{ k}\Omega} \Rightarrow 0.00358 \text{ A} \Rightarrow 0.00358 \text{ A}$$

$$0.00358 \text{ A} = 0.00358 \text{ A}$$

$$0.00358 \text{ A} = 0.00358 \text{ A}$$

We have, $V_{CE} = V_{CC} - I_C R_C$ or $V_{CC} = V_{CE} + I_C R_C$.

$$V_{CC} - V_{CE} = I_C R_C = 0.00358 \text{ A} \times 3.3 \text{ k}\Omega$$

$$I_C = hFE \times I_B$$

$$hFE = \frac{I_C}{I_B}$$

$$= hFE = 71.00$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{24 - 10}{3.3 \text{ k}\Omega}$$

$$I_C = 0.004242 \text{ A} \approx 4.242 \text{ mA}$$

→ Now $hFE = 100$

$$I_C = hFE \times I_B$$

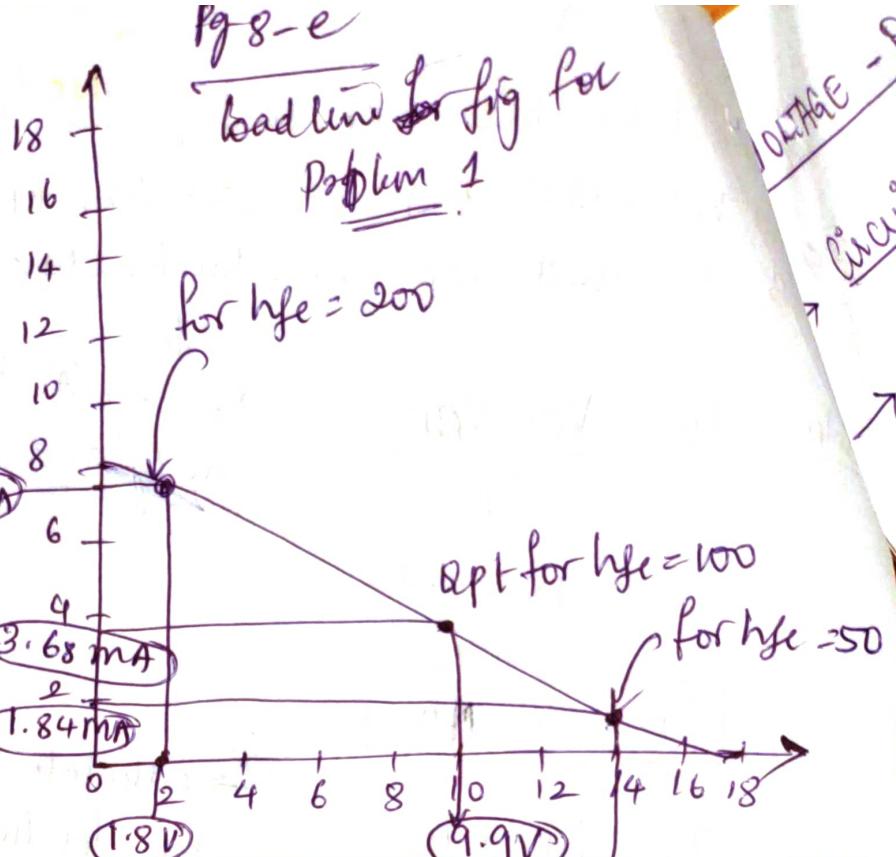
$$I_C = 100 \times 0.5974 \text{ mA}$$

$$I_C = 5.97 \text{ mA}$$

$$V_{CG} = V_{CC} - I_C R_C$$

$$= 24 - (5.97 \text{ mA})$$

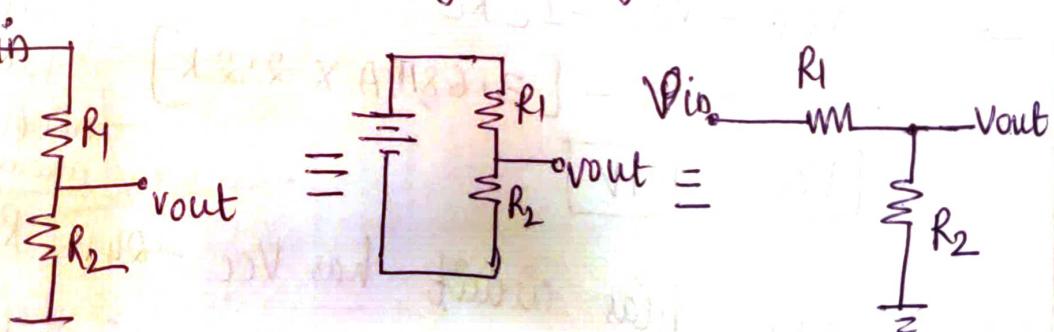
$$V_{CE} = 4.28 \approx 4.2$$



Additional Information ✤ [Voltage Divider Ckt]

→ Voltage divider ckt converts/tuns large Voltage to smaller one

→ Consider the ckt,



→ From the ckt, Acc to ohms law,

$$V_{out} = R_2 \cdot I_2 \quad \text{--- ①}$$

→ Assuming $I_1 = I_2 = I$ we get

$$V_{in} = I \times R \text{ ie } I = \frac{V_{in}}{R} \quad \text{--- ②}$$

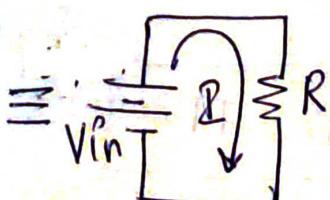
$$I = \frac{V_{in}}{R_1 + R_2} \quad \text{--- ③}$$

Since $I_2 = I$, we get

$$V_{out} = R_2 \cdot \frac{V_{in}}{R_1 + R_2}$$

$$\text{ie } V_{out} = \frac{R_2 \times V_{in}}{R_1 + R_2}$$

∴ $V_{in} = V_{tg}$ across both the resistors R_1 and R_2 . [R_1 & R_2 are in series]
ie $R = R_1 + R_2$



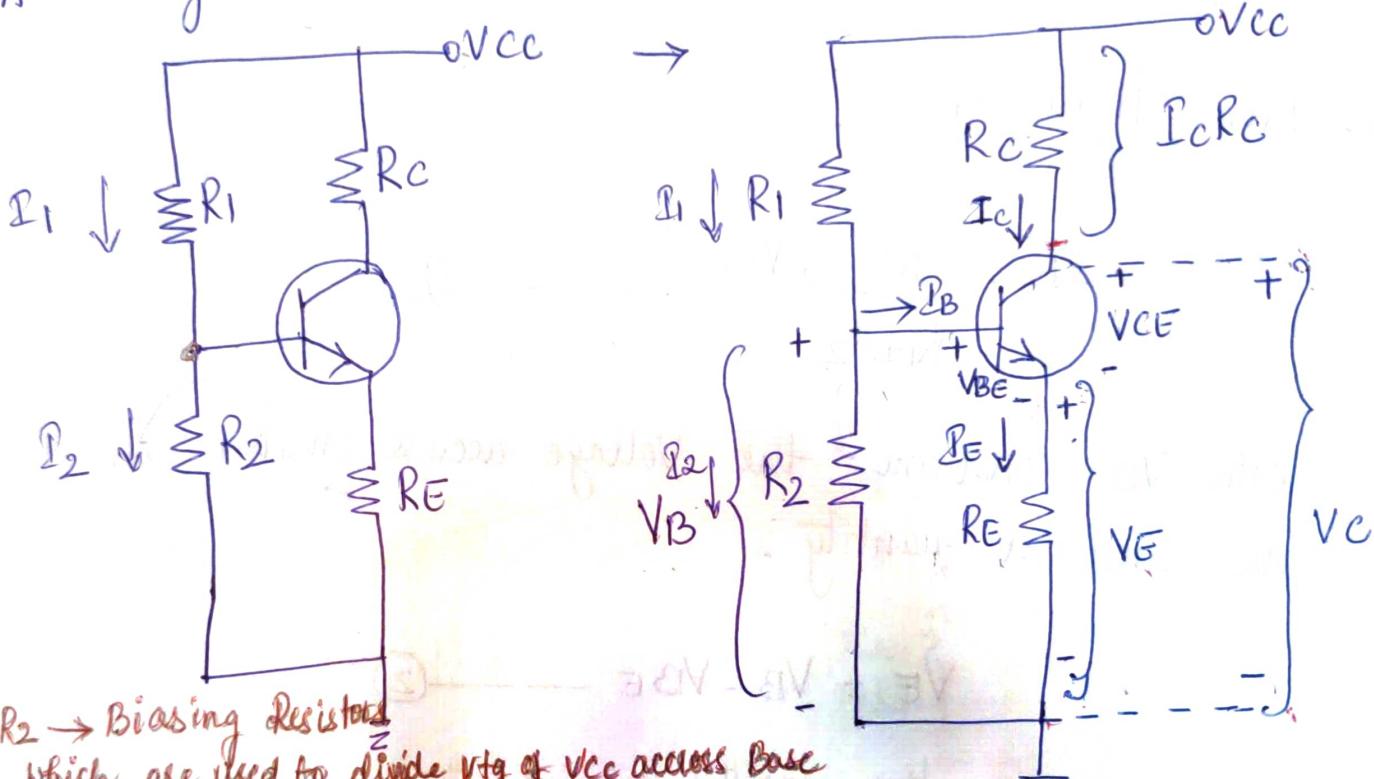
VOLTAGE-DIVIDER BIAS :- [APPROXIMATE METHOD NOT IN SYLLABUS]

Ques
⑨

→ Circuit operation :- ★★ (Approximate)

→ Voltage divider is the most stable of the three basic transistor bias circuits.

→ A voltage divider bias ckt is as shown:-



R_1 and R_2 → Biasing resistors

∴ Which are used to divide V_{CC} across Base

① → Voltage divider bias ckt

(b) Circuit currents and V_{tg} drops.

- It is seen that, like R_C , there is emitter resistance R_E connected in series with the transistor.
- The total de load in series with the transistor is $(R_C + R_E)$ and this total resistance must be used when drawing the de load line for the circuit.
- Resistors R_1 and R_2 constitute a V_{tg} divider that divides the supply voltage to produce the base bias voltage (V_B)

- Voltage divider bias circuits are normally designed to have the voltage divider current (I_2) very much larger than the transistor base current (I_B).
- In this situation, V_B is largely unaffected by I_B , so V_B can be assumed to remain constant.
- From figure 2,

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad \text{--- (1)}$$

With V_B constant, the voltage across emitter resistor is also constant quantity.

$$\therefore V_E = V_B - V_{BE} \quad \text{--- (2)}$$

This means the emitter current is constant.

i.e. $I_E = \frac{V_E}{R_E} \Rightarrow \frac{V_B - V_{BE}}{R_E} \quad \text{--- (3)}$

The collector current is approximately equal to emitter current so, I_C is held at constant level.

- Again referring to fig (2),

$$V_C = V_{CC} - I_C R_C \quad \text{--- (4)}$$

and the collector emitter voltage is

$$V_{CE} = V_C - V_E \quad \text{--- (5) } \star\star$$

V_{CE} can also be determined as,

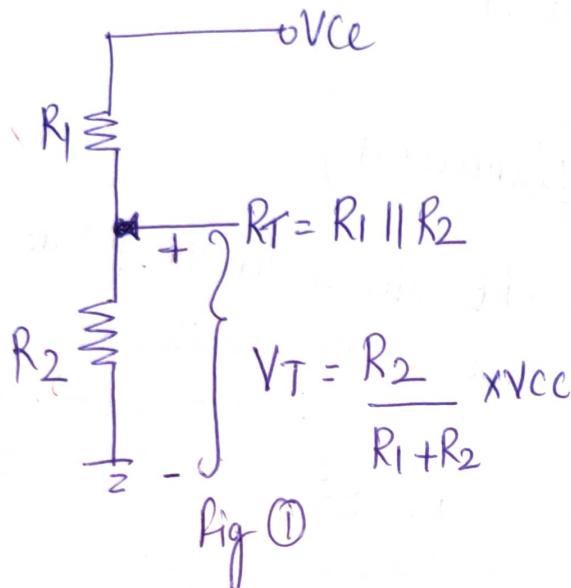
$$V_{CE} \approx V_{CC} A_{DC} R_C + V_E R_E$$

$$V_{CE} \approx V_{CC} - I_C (R_C + R_E) \quad \text{--- (6)}$$

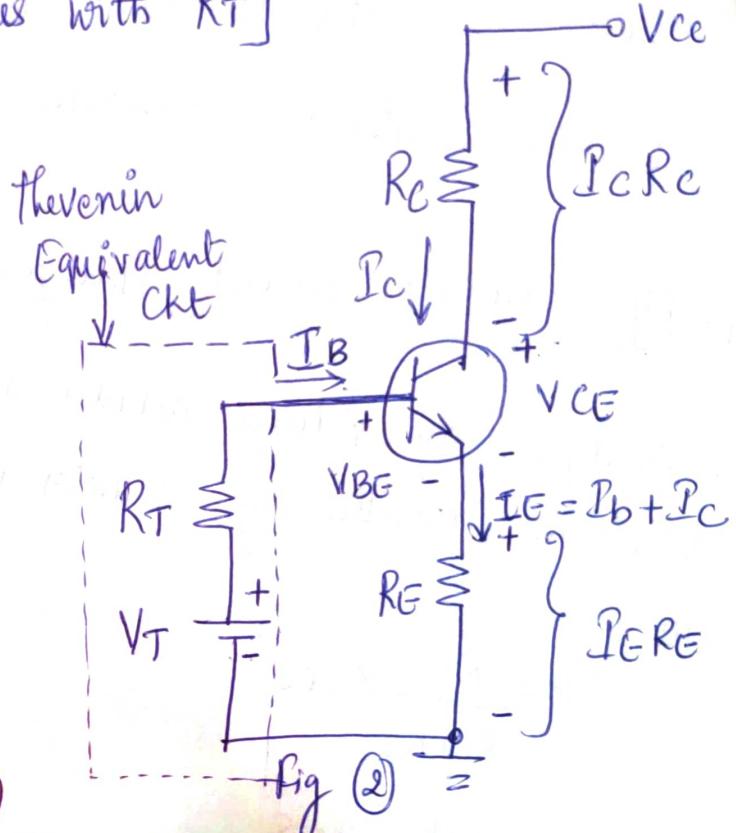
Clearly with I_C and R_E constant, the transistor collector emitter V_{tg} remains constant.

Precise Circuit Analysis [Accurate]

To analyse a voltage divider bias circuit precisely, the voltage divider must be replaced with its Thvenin equivalent ckt. [V_T in series with R_T]



$$\rightarrow V_T = V_{CC} \times \frac{R_2}{R_1 + R_2} \quad \text{--- ①}$$



$\rightarrow R_T$ is calculated as R_1 in parallel with R_2 .

$$R_T = R_1 \parallel R_2$$

\rightarrow Referring to figure 2, we can write the following equation for the voltage drops around the base-emitter ckt,

$$V_T = I_B R_T + V_{BE} + I_E R_E$$

$$V_T = I_B R_T + V_{BE} + R_E (I_B + I_C) \quad \text{--- ②}$$

Substituting $I_C = h_{FE} I_B$,

$$V_T = I_B R_T + V_{BE} + R_E (I_B + h_{FE} I_B)$$

(11)

$$\rightarrow V_T = I_B R_T + V_{BE} + R_E I_B (1 + h_{FE})$$

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})}$$

→ Once I_B has been determined, I_C can be calculated from the appropriate h_{FE} value and the transistor terminal voltages can be calculated.

★ ★ Transistor H_{FE} or h_{fe} are often quoted as the current gain. It is the forward transfer characteristic. ie transistor gain when used in the common emitter mode

→ It is same as the transistor β

$$\text{ie } \beta = \frac{I_C}{I_B}$$

if

$$h_{fe} = \frac{I_C}{I_B}$$

or

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Problem:

→ Accurately analyse the Voltage divider bias circuit in the Ckt to determine I_C , V_G , V_C and V_{CE} when $h_{FE} = 100$. (Refer Fig A in Approximate Ckt analysis section) ★. Draw the P_C load line.

Soln.

$$V_{IP} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$\rightarrow R_T = R_1 \parallel R_2$$

$$= 33k \parallel 12k$$

$$V_T = \frac{12k}{33k + 12k} \times 18$$

$$R_T = \frac{33k \times 12k}{33k + 12k}$$

$$\boxed{V_T = 4.8V}$$

$$\boxed{R_T = 8.8k\Omega}$$

$$\rightarrow V_T = I_B R_T + V_{BE} + R_E I_B (1 + h_{FE})$$

(ii)

$$I_B = \frac{V_T - V_{BE}}{R_T + R_E (1 + h_{FE})}$$

→ Once I_B has been determined, I_C can be calculated from the appropriate h_{FE} value and the transistor terminal voltages can be calculated.

★ ★ [Transistor H_{FE} or h_{fe} are often quoted as the current gain. It is the forward transfer characteristic. ie transistor gain when used in the common emitter mode ie transistor gain when used in the common emitter mode]

→ It is same as the transistor β

$$\text{ie } \beta = \frac{I_C}{I_B} \quad \text{if } h_{fe} = \frac{I_C}{I_B} \quad \text{or } \beta = \frac{\Delta I_C}{\Delta I_B}$$

Problem:

→ Accurately analyse the Voltage divider bias circuit in the ckt to determine I_C , V_G , V_C and V_{CE} when $h_{FE} = 100$.
 (Refer Fig A in Approximate Ckt analysis section) *

Draw the DC load line.

Soln.

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$V_T = \frac{12K}{33K + 12K} \times 18$$

$$V_T = 4.8V$$

$$\begin{aligned} \rightarrow R_T &= R_1 \parallel R_2 \\ &= 33K \parallel 12K \end{aligned}$$

$$R_T = \frac{33K \times 12K}{33K + 12K}$$

$$R_T = 8.8K\Omega$$

load line analysis

$$\rightarrow I_B = \frac{V_T - V_{BE}}{R_T + R_E (1+hFE)}$$

$$= \frac{4.8V - 0.7V}{8.8K + 1K (1+100)}$$

$$\boxed{I_B = 37.3 \text{ mA}}$$

$$\rightarrow \text{we have } hFE = \frac{I_C}{I_B}$$

$$\therefore I_C = hFE \times I_B \\ = 100 \times 37.3 \text{ mA}$$

$$\boxed{I_C = 3.73 \text{ mA}}$$

$$\rightarrow I_E = I_B + I_C$$

$$I_E = 37.3 \text{ mA} + 3.73 \text{ mA}$$

$$\boxed{I_E = 3.77 \text{ mA}}$$

$$\rightarrow V_E = I_E R_E$$

$$= 3.77 \text{ mA} \times 1K$$

$$\boxed{V_E = 3.77V}$$

$$\rightarrow V_C = V_{CC} - (I_C R_C)$$

$$= 18 - (3.73 \text{ mA} \times 1.2 \text{ k}\Omega)$$

$$\boxed{V_C = 13.52V}$$

$$\rightarrow V_{CE} = V_C - V_E \\ = 13.52 - 3.77$$

$$\boxed{V_{CE} = 9.75V}$$

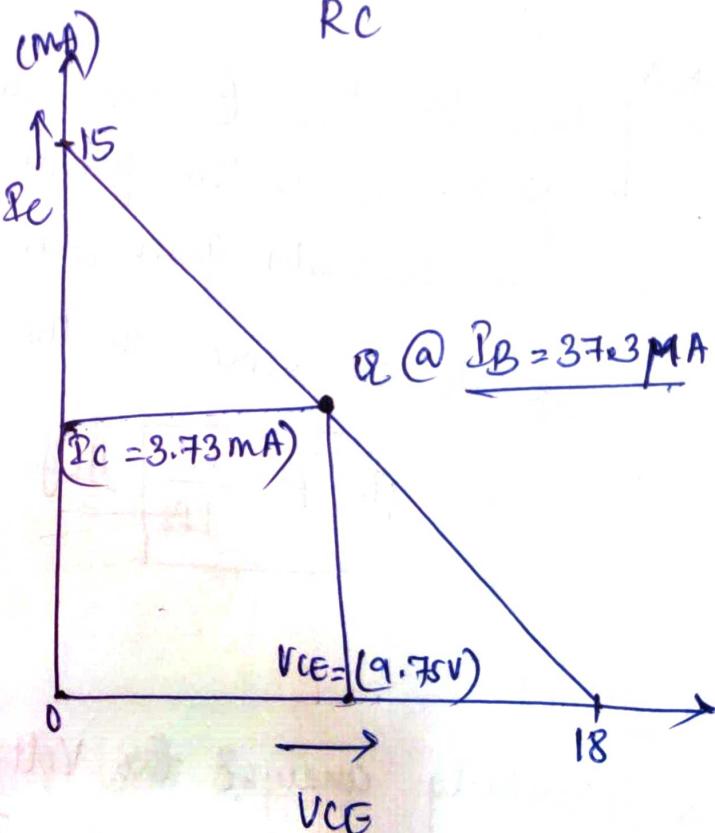
Case (i) @ $I_C = 0$

$$V_{CG} = V_{CC} - I_C R_C$$

$$\boxed{V_{CE} = V_{CC}} \rightarrow 18V$$

Case (ii) @ $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C} \Rightarrow 15 \text{ mA}$$



(a) $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$
 $V_{CE} - I_C R_C = V_{CE} + I_E R_E$
 If $I_C = I_E$ then
 $V_{CE} = V_{CC} - I_C [R_C + R_E]$

Practice Problems

① Accurately analyse the VTG divider bias ckt for the Fig A of previous section for the conditions

$$(i) h_{FE}(\min) = 50 \quad (\text{Ans } V_{CE} = 10.4V)$$

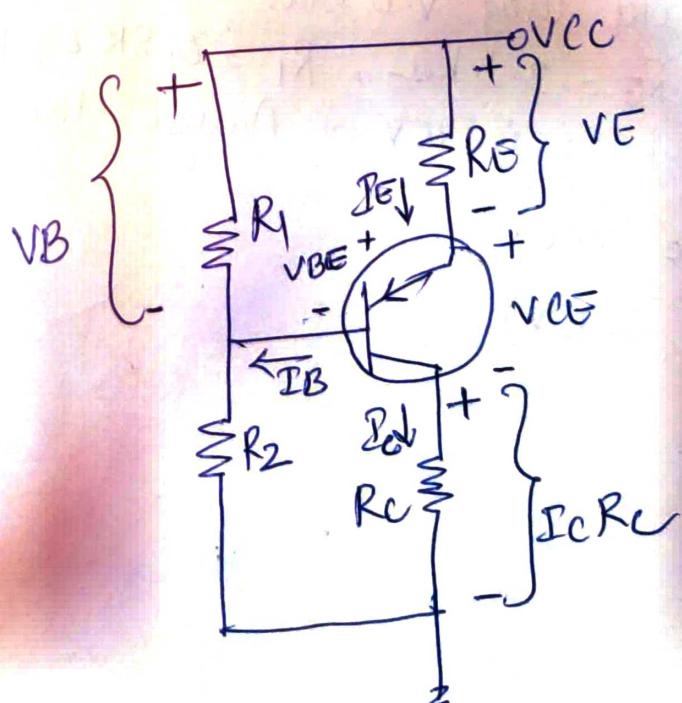
$$(ii) h_{FE}(\max) = 200. \quad (\text{Ans } V_{CE} = 9.4V)$$

② In a VTG divider bias ckt (Fig A), $V_{CC} = 24V$, $R_1 = 180k\Omega$, $R_2 = 56k\Omega$, $R_E = 4.7k\Omega$ and $R_C = 8.2k\Omega$. Calculate the approximate levels of I_c , V_E , V_C and V_{CE} .

③ In the above problem, ~~use~~ the ckt uses a transistor with $h_{FE}(\min) = 75$ and $h_{FE}(\max) = 250$. Accurately analyse a ckt to determine the max and min levels of V_{CE} .

④ In the VTG divider ckt, $V_{CE} = 20V$, $R_1 = 33k\Omega$, $R_2 = 100k\Omega$, $R_E = 3.9k\Omega$, and $R_C = 6.8k\Omega$. Calculate approximate levels of V_E and V_C

Ans
 $V_B = 5.69V$



- ★ ⑤ The V_{TG} divider bias ckt in Fig has $V_{CC} = 15V$, $R_1 = 6.8k\Omega$, $R_2 = 3.3k\Omega$, $R_3 = 900\Omega$ and $R_4 = 900\Omega$. and $hFE = 50$. Analyse the ckt approximately to determine the levels of I_C and V_{CE} .
- (Ans : $4.7mA$, $6.5V$)

- ⑥ Precisely analyse the ckt in problem ⑤ to determine R_{load} , the max level of I_C and V_{CE} when $hFE(\max) = 60$.

- ⑦ A V.D Bias ckt with a $25V$ supply has $R_E = 4.7k\Omega$, $R_E = 3.3k\Omega$, $R_1 = 33k\Omega$, $R_2 = 12k\Omega$ and $hfe = 50$. Use approx analysis method to calculate the V_{CE} level.
- (Ans : $10.6V$)

- ⑧ A transistor ckt using V.D Bias has the following components $R_C = 2.2k\Omega$, $R_E = 3.3k\Omega$, $R_1 = 6.8k\Omega$, $R_2 = 4.7k\Omega$. The Supply V_{TQ} is $15V$. Analyse the ckt approximately to determine V_{CE} .
- (Ans : $5.93V$)

