Soft Error Masking Circuit and Latch Using Schmitt Trigger Circuit

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Abstract

In recent high-density and low-power VLSIs, soft errors occurring on not only memory systems and the latches of logic circuits but also the combinational parts of logic circuits seriously affect the operation of systems. The conventional soft error tolerant methods for soft errors on the combinational parts do not provide enough high soft error tolerant capability with small performance penalty. This paper proposes a class of soft error masking circuits by using a Schmitt trigger circuit and pass transistors. The paper also presents construction of soft error masking latches (SEM-Latches) capable of masking transient pulses occurring on combinational circuits. Moreover, experimental results show that the proposed method has higher soft error tolerant capability than the existing methods. For driving voltage VDD=3.3V, the proposed method is capable of masking transient pulses of magnitude 4.0V or less.

1. Introduction

In recent high-density and low-power VLSIs, soft errors frequently occur. Soft errors are resulted from radiation-induced transient pulses caused by neutrons from cosmic rays and alpha particles from packaging material [1]. Traditionally, soft errors occurring on memory system and latches in logic circuits seriously affect the operation of VLSI systems. Error correcting (control) codings (ECCs) are important soft error tolerant methods for memory system and were studied by many researchers [2]. Many soft error tolerant methods for soft errors occurring on latches in logic circuits were also proposed, e.g. [3-6].

In recent VLSI systems, soft errors occurring on combinational parts of logic circuits also become a substantial problem. Based on this viewpoint, many soft error tolerant methods [7-10] and soft error analysis methods [11] for soft errors occurring on combinational parts of logic circuits were proposed. In [7], time redundancy method is proposed by Nicolaidis. In [8], Delay-Assignment-Variation (DAV) based optimization method is proposed by Dhillon. The soft error propagation to the primary outputs can be minimized by adding optimal amounts of capacity to the primary outputs. Therefore, in this method, the size, supply voltages and threshold voltages of internal gates are chosen to minimize the energy and delay overhead due to the added capacities. However, these methods bring to performance penalty. Another method was proposed by Kumar and Tahoori [9, 10]. This method uses pass transistor as low pass filter and is capable of reducing the magnitude of transient pulses. However, the peak voltage of transient pulses due to a particle strike will become bigger than the driving voltage in the future. In this condition, the method cannot mask soft errors enough.

This paper proposes a soft error masking circuit for masking soft errors i.e. drastically reducing the magnitude of the transient pulses with a little performance penalty. Even if the peak voltage of transient pulses exceeds the driving voltage, the proposed circuit can mask soft errors. The circuit uses a Schmitt trigger circuit and a pass transistor. This paper also

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presents construction of a soft error masking latch (SEM-Latch) capable of masking transient pulses occurring on combinational circuits.

The rest of this paper is organized as follows: Section 2 is preliminary. Section 3 explains the proposed soft error masking circuit and SEM-Latch, and the experimental results are given in Sect. 4. Finally, Sect. 5 concludes the paper.

2. Preliminary

2.1. Related Work

A method reducing the magnitude of transient pulses occurring on combinational parts of logic circuits has been proposed in [9]. Figure 1 shows an example of a circuit reducing the magnitude of transient pulses shown in [9]. In the method, multiple pass transistors are connected in series. The pass transistors are always conducting, i.e. the gates of the PMOS and NMOS transistors in the pass transistors are permanently connected to ground and VDD, respectively. Those pass transistors work as low pass filters.

While data signals can pass through the circuit with little change, the magnitude of transient pulses are reduced by the circuits. The two pass transistors make the technology the most efficient, under the condition that the size of the back pass transistor is four times larger than that of the front one shown in Fig. 1. In this case, the magnitude of transient pulses are reduced to about 40%. Unfortunately, the method cannot reduce the magnitude of transient pulses enough, especially when the transient pulses with large magnitude occur.

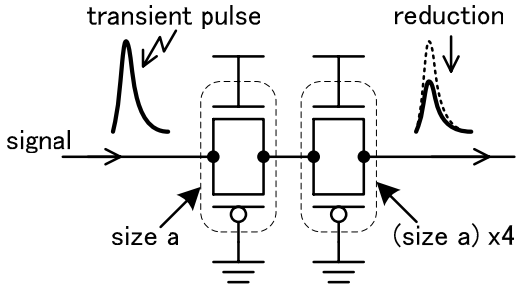


Figure 1. Circuit reducing magnitude of transient pulses using pass transistors

2.2. Schmitt Trigger Circuit

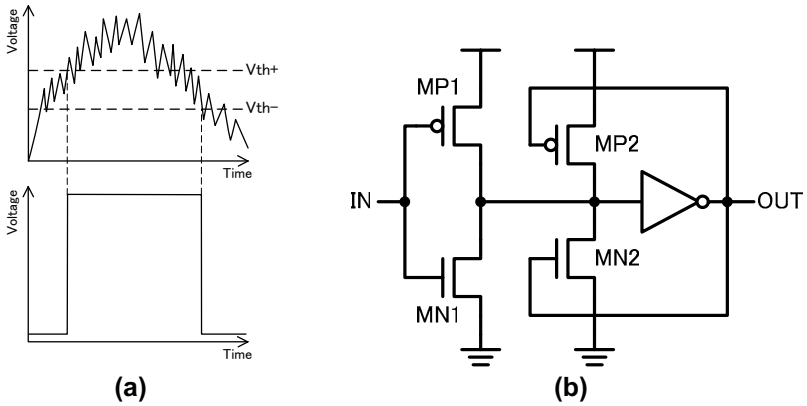


Figure 2. Schmitt trigger circuit

Schmitt trigger circuits are mainly used to eliminate chattering in A/D converters. As shown in Fig. 2(a), Schmitt trigger circuits have hysteresis property, i.e. the following two threshold voltages; a rising input threshold voltages Vth+ and a falling input threshold voltages Vth-. The output voltage can change from low to high only when the input voltage is higher than Vth+ while the output voltage can change from high to low only when the input voltage is lower than Vth-. Then, Schmitt trigger circuits can eliminate wide range noise, so that the input noise lower than Vth+ dose not appear at the output at 0 output state whereas the one larger than Vth- also dose not appear at 1 output state.

Figure 2(b) shows an example of Schmitt trigger buffers using CMOS transistors [12]. In the circuit, we can change threshold voltage by changing the size of transistors MP1, MN1, MP2 and MN2.

3. Soft Error Masking Method

3.1. Soft Error Masking Circuit

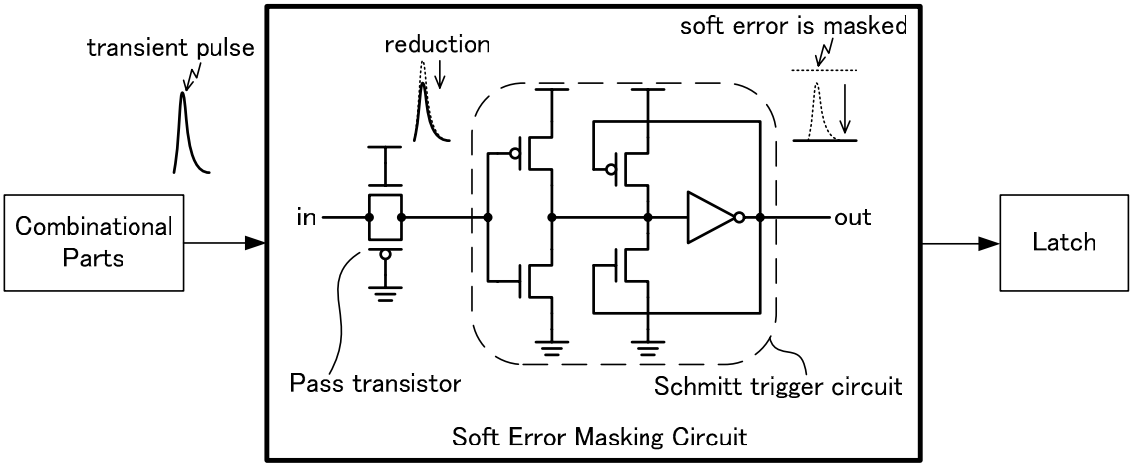


Figure 3. Soft error masking circuit

Here, a class of circuits capable of masking soft errors is proposed. When a signal with a transient pulses is input to the proposed circuit, the soft error at the circuit output can be eliminated while the transient pulses is not so much high. Figure 3 shows construction of the proposed circuit. The proposed circuit comprises a pass transistor and a Schmitt trigger circuit, i.e. the circuit enclosed with a dotted line in Fig. 3. The Schmitt trigger circuit has large hysteresis property in voltage in order to mask transient pulses with high peak voltage as shown in Fig.4.

Next, it is explained why the proposed soft error masking circuit can mask soft errors whose peak voltage is not so much high. Assume that logic "0" signal with a transient pulse is input to the proposed circuit. First, the pass transistor reduces the peak voltage of the transient pulse. It can reduce the peak voltage by about 10%. Next, the Schmitt trigger circuit reduces it further. The Schmitt trigger circuit can mask the soft error as long as the peak voltage of the transient pulse input to the circuit is reduced to less than the threshold voltage Vth+ by the pass transistor even if the peak voltage of the transient pulse input to the pass transistor is higher than Vth+. The same holds for the opposite logic "1" signals with transient pulses.

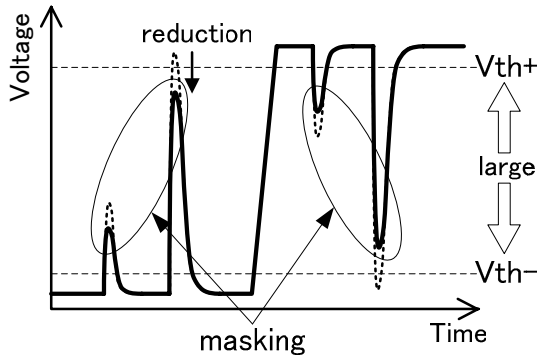


Figure 4. Peak voltage of transient pulses reduced by soft error masking circuit

3.2. Soft Error Masking Latch (SEM-Latch)

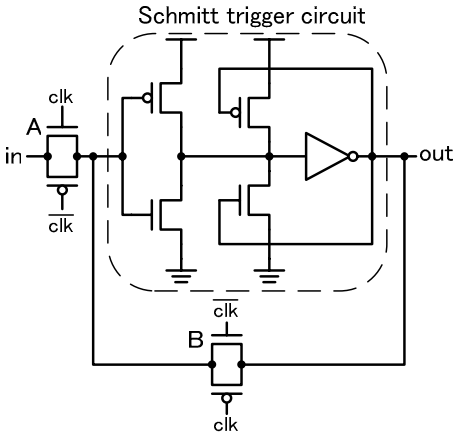


Figure 5. SEM-Latch

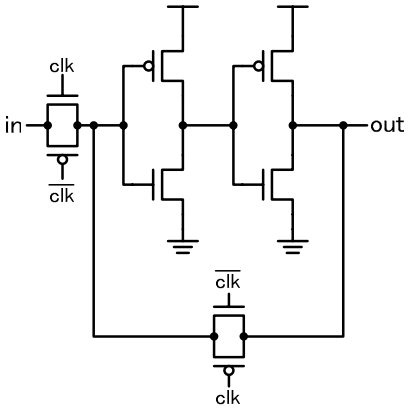


Figure 6. Normal latch

Here, a class of soft error masking latches (SEM-Latches) is proposed, which are capable of masking transient pulses occurring on combinational circuits. Construction of the SEM-Latch is shown in Fig. 5. The SEM-Latch comprises a Schmitt trigger circuit and two pass transistors A and B. A clock signal clk is supplied to the pass transistor A as the control signal and the inverted clock signal $\overline{clk}$ is supplied to B. Construction of the SEM-Latch is the same as that of a normal latch shown in Fig. 6 except that Schmitt trigger buffer is used instead of two normal inverters. The pass transistor A and the Schmitt trigger circuit are the same structure as the soft error masking circuits discussed in 3.1 except that clock signal is supplied to the gate of the pass transistor A. The pass transistor and the Schmitt trigger circuit mask transient pulses.

Figure 7 shows construction of a master-slave D-FF using the proposed SEM-Latch. The proposed SEM-Latch is used only as a master latch and is not used as a slave latch. Since there is only a wire between master and slave latches, using the proposed SEM-Latch as a slave latch has little effect in soft error masking capability. The D-FF using the proposed SEM-Latch is evaluated in Sect. 4.2.

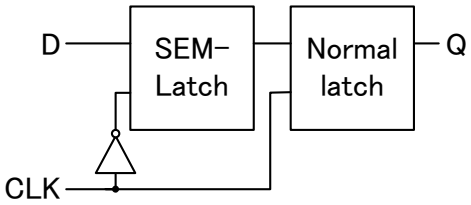
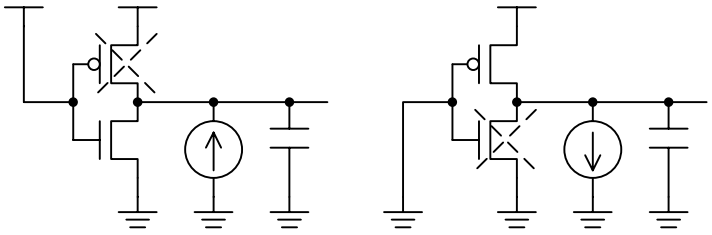


Figure 7. D-FF using SEM-Latch

4. Experimental Results

In our experiment, every circuit is designed in a 0.35um technology and simulated by HSPICE with driving voltage of 3.3V. The Schmitt trigger buffers with the structure shown in Fig. 2(b) are used. The channel widths of the transistors MP1, MN1, MP2, and MN2 in the Schmitt trigger circuit are 4.45um, 2.95um, 5.60um, and 1.62um, respectively. The threshold voltages of Schmitt trigger circuit Vth- and Vth+ are 0.59V and 2.71V, respectively. Just like [6], the outputs of latches or flip-flops are connected with a fan-out of four inverter loads. Rising and falling times of clock signal are set to 100ps. Figure 8 shows a soft error occurrence model [4] used in our experiment. In this figure, it is assumed that soft errors occur at an inverter without loss of generality. Figure 8(a) shows the case where the normal output value for the inverter is low and soft errors occurring at PMOS transistor generate a positive pulse whereas Figure 8(b) shows the case that the normal output value for the inverter is high and soft errors occurring at NMOS transistor generate a negative pulse. It is also assumed that the duration time of transient pulses is 0.3ns, that is the current source in Fig. 8 is turn on for 0.3ns.



(a) Fault in P-MOS **(b) Fault in N-MOS**

Figure 8. Soft error model

4.1. Evaluation of Soft Error Masking Circuit

Figure 9 shows waveforms of the input and output voltages of the proposed soft error masking circuit discussed in 3.1. It also shows that of the output voltage of the circuit proposed in [9], for comparison. Transient pulses of different size are provided for the input signal. The result indicates that the proposed method has higher soft error masking capability than the method proposed in [9]. For driving voltage VDD=3.3V, the proposed method can mask transient pulses of magnitude 4.0V or less. Therefore, even if the peak voltage of transient pulses is bigger than the driving voltage, the proposed circuit has soft error masking capability.

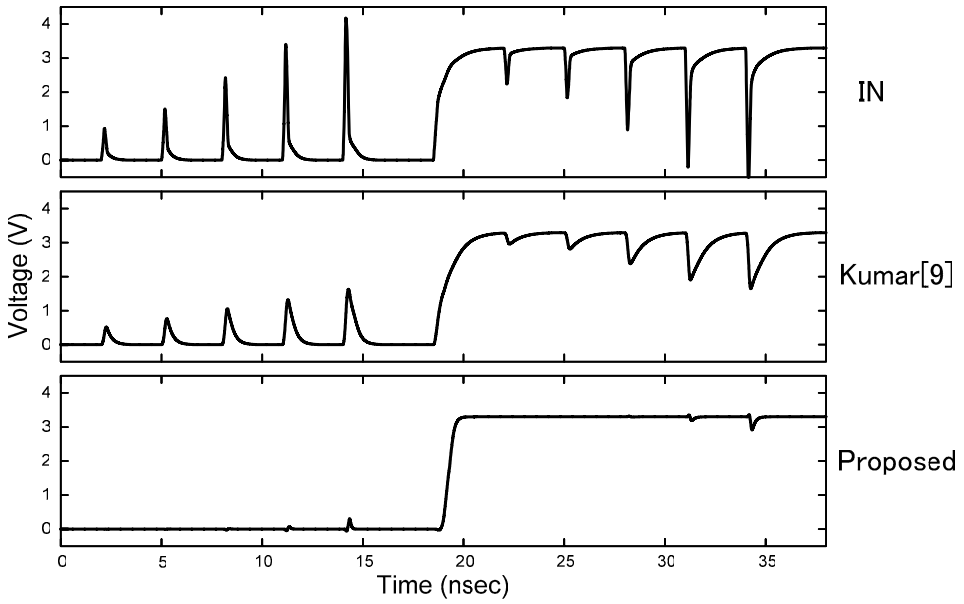


Figure 9. Waveforms of soft error masking circuit

4.2. Evaluation of SEM-Latch

A sample layout of the SEM-latch cell designed in a 0.35um technology is shown in Fig. 10. This cell includes the SEM-Latch and two inverters to provide stably clock signal to clk and $\overline{\text{clk}}$. The area of the normal latch and proposed SEM-Latch are shown in Table 1. The area of the SEM-Latch is 12.5% larger than that of a normal latch.

Figure 11 shows waveforms of the input and output voltages of the proposed SEM-Latch discussed in 3.2. In the experiment, soft errors occur on the input signal at the times of 4ns and 14ns. Note that pulses occurring on the input signal at the times of 2ns and 12ns, i.e. when the clock signal rise, are caused by not soft errors but discharging and charging current for changing value stored in the latch. The result gives evidence that the proposed SEM-Latch is capable of masking soft errors as well as the proposed soft error masking circuit.

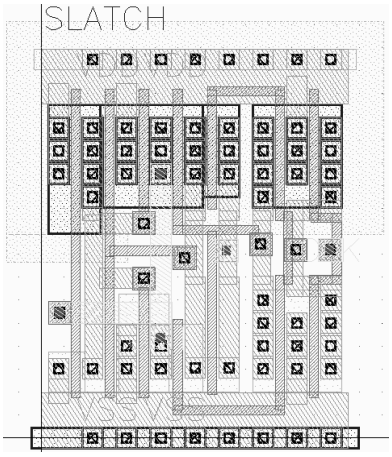


Figure 10. Layout of SEM-Latch

Table 1. Area of normal latch and SEM-Latch

Circuit	Area (nm^2)	Relative Area
Normal Latch	198.00	1.000
SEM-Latch	222.75	1.125

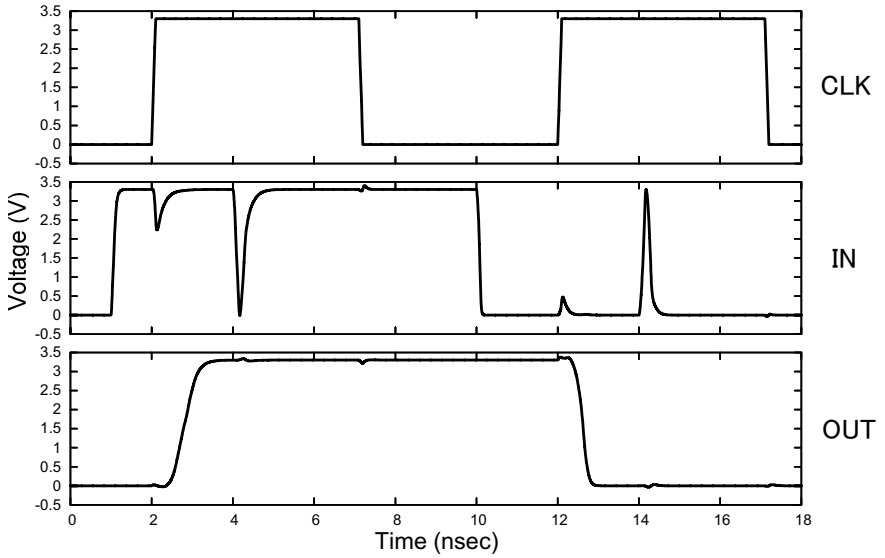


Figure 11. Waveforms of SEM-Latch

Figure 12 shows waveforms of the input and output voltages of the proposed D-FF shown in Fig. 7. Figure 13 shows the case where soft errors occur on the input signal at the time of clock signal rising. The output signal in Fig. 13 is similar to that in Fig. 12. The result gives evidence that the proposed D-FF is capable of masking soft errors.

Table 2 shows the setup and hold times of the proposed D-FF. Those of a normal master-slave D-FF are also shown for comparison. Like [6, 13], it is assumed that setup and hold times are D-CLK offsets corresponding to a 5% increase in the CLK-Q delay from its nominal value. The delay time caused by the increase of the setup and hold times is nearly equal to that of an OR-gate.

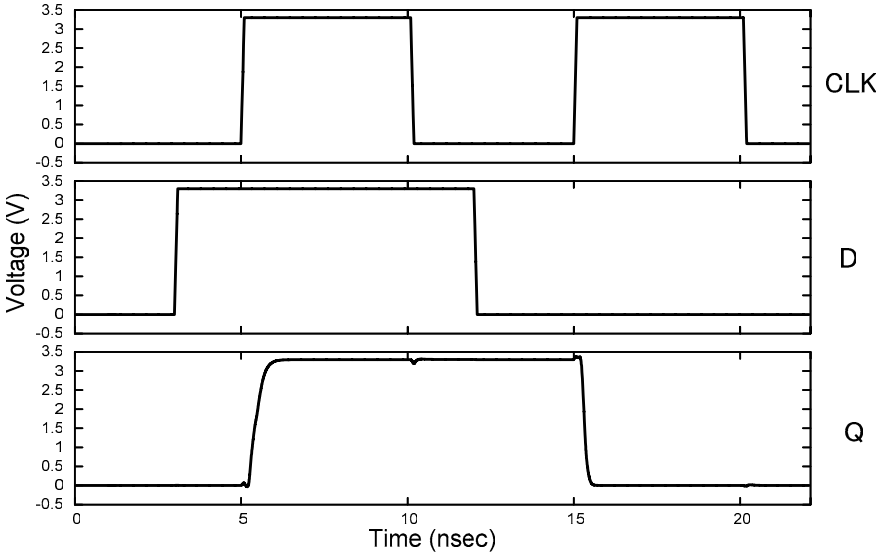


Figure 12. Waveforms of D-FF using SEM-Latch

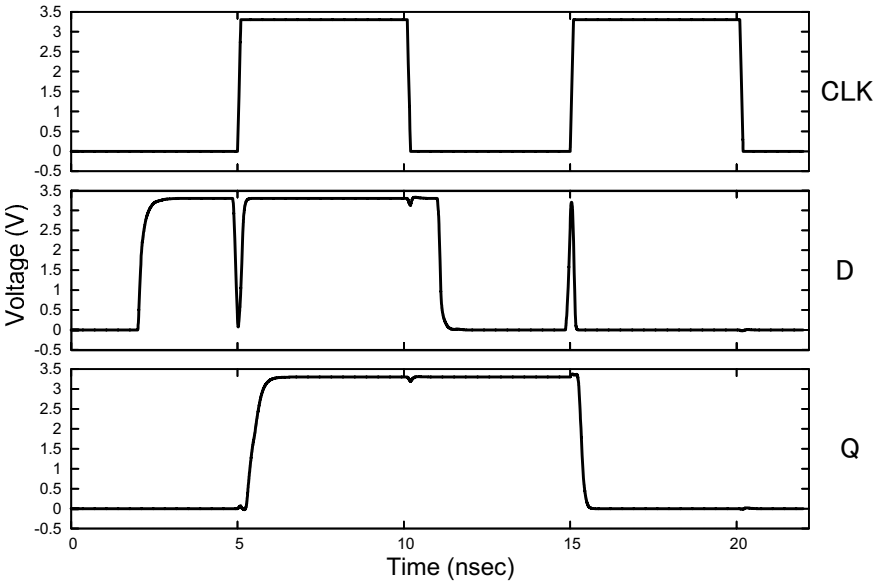


Figure 13. Waveforms of D-FF using SEM-Latch with transient pulses

Table 2. Setup and hold time of D-FF using SEM-Latch

		Setup time (ns)	Hold time (ns)
D-FF using normal latch	rising	0.20	0.05
	falling	0.23	0.05
D-FF using SEM-Latch	rising	0.41	0.05
	falling	0.46	0.10

5. Conclusions

This paper has proposed a soft error masking circuit capable of masking soft errors occurring on combinational parts of logic circuits. The circuit consists of a pass transistor and a Schmitt trigger circuit. Construction of a soft error masking latch (SEM-Latch) is also proposed. The SEM-Latch is a latch capable of masking soft errors, and is constructed by using the proposed soft error masking circuit. The proposed circuits are evaluated from the viewpoint of soft error masking capability, area overhead, and setup and hold times. For example, for driving voltage VDD=3.3V, the proposed soft error masking circuit is capable of masking transient pulses of magnitude 4.0V or less. The area overhead of the proposed SEM-Latch is 12.5% larger than that of a normal latch. The setup and hold times of a master-slave D-FF whose master latch is the proposed SEM-Latch are 0.41ns and 0.05ns at rising, 0.46ns and 0.10ns at falling, respectively.

The proposed SEM-Latch is capable of masking only transient pulses occurring on combinational parts of logic circuits but not those occurring on the SEM-Latch. Future work includes development of latches capable of masking transient pulses occurring on the SEM-Latch.

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