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CMOS NAND and NOR Schmitt circuits

Branko L. Dokić

Faculty of Electrical Engineering, University of Banja Luka, Trg Palih Boraca 2/II, 78000 Banja Luka, Serbia

Original solutions of m-input NAND and NOR logic circuits with hysteresis in the transfer characteristics are proposed. Multiple inputs are done similarly to standard NAND and NOR logic circuits. The logic circuits proposed in this paper consist of $2m + 1$ pairs of enhancement CMOS transistors. The hysteresis voltage depends on supply voltage and transistor geometry. The proposed solutions always guarantee hysteresis, even with very large process variations. The noise immunity is typically greater than 50% of supply voltage. Analysis using simple device models together with computer simulations and experimental results is given. Copyright © 1996 Elsevier Science Ltd.

1. Introduction

In the conventional simple digital NOR and NAND gates at any point in time the output is directly related to the input by some logic combination. Therefore, these circuits are known as combinational logic circuits. A characteristic of combinational circuits is the lack of intentional connections between outputs and inputs.

There is another class of circuits, known as sequential logic circuits, in which the outputs are also dependent on preceding values of input data. A characteristic of sequential circuits is that one or more output nodes are intentionally connected back to inputs to give positive feedback, i.e. regeneration. Therefore, these circuits are also known as regenerative circuits. Common examples of these circuits are the multivibrator circuits (the bistable circuits — latches and flip-flops, the monostable circuits and the astable circuits).

Another family of regenerative circuits, particularly useful in digital systems, is the Schmitt trigger [1–5]. A characteristic of these circuits is that the voltage transfer characteristic has different input threshold for positive-going and negative-going voltage signals. Therefore, there is hysteresis in the transfer characteristic. Another important feature is that this circuit responds to a slowly changing input waveform with a fast transition at the output. If the output of the Schmitt trigger is directly related to the input by some logic combination, such a circuit is known as the Schmitt trigger logic circuit. Common examples of these circuits are the NAND and NOR Schmitt triggers.

Original solutions of m-input NAND and NOR Schmitt triggers are described in this paper. They consist only of enhancement transistors and can be implemented using conventional CMOS technology. The circuits are simple and demonstrate hysteresis even with very large process variations. This is an important feature in comparison with NAND and NOR circuits described in [2].

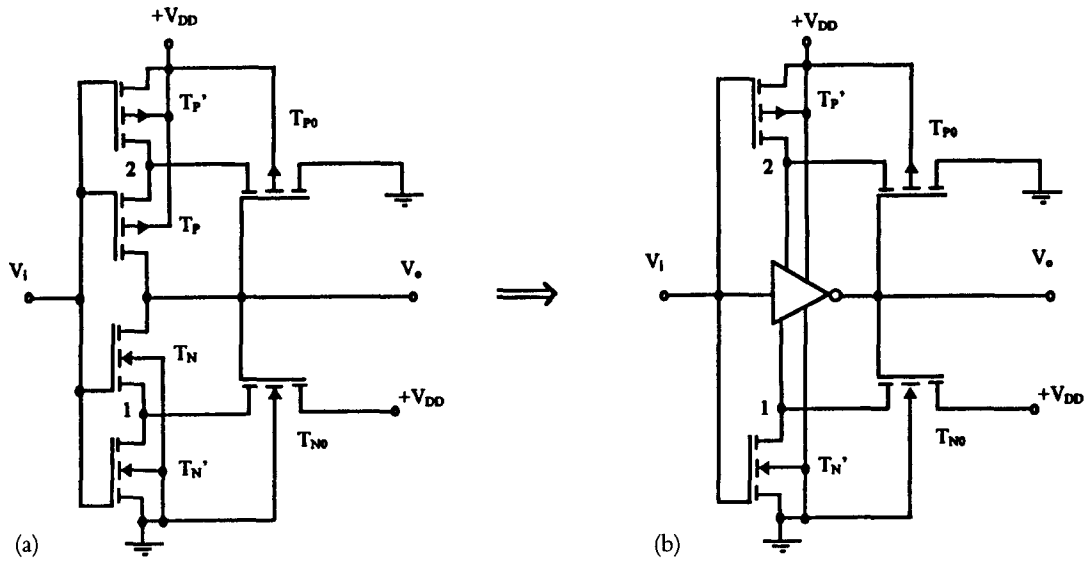

Fig. 1. Schmitt trigger-inverter with three pairs of CMOS transistors.

2. Schmitt trigger-inverter

The basic circuit is the Schmitt trigger-inverter [1] with three pairs of CMOS transistors (Fig. 1). Transistors T_n and T_p form the standard inverter I (Fig. 1b). Transistors T_{n0}, T_n and T_{p0}, T_p are operating as the inverting NMOS and PMOS amplifier, respectively. They also introduce hysteresis by feeding back the output voltage to points 1 and 2. To describe the circuit, assume the threshold voltages of all NMOS and PMOS transistors are V_{tn} and V_{tp}, respectively. Constants β of the transistors T_{n0} and T_{p0} are β_{n0} and β_{p0}, and constants β of the other NMOS and PMOS transistors are β_n and β_p, respectively, where

$$\beta_n = \frac{\mu_n \varepsilon_{ox}}{2t_{ox}} \frac{W_n}{L_n} \quad \text{and} \quad \beta_p = \frac{\mu_p \varepsilon_{ox}}{t_{ox}} \frac{W_p}{L_p}$$

μ is the mobility of the carriers in the channel, ε_{ox} the oxide dielectric constant, t_{ox} the oxide thickness, L the channel length and W the channel width.

Now with $V_i = 0\,V$, the two stacked p-channel transistors T_p and T'_p will be on with negligible conducting drain current, since T_n and T'_n are off, and $V_{out} = V_{DD}$. The transistor T_{p0} is off, and T_{n0} is at the threshold of conduction and $V_1 = V_{DD} - V_{tn}$. When V_i rises to V_{tn} T'_n starts to turn on, but T_n is off because $V_1 > V_{tn}$. Now T'_n and T_{n0} are in the saturated region and form the inverting NMOS amplifier with a voltage gain of about $-A$ (2). Namely, with equalization of the drain current of T_{n0} and T'_n V_1 is given by

$$V_1 = V_{DD} - V_{tn} - A_n(V_i - V_{tn}) \tag{1}$$

where

$$A_n = \sqrt{\frac{\beta'_n}{\beta_{n0}}} = \sqrt{\frac{W_n/L_n}{W_{n0}/L_{n0}}} \tag{2}$$

Thus, as V_i rises, V_1 is falling. At $V_i = V_1 + V_{tn}$, T_n turns on. Then T_{p0} is off so that the series transistors T'_p and T_p can be replaced by an equivalent one with constant β [6]

$$\beta_{pe} = \beta_p/2 \tag{3}$$

When both the T_n and equivalent PMOS transistors are in saturation, regenerative switching is about to take over and the output rapidly goes to 0 V, turning off T_{n0} and turning on T_{p0}. The input voltage at which these changes occur is the high threshold V_t^+ of the Schmitt trigger. The

currents of the T_n and equivalent PMOS transistors are equal so that

$$\beta_n(V_t^+ - V_1 - V_{tn})^2 = \beta_{pe}(V_{DD} + V_{tp} - V_t^+)^2 \tag{4}$$

where V_1 is given by eq. (1) with $V_i = V_t^+$. Combining eqs. (4) and (1), we obtain

$$V_t^+ = \frac{V_{DD} + V_{tp} + B_1(V_{DD} + A_n V_{tn})}{1 + B_1(1 + A_n)} \tag{5}$$

where

$$B_1 = \sqrt{\frac{\beta_n}{\beta_{pe}}} = \sqrt{2\frac{\beta_n}{\beta_p}} \tag{6}$$

Assume that the input voltage V_i decreases from V_{DD} to 0 V. For $V_i = V_{DD}$ T_p, T'_p and T_{n0} are off, T_n and T'_n are on, and T_{p0} is at the threshold of conduction. That is $V_o = 0$ and $V_2 = |V_{tp}|$. The transistor T_p turns on at $V_i = V_{DD} + V_{tp}$. As T'_p and T_{p0} are saturated, V_2 increases linearly as V_i decreases, and is given by

$$V_2 = A_p(V_{DD} + V_{tp} - V_i) - V_{tp} \tag{7}$$

where

$$A_p = \sqrt{\frac{\beta'_p}{\beta_{p0}}} = \sqrt{\frac{W_p/L_p}{W_{p0}/L_{p0}}} \tag{8}$$

With $V_i = V_2 + V_{tp}$, T_p turns on. Then T_{n0} is off so that T_n and T'_n can be replaced by an equivalent transistor with constant β [6]

$$\beta_{ne} = \beta_n/2 \tag{9}$$

When the equivalent NMOS and T_p transistors are saturated, the regenerative process takes place and V_0 rapidly goes to V_{DD}, turning off T_{p0} and turning on T_{n0}. Then the input voltage is equal to the low threshold voltage V_t^-. Thus, at $V_i = V_t^-$ we obtain

$$\beta_{ne}(V_t^- - V_{tn})^2 = \beta_p(V_2 + V_{tp} - V_t^-)^2 \tag{10}$$

so that

$$V_t^- = \frac{A_p(V_{DD} + V_{tp}) + B_2 V_{tn}}{1 + A_p + B_2} \tag{11}$$

where

$$B_2 = \sqrt{\frac{\beta_{ne}}{\beta_p}} = \sqrt{\frac{\beta_n}{2\beta_p}} \tag{12}$$

Besides the supply voltage, the threshold voltages V_t^+ and V_t^- depend on the ratio of transistor β constants. The optimal characteristics will be when transistors' T_n, T'_n, T_p and T'_p β constants are equal. Then, V_t^+ and V_t^- depend on the transistors' T_{n0} and T_{p0} geometry if the supply voltage is constant (Fig. 2).

Figure 3 shows the average propagation delay time, obtained by computer simulation using the program SPICE as a function of the constants $A_n = A_p$ and the capacitive load at $V_{DD} = 5$ V. The simulation was made for parameters of the

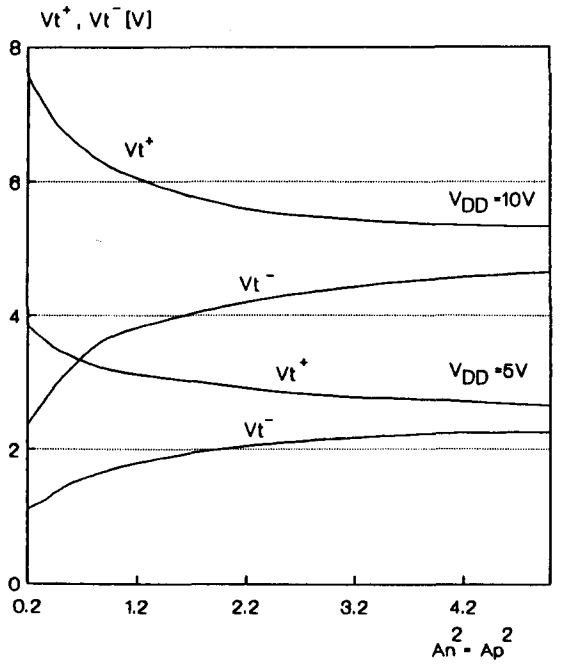

Fig. 2. The threshold voltages V_t^+ and V_t^- as a function of the ratios $(W_n/L_n)/(W_{n0}/L_{n0}) = (W_p/L_p)/(W_{p0}/L_{p0})$ at $V_{DD} = 5$ V and $V_{DD} = 10$ V given by SPICE.

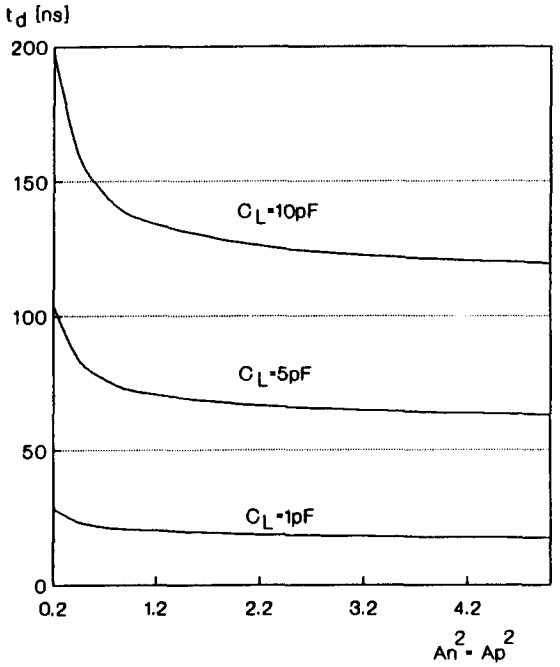

Fig. 3. Average propagation delay time as a function of $(W_n/L_n)/(W_{n0}/L_{n0}) = (W_p/L_p)/(W_{p0}/L_{p0})$ and capacitive load C_L.

2 μm CMOS technological process. For $A_n = A_p > 1$ the propagation delay time almost does not depend on the T_{n0} and T_{p0} geometry. Therefore, by controlling the hysteresis through change A_n and A_p (Fig. 2), the propagation delay time is nearly held constant.

3. NAND and NOR circuit design

Thus, the Schmitt trigger-inverter (Fig. 1) consists of one conventional CMOS inverter (T_n, T_p), one NMOS inverter (T'_n, T_{n0}) and one PMOS inverter (T'_p, T_{p0}). The same principle is used for design of the new NAND and NOR Schmitt circuits shown in Figs. 4 and 5 which are proposed in this paper. In this case conventional CMOS, NMOS and PMOS NAND and NOR gates are used instead of the corresponding inverters.

Since the transistors $T'_{n1}, \ldots, T'_{nm}$ and the NMOS transistors of the conventional CMOS NAND gates are connected in series, the output of the circuit in Fig. 4 will be low only when all inputs are high, i.e. $\overline{Z} = X_1 X_2, \ldots, X_m$ so that $Z = \overline{X_1 X_2, \ldots, X_m}$. Hence this is an m-input NAND gate.

The output of the circuit in Fig. 5 will be high only when all inputs are low ($T'_{p1}, \ldots, T'_{pm}$ and PMOS transistors of the conventional NOR gate are connected in series and must be conducting), i.e. $Z = \overline{X}_1 \overline{X}_2, \ldots, \overline{X}_m$ or $Z = \overline{X_1 + X_2 + , \ldots, + X_m}$. Hence this is an m-input NOR gate.

Transistors T_{n0} and T_{p0} provide feedback to effect rapid change of the output voltage and the transfer characteristic has the shape of the hysteresis curve. Hence the circuits in Figs. 4 and 5 are m-input NAND and NOR Schmitt circuits, respectively.

3.1 NAND circuit analysis

3.1.1 DC characteristics

Parallel or series transistors can be replaced by one transistor such as the conventional NAND and NOR circuits [6]. In this way, NAND and NOR Schmitt circuits can be replaced by an equivalent Schmitt trigger-inverter (Fig. 7) by dc analysis. It will be shown by analysing an m-input NAND Schmitt circuit (Fig. 6).

Assume that n inputs are active, where $1 \leqslant n \leqslant m$, and that the other $m-n$ inputs are at V_{DD} (the active input is one with changeable input voltage). Let the input voltage V_i increase from zero to V_{DD}. For $0 \leqslant V_i \leqslant V_t^+$ the NAND circuit in Fig. 6 can be replaced by the equivalent circuit in Fig. 7a. T_{p0} is off and it does not exist in Fig. 7a. $m-n$ PMOS transistors at $V_i = V_{DD}$ are off, too. Therefore, the equivalent PMOS transistor T_{pe} consists of n pairs of PMOS transistors T_{pi}, T'_{pi} with active inputs. Hence T_{pe} constant β is given by

$$\beta_{pe} = n\frac{\beta_p}{2} \tag{13}$$

The equivalent constant β of series transistors depends on the number of transistors and position of the first active input [6]. Consequently,

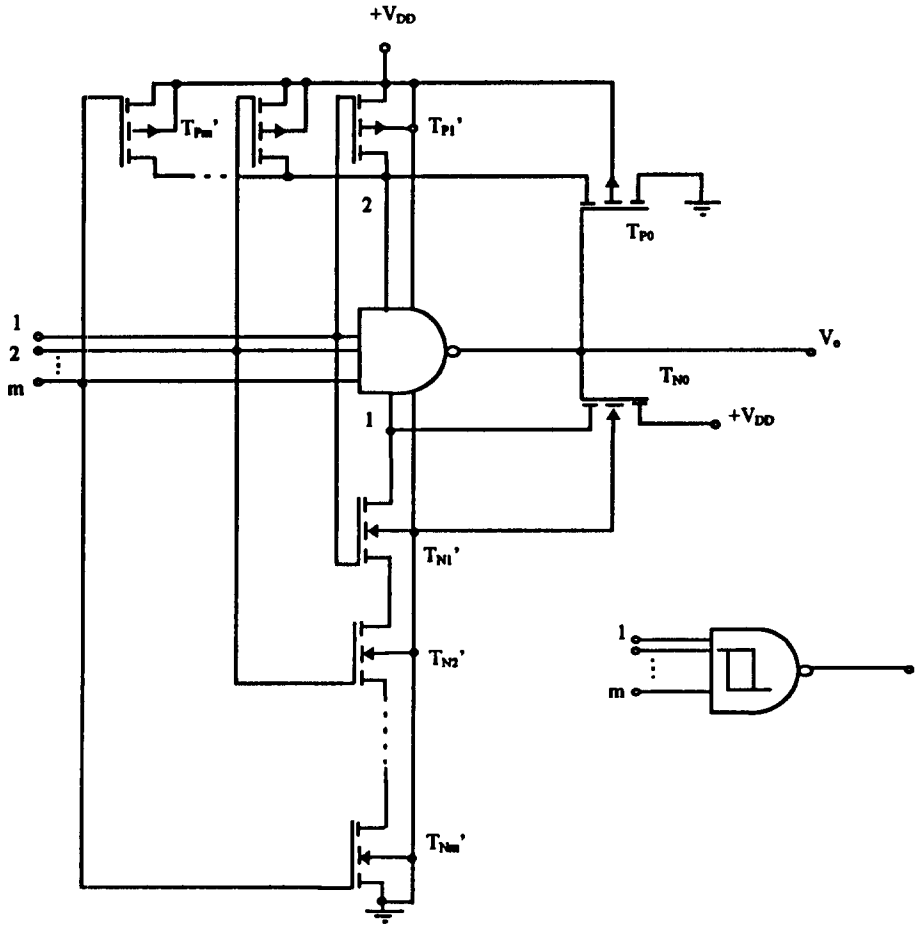

Fig. 4. m-Input NAND Schmitt circuit.

for the case of n active inputs the transistors $T_{nl}, \ldots, T_{nm}$ and $T'_{nl}, \ldots, T'_{nm}$ can be replaced by the equivalent transistors T_{ne1} and T_{ne2}, respectively, whose constants β are given by

$$\beta_{ne1} = \beta_{ne2} = \frac{\beta_n}{m-k+1} \tag{14}$$

where k marks the position of the first active input (for example, if $k = 3$ the inputs of the transistors T_{n1}, T'_{n1} and T_{n2}, T'_{n2} are at V_{DD}, and T_{n3}, T'_{n3} are at V_i).

Now, the ratios of T_{ne2} to T_{n0}, and T_{ne1} to T_{pe} are given by

$$A_{ne} = \sqrt{\frac{\beta_{ne2}}{\beta_{n0}}} = A_n(m-k+1)^{-1/2} \tag{15}$$

$$B_{le} = \sqrt{\frac{\beta_{ne1}}{\beta_{pe}}} = B_l[n(m-k+1)]^{-1/2} \tag{16}$$

where A_n and B_l are given by eqs. (2) and (6), respectively.

From eq. (5), replacing A_n by A_{ne} and B_l by B_{le} we obtain the high threshold voltage of the m-inputs NAND Schmitt circuit

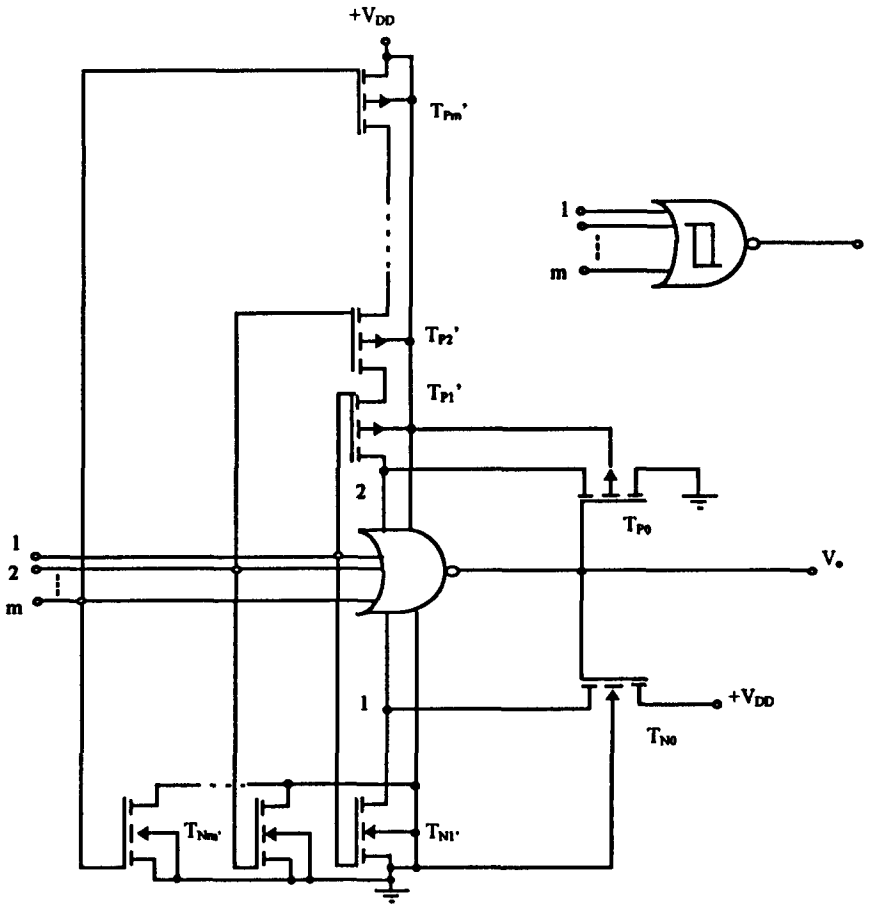

Fig. 5. m-Input NOR Schmitt circuit.

$$V_t^+ = \frac{V_{DD} + V_{tp} + B_1[n(m-k+1)]^{-1/2}\,[V_{DD} + A_n(m-k+1)^{-1/2}V_{tn}]}{1 + B_1[n(m-k+1)]^{-1/2}\,[1 + A_n(m-k+1)^{-1/2}]} \tag{17}$$

To calculate V_t^- the circuit in Fig. 4 can be replaced by an equivalent one shown in Fig. 7b. Namely, T_{n0} is off. $T_{n1},\ldots,T_{nm}, T'_{n1},\ldots,T'_{nm}$ are on and can be replaced by an equivalent one T_{ne} with the constant β [6]

$$\beta_{ne} = \frac{\beta_n}{2m} \tag{18}$$

T_{p0} is on. T_{pi} and T'_{pi} $(i = 1,\ldots,n)$ with active input can be replaced by equivalent transistors T_{pe1} and T_{pe2}, respectively, with the constants β

$$\beta_{pe1} = \beta_{pe2} = n\beta_p \tag{19}$$

The β ratios of T_{pe2} to T_{p0}, and T_{ne} to T_{pe1}, respectively, are given by:

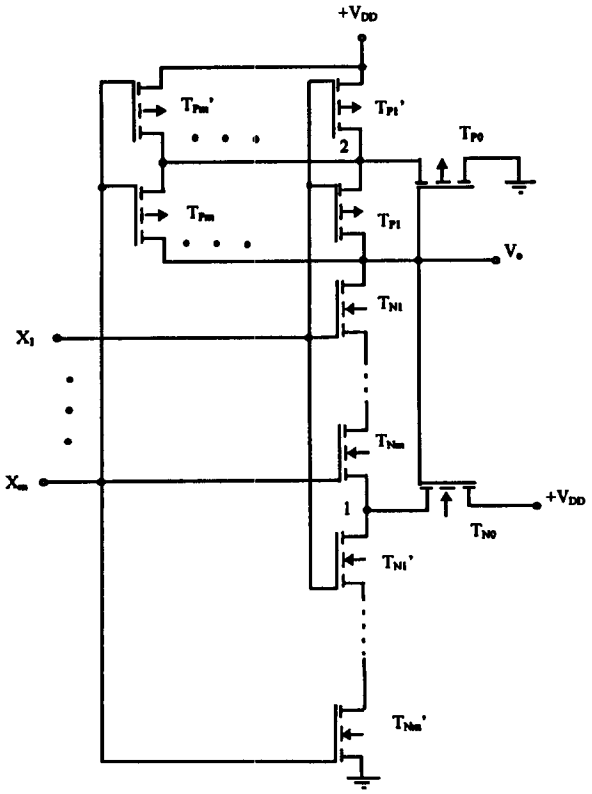

Fig. 6. Complete scheme of the m-input NAND Schmitt circuit.

$$A_{pe} = \sqrt{\frac{\beta_{pe2}}{\beta_{p0}}} = A_p n^{1/2}, \tag{20}$$

$$B_{2e} = \sqrt{\frac{\beta_{ne}}{\beta_{pe1}}} = B_2 (mn)^{-1/2} \tag{21}$$

From eq. (11), replacing A_p by A_{pe} and B_2 by B_{2e}, we obtain the low threshold voltage of the m-inputs NAND Schmitt circuit

$$V_t^- = \frac{A_p n^{1/2}(V_{DD} + V_{tp}) + B_2 (mn)^{-1/2} V_{tn}}{1 + A_p n^{1/2} + B_2 (mn)^{-1/2}} \tag{22}$$

where A_p and B_2 are given by eqs. (8) and (12), respectively.

The threshold voltages V_t^+ and V_t^- depend on supply voltage V_{DD}, the ratio of the constants β_n/β_p, β_n/β_{n0}, i.e. β_p/β_{p0}, number of inputs m, and number of active inputs n. Besides, V_t^+ depends on the position of the first active input k.

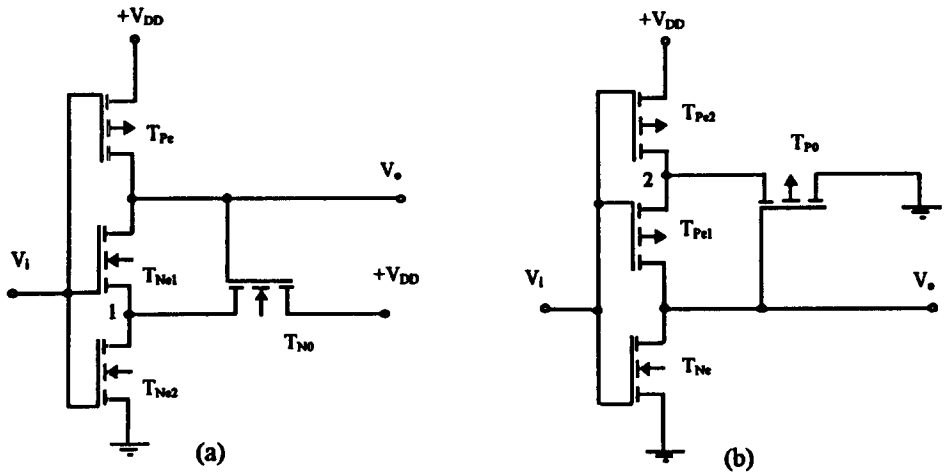

Fig. 7. Equivalent circuit of m-input NAND or NOR circuit (a) at $V_0 = V_{DD}$, and (b) at $V_0 = 0$ V.

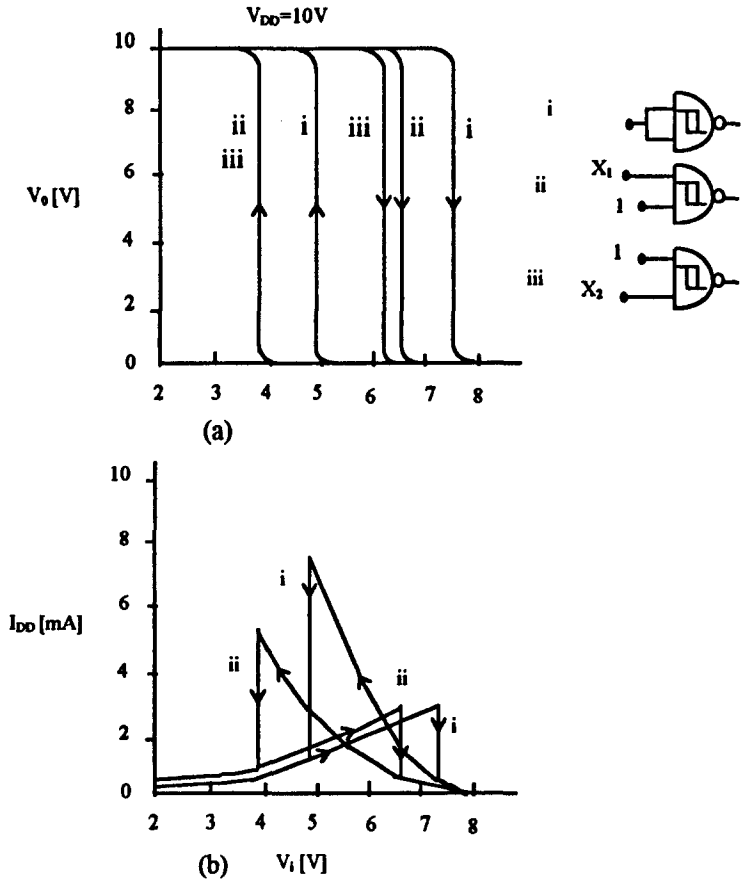

Fig. 8. Oscillograms of (a) voltage and (b) current transfer characteristic of the two-input NAND Schmitt circuit.

3.1.2 Measurements and computer simulation

Measurements and computer simulation are made on a two-input NAND Schmitt circuit. An experimental model was built using CMOS integrated circuits of type CD4007 (dual complementary pair plus inverter). Oscillograms of the voltage and current transfer characteristics of the two-input NAND Schmitt circuit for various numbers and combinations of active inputs are shown in Fig. 8. Figure 8 confirms that V_t^+ depends and V_t^- does not depend on the combination of active inputs. Namely, when first input X_1 is active only ($n = 1$, $k = 1$) $V_t^+ = 6.1\,\text{V}$, and for the second input active only ($n = 1$, $k = 2$) $V_t^+ = 6.7\,\text{V}$. In both cases, $V_t^- = 3.8\,\text{V}$. This was also confirmed by SPICE simulation (Fig. 9). Simulation was made at $V_{DD} = 5\,\text{V}$ with parameters of the 2 μm CMOS process.

3.2 NOR circuit

As the NOR circuit is obtained from the NAND one through the interchange of the p-channel and n-channel transistors and a power supply polarity change, the previous analysis can be applied analogously to this circuit. In this way we obtain

$$V_t^+ = \frac{V_{DD} + V_{tp} + B_1(mn)^{1/2}(V_{DD} + A_n n^{1/2} V_{tn})}{1 + B_1(mn)^{1/2}(1 + A_n n^{1/2})} \tag{23}$$

$$V_t^- = \frac{A_p(m-k+1)^{-1/2}(V_{DD}+V_{tp}) + B_2[n(m-k+1)]^{1/2}V_{tn}}{1 + A_p(m-k+1)^{-1/2} + B_2[n(m-k+1)]^{1/2}} \quad (24)$$

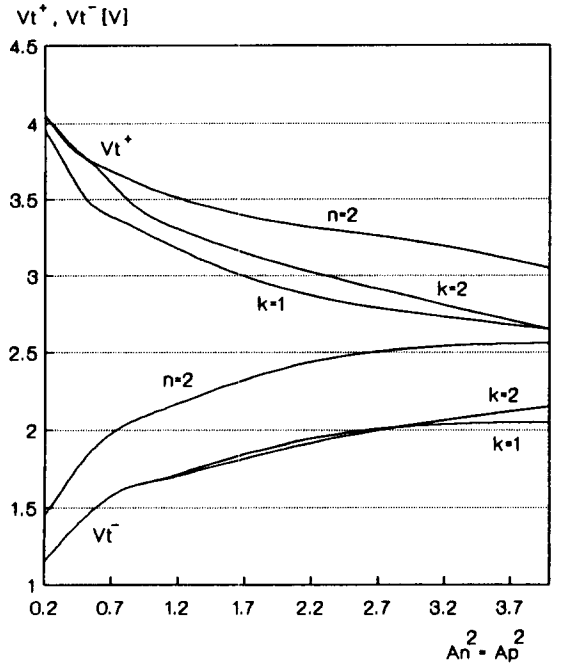

Fig. 9. SPICE values of V_t^+ and V_t^- for two-input NAND circuit versus $(W_n/L_n)/(W_{n0}/L_{n0}) = (W_p/L_p)/(W_{p0}/L_{p0})$ for various numbers and combinations of active inputs at $V_{DD} = 5$ V and for optimum geometry ratio of NMOS and PMOS transistors [6], that is at $\beta_n/\beta_p = 2$.

Therefore, the threshold voltages depend on exactly the same parameters as the thresholds of the NAND circuit except that in the NOR circuit V_t^- depends on the position of the first active input k.

4. Conclusion

The basic circuit for NAND and NOR Schmitt circuit design is the Schmitt trigger-inverter with six MOS transistors. Multiple inputs are realized by adding series and parallel pairs of MOS transistors per input (one NMOS pair and one PMOS pair). As with the conventional CMOS gates the NAND Schmitt circuit is obtained when pairs of NMOS transistors are in series and PMOS are parallel, and for the NOR Schmitt circuit it is the opposite. The total number of transistors of an m-input circuit is $2(2m + 1)$.

The voltage hysteresis depends on supply voltage V_{DD}, threshold voltage and geometry of transistors, as well as on the number of inputs and number of active inputs and combinations of active inputs. The hysteresis increases with increasing geometry of the transistors T_{n0} and T_{p0} in the feedback loop relative to the geometry of the other transistors. When the W/L ratio of the transistors T_{n0} and T_{p0} is less than W/L of the other transistors the average propagation delay time almost does not depend on the T_{n0} and T_{p0} geometry.

It is worth noting that the described circuits always guarantee hysteresis, even with very large process variations.

References

[1] B.L. Dokić, CMOS Schmitt triggers, *IEE Proc.*, 131(5) (Oct. 1984) 197–202.
[2] B.L. Dokić and Z.V. Bundalo, Regenerative logic circuits with CMOS transistors, *Int. J. Electron.*, 58(6) (1985) 907–920.
[3] Zhenhua Wang, CMOS adjustable Schmitt triggers, *IEEE Trans. Instrum.*, 40(3) (June 1991) 601–605.
[4] Daejeong Kim, Joongsik and Wonchan Kim, A new waveform reshaping circuit: an alternative approach to Schmitt trigger, *IEEE J. Solid-State Circuits*, 28(2) (Feb. 1993) 162–164.
[5] J. Exalto, HCMOS Schmitt-trigger applications, *Electron. Components Applications*, 7(3) (1985) 144–151.
[6] B.L. Dokić, Influence of series and parallel transistors on DC characteristics of CMOS logic circuits, *Microelectronics J.*, 13(2) (March/April 1982) 25–30.