Reduction of Random Telegraph Noise in High-κ / Metal-gate Stacks for 22 nm Generation FETs

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Abstract

This work demonstrates, for the first time, the reduction of random telegraph noise (RTN) in high-κ / metal gate (HK / MG) stacks incorporated in 22 nm generation FETs. Many thousands of such FETs have been fabricated, measured, and analyzed using a statistical technique to separate RTN as a major noise component from 1/*f* noise as a minor component. Based on a statistical comparison of these FETs, we find that high temperature forming gas annealing can suppress RTN threshold voltage variation (ΔV_{th}). In addition, properly annealed HK FETs have smaller RTN ΔV_{th} than SiON FETs, due mostly to fewer traps and partly to thinner inversion thickness in HK / MG. Based on these results, we project that random dopant fluctuations will have a greater impact on SRAM yield than RTN until at least the 15 nm generation, for doped channel FETs.

Introduction

Random telegraph noise (RTN) has attracted much attention recently because threshold voltage variation (ΔV_{th}) due to RTN increases with scaling, just as variations due to random dopant fluctuation (RDF) also increase [1]. However these two processes have differences in size dependence and in statistical distribution of ΔV_{th}. The size dependence of RTN is relatively stronger than RDF. Moreover RTN has a long-tailed non-Gaussian distribution (~log normal), while RDF has a Gaussian distribution. Therefore, RTN ΔV_{th} may exceed that of RDF in the tail of the distribution. RTN has been predicted to be a very serious threat to SRAM stability at 22 nm and beyond [2].

In these generations, high-κ / metal-gate (HK / MG) FETs will be employed because of their more optimal power and performance compared to SiON / Poly-Si gate stack [3 - 5]. However, reliability issues due to the HK / MG complex interface structures, e.g. low frequency noise and bias temperature instability, are not fully resolved [6 - 8]. In particular, although defect density in HK / MG is expected to be larger, which may lead to a larger RTN, the RTN properties of scaled HK / MG have not previously been reported. In this study, we experimentally evaluate the RTN of 22 nm HK / MG FETs, as described below, and find that properly annealed HK FETs can in fact have smaller RTN ΔV_{th} than SiON FETs.

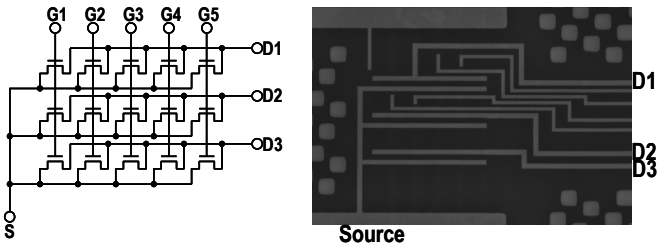
Device fabrication and measurement

Mixed e-beam / optical processing has been used to fabricate devices (nFETs) with gate length (L_g) from 20 to 90 nm and width (W_g) from 25 to 180 nm, incorporating HK / MG. For a comparison, devices with SiO_2 and SiON / Poly-Si gate stack were also fabricated. The HK FETs have smaller T_{inv} and larger transconductance (G_m) than the pure-SiO_2 and SiON FETs, as shown in Table 1. To evaluate the effect of hydrogen passivation of interface traps [9], high temperature forming gas annealing (HTFGA) was performed on some HK / MG FETs. HTFGA is expected to passivate RTN traps and suppress RTN ΔV_{th}. Because RTN has a long-tailed non-Gaussian distribution, statistical analysis of many FETs is vital [2]. As shown in Fig. 1, test array structures were designed for easy measurement of large numbers of devices (27000 / die) to enable statistical analysis of RTN ΔV_{th} variation.

Table 1 Features of FETs.

Gate dielectric	SiON	High-κ
Gate	Poly Si	Metal Gate
Split N conditions	With or W/O	
Split HTFGA		With or W/O
T_{inv} (nm)	1.83(SiON)	1.49
G_m	Small	Large

*HTFGA: High temperature forming gas anneal, 475℃



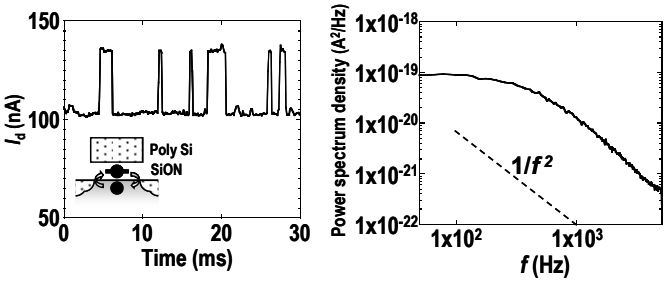
(a) Circuit schematic of array. (b) SEM top view.

Fig. 1 Terminal of array: A matrix has 15 same-size FETs.

A fast measurement unit (Agilent 1530A) which enables a wide band width of up to 1 MHz was used to measure the RTN signals. Between 10^5 and several 10^6 sampling points were used for each time series. Almost all time series are measurements of drain current (I_d) at a drain voltage of 50 mV and at the gate voltage (V_g) for which the average I_d = 100 nA for the FET being measured.

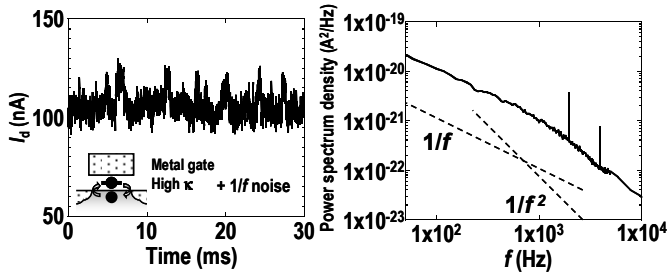
Low frequency noise in HK / MG and SiON / Poly-Si FETs

An example of binary fluctuation due to trapping and detrapping of a carrier at a trap and of its power spectrum density (PSD) in a SiON / Poly-Si and a HK / MG FET of L_g / W_g = 25 / 45 nm, are shown in Figs. 2 and 3. In the case of SiON FETs, the RTN features, i.e., the plateau value and the $1/f^2$ decay (f is frequency), are clear and the PSD does not include other noises, while HK FETs have not only RTN but also other noise because the HK FET's PSD does not clearly show the corner frequency between the $1/f^2$ decay and the plateau value. On the other hand, the PSD of HK FET's background noise without RTN shows it is $1/f$ noise as seen in Fig. 4. This result has an important implication. In general, $1/f$ noise is explained by number fluctuations and/or mobility fluctuations. The number fluctuations are caused by trapping / detrapping of charges at many defects in the gate dielectric, in other words, a large number of RTNs. On the other hand, the mobility fluctuations are explained as a result of the effect of coulomb potential associated with a variety of factors. In this case, number fluctuations with small amplitude or a variety of mobility–fluctuation factors is likely to cause $1/f$ noise. However, since the channel area of the 25 nm FETs is so small and the average number of traps per FET is also small, $1/f$ noise is more likely to originate from mobility fluctuations than number fluctuations.



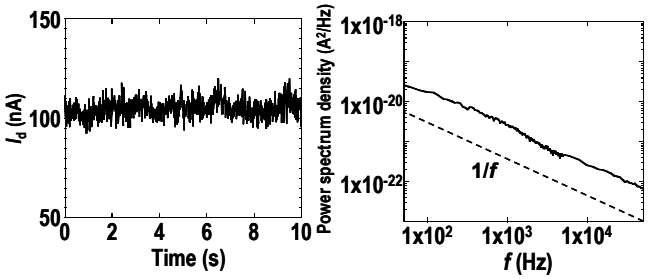
(a) I_d fluctuation due to RTN. (b) Power spectrum density.

Fig. 2 RTN in 25 nm SiON FET.



(a) I_d fluctuation due to RTN. (b) Power spectrum density.

Fig. 3 RTN in 25 nm HK FET.



(a) I_d fluctuation without RTN. (b) Power spectrum density.

Fig. 4 Background noise in 25 nm HK FET.

The differently-originated RTN and $1/f$ noise need to be separated to analyze experimental data. We separate the RTN signals from the $1/f$ noise using the method shown in Fig. 5; histograms of the time series data are fitted with multiple Gaussian peaks to provide $1/f$ noise values at 1σ and RTN ΔI_d which is defined as the peak-to-peak value. J. S. Kolhatkar et al. reported the Hooge parameter for extracted $1/f$ noise using a similar histogram separation method [10]. Moreover, it was confirmed that there is no correlation between RTN and $1/f$ noise as indicated in Fig. 6. This result supports the propriety of the separation between RTN and $1/f$ noise in small FETs.

Comparing their impact, RTN is much more important than $1/f$ noise because $1/f$ noise obeys Gaussian statistics, while RTN obeys a log normal distribution as seen in Fig. 7. This work therefore focused on reduction and control of RTN ΔV_{th}.

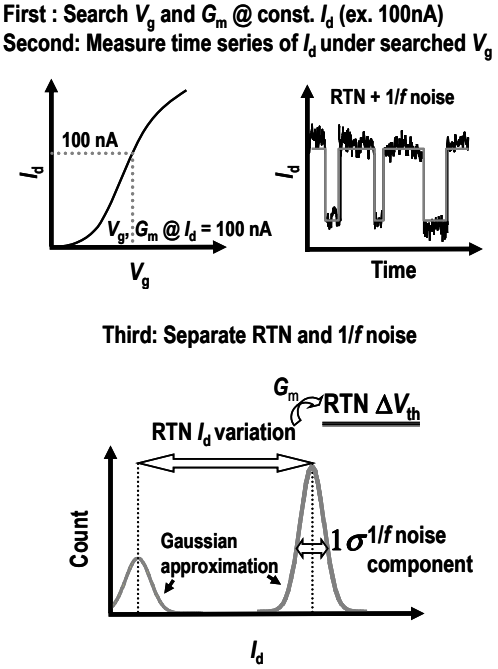


Fig. 5 Component separation between RTN and $1/f$ noise.

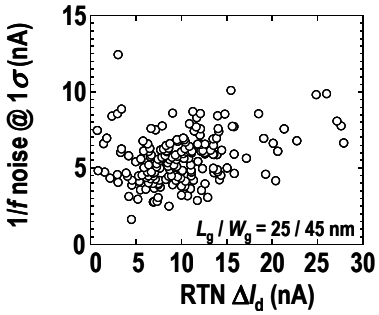


Fig. 6 Non-correlation pattern between RTN and 1/*f* noise.

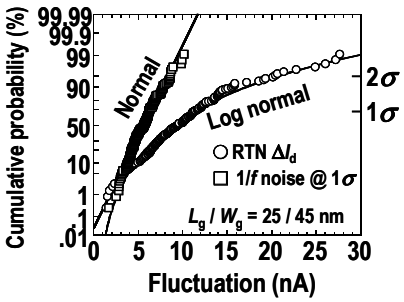


Fig. 7 Comparison between RTN and 1/*f* noise impacts.

Inhibitory effect of HK / MG techniques on RTN ΔV_{th}

Figure 5 indicates that the input-referred RTN voltage noise ΔV_{th} is given by $\Delta I_d / G_m$. Moreover, the RTN ΔV_{th} distribution is almost independent of the bias condition as shown in Fig. 8, indicating that the slope and magnitude are mainly determined by device features. This fact permits comparison of RTN V_{th} variations between the different FETs. This section shows the reduction effect of HTFGA on RTN and a comparison between HK and SiON FETs.

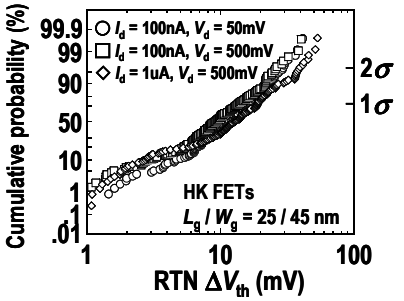


Fig. 8 Relationship between bias conditions and distribution of RTN ΔV_{th}.

HTFGA is expected to passivate RTN traps and suppress RTN ΔV_{th}. Figure 9 shows the effect of HTFGA on the distributions of RTN ΔV_{th} in 25 nm FETs. As expected, RTN is well suppressed by HTFGA. The RTN magnitude at the 2σ level for these two cases differs by ~2× as indicated in Fig. 10.

The comparison of RTN ΔV_{th} between HTFGA HK, pure-SiO_2 and SiON FETs is indicated in Fig. 11. RTN ΔV_{th} of HK and pure-SiO_2 FETs are quite comparable. On the other hand, both the median value and the variation of HK FETs are obviously smaller than those of SiON FETs due mostly to low trap density and partly to $0.75\times T_{inv}$ scaling in our HK FETs.

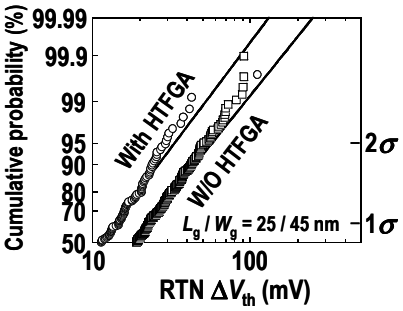
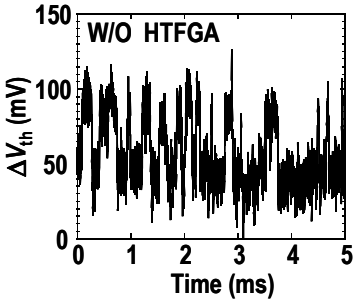
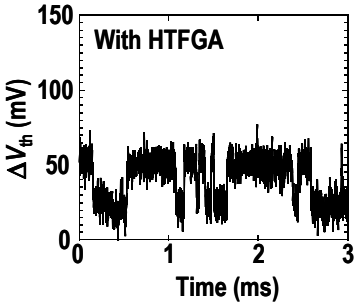


Fig. 9 Comparison of RTN in 25 nm FETs with or without HTFGA.



(a) Without HTFGA



(b) With HTFGA

Fig. 10 RTNs @ 2σ level in 25 nm HK FET.

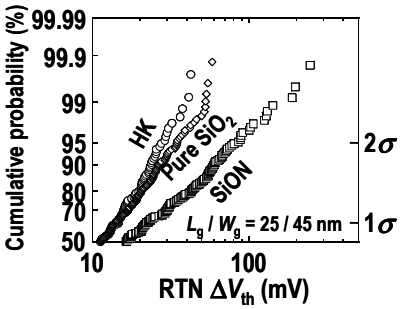


Fig. 11 Comparison of RTN between HK with HTFGA, pure-SiO_2 and SiON FETs.

The distribution of RTN ΔV_{th} of HK / MG FETs shows strong device-size dependence as seen in Fig. 12. The 90 nm FET has small ΔV_{th} of approximately 4 mV at 2σ, while the 45 nm and 25 nm FETs have several tens of mV. The variation also increases with scaling. Figure 13 indicates the device-size dependence of ΔV_{th} at 1 and 2σ. As in the case of SiON FETs [2], the power law exponent of 0.8 is less than the classical RTN theory. Other factors, e.g. current percolation path, seem to be associated with the small power law exponent [11]. On the other hand, the RTN power law exponent of 0.8 is much larger than the 0.5 that is generally observed for RDF [12].

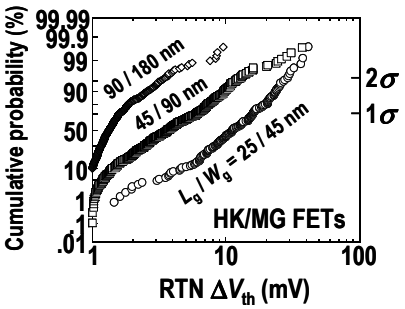


Fig. 12 RTN ΔV_{th} distributions.

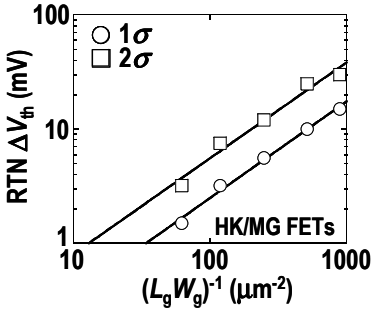


Fig. 13 Device-size dependence of RTN ΔV_{th}.

As seen in Figs. 7-9, RTN has a log-normal distribution, while RDF has been shown to be Gaussian out to at least 5σ [13]. We previously compared the impact of RTN with RDF using the cross point between RTN and RDF in poly-Si /SiON FET [2]. However, since HK / MG gate stack is absolutely essential for 22 nm FET, we now compare RTN with RDF in HK FET. As shown in Fig. 14, at the 22 nm generation RTN V_{th} variations exceed RDF V_{th} variations at the ~3 sigma level in the poly-Si / SiON gate stack, while the cross point can be extended to ~5 sigma level in the case of HK / MG. We therefore conclude that the influence of RTN is less than that of RDF in the 22 nm generation. Considering the size dependence of RTN as shown in Fig. 13, however, RTN may pose a difficult challenge for the 15 nm generation.

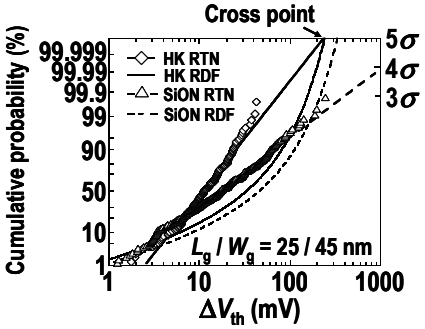


Fig. 14 Comparison between RTN and RDF impacts. *RDF data are based on T. Tunomura, et al., VLSI, p.156, 2008.

Conclusions

22 nm generation HK / MG FETs have random telegraph noise as a major noise component and 1/*f* noise as a minor component. The RTN component can be reduced by suitable annealing, such as HTFGA, and by the thin T_{inv} and large G_m that are achievable with HK / MG, and as a result, properly annealed HK FETs can have smaller RTN ΔV_{th} than SiON FETs. RTN impact may, however, become severe in the 15 nm generation and beyond.

Acknowledgements

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