A 160 mV, Fully Differential, Robust Schmitt Trigger Based Sub-threshold SRAM

Jaydeep P. Kulkarni
School of ECE, Purdue University
465, Northwestern Avenue,
W. Lafayette, IN, 47907
+1- 765-337-1463
jaydeep@ecn.purdue.edu

Keejong Kim
School of ECE, Purdue University
465, Northwestern Avenue,
W. Lafayette, IN, 47907
+1- 765-494-3372
keejong@ecn.purdue.edu

Kaushik Roy
School of ECE, Purdue University
465, Northwestern Avenue,
W. Lafayette, IN, 47907
+1- 765-494-2361
kaushik@ecn.purdue.edu

ABSTRACT

We propose a novel Schmitt Trigger (ST) based fully differential 10 transistor SRAM (Static Random Access Memory) bitcell suitable for sub-threshold operation. The proposed Schmitt trigger based bitcell achieves 1.56X higher read static noise margin (SNM) (V_{DD} = 400mV) compared to the conventional 6T cell. The robust Schmitt trigger based memory cell exhibits built-in process variation tolerance that gives tight SNM distribution across the process corners. It utilizes fully differential operation and hence does not require any architectural changes from the present 6T architecture. At iso-area and iso-read-failure probability the proposed memory bitcell operates at a lower (175mV) V_{DD} with 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 6T cell. Simulation results show that the proposed memory bitcell retains data at a supply voltage of 150mV. Functional SRAM with the proposed memory bitcell is demonstrated at 160mV in 0.13µm CMOS technology.

Categories and Subject Descriptors

B.3.1 [Semiconductor Memories]: Static Random Access Memory

General Terms

Design.

Keywords

Low power SRAM, Low voltage SRAM, Process variations, Schmitt trigger, subthreshold SRAM.

1. INTRODUCTION

Aggressive scaling of transistor dimensions with each technology generation has resulted in increased integration density and improved device performance. Leakage current increases with the scaling of the device dimensions. Increased integration density along with the increased leakage necessities ultra low power operation in present power constrained design environment.

ISLPED'07, August 27–29, 2007, Portland, Oregon, USA.

Power requirement for battery operated devices such as cell phones, medical devices is even more stringent. Reducing the supply voltage reduces the dynamic power quadratically and leakage power linearly to the first order. Hence, supply voltage scaling has remained the major focus of the low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [1]. However, as the supply voltage is reduced the sensitivity of the circuit parameters to process variations increases [2]. Process variations limit the circuit operation in the sub-threshold region, particularly the memories [2, 3]. Embedded cache memories are expected to occupy 90% of the total die area of a system-on-a-chip [2]. Nano-scaled SRAM bitcells having minimum sized transistors are vulnerable to inter-die as well as intra-die process variations. Intra-die process variations include random dopant fluctuation (RDF), line edge roughness (LER) etc. This may result in a threshold voltage mismatch between the adjacent transistors in a memory cell[4]. Coupled with inter-die and intra-die process variations, lower supply voltage operation results in various memory failures i.e. read failure, hold failure, access time failure and write failure [4]. Memory failure probability is predicted to be higher in the future technology nodes [5]. Adaptive circuit techniques such as source basing, dynamic V_{DD} have been proposed to improve the process variation tolerance [6]. Self calibration techniques to achieve low voltage operation while keeping the failure probability under control are also proposed [7]. The 6 transistor cell which uses cross coupled inverter pair is the '*de facto*' memory bitcell used in the current SRAM designs. Different types of SRAM bitcells have been proposed to improve the memory failure probability at a given supply voltage (Fig. 1). 6T and 7T bitcells utilize differential read operation while 5T, 8T and 10T bitcells employ single ended reading scheme. 8T and 10T cells use an extra sensing circuit for reading the cell contents; achieving improved read SNM.

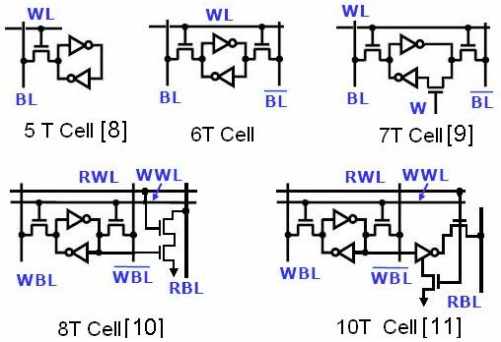


Fig. 1. Various SRAM bitcells [8-11]

TABLE 1 Comparison of various SRAM bitcells

Sr. No.	5T [8]	6T	7T[9]	8T[10]	10T[11]
Read	Single Ended	Differ-ential	Differ-ential	Single Ended	Single Ended
#WL	1	1	1	2	2
#BL	1	2	2	3	3
Area	0.8	1	--	1.3	1.66
#PMOS	2	2	2	2	3
#NMOS in Read Path	2	2	2 or 3	2	3

The detailed comparison of various SRAM bitcells is shown in TABLE 1. Recently, a memory cell with single ended read operation and operating at 103mV supply voltage has been reported [12]. For a stable SRAM bitcell operating at lower supply voltages, the stability of the inverter pair should be improved. None of the aforementioned bitcell has a mechanism to improve the stability of the inverter pair under process variations. We propose a Schmitt trigger based fully differential bitcell having built-in feedback mechanism for improved process variation tolerance. In particular we have:

1) proposed a novel Schmitt trigger based, fully differential, 10 transistor SRAM bitcell having built-in feedback mechanism. It requires no architectural change compared to the present 6T cell architecture.

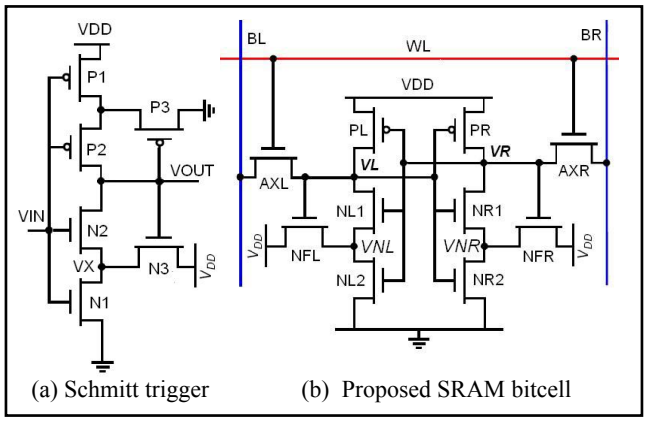
2) demonstrated that with respect to 6T cell, the proposed Schmitt trigger based bitcell gives better read stability, better write-ability, improved process variation tolerance, lower read failure probability, low voltage/low power operation and improved data retention capability at ultra low voltage.

3) fabricated a test chip in 0.13µm logic process technology and validated the proposed technique. An SRAM array containing the proposed memory bitcell is functional at 160mV of supply voltage.

To maintain the clarity of the discussion, the 10T cell is referred as the memory cell reported in [11]. The proposed Schmitt Trigger (ST) based 10 transistor memory cell is referred as 'ST bitcell' hereafter. The rest of the paper is organized as follows. In section II the proposed ST bitcell operation is described. In section III comparison is done among 6T/8T/10T/ST bitcells for various SRAM metrics. Measurement results are discussed in section IV. Section V concludes the paper.

2. SCHMITT TIGGER BASED 10T SRAM

The proposed Schmitt Trigger based (ST) 10 transistor SRAM cell focuses on making the basic inverter pair of the memory cell robust. At very low voltages, the cross-coupled inverter pair stability is of concern. To improve the inverter characteristics, Schmitt trigger configuration is used. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition [13]. This adaptation is achieved with the help of a feedback mechanism. One possible implementation of the Schmitt trigger is shown in Fig. 2(a). This structure is used to form the inverter of our memory bitcell. The basic Schmitt trigger requires 6 transistors instead of 2 transistors to form an inverter. Thus it would need 14 transistors in total to



(a) Schmitt trigger (b) Proposed SRAM bitcell

Fig. 2. Schmitt trigger based 10 transistor SRAM bitcell

form an SRAM cell, which would result in large area penalty. Since PMOS transistors are used as weak pull-ups to hold the '1' state, feedback mechanism in PMOS pull up branch is not used. Feedback mechanism is used only in the pull down path. The complete schematic for the proposed ST bitcell is shown in Fig. 2(b). Transistors PL-NL1-NL2-NFL form one ST inverter while PR-NR1-NR2-NFR form another ST inverter. AXL and AXR are the access transistors. The positive feedback from NFL/NFR adaptively changes the switching threshold of the inverter depending on the direction of input transition. During a read operation, (with V_L= 0 and V_R=V_{DD} say) due to voltage divider action between the access transistor and the pull down NMOS, the voltage of V_L node rises. If this voltage is greater than the switching threshold (trip point) of the other inverter, the contents of the cell can get flipped resulting in a read failure event [4]. In order to avoid a read failure, the feedback mechanism should increase the switching threshold of the inverter PR-NR1-NR2. Transistors NFR and NR2 raise the voltage at node V_{NR} and increase the switching threshold of the inverter storing '1'. Thus Schmitt trigger action is used to preserve the logic '1' state of the memory cell. The proposed ST bitcell utilizes differential operation giving better noise immunity [13]. It requires no architectural change compared to the conventional 6T cell architecture.

3. SIMULATION RESULTS

HSPICE simulations are done using 0.13µm logic process technology. Typical NMOS (PMOS) V_T is 350mV (300mV). 6T/8T/10T and the proposed ST bitcell are compared for various SRAM metrics. For the 6T cell, the transistor widths $W_{PU}/W_{AX}/W_{PD}$ are 160nm/240nm/320nm respectively. For the ST bitcell extra transistors NFL/NL2 are of minimum width (160nm) while other transistors are having the same dimensions as that of the 6T cell.

3.1 Read stability:

For improving the cell stability, the proposed ST bitcell focuses on making the inverter pair robust. Feedback transistors NFL/NFR increase the inverter switching threshold whenever the node storing '1' is discharged to the '0' state. Thus cell asymmetry changes based on the direction of the node voltage transition. Fig. 3(b) shows the inverter characteristics indicating the cell asymmetry. When V_L is increased from 0 to V_{DD}, the other node (V_R) makes a transition from V_{DD} to 0.

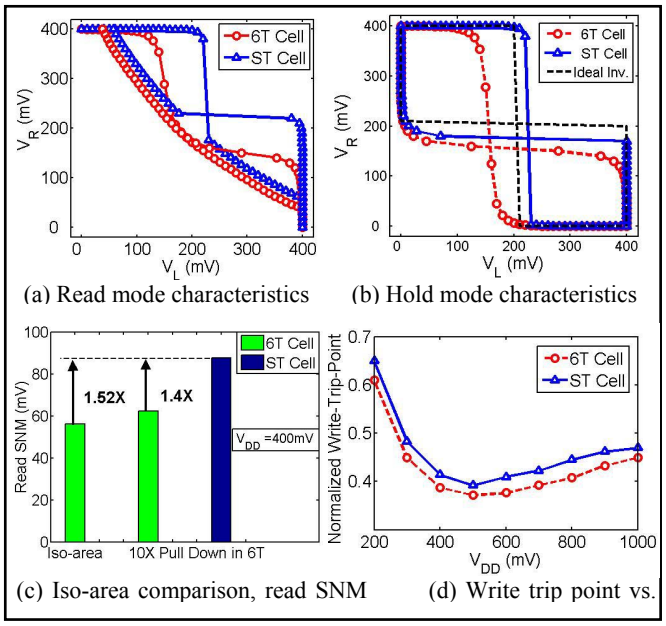


Fig. 3. Read stability, write-ability comparison

During this time, the feedback mechanism due to NFR-NR2 raises the node voltage V_{NR} and tries to maintain the logic '1' state of the V_R node. This gives a near-ideal inverter characteristics essential for robust memory cell operation. Static Noise Margin (SNM) is estimated graphically as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve [14]. The ST bitcell has 1.56X improvement in the read SNM, compared to the conventional 6T counterpart, shown in Fig. 3(a) (V_{DD}=400mV). Since the proposed ST bitcell consumes more area (~34%) compared to the 6T cell it is worthwhile to compare these cells under "iso-area" condition. For iso-area condition, the cell ratio (W_{PD}/W_{AX}) in the 6T cell is increased so as to have same area as that of the ST bitcell. Under iso-area condition, the 'minimum sized' ST bitcell gives 1.52X improvement in read SNM than the 6T cell (V_{DD}=400mV) shown in Fig. 3(c). At higher supply voltages (i.e. in super-threshold regime), the drain current varies ~linearly with the gate voltage. Transistor upsizing increases the SNM considerably. However in the sub-threshold regime drain current depends exponentially on the gate voltage. Any device upsizing will result in marginal change in the drain current. Thus in the sub-threshold region, SNM is relatively independent of the device sizing. [15]. Even with 10X increased cell ratio (W_{PD}/W_{AX}) in the 6T cell, the proposed 'minimum area' ST bitcell shows 1.4X improvement in the read SNM shown in Fig. 3(c). This shows that for a stable SRAM cell operating at a lower supply voltage, a feedback mechanism can be more effective than simple transistor upsizing as in a conventional 6T cell.

3.2 Write-ability:

Write-ability of a bitcell gives an indication on how easy or difficult it is to write to the cell. Write-trip-point defines the maximum bitline voltage (V_{BL}^{MAX}) needed to flip the cell content [16]. Higher the bitline voltage, easier it is to write to the cell. Normalized write-trip-point is defined as: Normalized-Write-Trip-Point = V_{BL}^{MAX}/ VDD. Initially consider V_L = '0' and V_R = '1'.

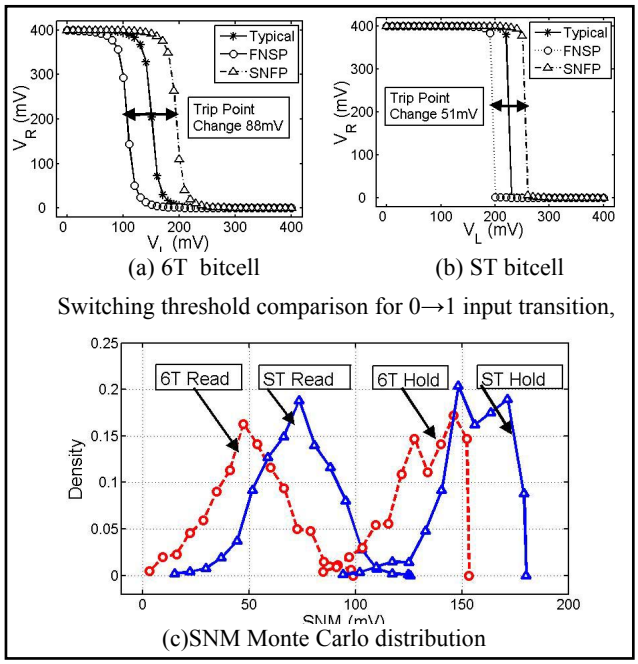


Fig. 4. Process variation tolerance comparison

In order to write a '0' to node V_R, BR is pulled down to ground, BL is kept at V_{DD} and word line is turned ON. The voltage at node V_R is determined by the size of the pull up transistor (PR) and the access transistor (AXR). The other node V_L is transitioning from '0' state to '1' state. During this transition, the feedback transistor (NFL) is OFF. This results in the reduced pull down transistor strength at node V_L due to stacked (series connected NL1-NL2) NMOS transistors. Compared to the 6T cell, the effective strength of pull down transistor is reduced in the ST bitcell during 1 →0 input transition. Hence, the node storing '0' (V_L) gets flipped at a much higher voltage giving higher write-trip-point compared to the 6T cell shown in Fig. 3(d). Unlike the conventional 6T cell, the ST bitcell gives better read stability as well as better write-trip point. Schmitt trigger action gives better read stability while reduced pull down strength (series connected NMOS) and absence of feedback during 1→0 input transition enables ST bitcell to achieve better write-trip point than the 6T cell.

3.3 Process variation tolerance:

The proposed ST bitcell has a built-in process variation tolerance. Fig. 4(a) and 4(b) show the inverter voltage transfer characteristics (during a 0→1 input transition) for a standard 6T cell and the proposed ST bitcell for typical and skewed process corners. (FNSP= Fast NMOS, Slow PMOS; SNFP=Slow NMOS and fast PMOS). As V_L varies from V_{GND} to V_{DD}, the feedback transistor NFR raises the node voltage V_{NR} above V_{GND}. It increases the switching threshold when V_R is transitioning from '1' state to '0' state. This results in sharp inverter characteristics shown in Fig. 4(b). In a Fast NMOS process corner, threshold voltage of NMOS (NFR) would reduce. This would increase the intermediate node voltage (V_{NR}) closer towards V_{DD} and would increase the switching threshold of the inverter compared to conventional inverter. Similarly for a slow NMOS corner, NMOS (NFR) V_T would increase, feedback effect not significant and switching threshold would be reduced compared to conventional inverter.

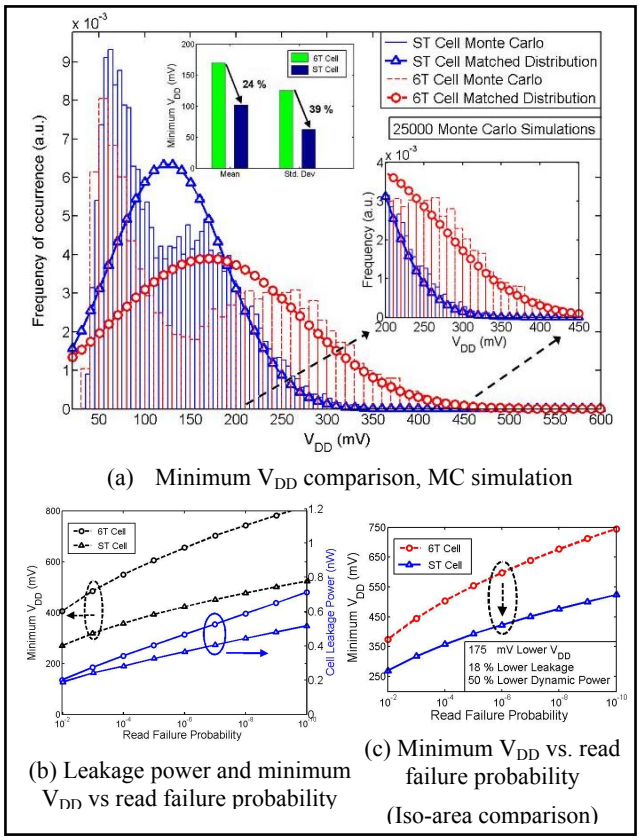


Fig. 5 Low voltage operation, read failure probability comparison

The variation in switching threshold is 51mV in the ST bitcell compared to 88mV in the 6T cell indicating improved process variation tolerance (Fig. 4(a)-(b)). In order to evaluate the effectiveness of the ST bitcell under process variations, Monte-Carlo simulations (V_{DD} = 400mV) are done for read and hold case (Fig. 4(c)). It is observed that the proposed ST bitcell gives higher mean read (hold) SNM 1.44X (1.22X) compared to the 6T cell. Further, standard deviation in read (hold) SNM is reduced by 13% (11%) compared to the standard 6T cell (V_{DD}=400mV).

3.4 Low voltage/low power operation:

Supply voltage is reduced gradually from the nominal value of 1.0V to the point where memory cell contents are about to flip or reach a metastable point. For estimating the minimum V_{DD} required during read operation, 25000 Monte Carlo simulations are done. The distribution of minimum V_{DD} required to avoid a read failure is shown in Fig. 5(a). The tail of the matched distribution is shown in the inset. The proposed ST bitcell requires 24% lower average V_{DD} with 39% reduced standard deviation than the 6T cell. Based on the minimum V_{DD} distributions, cumulative distributive functions (CDF) are calculated and the minimum V_{DD} required for a given read failure probability is estimated. It is observed that, at iso-read-failure probability, the ST bitcell operates at a lower voltage than the conventional 6T cell. Minimum V_{DD} versus the read failure probability is shown in Fig. 5(b). Due to reduced V_{DD}, the ST bitcell consumes lower leakage power compared to the 6T cell in spite of 4 extra transistors.

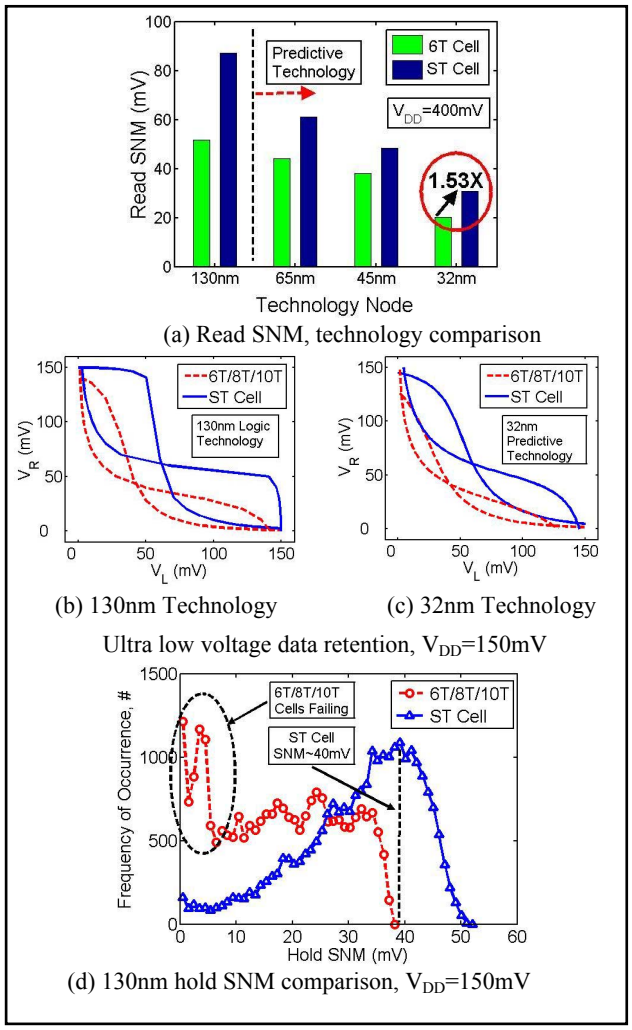


Fig. 6. Read SNM comparison vs. technology nodes,

As the access transistor size in the ST bitcell is the same as the 6T cell, the bit-line and word-line capacitance is unchanged. This reduces read/write dynamic power dissipation quadratically ($C_L V_{DD}^2 f$) with reduced V_{DD}. Note that the difference in 'minimum V_{DD}' increases as the read failure probability decreases. Again, Monte Carlo simulations are done for a read operation under "iso-area" condition. The minimum V_{DD} required to avoid a read failure at iso-area and iso-read-failure probability (for this example 10^{-6}) show that, the proposed ST bitcell operates at 175mV lower supply voltage than the 6T cell. The ST bitcell operating at a lower supply voltage gives 18% saving in the leakage power and 50% savings in the dynamic power (at read failure probability of 10^{-6} and at iso-area condition) shown in Fig. 5(c).

3.5 Scalability:

Using predictive technology models, the proposed ST bitcell is compared with the 6T cell to verify the effectiveness of our technique in scaled technologies [17]. The ST bitcell consistently predicts better read and hold SNM compared to the 6T cell in scaled technologies. For 32nm technology, using predictive models, the ST bitcell predicts 1.53X improvement in read SNM compared to its 6T counterpart (V_{DD} =400mV) shown in Fig. 6(a) [17-18].

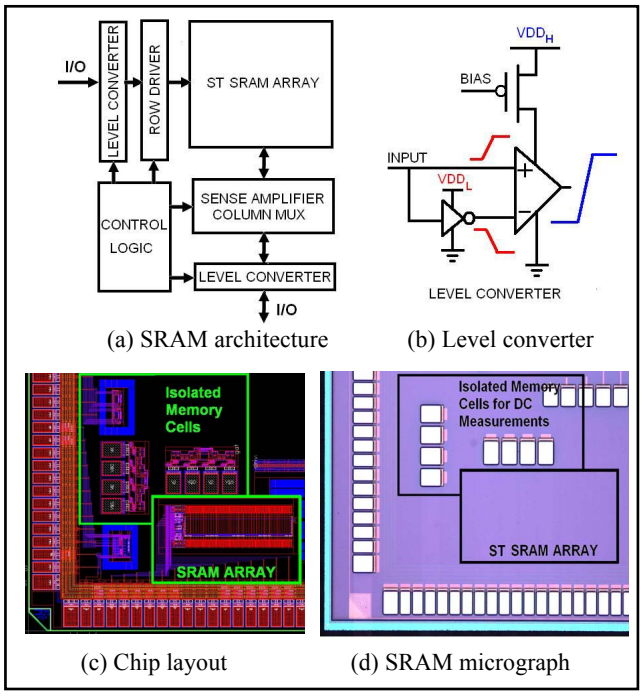


Fig. 7. SRAM architecture and test chip photographs

Thus proposed ST bitcell can be scalable into future technologies. As technology scales, with increased process variations, the memory cell failure probability would worsen at lower supply voltages. In such a scenario, the proposed ST bitcell having built-in feedback mechanism would be useful for low V_{DD} operation.

3.6 Ultra low voltage operation:

During the standby mode, the supply voltage of a memory array is reduced to minimize the leakage power. However the supply voltage can not be reduced arbitrarily as memory bitcells would not be able to hold the contents of the cell. This voltage is termed as data retention voltage (DRV) [19]. 6T/8T/10T/ST bitcells are compared for Hold SNM at low supply voltages. As 6T, 8T and 10T cells use the same inverter pair, they would show almost same characteristics in hold mode. Fig. 6(b) and Fig. 6(c) show the inverter characteristics for 6T/8T/10T and the proposed ST bitcell at ultra low V_{DD} (150mV). It is clearly seen that the proposed ST bitcell exhibits superior transfer characteristics than 6T/8T/10T cells. In 0.13µm technology hold SNM for 6T/8T/10T cell is 18mV, while the proposed ST bitcell exhibits 42mV hold SNM (2.3X better) (Fig. 6(b)). Similarly, for 32nm technology node, the proposed ST bitcell predicts >2X improvement in the hold SNM (at V_{DD} = 150mV) compared to the 6T cell (Fig. 6(c)). Thus the proposed ST bitcell could be useful for ultra low voltage data retention in future nano-scaled technologies. The Monte Carlo simulations for the hold SNM are done at 150mV V_{DD} (25000 simulations). The hold SNM distribution for various cells is shown in Fig. 6(d). At 150mV of V_{DD} 6T/8T/10T cells no longer exhibit a Gaussian distribution, but a uniform distribution. Also, the hold failure probability is very high with many cells having hold SNM close to zero, indicating possible data flipping. The proposed ST bitcell results in better hold SNM; close to $V_{DD}/4$. The SNM distribution for the proposed ST bitcell is skewed towards the higher values. Due to built-in process variation tolerance (one NMOS (NFL/NFR) opposing

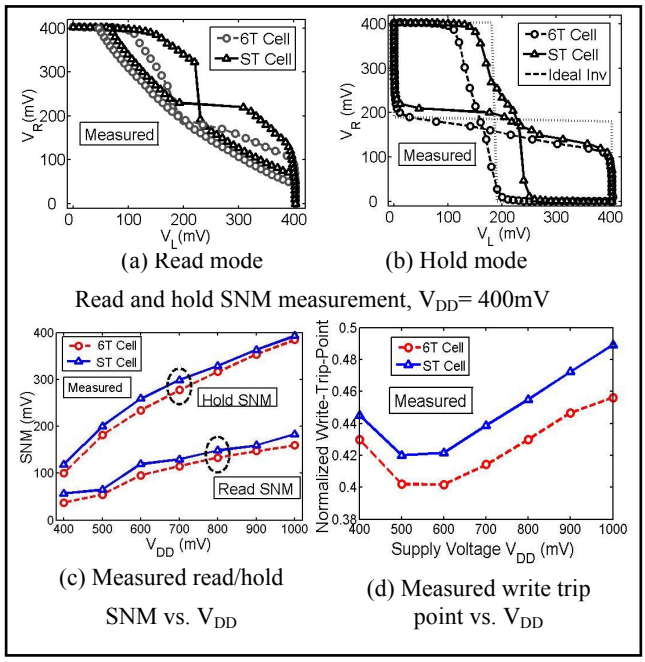
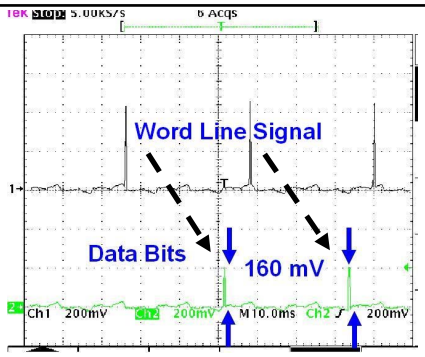


Fig. 8. SNM, write trip point measurement results

another NMOS (NL1/NR1)) the distribution is tight. Also notice that the hold failure probability in the ST bitcell is very low compared with 6T/8T/10T cells. This analysis points out the importance of the stability of cross coupled inverter pair for robust SRAM bitcell operating at ultra low voltages.

4. MEASUREMENT RESULTS

A test chip containing 256X16 cells (4Kbits, 1 block) SRAM array has been fabricated using 0.13 µm CMOS technology. Fig. 7(a) and Fig. 7(b) show the implemented SRAM architecture with the level conversion stage at I/O. A level shifter converts low V_{DD} data (400mV) to high V_{DD} data (1.2V) to drive the package capacitance (~10-20pF). The level converter consists of an operational amplifier (op-amp) operating in open loop configuration and is driven by the complementary input signals (Fig. 7(b)). In addition, buffers are implemented to bypass the level conversion stage in order to monitor various internal signals operating at low supply voltages. For SNM measurements, separate isolated 6T/ST memory bitcells with each transistor having 10 fingers are fabricated. The width of each finger is kept the same as the width of a bitcell transistor used in the SRAM array. As threshold voltage (V_T) depends on the width of the transistor, the finger structure would generate transistors having same V_T as that used in the SRAM array. The transfer characteristics of a memory bitcell depends on "relative sizes" (or relative current driving capabilities) of the transistors. Increasing the number of fingers of all transistors equally would not change the transfer characteristics and hence would not alter SNM values. Chip layout and photograph are shown in Fig. 7 (c) and (d). Fig. 8(a) and Fig. 8(b) show the measured butterfly curves (V_{DD} =400mV) for the read and hold case. The proposed ST bitcell shows near-ideal inverter characteristics compared to the 6T cell as seen in the hold case. Thus the proposed ST bitcell consistently gives higher read and hold SNM for different supply voltages; shown in Fig. 8(c).



160mV functional SRAM; Word line and data bits waveform, The X axis (time) unit is in ms, indicating a delay between the internal word line signal and the output data bits.

Fig. 9. Functional SRAM; measurement results

Measured SNM results match well with the simulation results. It is found that the write-trip-point in the ST bitcell is higher than 6T cell shown in Fig. 8(d). Thus the proposed ST bitcell clearly demonstrates improved read stability as well as improved write-trip point than the 6T cell. Array leakage power and the maximum frequency of operation are measured for various supply voltages. At 400mV the SRAM operates at 620KHz consuming 0.146µW. Supply voltage is reduced gradually to verify the SRAM array functionality. Various rows in two different test chips are checked for the correct read operation. The proposed ST bitcell array is functional at 160mV shown in Fig. 9. The data waveforms are captured by enabling the buffer chain in the I/O buffer. The level converter stage is bypassed in this case. The top waveform in Fig. 10 shows the monitored word line signal and the bottom waveform shows the observed data bits at the output pin.

5. CONCLUSIONS

We proposed a Schmitt trigger based fully differential, robust, 10 transistor SRAM bitcell suitable for sub-threshold operation. The proposed ST bitcell achieves higher read SNM (1.56X) compared to the conventional 6T cell (V_{DD}=400mV). The robust memory cell exhibits built-in process variation tolerance that gives a tight SNM distribution across the process corners. It incorporates fully differential operation and hence it does not require any architectural changes from the present 6T architecture. At iso-area and iso-read-failure probability, the proposed ST bitcell operates at a lower V_{DD} with lower leakage and reduced read/write power. Simulation results show that the ST bitcell can retain the data at low supply voltage (150mV). An SRAM array functional at 160mV supply voltage is demonstrated using 0.13µm CMOS technology.

ACKNOWLEDGEMENTS

This work is sponsored in part by Semiconductor Research Corporation (SRC) and DARPA. Authors would like to thank Nanoelectronics Research Lab members and Dinesh Somasekhar of Intel for useful technical discussions.

REFERENCES

[1] H. Soeleman and K. Roy; "Ultra-low power digital subthreshold logic circuits," *Proc. of International symposium on Low power Electronics and Design*, pp. 94-96, 1998

[2] N. Yoshinobu, H. Masahi, K. Takayuki and K. Itoh; "Review and future prospects of low-voltage RAM circuits," *IBM journal of research and development*, vol. 47, No. 5/6, pp.525-552, 2003

[3] A. Bhavnagarwala, X. Tang, and J. Meindl; "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 658-665, April 2001.

[4] S. Mukhopadhyay, H. Mahmoodi and K. Roy; "Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nanoscaled CMOS," *IEEE Transactions on Computer Aided Design*, pp 1859-1880, December 2005.

[5] A. Raychowdhury, S. Mukhopadhyay and K. Roy; "A feasibility study of subthreshold SRAM across technology generations," *Proc. of International Conference on Computer Design*, pp. 417-422, October 2005

[6] H. Kawaguchi, Y. Itaka and T.Sakurai; "Dynamic leakage cutoff scheme for low-voltage SRAMs," *VLSI Circuit Symposium, pp.140-141*, June 1998

[7] S. Ghosh, S. Mukhopadhyay, K. Kim and K. Roy; "Self-calibration technique for reduction of hold failures in low-power nano-scaled SRAM," *Proc. of 43rd Design Automation Conference*, pp. 971-976, July 2006.

[8] I. Carlson, S. Andersson, S. Natarajan and A. Alvandpour; "A High Density, Low Leakage, 5T SRAM for Embedded Caches," *Proc. of 30th European Solid State Circuits Conference*, pp.215-218, September 2004

[9] R. Aly, M. Faisal and A. Bayoumi; "Novel 7T sram cell for low power cache design," *Proc. of IEEE SOC Conference*, pp.171-174, 2005.

[10] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. R. Montoye, L. Sekaric, S. McNab, W. Topol, C. Adams, K. Guarini and W. Haensch; "Stable SRAM Cell Design for the 32 nm Node and Beyond," *Symposium on VLSI Technology*, pp.128-129, 2005

[11] B. H. Calhoun and A. P. Chandrakasan; "A 256kb Sub-threshold SRAM in 65nm CMOS," *Proc. of International Solid State Circuits Conference*, pp. 628-629, February 2006

[12] J. Chen, L. Clark and T. Chen; "An Ultra-Low-Power Memory With a Subthreshold Power Supply Voltage," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2344 – 2353, October 2006

[13] J. Rabaey, A. chandrakasan and B. Nikolic; "*Digital Integrated Circuits: A Design perspective,*" 2nd edition, New Jersey, Prentice-Hall Inc., 2002.

[14] E. Seevinck, F. List, and J. Lohstroh, "Static noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 5, pp. 748–754, Oct. 1987

[15] B.H Calhoun and A.P. Chandrakasan; "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1673 – 1679, July 2006

[16] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene; "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2577 – 2588, Nov. 2006

[17] W. Zhao et al., "New generation of Predictive Technology Model for sub-45nm design exploration," *Proc. of International Symposium on Quality Electronics Design*, pp. 585-590, 2006.

[18] Predictive Technology Models: available online at http://www.eas.asu.edu/~ptm/

[19] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu and J. Rabaey; "SRAM leakage suppression by minimizing standby supply voltage," *Proc. of International Symposium on Quality Electronic Design*, pp. 55-60, March 2004.