Architecture et Système 2020-2021

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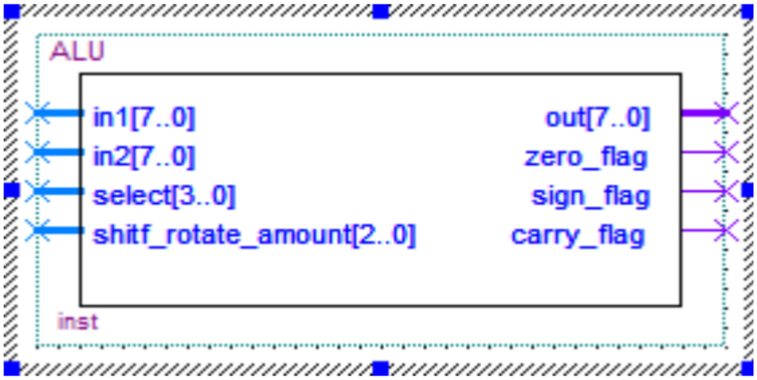
TP 5 : Arithmetic logic unit and Register File

ALU

We are going to design an eight-bit ALU that we will use it in the final phase of the project. The inputs of of this ALU are as the following :

- Two 8-bit inputs as the operands.
- One 4-bit input to select the operation.
- One 3-bit input to determine the numbers of bits that we use it for the **SHIFT** and **ROTATE**.

And for the outputs, we have one 8-bit output for the result, a zero flag, a sign flag, and a carry flag.

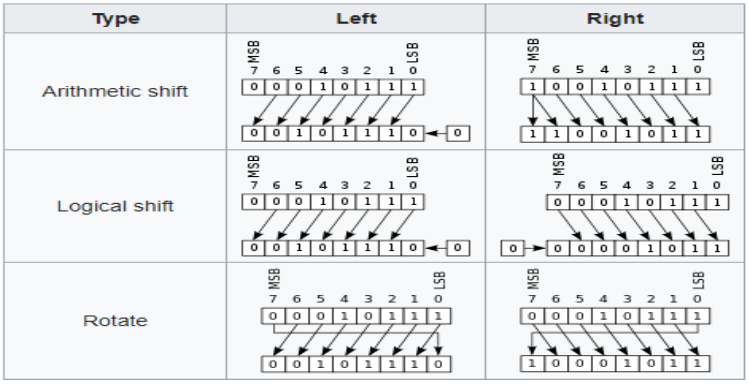


The zero flag (rep. sign flag) will be set once the the result of ALU is zero (resp. negative). And we set carry flag if one of the following occurs :

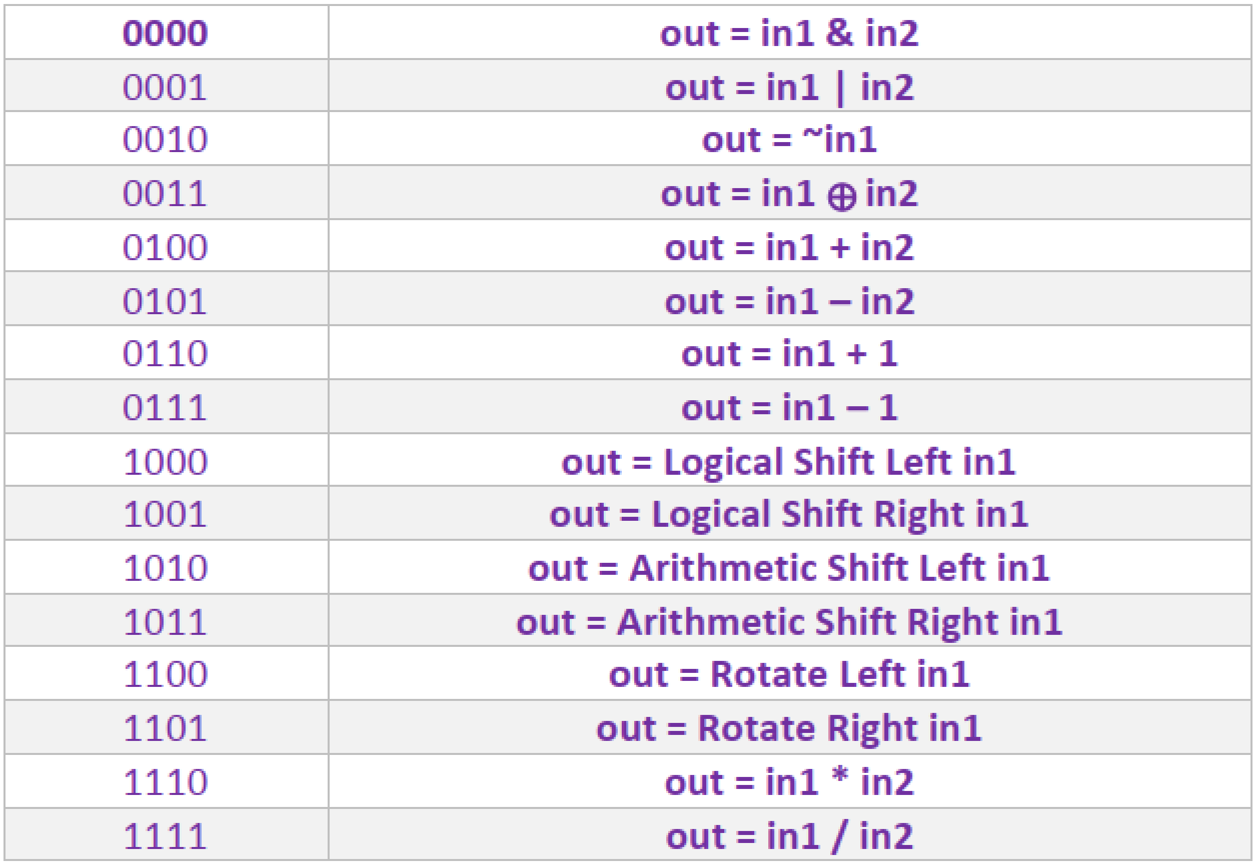
- There is a carry resulting from an addition operation.
- There is a borrow resulting from a subtraction operation.
- The overflow bit resulting from a binary shift operation or a rotate operation is 1.

Once you are done with the design of the ALU, try some functional simulation.
**Note that you can only use the primitives of Quartus.

Bit shift examples for an eight-bit ALU :



Here you can see the ALU Instructions :



0000	**out = in1 & in2**
0001	out = in1 | in2
0010	out = ~in1
0011	out = in1 ⊕ in2
0100	out = in1 + in2
0101	out = in1 – in2
0110	out = in1 + 1
0111	out = in1 – 1
1000	out = Logical Shift Left in1
1001	out = Logical Shift Right in1
1010	out = Arithmetic Shift Left in1
1011	out = Arithmetic Shift Right in1
1100	out = Rotate Left in1
1101	out = Rotate Right in1
1110	out = in1 * in2
1111	out = in1 / in2

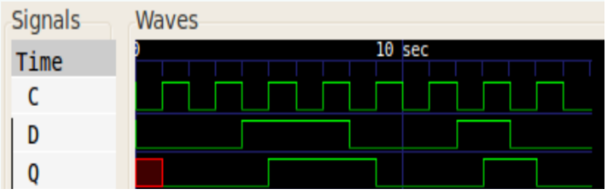
Register File

A register is a set of flip-flops which each flip-flop capable of storing one bit of information. So, an n-bit register has a group of n flip-flops. In addition to flip-flops, a register may have logical gates that perform certain data-processing tasks. The flip-flops hold the binary information and the gates control when and how new information is transferred into the register.

Question 1

Using D Flip-Flops, construct an 8-bit register with a parallel load and also a clock input. That is to say this register has eight data input bits $D_0, \cdot, D_7$ and eight data output bits $O_0, \cdots, O_7$. In addition the register has a **Load** input which, when at logic level 1, sets the flip-flops data inputs to the register's eight input bits. When Load is at logic level 0, the eight flip-flops have their outputs fed into their inputs. This effectively disables loading from the four input bits.

Reminder : A simulation of D flip-flop with the clock input :



Question 2

A register file is an array of registers. Design an eight-bit register file that has four registers. The block diagram of it is as follows :

register file.png

Description of the register file :

— The output of two registers, which are determined by **address-read1** and **address-read1**, will be sent to **data-read1** and **data-read2** respectively.

— If **write-enable** is 1 and the edge of the clock is rising, then the **data-write** will be sent to the register with the address "**address-write**".

— If **clr** is 1, then the output of all registers will be zero.