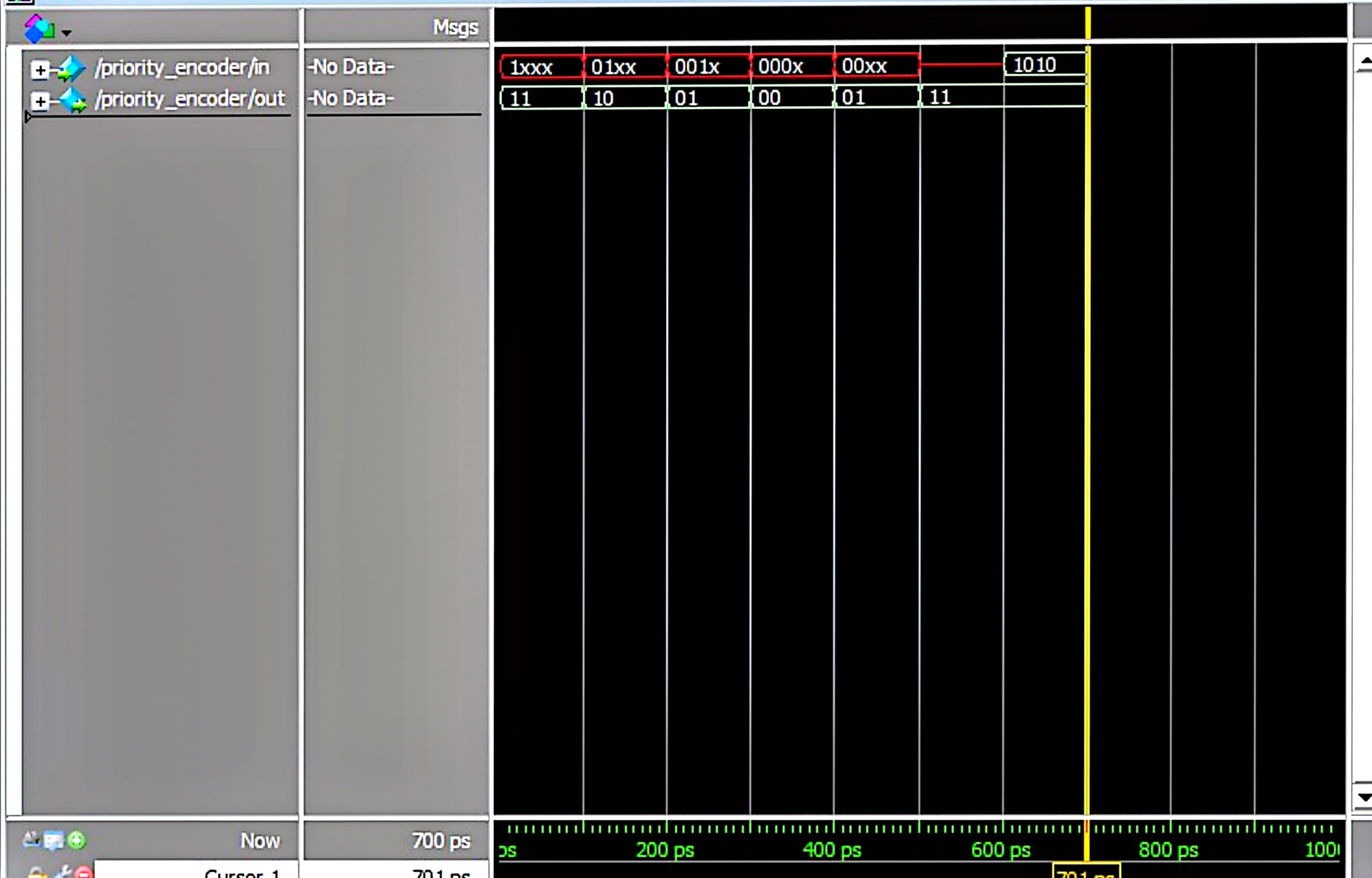


```
1  module Task_1_ALU (A, B, opcode, ALU_Out);
2      input [3:0] A ;
3      input [3:0] B;
4      input [1:0] opcode;
5      output reg [3:0] ALU_Out;
6
7
8      always @(*) begin
9          case (opcode)
10             2'b00: ALU_Out = A + B;
11             2'b01: ALU_Out = A - B;
12             2'b10: ALU_Out = A | B;
13             2'b11: ALU_Out = A ^ B;
14             default: ALU_Out = 4'b0000;
15          endcase
16      end
17 endmodule //Task_1_ALU
```

		Msgs
+ /Task_1_ALU/A	0001	
+ /Task_1_ALU/B	0001	
+ /Task_1_ALU/opcode	01	
+ /Task_1_ALU/ALU_...	0000	

```
1  module priority_encoder (  
2      input [3:0] in,  
3      output reg [1:0] out  
4  );  
5  
6      always @(*) begin  
7          casex (in)  
8              4'b1xxx: out = 2'b11;  
9              4'b01xx: out = 2'b10;  
10             4'b001x: out = 2'b01;  
11             4'b000x: out = 2'b00;  
12             default: out = 2'b00;  
13         endcase  
14     end  
15  
16 endmodule //priority_encoder
```

≡ mux_4x1_Gates.v

```
1  module mux_4x1_Gates (in0,in1,in2,in3,c0,c1,out);
2
3      input in0, in1, in2, in3,c0,c1;
4      output out;
5      wire [5:0] w;
6
7
8      not not0 (w[0],c0);
9      not not1 (w[1],c1);
10
11
12     and and0 (w[2],in0,w[0],w[1]);
13     and and1 (w[3],in1,c0,w[1]);
14     and and2 (w[4],in2,w[0],c1);
15     and and3 (w[5],in3,c0,c1);
16
17     |
18
19     or or0 (out,w[2],w[3],w[4],w[5]);
20
21     endmodule //mux_4x1_Gates
```

