Task_1.v

```
1   module Task_1(A,B,C,D,E,F,sel,out,out_bar);
2   input A,B,C,D,E,F,sel;
3   output out,out_bar;
4   wire ABC,DEF;
5   assign ABC=A&B&C;
6   assign DEF=~(D^E^F);
7   assign out=(sel)?DEF:ABC;
8   assign out_bar=~out;
9   endmodule
```

Task_2.v

```
1    module Task_2(a,b,c,f);
2    input a,b,c;
3    output f;
4    wire a_xor_b,b_xnor_c;
5    assign a_xor_b=a^b;
6    assign b_xnor_c=~(b^c);
7    assign f=a_xor_b&b_xnor_c&c;
8
9    endmodule
```