



Faculty of Engineering and Material Sciences  
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## Modulation Techniques for Inverter Control

A thesis submitted in partial fulfilment of the  
requirements for the degree of Bachelor of Science (B.Sc.)  
in Mechatronics Engineering

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# **Declaration**

This is to certify that:

- (i) the thesis comprises only my original work toward the Bachelor of Science (B.Sc.) at the German University in Cairo (GUC),
- (ii) due acknowledgement has been made in the text to all other material used

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19 May, 2024

# Abstract

Pulse Width Modulated Voltage Source Inverters (PWM-VSI) are widely utilized in motor drive and other three-phase power conversion applications as voltage/current sources with controllable output frequency and magnitude. The choice of pulse width modulation method strongly affects the inverter energy efficiency, waveform quality, and voltage linearity. However, the dependence of these performance characteristics on the modulator type is not well understood. This thesis attempts an in-depth analysis and investigation of different modulation techniques, and their waveform quality, and voltage linearity characteristics of the modern PWM methods. The analytical results aid the development of simple, yet highly efficient modulation strategies and control algorithms. A Discontinuous PWM method (DPWM) which minimizes the switching losses and provides a wide voltage linearity range has been developed. Algorithms which combine the superior performance characteristics of the DPWM method with other high performance PWM methods have been established. Modulator voltage linearity characteristics have been thoroughly investigated. Both the per carrier cycle voltage linearity and per output voltage fundamental cycle voltage linearity characteristics have been analytically modeled. In the nonlinear modulation (overmodulation) range, the influence of the modulator non linearity on the drive steady state and dynamic performance has been thoroughly investigated. As a result high performance overmodulation algorithms could be developed for various drives and applications. With a strong emphasis on the overmodulation region performance of both open loop voltage feedforward controlled drives and closed loop current controlled drives, all the performance characteristics could be enhanced by employing the novel modulation methods and control algorithms. The theory has been supported with computer simulations and laboratory experiments and strong correlation has been obtained. In addition to developing new modulation methods

and control algorithms, this thesis establishes analytical and graphical methods for the study, performance evaluation, and design of the modern PWM methods. Also simple techniques for generating the modulation waves of the high performance PWM methods are described.

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# List of Symbols

- $A$ : Ampere
- $A_c$ : Amplitude of the Carrier wave
- $A_r$ : Amplitude of the Reference wave
- $f_s$ : Switching frequency
- $I_1$ : Magnitude of fundamental current
- $I_C$ : Collector Current
- $I_D$ : Drain Current
- $K$ : Amplification factor
- $L$ : Inductance of the inductor
- $L_m$ : Length of the channel
- $M_a$ : Amplitude Modulation index
- $M_f$ : Frequency Modulation ratio
- $R$ : Resistance
- $S$ : Second
- $T$ : Period of square wave
- $T_c$ : Period of Carrier Wave
- $T_k$ : Period of the waveform

- $T_0$ : Duration of the zero vector
- $T_1$ : Duration of the first vector activation
- $T_2$ : Duration of the second vector activation
- $T_s$ : Period of sampling
- $V$ : Volt
- $V_{AN}$ : Phase Voltage of point A
- $V_{AO}$ : Voltage between point A and point O
- $V_{BN}$ : Phase Voltage of point B
- $V_{BO}$ : Voltage between point B and point O
- $V_{CE}$ : Voltage between the Collector and the Emitter
- $V_{CN}$ : Phase Voltage of point C
- $V_{CO}$ : Voltage between point C and point O
- $V_{DC}$ : DC voltage source
- $V_{DS}$ : Voltage between Drain and the Source
- $V_{GE}$ : Voltage between the Gate and the Emitter
- $V_{GS}$ : Voltage between the Gate and the Source
- $V_{MOSFET}$ : Voltage between the MOSFET section
- $V_{NO}$ : Voltage between point N and point O
- $V_{dc}$ : DC voltage source
- $V_{drift}$ : Voltage between the drift region
- $V_{ra}^*$ : Reference signal a with common mode injection
- $V_{rb}^*$ : Reference signal b with common mode injection

- $V_{rc}^*$ : Reference signal c with common mode injection
- $V_{ref}$ : Reference voltage vector
- $|V_{ref}|$ : Reference voltage vector magnitude
- $V_{Pn+}$ : Voltage between the collector junction
- $V_{th}$ : Threshold Voltage
- $W$ : Width of the channel

## Greek Symbols

- $\Omega$ : Ohm
- $\mu_n$ : Electron Mobility
- $\pi$ : Constant approximately equals  $\frac{22}{7}$
- $\alpha^\circ$ : Angle of the reference vector
- $\delta$ : On duration in symmetrical sampling
- $\delta'$ : Off duration in symmetrical sampling
- $\gamma(\phi)$ : Common mode zero sequence
- $\gamma(\phi)_{SVPWM}$ : Common mode zero sequence for Space vector pulse width modulation
- $\gamma(\phi)_{THIPWM}$ : Common mode zero sequence for Third harmonic injection
- $\phi$ : Phase Angle
- $\psi$ : Phase shift angle between voltage and the current

# List Of Abbreviations

**AC** Alternating Current

**BJT** Bipolar junction transistor

**CB** Carrier Based

**CSI** Current Source Inverter

**DC** Direct Current

**DPWM** Discontinuous Pulse Width Modulation

**DTC** Direct torque control

**EV** Electric Vehicle

**FOC** Field oriented control

**GDPWM** Generalized Discontinuous Pulse Width Modulation

**IGBT** Insulated Gate Bipolar Transistor

**MLIS** Multi Level Inverters

**PMSM** Permanent Magnet Synchronous Motor

**PRC** Proportional resonant controller

**PWM** Pulse Width Modulation

**RMS** Root Mean Square

**SHE** Selective Harmonic Elimination

**SPWM** Sinusoidal Pulse Width Modulation

**SVPWM** Space Vector Pulse Width Modulation

**TWIPWM** Third Harmonic Injection Pulse Width Modulation

**VSI** Voltage Source Inverter

# Chapter 1

## Introduction

### 1.1 Introduction

Pulse-width modulation (PWM) is one of the core technologies of power electronic converters and it was initially proposed to allow inverters to output sinusoidal AC voltage and current. Up to now, it has been applied to the AC–AC matrix converters and PWM rectifiers. Although PWM has been proposed for nearly 60 years since 1964, due to the continuous emergence of various new power electronic converters and the increasing requirements for the quality of converters' output voltage and current, PWM is still one of the most popular research directions in the field of power electronics, and continues to attract attention and interest of researchers. PWM methods are usually divided into sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM) according to the principle of generation. For inverters, there are three main indicators to evaluate the performance of PWM method: (1) Harmonic content; (2) Utilization of the DC voltage; and (3) Switching times. Besides, with the development of PWM method, it is necessary to consider the difficulty of the control method implementation, the possibility of soft switching, and the ability to suppress common mode (CM) and differential mode (DM) interferences simultaneously. In today's world, inverters play a vital role in various aspects of our daily lives. They are extensively utilized in motor control systems of electric vehicles, renewable energy sources, HVAC (Heating, Ventilation, and Air Conditioning) systems, and more. The development of efficient and high-performing control algorithms and strategies

for inverters has become an intriguing challenge.

The optimization and enhancement of inverter control algorithms and strategies are of utmost importance to achieve optimal performance and efficiency. These advancements are crucial for maximizing the utilization of inverters in different applications, ensuring seamless integration with various systems, and meeting the ever-increasing demands of modern technologies.

In the context of electric vehicles, inverters are responsible for controlling the power flow from the battery to the motor, enabling efficient operation and enhancing overall vehicle performance. By devising sophisticated control algorithms, it becomes possible to achieve smoother acceleration, regenerative braking, and improved energy management, thereby enhancing the driving experience and extending the vehicle's range. In the realm of renewable energy, inverters play a

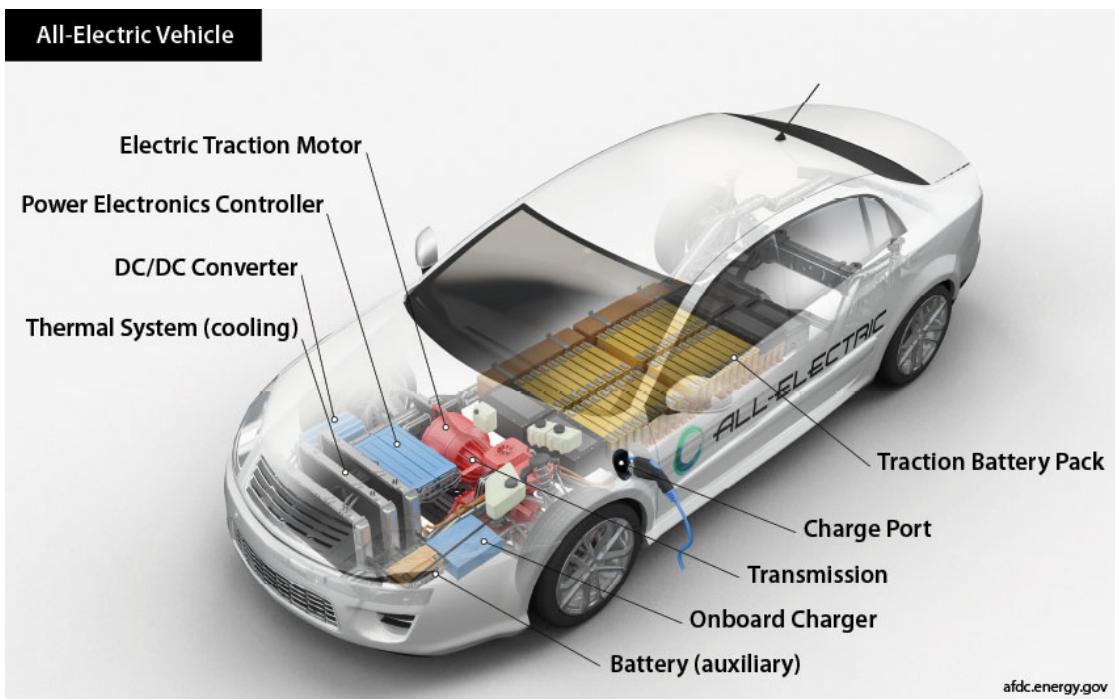


Figure 1.1: Electric Vehicle with Traction Inverter.

crucial role in converting the direct current (DC) produced by solar panels or wind turbines into alternating current (AC) for grid integration. The development of advanced control strategies helps optimize power conversion efficiency, ensure grid stability, and facilitate the seamless integration of renewable energy sources

into the existing power infrastructure. In HVAC systems, inverters are utilized

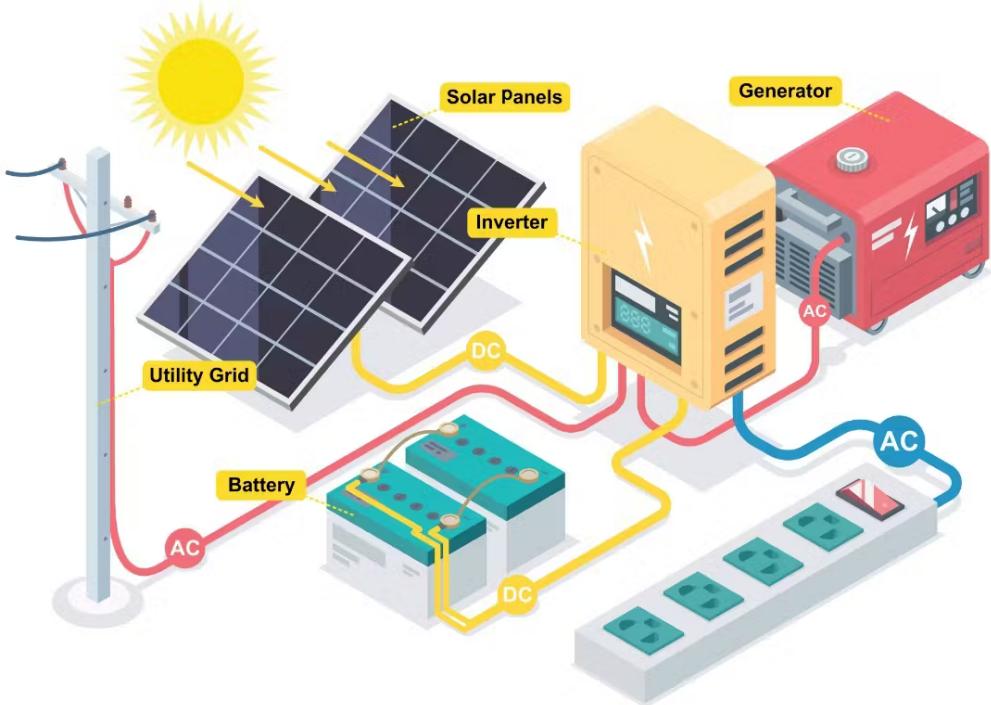


Figure 1.2: Renewable Energy Photovoltaic system with Inverter.

to regulate the speed and power consumption of compressors and fans. By implementing intelligent control algorithms and strategies, it becomes feasible to achieve precise temperature control, reduce energy consumption, and enhance overall system performance, leading to improved comfort and energy efficiency in residential, commercial, and industrial buildings.

## 1.2 Motivation

In today's world, where energy consumption is ever-increasing, even minor advancements in energy performance, efficiency, generation, or transmission can have a profound impact on overall outcomes. From electrical motor driving systems to renewable energy generation processes, the demand for enhanced energy conversion technologies is becoming increasingly urgent, particularly with the anticipated depletion of non-renewable fuel resources in the coming decades. In this context,

power electronics play a pivotal role, facilitating efficient energy conversion in various applications.

The rise of electric vehicles (EVs) represents a significant shift towards sustainable transportation practices, driven by the pressing need to address environmental degradation and reduce reliance on fossil fuels. In the realm of EV propulsion systems, inverters serve as critical components, orchestrating the generation of commands to the motor, the primary driver of vehicle propulsion.

Modulation techniques emerge as essential tools for optimizing inverter performance in EV systems. By dynamically controlling the switching patterns of power semiconductors, modulation techniques enable efficient power conversion, improved motor control, and enhanced overall system performance. Therefore, investigating and implementing diverse modulation techniques tailored specifically for electric vehicle systems (EVS) applications become imperative.

This thesis aims to delve deeply into the exploration and practical implementation of various modulation techniques for inverter control in EV systems. By conducting comprehensive analyses and innovative implementations, the goal is to advance the field of sustainable transportation technologies. Through insightful research and practical solutions, this thesis endeavors to contribute to the ongoing efforts towards achieving more efficient and environmentally friendly electric vehicle propulsion systems.

### 1.3 Objective

The primary objective of this research is to achieve a pure AC sinusoidal waveform from an inverter. To accomplish this, the performance of the inverter will be thoroughly investigated using various modulation techniques. A comparative analysis will be conducted to evaluate the wave quality, DC-bus utilization, and switching losses associated with each technique.

By employing the power of MATLAB/Simulink software, the chosen modulation techniques will be implemented and analyzed. This software provides a robust platform for simulating and assessing the performance of different modulation strategies.

The research aims to identify the most effective modulation technique that can deliver a high-quality sinusoidal waveform while optimizing the utilization of the

DC-bus and minimizing switching losses. Such findings are crucial for enhancing the overall efficiency and performance of inverters in various applications.

## 1.4 Summary

This thesis focuses on the study and comparison of different modulation techniques for inverters. It explores their digital implementation using a digital microcontroller and compares the results with simulation outputs.

Chapter II provides a comprehensive literature review, discussing pulse width modulation (PWM) and its various methods, including inverter over-modulation.

Chapter III delves into the field of power electronics, examining the distinctions between power electronic switches and providing an overview of inverters. Additionally, it sheds light on the concept of harmonics from a macroscopic perspective.

Chapter IV presents a detailed explanation of the fundamentals of sinusoidal pulse width modulation (SPWM) and its simulations with its hardware implementation.

Chapter V illustrates the foundation of space vector pulse width modulation (SVPWM) and demonstrates its simulation and hardware implementation. Chapter VI explores the fundamental concepts of Discontinuous Pulse Width Modulation (DPWM) and provides a detailed examination of its various modes and the broader concept of Generalized Discontinuous Pulse Width Modulation (GDPWM).

Finally, Chapter VII summarizes the key findings and results of the thesis.

# Chapter 2

## Literature Review

Over the past 150 years, significant advancements have been made in the field of electric machines, while power electronics has seen about 75 years of progress. The areas of micro-electronics/macro-electronics and control fields have also experienced advancements over the last 50 years. These breakthroughs have greatly influenced the development of state-of-the-art PWM-VSI (Pulse-Width Modulation Voltage-Source Inverter) drives, which are now cost-effective, efficient, compact, and reliable high-performance systems.

Due to the interdisciplinary nature of PWM-VSI drives and their consistent demand in the market, researchers worldwide have been actively engaged in their study. As a result, a substantial amount of literature has been accumulated, particularly focusing on PWM methods and drive control algorithms. Thousands of publications have been dedicated to this subject, reflecting the immense attention and interest these drives have garnered.

In the following section, we will provide an overview of the historical progression of early drives before delving into a comprehensive description of PWM-VSI drives.

### 2.1 A Brief History of Inverters Drives

The nineteenth century marked significant milestones in the field of electric machines following the discoveries of electricity and magnetism laws. Inventions such as the DC machine, synchronous machine, induction machine, and squirrel cage rotor induction machine revolutionized the industry. The induction machine, in

particular, became widely utilized and remains a cornerstone of industrial applications.

Over time, the electric machines field has experienced continuous progress, resulting in machines with improved structure, performance characteristics, and reduced manufacturing costs. As a deeper understanding of machine characteristics emerged, high-performance control methods were developed.

In the early 1890s, Ward Leonard established speed regulation of DC machines through armature voltage control. Subsequently, methods for high-performance speed, position, and torque control of DC machines were established. In the first half of the twentieth century, the constant operation principle of voltage feedforward controlled open-loop AC induction motor drives was established. However, it was not until the late 1960s that high-performance control methods for induction machines were developed. Understanding the complex dynamics of induction machines required mathematical methods, and the Field Orientation Control (FOC) method was established in the late 1960s as a high-performance control approach for induction motor drives. FOC enabled induction machines to approach or surpass the performance of DC machines while offering cost reduction and ruggedness. More recently, Permanent Magnet (PM) AC machines have emerged as superior

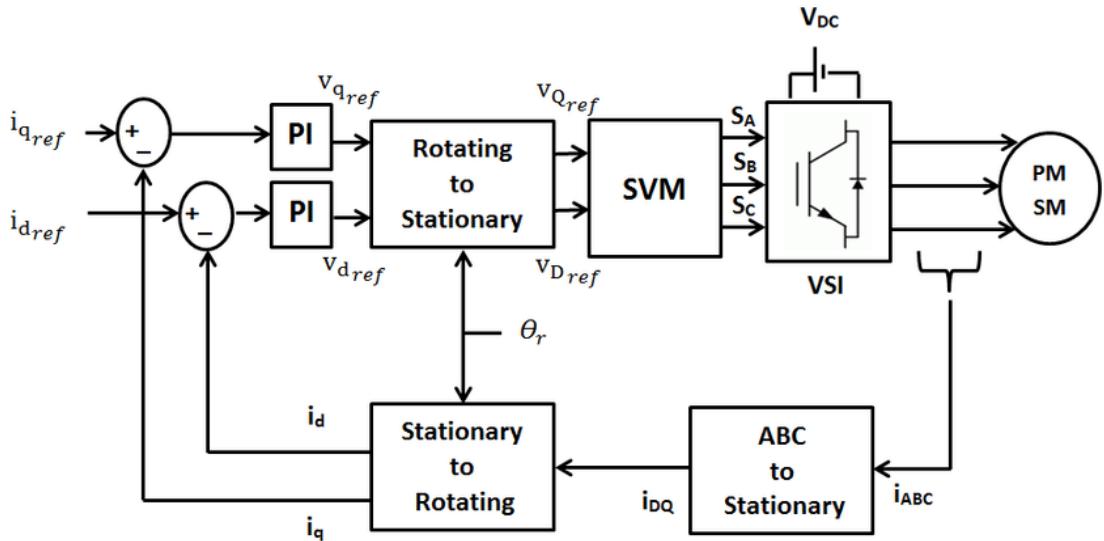


Figure 2.1: Field Oriented Control of PMSM.

alternatives for high-performance servo drive applications due to their high energy

density, efficiency, and reliability. Additionally, observer-based shaft encoderless motion control methods for AC machines have been under development since the late 1970s.

The progress in electric machines and their control has been continuous and accelerating. However, advanced control methods necessitate sophisticated controllers and, more importantly, power electronic converters with controllable characteristics. Therefore, advancements in the field of electric machines have closely paralleled developments in power electronics, control theory, and analog/digital microelectronics.

## 2.2 Modulation Methods

In the on-off current controlled drives and torque/flux regulated DTC drives, the switching signals are available immediately at the controller outputs. However, in PI controller based (linear) current regulated drives, and voltage feedforward controlled drives the switching signals are determined in an additional block termed as the "modulation" block. In this block the reference voltages are evaluated and proper switching device gate logic signals are generated for all the three inverter legs. Since voltage source inverters employ switching devices with finite turn-on time and turn-off time characteristics, inverter switching losses are inevitable. Because the switching losses strongly affect the energy efficiency, size and reliability of an inverter, a modulation method with high performance is desirable. Therefore, the modulation method choice is significantly important. Of the variety of modulation methods, the carrier based PWM methods and the programmed pulse modulation method are the two most recognized methods. In the programmed pulse modulation methods the switching patterns are precalculated for a given performance optimization criteria and the commutation angles are stored in a memory array. During operation the memory array is accessed on-line through the drive controller to generate the inverter gating signals for a given reference voltage phase and magnitude value. Various performance optimization criteria have been considered in generating the commutation angle table. A harmonic elimination method which totally eliminates certain harmonics from the output waveform (typically the unwanted harmonics are the 5th, 7th, 11th, 13th etc.) was first developed by Turnbull [8] and later further investigated

by Patel and Hoft [8]. Following this work proposed an output current THD minimization criteria for optimizing the pulse pattern .Efficiency optimized pulse patterns, and torque ripple minimized pulse pattern have also been characterized. Utilizing such optimal switching patterns as a template. developed trajectory tracking methods which improve the dynamic performance of voltage feedforward drives . All the programmed pulse methods require large computer memory space and in most methods the number of pulses per fundamental cycle is limited to a small number, typically less than five switchings per phase and per quarter cycle. In particular, in the high voltage utilization range, the optimal angles near the peak of the fundamental component of the voltage become significantly close, with no sufficient room left for commutation or blanking time. Due to this fundamental limitation, the programmed modulation methods can not operate with high switching frequency. Therefore, they can not provide output waveforms with very low harmonic distortion waveform. The application of the programmed pulse methods is usually limited to very high power drives with power rating above a megawatt level low switching frequency is selected for low switching losses. Unlike the programmed pulse modulation methods, the carrier based PWM methods can operate with high switching frequency and they offer high wave- form quality and implementation advantages. Carrier based PWM methods employ the per carrier cycle volt-second balancing principle to program a desirable inverter output voltage waveform. The first important contribution in the carrier based PWM area was done by Schönung and Stemmler [8] in 1964 with the development of the sinusoidal PWM (SPWM) method. As shown in Fig.2.5, in this method the sinusoidal reference waveform (the modulation wave) of each phase and a periodic triangular carrier wave are compared and the intersection points determine the commutation instants of the associated inverter leg switches. The well established modulation theory indicates that for sufficiently high carrier frequency to modulation wave fundamental frequency ratio, the modulation waveform fundamental component magnitude and the inverter output voltage fundamental component magnitude are linearly related until the modulation wave magnitude becomes large and the sine and triangle intersections begin to disappear . Within the linear modulation range, the sinusoidal PWM method sub-carrier frequency harmonic content is significantly low, and the switching frequency is fixed. Due to its simplicity and its well defined harmonic spectrum which is concentrated at the carrier frequency, its

sidebands, and its multiples with their sidebands, the SPWM method has been utilized in a wide range of AC drive applications. However, the method has a poor voltage linearity range, which is at most 78.5 % of the six-step voltage fundamental component value, hence poor voltage utilization. Therefore, the zero sequence signal injection techniques that extend the SPWM linearity range have been introduced for isolated neutral load applications which comprise the large majority of AC loads [7].

## 2.3 Pulse width modulation techniques

In the realm of power electronic converters, the fundamental principle revolves around transforming electrical energy from one level of voltage, current, or frequency to another, employing semiconductor-based electronic switches. Unlike conventional electrical circuits where control elements operate within a linear active region, power electronic circuits typically feature switches that function solely in either a fully ON or fully OFF state.[9]

As the field of power electronics has advanced, various families of power electronic converters have emerged, often characterized by power level, switching devices, and topological origins. With significant improvements in semiconductor technology, offering higher voltage and current ratings alongside enhanced switching characteristics, the application areas of power converters have expanded considerably.

Modern power electronic converters boast numerous advantages, including high efficiency, low weight, compact dimensions, rapid operation, and high-power densities. The process of transitioning electronic devices within a power electronic converter from one state to another is termed 'modulation'. Each converter family aligns with specific modulation strategies designed to optimize circuit operation based on target criteria pertinent to that family.

Parameters such as switching frequency, distortion, losses, harmonic generation, and response speed are critical considerations in the development of modulation strategies for a particular converter family. While the ideal output voltage of a power inverter should ideally exhibit a pure sinusoidal waveform with minimal distortion, practical inverters typically yield a series of rectangular waveforms.[9] The principal challenge in controlling power inverters lies in achieving suitable modulation methods to govern the output rectangular waveforms for synthesizing

the desired waveforms effectively. Hence, modulation control methods become indispensable to attain the desired fundamental frequency voltage and minimize higher-order harmonics.

Pulse Width Modulation (PWM) stands as a cornerstone in modern converters, offering a high-speed modulation process spanning from a few kilohertz for motor control applications to several megahertz for resonant converters in power supply systems. Hence, it is imperative to delve into the principles and diverse topologies associated with PWM modulation.

### 2.3.1 Pulse width modulation

Pulse Width Modulation (PWM) stands as a cornerstone in the domain of power electronics, revered for its versatility and efficacy in controlling the alternating current (AC) output of power electronic converters. At its core, PWM entails the manipulation of converter switch duty cycles at high frequencies, enabling the attainment of desired average low-frequency output voltages or currents. For more than three decades, modulation theory has remained a focal point of research within the realm of power electronics, garnering unwavering attention and interest. As technology evolves and demands for efficient energy conversion intensify, PWM continues to be a pivotal area of exploration and innovation, poised to shape the landscape of power electronics for years to come.[\[10\]](#) In principle, all modulation schemes aim to create trains of switching pulses that have the same fundamental volt-second average as a target reference waveform at any instant. The major difficulty with these trains of switched pulses is that they also contain unwanted harmonic components that should be minimized. Hence, for any PWM scheme, the primary objective can be identified, which is to calculate the converter switching ON times, which creates the desired (low-frequency) target output voltage or current. Having satisfied this primary objective, the secondary objective for a PWM strategy is to determine the most effective way of arranging the switching process to minimize unwanted harmonic distortion, switching losses, or any other specific performance criterion [\[11\]](#).

The dc input to the inverter is chopped by switching devices in the inverter. The amplitude and harmonic content of the ac waveform is controlled by varying the duty cycle of the switches. The fundamental voltage  $V_1$  has a maximum amplitude

of  $\frac{4V_d}{\pi}$  for a square wave output, but by creating notches, the amplitude of  $V_1$  is reduced.[11]

Usually, the power switches in one inverter leg are always either in ON or OFF state. Therefore, the inverter circuit can be simplified into 3 two-position switches. Either the positive or the negative dc bus voltage is applied to one of the motor phases for a short time. PWM is a method whereby the switched voltage pulses are produced for different output frequencies and voltages. A typical modulator produces an average voltage value, equal to the reference voltage within each PWM period. Considering a very short PWM period, the reference voltage is reflected by the fundamental of the switched pulse pattern. The concept of pulse width modulation is shown in Figure 2.2 In the realm of Pulse Width Modulation (PWM),

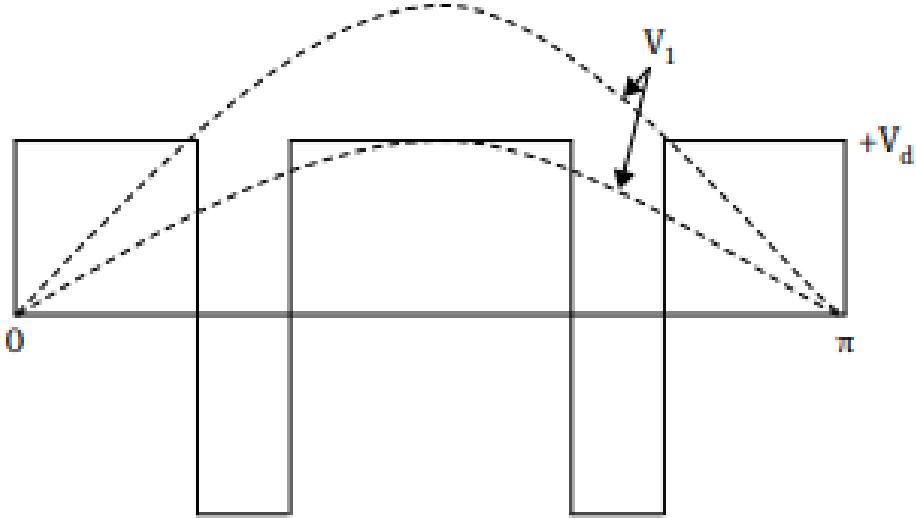


Figure 2.2: Principle of pulse width modulation.[1]

various techniques exist, each differing in their implementation methods. However, the overarching objective remains consistent: to generate an output voltage that, upon filtration, yields a high-quality sinusoidal waveform of the desired fundamental frequency and magnitude. Despite efforts, reducing overall voltage distortion caused by harmonics in inverters may pose challenges. However, through precise switching control, the magnitudes of lower-order harmonic voltages can often be mitigated, albeit potentially increasing higher-order harmonic voltages. Typically, this trade-off proves acceptable, as higher-frequency harmonic voltages can be effectively filtered using smaller filters and capacitors.

Many loads, such as motor loads, inherently suppress high-frequency harmonic currents, rendering external filters unnecessary in certain scenarios. Evaluating the voltage quality produced by a PWM inverter necessitates comprehensive harmonic analysis of the voltage waveform. Notably, by eliminating third and multiples of third harmonics from the pole voltage waveform, one can derive the corresponding load phase voltage waveform. Analyzing pole voltage waveforms of three-phase inverters offers a simpler visualization and analysis approach, facilitating harmonic analysis of load phase and line voltage waveforms. It is crucial to note that third and multiples of third-harmonic components present in pole voltage waveforms do not affect load phase and line voltages, underscoring the importance of this analytical approach.[\[1\]](#)

### 2.3.2 Basic pulse width modulation techniques

#### 1. Single pulse width modulation

In single PWM control, the width of the pulse is varied to control the inverter output voltage, and there is only one pulse half per cycle. By comparing the rectangular reference signal with the triangular carrier wave the gating signals are generated, as shown in Fig.2.3. The frequency of reference signal determines fundamental frequency of the output voltage. The advantages of this technique are that the even harmonics are absent due to the symmetry of the output voltage along the x-axis and that the Nth harmonics can be eliminated from inverter output voltage if the pulse width is made equal to  $\frac{2\pi}{n}$ . However, the disadvantages are that the output voltage introduces a great deal of harmonic content and that at a low output voltage, the distortion factors increases significantly.[\[8\]](#)

#### 2. Multiple pulse width modulation

In multiple PWM, multiple equidistant pulses are generated per half cycle, as depicted in Fig.2.4. By employing numerous pulses within each half cycle of the output voltage, the harmonic content can be mitigated. This technique leads to a reduction in the amplitudes of lower-order harmonics and significantly lowers the derating factor. However, there is a trade-off: while the fundamental component of the output voltage decreases, the amplitudes of higher-order harmonics increase notably, accompanied by an increase in

switching losses.[7]

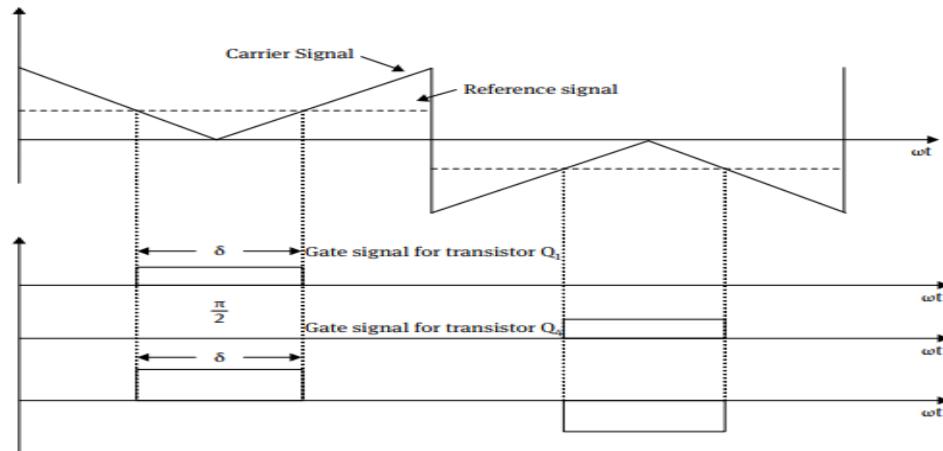


Figure 2.3: Single pulse width modulation.[1]

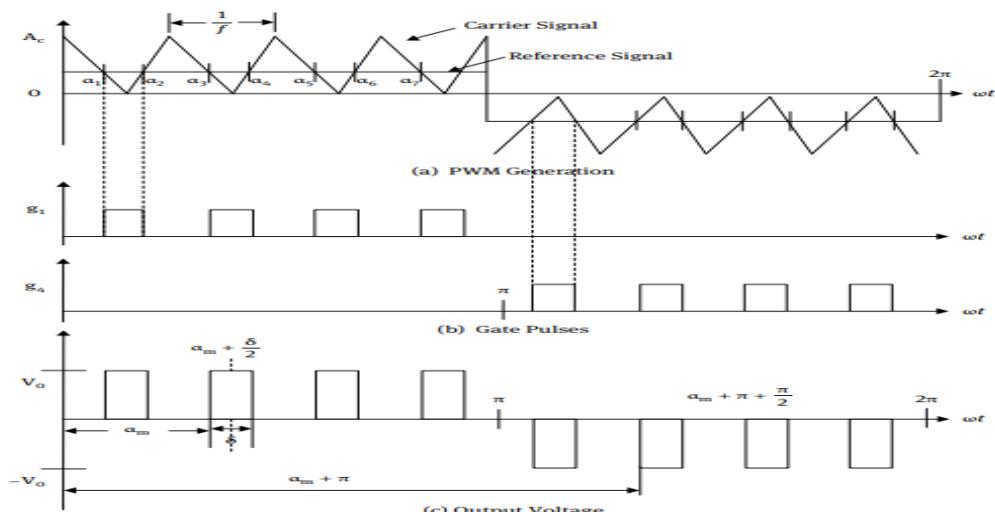


Figure 2.4: Multiple pulse width modulation.[1]

### 2.3.3 Sinusoidal pulse width modulation

In numerous industrial applications, Sinusoidal Pulse Width Modulation (SPWM) is commonly employed to regulate the inverter output voltage. SPWM ensures robust performance across the entire operational range, typically between 0 and 78% of the square wave operation value. If the modulation index surpasses this threshold, a linear relationship between the modulation index and the output voltage is compromised, necessitating over-modulation techniques.[3]

SPWM entails generating PWM outputs using a sine wave as the modulating signal. This method determines the ON and OFF instances of PWM signals by comparing a reference signal with a high-frequency triangular wave, as illustrated in Fig.2.5. The output voltage frequency corresponds to the modulation wave frequency, while the peak amplitude of the modulating wave dictates the modulation index, consequently controlling the RMS value of the output voltage. Altering the modulation index results in corresponding changes in the RMS value of the output voltage. SPWM significantly improves the distortion factor compared to alternative multi phase modulation methods. It effectively eliminates all harmonics up to  $(2n - 1)$ , where  $n$  represents the number of pulses per half cycle of the sine wave. Although the inverter's output voltage still contains harmonics, they are concentrated around the carrier frequency and its multiples.[7]

$$\text{Amplitude Modulation index: } M_a = \frac{\text{peak amplitude of } V_r}{\text{Peak value of } V_c}$$

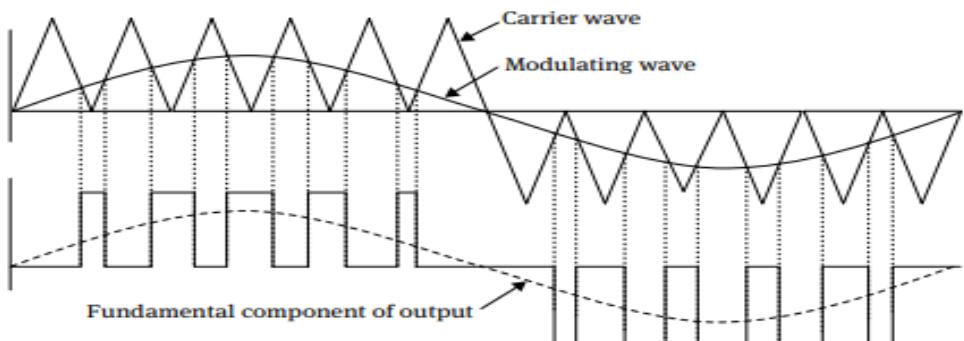


Figure 2.5: Sinusoidal pulse width modulation.[2]

where  $V_1$  is the fundamental frequency component of the pole voltage  $V_{AN}$ . The frequency modulation ratio  $M_f$ , which should be an odd integer, is the ratio between the PWM frequency and the fundamental frequency.

1. If  $m_f$  is not an integer, sub harmonics may exist at the output voltage.
2. If  $m_f$  is not odd, a DC component may exist, and even harmonics are present at the output voltage.
3.  $m_f$  should be a multiple of 3 for three-phase PWM inverter.
4. An odd multiple of three and even harmonics are suppressed.

#### 2.3.4 Advanced modulation techniques

##### 1. Trapezoidal modulation

By comparing a triangular carrier wave  $V_c$  with a reference trapezoidal wave  $V_r$  the switching instance to semiconductor devices are generated as shown in Fig.2.6 This type of modulation increases the peak fundamental output voltage up to  $1.05 V_{dc}$ , but output voltage contains lower-order harmonics.[1]

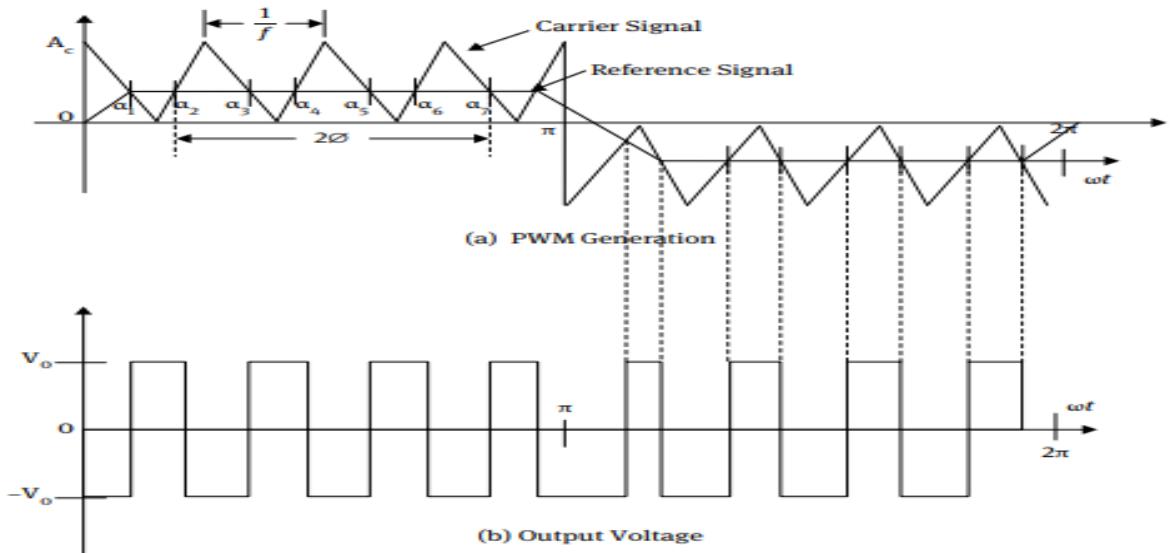


Figure 2.6: Trapezoidal modulation with the output voltage.[1]

## 2. Delta modulation

In this modulation, a triangular wave oscillates within a defined window  $\Delta v$  above and below the reference wave  $V_r$ . The output voltage is generated from the vertices of the triangular wave  $V_c$ , as illustrated in Fig.2.7. This modulation technique is also known as hysteresis modulation. Altering the frequency of the modulating wave while maintaining the slope of the triangular wave constant results in changes in the number of pulses and pulse widths of the modulated wave.

The fundamental output voltage can reach up to  $V_{dc}$  and is contingent upon the peak amplitude  $A_r$  and frequency  $f_r$  of the reference voltage. This modulation method enables control over the voltage-to-frequency ratio. The choice of a specific PWM technique depends on factors such as permissible harmonic content in the inverter output voltage, machine type, power level, and semiconductor switching devices utilized for a particular application.[12]

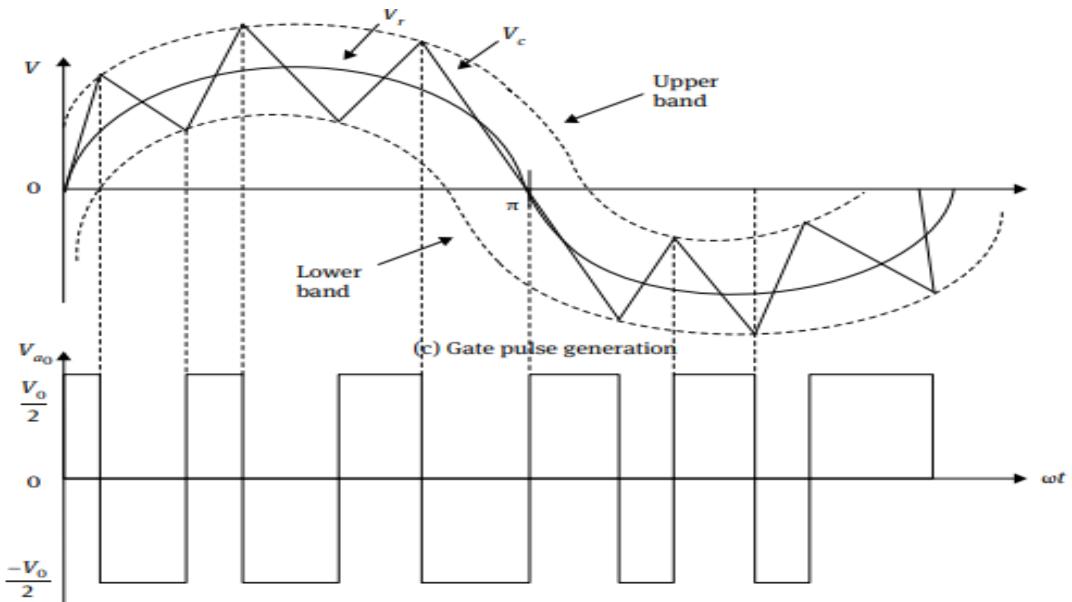


Figure 2.7: Delta modulation with the output voltage.[1]

## 3. Space vector pulse width modulation

Space Vector Pulse Width Modulation (SVPWM) is a relatively modern

and widely adopted technique for controlling motor devices. In SVPWM, the output voltage is approximated by selecting the nearest three output vectors that form a triangle enclosing the reference vector in the space vector diagram of the inverter. As the reference vector transitions between different regions, it can lead to sudden changes in the output vector. Moreover, it is necessary to compute the switching sequences and switching times of the states whenever the location of the reference voltage changes.[2]

#### 4. Selective harmonic elimination.

Selective harmonic elimination (SHE) techniques are widely employed in multilevel inverters (MLIs) for the calculation of switching angles in such a manner that the desired fundamental output voltage is obtained while simultaneously eliminating the dominant low order harmonics. In order to obtain this objective, the solution of nonlinear transcendental equations by means of algebraic, iterative and optimization techniques is required.[13]

#### 2.3.5 Advantages of Pulse Width Modulation Techniques

1. PWM techniques allow for the elimination or minimization of lower-order harmonics in the output voltage, reducing the need for extensive filtering.[1]
2. Both output voltage and frequency control can be achieved within a single power stage of the inverter, without requiring additional components.
3. The presence of a constant DC supply enables the parallel operation of multiple independent PWM inverters on the same rectifier power supply. PWM inverters exhibit superior transient response compared to quasi-square wave rectifiers.
4. The commutation capability of PWM inverters remains stable regardless of voltage and frequency settings, unlike variable DC-link inverters.
5. The system's power factor is improved, as a diode rectifier can be utilized on the line side.
6. PWM operation with a constant DC supply enables commutation even at low voltages, whereas a six-step inverter requires an auxiliary DC supply for

thyristor commutation at low output voltages.

7. Torque pulsations are minimized, even at low speeds.
8. Advanced PWM techniques effectively eliminate lower-order harmonics in motor current, low-speed torque pulsations, and cogging effects.[13]

## 2.4 Inverter Overmodulation

Since the DC link voltage of a PWM-VSI drive has a finite value, the voltage linearity of a modulator is confined to a limited voltage range. Therefore, the reference voltage-output voltage relation of a PWM-VSI drive is linear until the reference voltage magnitude exceeds the modulator linearity limit. As shown in Fig.2.9, for SPWM, when the reference voltage magnitude exceeds  $\frac{V_{Dc}}{2}$ , or equivalently 78.5 % of the six-step voltage fundamental component value, the sine-triangle intersections begin to disappear [1], and voltage pulses are dropped. Although during these intervals the corresponding upper switch operates with 100% duty cycle, it can not match the reference voltage and nonlinear relations result between the reference and output waveforms. The same condition repeats during the negative half of the cycle, and the large negative reference signal can not be matched by the inverter. The term "overmodulation" is adopted to distinguish this non linearity of a modulator and the "overmodulation region" is the voltage range beginning from where the non linearity begins and ending at the six-step operating point. Similar to SPWM, the other conventional modulators also have nonlinear gain relations in their overmodulation region. Although the range of linearity is wider for the popular zero sequence signal injection modulators, their linear voltage gain relations eventually ends at 90.7 % of the six-step voltage value. As a result, the controller reference voltage  $V_{ref}$  and the PWM-VSI output voltage  $V_{out}$  are not equal in the overmodulation range of operation for all the conventional carrier based modulators. In addition to this fundamental component gain non linearity, the reference voltage and output voltage phase angles are non-linearly related also. The implication of the phase and magnitude errors can be different and depend on the drive type.[3]

In voltage feedforward controlled constant  $\frac{V}{f}$  drivers ,entrance into the overmodulation region results in waveform quality degradation and voltage gain loss. As a

result, the harmonic losses and the current/voltage stress on the VSI active and passive components increase with significant increase in the torque ripples. The vector space based overmodulation illustrated in Fig.2.8 method developed by Habetler et al [14]. selects the largest voltage vector that is aligned with the reference vector and it was utilized in a dead beat current controlled drive. Another intuitive approach developed by Mochikawa et al. selects the voltage vector that is vectorially closest to the reference by projecting the reference voltage vector tip point on the closest inverter hexagon side. The one step optimal control characteristic of this approach was later, is limited in voltage capability (its output voltage is less than 95% of the six- step voltage).

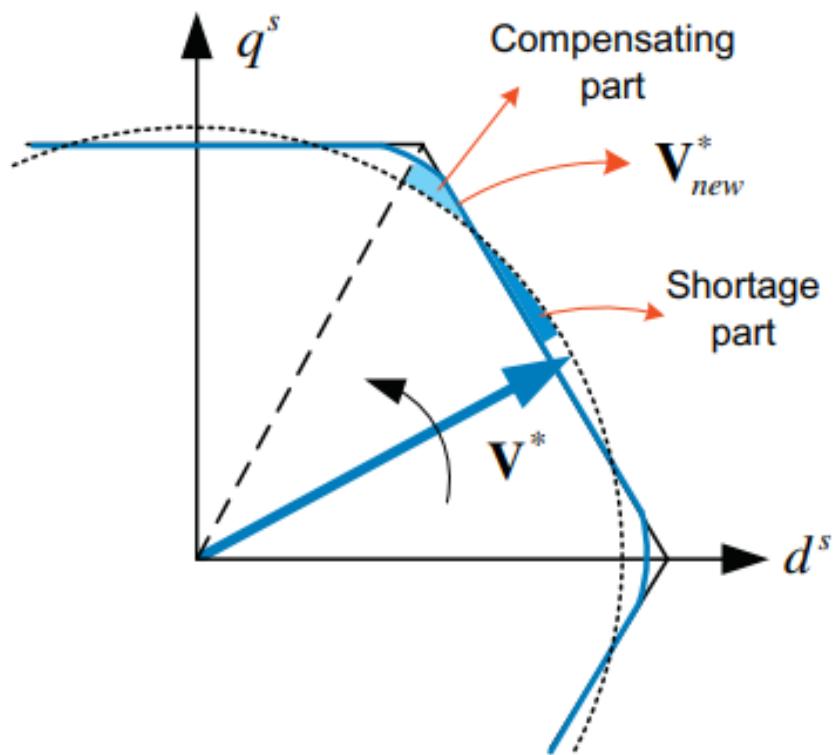


Figure 2.8: Overmodulation mode of space vector.[3]

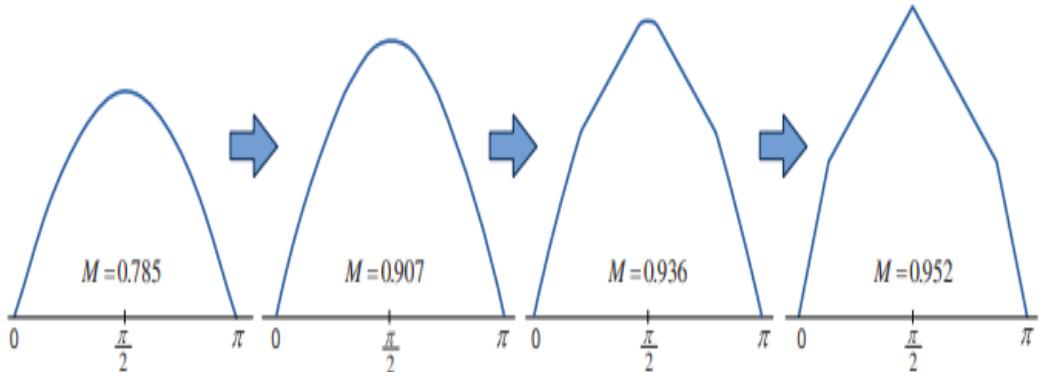


Figure 2.9: Phase voltage reference in the overmodulation mode.[3]

## 2.5 Summary

This chapter surveyed the literature on inverter drives, focusing on modulators and advanced PWM methods for inverter control. Inverter drives have experienced major breakthroughs, revolutionizing industrial processes with impressive performance advancements. However, despite numerous books and articles on PWM and drives, the field has not reached full maturation. While many switching algorithms have been developed and accepted, the performance of modern drives using advanced modulation and control methods is limited, especially in the over modulation region. Further progress is necessary to improve performance.

# Chapter 3

## Power Electronics

### 3.1 Power Electronic Switches

Power electronic switches serve as the writing instruments for power converter systems such as rectifiers, inverters, and choppers. These switches can be classified in several ways. One classification method is based on their controllability. Uncontrolled electronic switches, like power diodes, turn on and off according to the circuit's conditions. Semi-controlled electronic switches turn on based on circuit conditions and an external signal, but turn off based on the circuit conditions (e.g., thyristors). Controlled electronic switches, including IGBTs, MOSFETs, and GTOs, turn on and off based on circuit conditions and the presence of an external signal.

Another classification criterion is the power rating and switching frequency. These factors are inversely related. A higher switching frequency corresponds to a lower power rating, and vice versa. In power inverters, IGBTs and MOSFETs are commonly used switches. They are chosen based on the desired power level and switching frequency requirements.[15]

### 3.1.1 Metal Oxide Semiconductor Field Effect Transistor

The MOSFET, or metal–oxide–semiconductor field-effect transistor, is a fully controllable power electronic switch. It is a type of field-effect transistor commonly fabricated through controlled oxidation of silicon. The MOSFET operates as a voltage-controlled device, where the applied voltage between the gate and the source (VGS) regulates the current flow from the drain to the source. It is known for its high switching frequency among power electronic switches, particularly for low to medium power ratings. With an average switching frequency of 100 to 500 KHz [16].

Figure 3.1 depicts the MOSFET's physical structure, showcasing the source, gate, and drain terminals. It includes both n and p channels and utilizes a non-metal oxide material which is Silicon dioxide, and Z for channel width and L for channel length.[17]

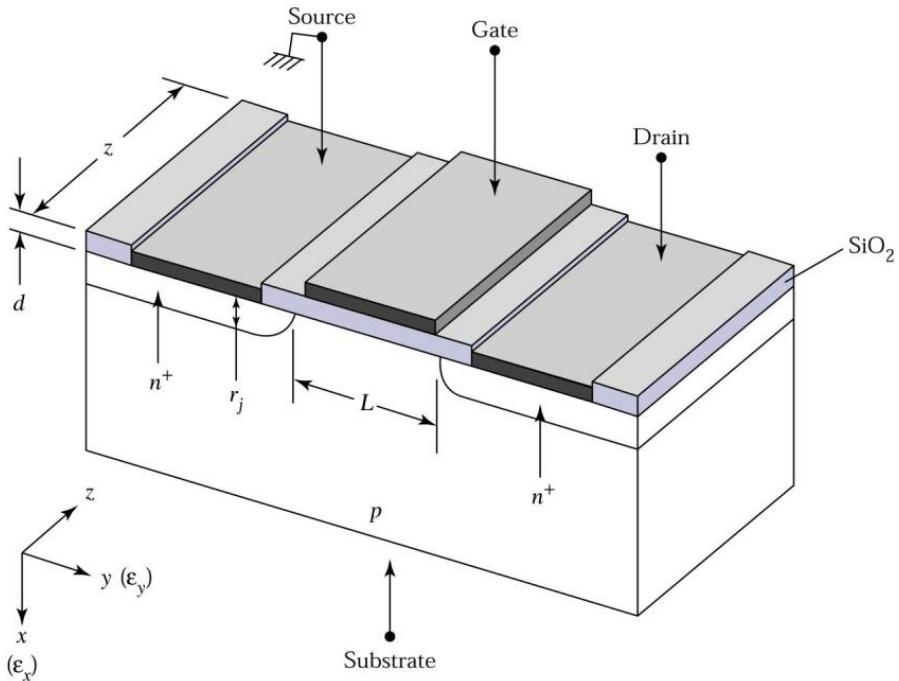


Figure 3.1: Physical structure of MOSFET in 3D space

Figure 3.2 represents the symbol of a MOSFET, where G represents the Gate, D represents the Drain, and S represents the Source.

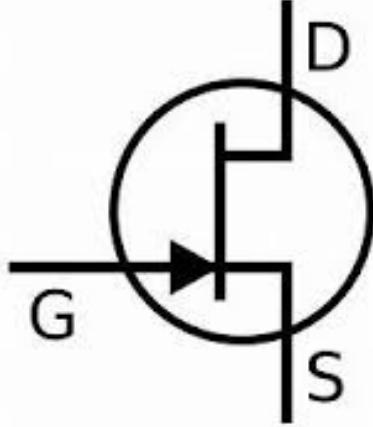


Figure 3.2: N-Channel MOSFET Circuit Symbol

MOSFET exhibit three distinct regions of operation: cutoff region, triode region, and saturation region, each serving different applications. In the cutoff region, the Gate-to-Source voltage  $V_{GS}$  is lower than the threshold voltage  $V_{th}$  of the device. As a result, no current flows between the Drain and Source ( $I_D = 0$ ). This region is employed for switch OFF functionality. In the triode region, the Gate-to-Source voltage  $V_{GS}$  exceeds  $V_{th}$ , while the Drain-to-Source voltage  $V_{DS}$  remains below the transistor's saturation voltage. In this region, current starts to flow from the Drain to the Source as the transistor operates as a switch ON. The magnitude of the current depends on the  $V_{GS}$  and  $V_{DS}$  values.<sup>[18]</sup> The saturation region is characterized by increasing  $V_{DS}$  beyond a point where  $V_{DS} > V_{GS} - V_{th}$ . In this region, the transistor operates in saturation, and the current  $I_D$  becomes relatively independent of  $V_{DS}$ . Amplifiers commonly utilize the saturation region due to its ability to provide consistent current levels. However, increasing  $V_{GS}$  can still impact the current  $I_D$ .

Figure 3.3 illustrates the I-V characteristics of the MOSFET, showcasing how it behaves in the three operation modes: cutoff, triode, and saturation. The graph demonstrates the influence of Gate-to-Source voltage  $V_{GS}$  and Drain-to-Source voltage  $V_{DS}$  on the Drain current  $I_D$ . Of particular importance for power inverters is the triode state, also known as the ohmic region. In this mode, the MOSFET acts as an efficient on-off switch.[18]

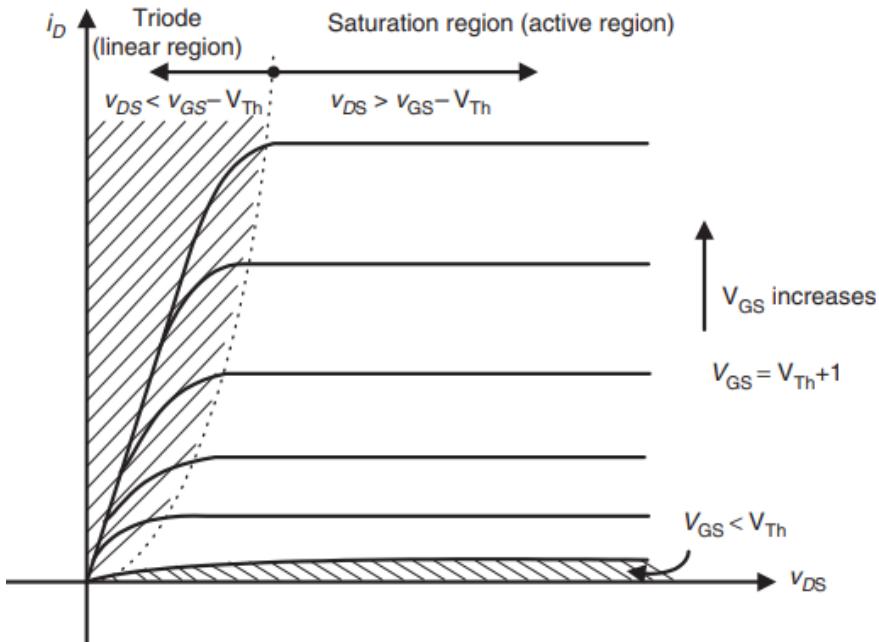


Figure 3.3: N-Channel MOSFET I-V characteristics [4]

To ensure the triode mode of operation in a MOSFET, certain conditions need to be satisfied. These conditions are:

$$V_{GS} > V_{th} \quad \text{and} \quad V_{DS} < V_{GS} - V_{th} \quad (3.1)$$

After confirming that the MOSFET is operating in the Triode region, the drain current can be mathematically approximated as follows:

$$I_D = K_s [2(V_{GS} - V_{th})V_{DS} - V_{DS}^2] \quad (3.2)$$

Where,

$$K_s = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L_m} \right) \quad (3.3)$$

The comprehensive exploration of the MOSFET's various operational regions is extensively elucidated within the referenced textbook [4]. However, our current discourse specifically focuses on the elucidation of the ohmic region

Figure 3.4 Demonstrate the input transfer characteristics of the MOSFET, elucidating the influence of the potential difference between the Gate and the Source  $V_{GS}$  on the Drain current  $I_D$ . Where  $C_{ox}$  is oxide capacitance per unit area,  $\mu_n$  is Electron Mobility and W,L is Width and the length of the channel respectively.

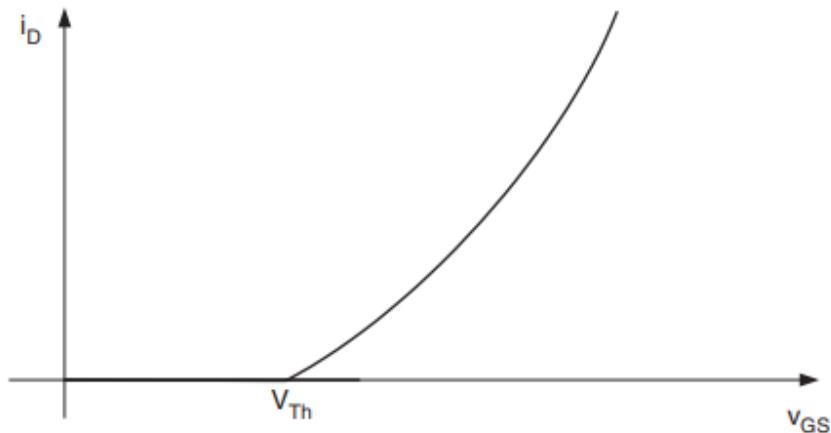


Figure 3.4: Input transfer characteristics for a N-Channel MOSFET [4]

The transfer characteristic links the drain current  $I_D$  to the input gate-source driving voltage  $V_{GS}$ . As the gate terminal is isolated from the other terminals drain, and source, the gate current remains negligible, thus not influencing device characteristics.

### 3.1.2 Insulated Gate Bipolar Transistor

The Insulated Gate Bipolar Transistor IGBT emerged as a significant advancement in power electronics during the early 1980s. It offered notable advantages over traditional devices like the Power Bipolar Junction Transistor BJT and the Power Metal-Oxide Semiconductor Field-Effect Transistor MOSFET, especially in motor drive applications. While the BJT is proficient in current control and handling high currents, it suffers from extended switching times during turn-off. Conversely, the MOSFET boasts swift switching speeds but faces limitations in high-power applications. IGBTs blend the desirable characteristics of both BJT and MOSFET. They showcase an impressive safe operating area, superior on-state attributes, and quick switching capabilities. Consequently, IGBTs have emerged as the preferred choice for power switches across a range of medium to high-power scenarios, ensuring efficient performance across various voltage and frequency requirements.[\[19\]](#)

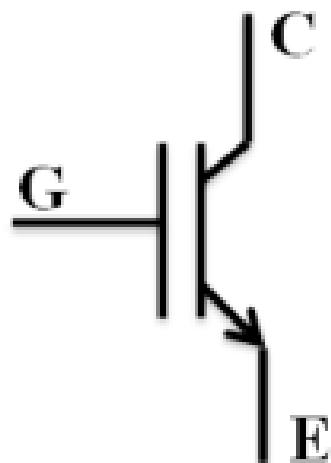


Figure 3.5: IGBT Circuit Symbol

Figure 3.5 Illustrate the circuit symbol of the IGBT, Where G is the Gate, C is the Collector, and E is the Emitter

## Construction and switching

IGBTs are three-terminal devices consisting of a gate, emitter, and collector. They operate using a combination of power BJT and n-channel MOSFET principles for control. The IGBT's structure, illustrated in Fig. 3.6, is composed of four layers of NPNP semiconductor, which form two parasitic transistors: an inactive NPN transistor and a low-gain PNP transistor. The NPN transistor's N-P junction is shorted by the MOSFET's source-metal connection. The majority of collector current  $I_C$  flows through the wide-based PNP transistor controlled by the MOSFET. To turn on the IGBT during the forward state, a positive voltage is applied to the collector, the emitter is grounded (or at a negative voltage), and a positive voltage greater than the threshold voltage is applied to the gate. Conversely, during the blocking state, the IGBT can be turned off by reducing the gate voltage to zero or applying a negative voltage lower than  $V_{th}$ . With an average switching frequency from 20 to 50 KHz.

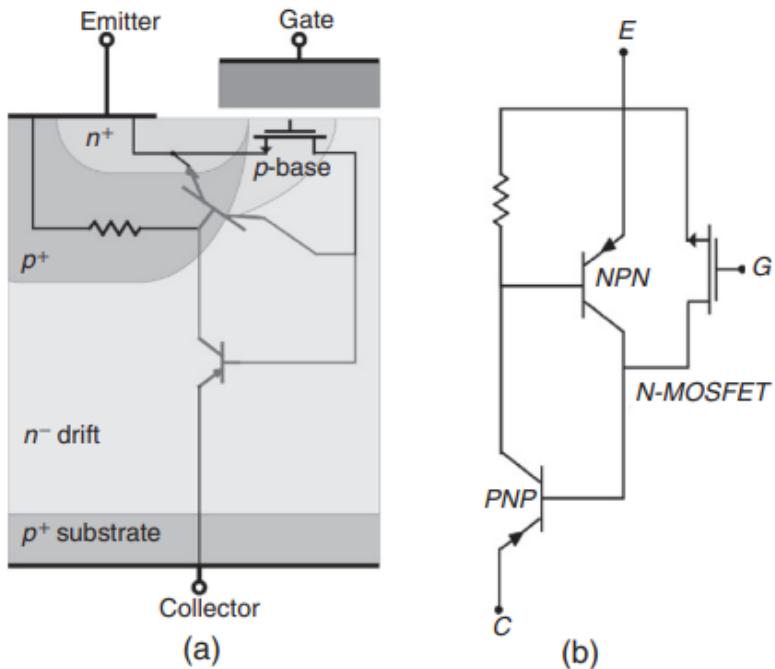


Figure 3.6: IGBT:(a) half-cell vertical cross section and (b) equivalent circuit model. [4]

There is such a problem with IGBTs in terms of switching time, where they exhibit fast conduction during the forward state but experience longer blocking state durations. This issue is resolved by introducing an additional layer, known as the "n buffer," between the collector and the base. This modified version is called a Punch Through IGBT (PT-IGBT). In general, there are two types of IGBTs: PT-IGBT and non-PT-IGBT. Non-PT-IGBTs have lower on-state losses compared to PT-IGBTs, but PT-IGBTs considered to have faster turn-off.

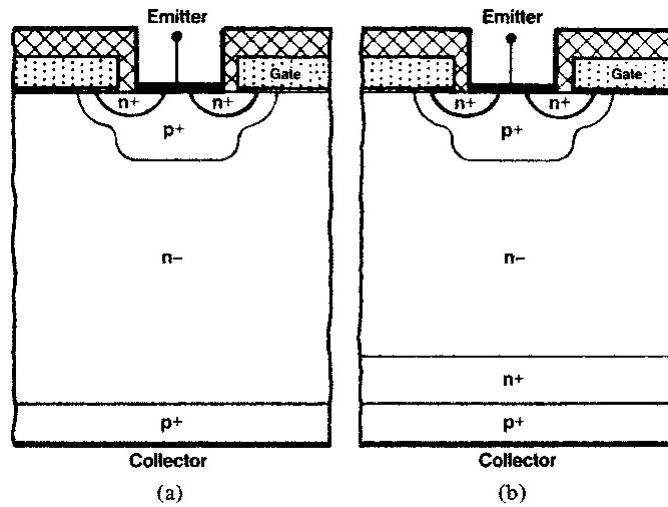


Figure 3.7: IGBT:(a) Non-Punch Through IGBT (b) Punch Through IGBT.[5]

Fig. 3.7 depicts the structural difference between the nonpunch-through (NPT) and punch-through (PT) IGBT. The major differences between the two structures are that the PT structure has an n - -buffer layer and the n + -base width of the NPT BJT is twice as thick as that of the PT BJT.

## IGBT Characteristics

### Forward characteristics

The forward characteristic of an IGBT represents the relationship between the collector current ( $I_C$ ) and the voltage across the collector and emitter ( $V_{CE}$ ). This re-

lationship is illustrated in Figure 3.8 while varying the gate-emitter voltage ( $V_{GE}$ ). The voltage across the collector and emitter ( $V_{CE_{ON}}$ ) during the on-state of the IGBT is the combined result of voltage drops across the MOSFET section, the collector junction, and the drift region, Equation (3.4). It represents the on-state voltage drop of the IGBT.

$$V_{CE.ON} = V_{P^{n+}} + V_{drift} + V_{MOSFET} \quad (3.4)$$

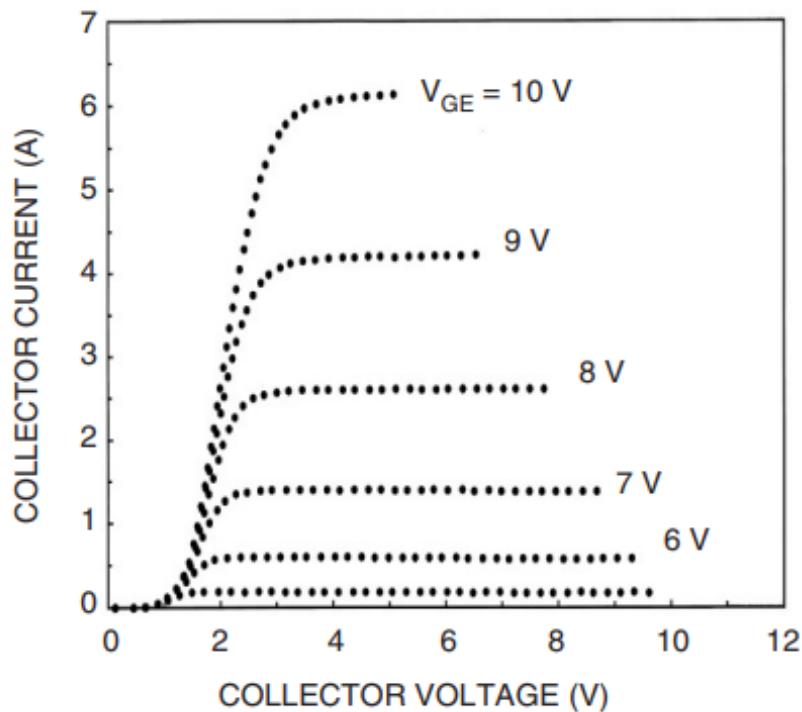


Figure 3.8: IGBT:forward characteristics.[4]

### Transfer characteristics

Transfer characteristic defines the relationship between  $I_C$  and  $V_{GE}$  as shown in Fig. 4.3-(b). The capability of the device to handle a large current and low

$V_{GE}$  is desirable and it is achieved by designing IGBT with a large transconductance,  $g_{fs}$ . The transconductance of IGBT is dictated by the gate and the channel structures and it can be approximated to be equal the slope of the transfer characteristic at a specified temperature. Equation 3.5

$$g_{fs} = \frac{\partial I_C}{\partial V_{GE}}|_{V_{GE}=constant} \quad (3.5)$$

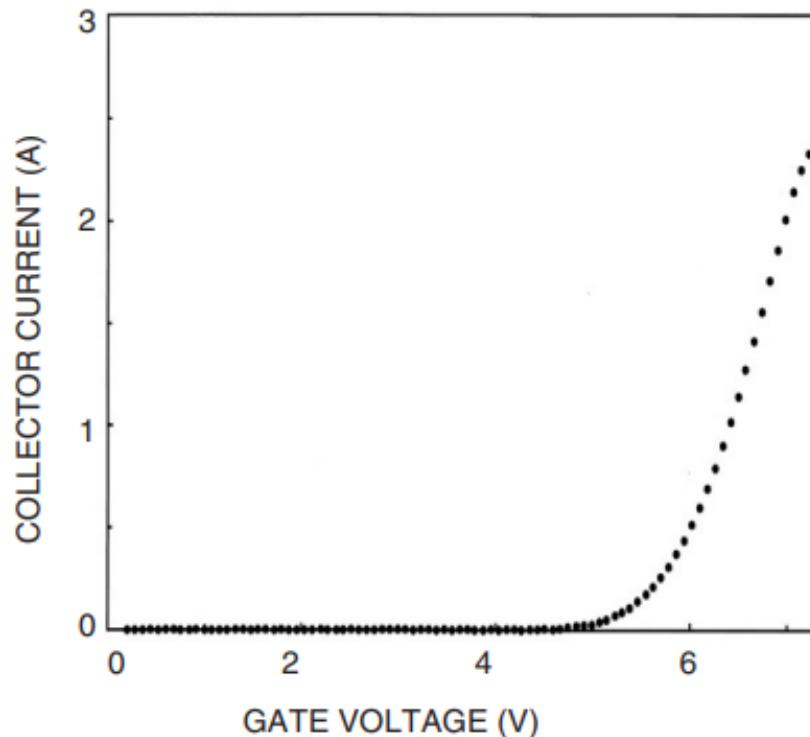


Figure 3.9: IGBT:transfer characteristics.[4]

The IGBT and MOSFET exhibit similar characteristics as voltage-controlled devices. Both devices have a high impedance, leading to negligible gate current. However, the IGBT surpasses the MOSFET in terms of power ratings, making it

more suitable for medium to high power systems that require efficient switching at acceptable frequencies.

## 3.2 Power Inverters

An inverter is an essential power electronic device that facilitates the conversion of DC power to AC power. Its utility can be broadly categorized into three primary purposes. Firstly, inverters are deployed to establish a connection between DC power sources, such as solar panels, wind turbines, and fuel cells, and the electrical grid. This integration allows for efficient utilization of renewable energy sources. Secondly, inverters play a crucial role in long-distance power transmission and interconnection between disparate systems, including HVDC systems. These applications enable effective power transfer over extended distances. Lastly, inverters are extensively utilized for controlling the magnitude, frequency, and phase of the output waveform (current or voltage). This control capability empowers the regulation of motor speed, position, and torque, serving a wide range of industrial applications.

The conversion process is achieved by employing precise control techniques for power electronic switches, which establish the connection between the DC power source and the AC motors. This control methodology, commonly referred to as modulation, governs the switch arrangement and conduction states within the power electronic converter. By appropriately modulating these switches, the desired AC output power can be generated, fulfilling specific application requirements.

### 3.2.1 Current source inverters

The Current Source Inverter (CSI) is an electrical device that converts direct current (DC) into alternating current (AC). It incorporates an inductor filter connected in series with the DC source, serving the purpose of energy storage and

controlling current ripple. The CSI enables precise control over the magnitude, phase, and frequency of the AC current waveform. Consequently, the load current or output current remains unaffected by changes in the load impedance, ensuring stability and predictability. However, in the CSI configuration, the load voltage is dependent on the load impedance, which introduces a variable aspect. One significant advantage of the CSI is its inherent protection against short circuits. This is due to the regulation of the DC source current, which governs the output current of the inverter.[20]

### 3.2.2 Voltage source inverters

The Voltage Source Inverter (VSI) operates with a constant DC source voltage, although it can also work with a variable DC source. It receives power from a rectified voltage source and a capacitor, known as the DC link. The VSI produces a switched voltage waveform at the output, allowing for adjustable amplitude, phase, and frequency of the fundamental voltage component. This flexibility enables the VSI to generate a desired voltage profile.

The current waveform of the VSI is determined by the load connected to it. Depending on the specific application, the VSI can deliver either single-phase or three-phase voltage output. It is commonly employed in low to medium power applications, which aligns with the focus of our research.

### 3.2.3 Three phase voltage source inverter

The three-phase Voltage Source Inverter (VSI) comprises six power electronic switches, typically IGBTs (Insulated Gate Bipolar Transistors), and six freewheeling diodes, also known as antiparallel diodes. Its fundamental operation is analogous to three separate branches, which can be visualized as three half-bridges (single-phase VSIs) connected in parallel. This operational concept is derived from the work of Wilamowski and Irwin (2011).[21]

Figure 3.10 illustrates Single-phase half-bridge Voltage source inverter with Generic Semiconductor Switches and The purpose of the anti-parallel diodes is to provide a path for the load current when its polarity is change through the operation when the load is inductive. The purpose of the antiparallel diodes is to provide a path for the load current when its polarity is change through the operation. The capacitors divide the total DC link to provide a neutral point (N) with zero voltage. The load will be connected between neutral point (N) and the inverter branch output point (a).

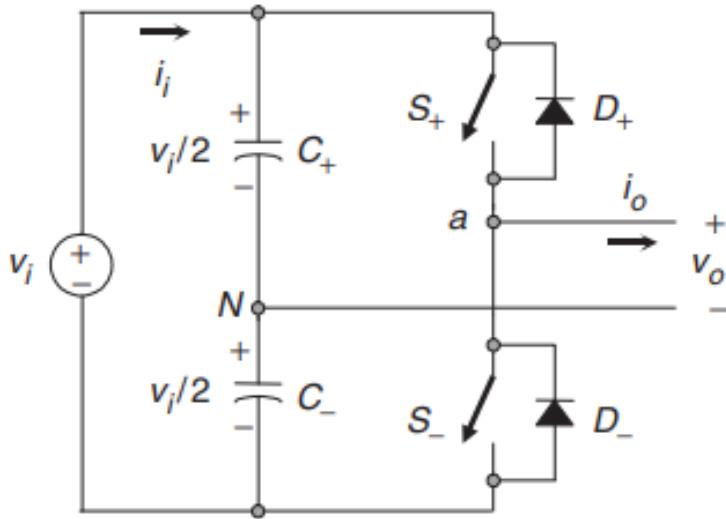


Figure 3.10: Single-phase half-bridge VSI.[4]

The switches ( $S_+$  and  $S_-$ ) are controlled by binary gate signals  $S$  and  $\bar{S}$  (1, 0), respectively, where 1 represents the on-state and 0 represents the off-state.  $\bar{S}$  is the logic complement of  $S$ . The purpose of this alternate control is to prevent shortening the DC link circuit by having both switches in the on-state simultaneously. Therefore, when  $S$  is 1,  $S_+$  turns on and connects the positive bus bar to the output, resulting in a positive voltage ( $V_{AN} = \frac{V_i}{2}$ ). On the other hand, when  $\bar{S}$  is 0,  $S_+$  turns off and  $S_-$  turns on, connecting the negative bus bar to the inverter output, resulting in a negative voltage ( $V_{AN} = -\frac{V_i}{2}$ ). As a result, the output voltage of one branch inverter is an AC switched waveform that alter-

uates between  $(-\frac{V_{AN}}{2}$  and  $\frac{V_{AN}}{2}$ ) due to the interchange of switching between the two switches.

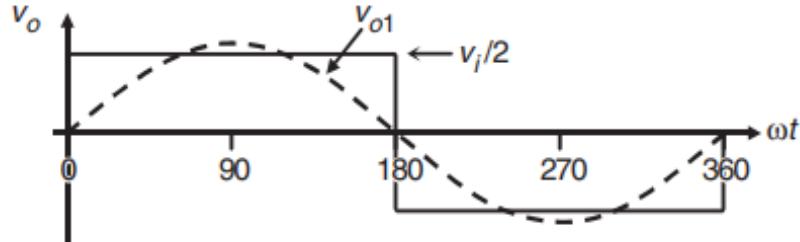


Figure 3.11: The half-bridge VSI. Ideal waveforms for the square-wave modulating technique: AC output voltage.[4]

### Mathematical Analysis of Phase Voltages in a Three-Phase Inverter

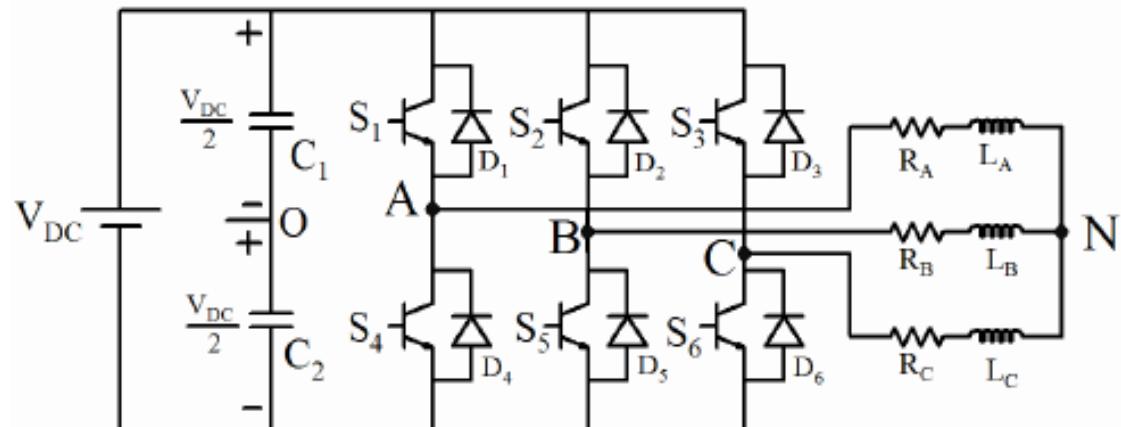


Figure 3.12: Three Phase Inverter VSI with a Three Phase Balanced Load. [6]

As previously demonstrated, the three-phase voltage source inverter can be visualized as three separate half-bridge single voltage source inverters. Additionally, it has been clarified that when the upper switch in a leg is turned on, the output voltage is equal to half of the DC voltage ( $\frac{V_{DC}}{2}$ ).  $(-\frac{V_{DC}}{2})$  when lower switch conducts.

### Introduction to Kirchhoff's Voltage Law:

Introduce Kirchhoff's voltage law, which states that the sum of the voltages around any closed loop in an electrical circuit is zero. Explain how this law is based on the conservation of energy principle and its application in circuit analysis [4].

### Applying Kirchhoff's Voltage Law to the Three-Phase Inverter

$$V_{AO} = V_{AN} + V_{NO} \quad (3.6)$$

$$V_{BO} = V_{BN} + V_{NO} \quad (3.7)$$

$$V_{CO} = V_{CN} + V_{NO} \quad (3.8)$$

Since the system is three phase and balanced, Hence

$$V_{AN} + V_{BN} + V_{CN} = 0 \quad (3.9)$$

Sum up the three equations (3.6),(3.7),(3.8) Results:

$$V_{NO} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \quad (3.10)$$

Substitute by equation (3.10) in equations (3.6),(3.7),(3.8) Results:

$$V_{AN} = \frac{2}{3}V_{AO} - \frac{1}{3}(V_{BO} + V_{CO}) \quad (3.11)$$

$$V_{BN} = \frac{2}{3}V_{BO} - \frac{1}{3}(V_{AO} + V_{CO}) \quad (3.12)$$

$$V_{CN} = \frac{2}{3}V_{CO} - \frac{1}{3}(V_{AO} + V_{BO}) \quad (3.13)$$

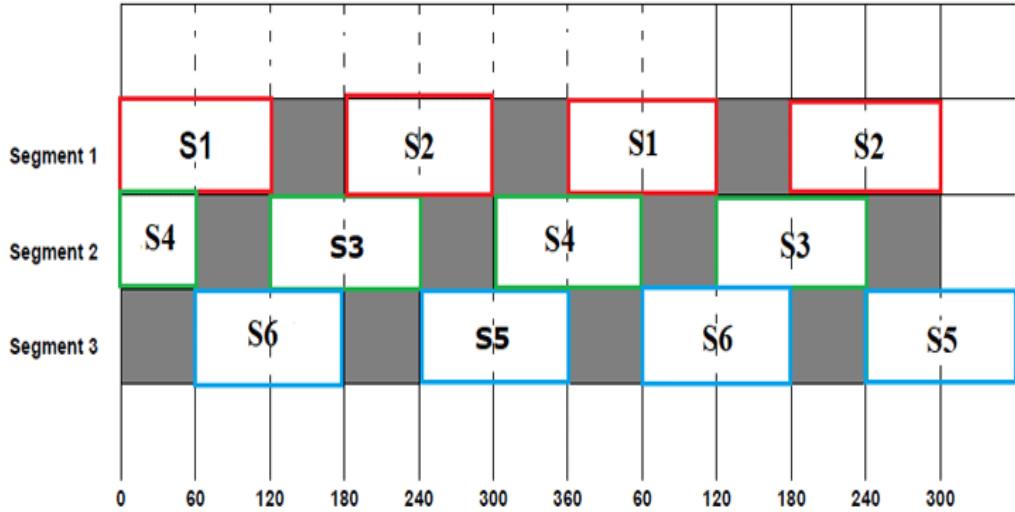
From the the equation (3.11),(3.12),(3.13) the phase voltage is determined for any phase and similar for the line voltages as it is defined the the difference between two given phase voltages.

### 3.3 Conduction Modes in VSI

There are two conduction modes for a three-phase inverter. In the first mode, the power electronic switch conducts for 120 degrees and turns off for the next 240 degrees within one cycle. In the second mode, the power electronic switch conducts for 180 degrees and turns off for the next 180 degrees within one complete cycle of 360 degrees. Both modes utilize a three-phase inverter (VSI) comprising six power electronic switches, as depicted in Figure 3.12.

#### 3.3.1 Three phase inverter 120° conduction

The circuit diagram of the inverter is identical to Figure 3.12. In the 120° conduction mode, S1 conducts for 120°, and for the next 60 degrees, neither S1 nor S4 are conducted. Then, S4 conducts for the subsequent 120 degrees, starting from 180 degrees and ending at 300 degrees. After 300 degrees, both S1 and S4 remain off for 60 degrees. Following this, S1 conducts for 120 degrees until 180 degrees, during which S1 and S4 are off. Then, S4 conducts for 120 degrees, and the pattern continues[22]. This conduction mode is similar to the 180-degree conduction mode regarding the sequence of conduction for the upper and lower Switches. So, if S1 conducts at  $\omega t = 0$  degrees, S3 conducts at  $\omega t = 120^\circ$  [23], and S5 conducts at  $\omega t = 240^\circ$  for the upper switches group. The same applies to the lower switches group. The purpose of this pattern is to invert a three-phase output voltage with a 120° phase shift. Therefore, one cycle is divided into six intervals of 60 degrees. As shown in Figure 3.13, S1 and S6 should be conducted during interval I, S1 and S2 for interval II, S2 and S3 for interval III, and so on for the remaining intervals. In each interval, only two switches are conducted: one from the upper group and another from the lower group. During the first interval ( $0^\circ \leq \omega t \leq 60^\circ$ ), S1 connects phase-a to the positive bus bar, and S6 connects phase-b to the negative bus bar, while phase-c is not connected to the DC source. As a result, the phase voltages become  $V_{ao} = \frac{V_{dc}}{2}$ ,  $V_{bo} = -\frac{V_{dc}}{2}$ , and  $V_{co} = 0$ . In the subsequent 60-degree interval, S1 still connects phase-a to the positive bus bar, maintaining a voltage of  $V_{ao} = \frac{V_{dc}}{2}$ . However, S6 turns off, causing the phase-b voltage to become zero. Then, S2 connects phase-c to the negative bus bar with a voltage of  $V_{co} = -\frac{V_{dc}}{2}$ , and this pattern continues for the remaining intervals.

Figure 3.13:  $120^\circ$  Conduction Mode Diagram.

The Output line voltage can be obtained by:

$$V_{ab} = V_{ao} - V_{bo} \quad (3.14)$$

$$V_{bc} = V_{bo} - V_{co} \quad (3.15)$$

$$V_{ca} = V_{co} - V_{ao} \quad (3.16)$$

Consequently, the root mean square line and phase voltage are ( $V_{L-RMS} = 0.707V_{dc}$ ) and Phase voltage ( $V_{L-RMS} = 0.408V_{dc}$ )[23]. In conclusion, we get line voltage that has six step waveform per cycle, and the quasi square wave for the phase voltage. Where  $120^\circ$  phase shift is between the line voltage as well as phase voltage. Fig.3.14 - 3.15 are shown the output wave-forms of the phase voltage and for the line voltage respectively.

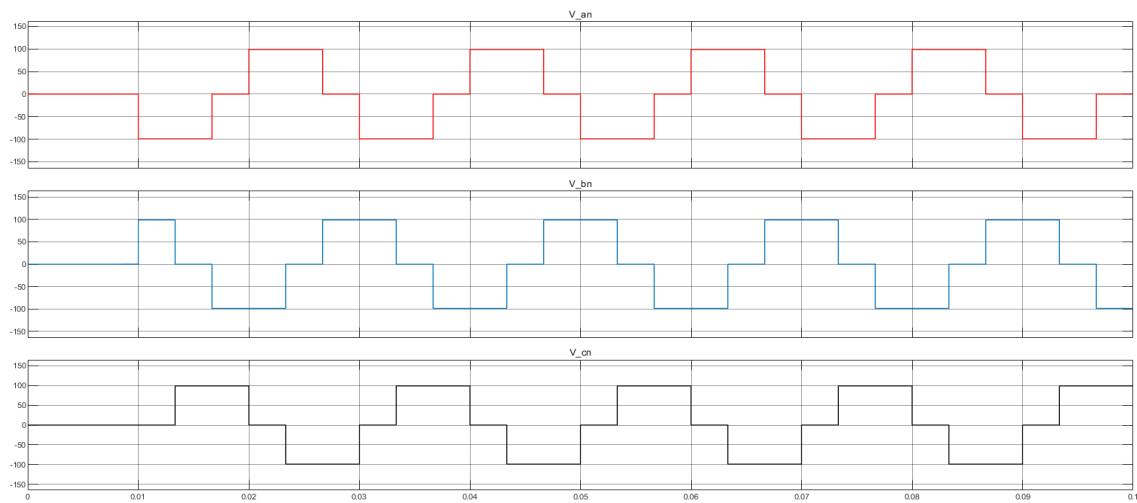


Figure 3.14: Output phase voltages using  $120^\circ$  Conduction Mode Diagram.

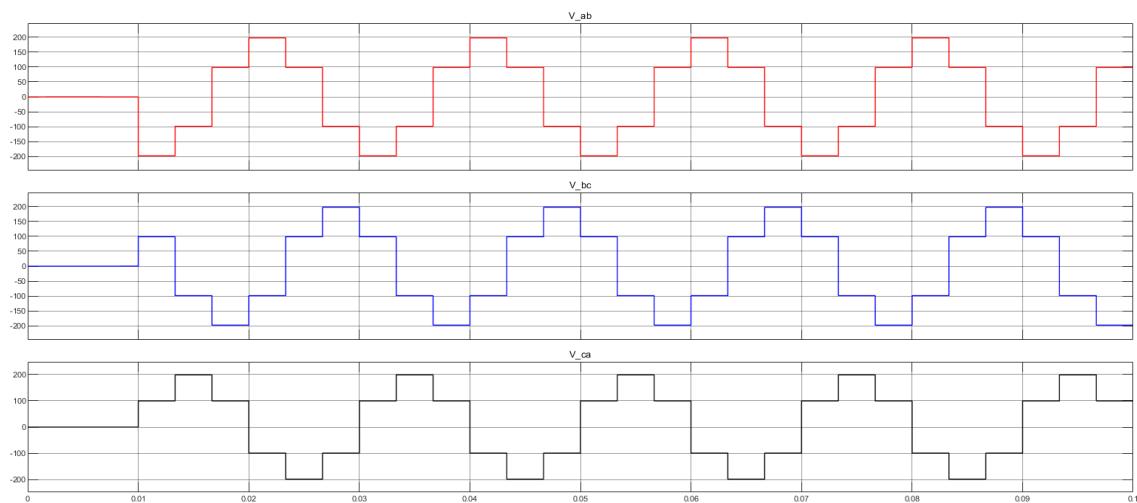


Figure 3.15: Output line voltages using  $120^\circ$  Conduction Mode Diagram.

### 3.3.2 Three phase inverter 180° conduction

As shown in the power circuit diagram above, in this mode each switch (S) conducts for 180° of a cycle. The upper switch group (S1, S3, and S5), which connect to the positive bus bar of the DC voltage source, work in this pattern. S1 conducts when ( $\omega t = 0^\circ$ ), then S3 conducts at ( $\omega t = 120^\circ$ ) and S5 at ( $\omega t = 240^\circ$ ). Similarly, the lower three switches (S4, S6, and S2), which connect to the negative bus bar of the DC voltage source, are conducted, but they start conducting from ( $\omega t = 180^\circ$ ) instead of ( $\omega t = 0^\circ$ ). The purpose of these delays in the conduction among the same switch group is to create a three-phase pulsing output that has a phase shift of 120° between each other. However, in one branch, such as branch S1 and S4, S1 conducts for 180°, S4 for the next 180°, again S1 for 180° and so on. The second and third branches work in the same manner. Hence, one cycle is divided into six steps or intervals of 180° depending on the conduction of switches. Accordingly, S1, S5, and S6 should be conducted for the first interval I, as shown in Fig. 3.16. S1, S2, and S6 for Interval II, and so on for the remaining intervals [22]. In each 60° interval, there are only three switches that conduct: one from the upper switch group and two from the lower switch group, or two from the upper and one from the lower switch group [22].

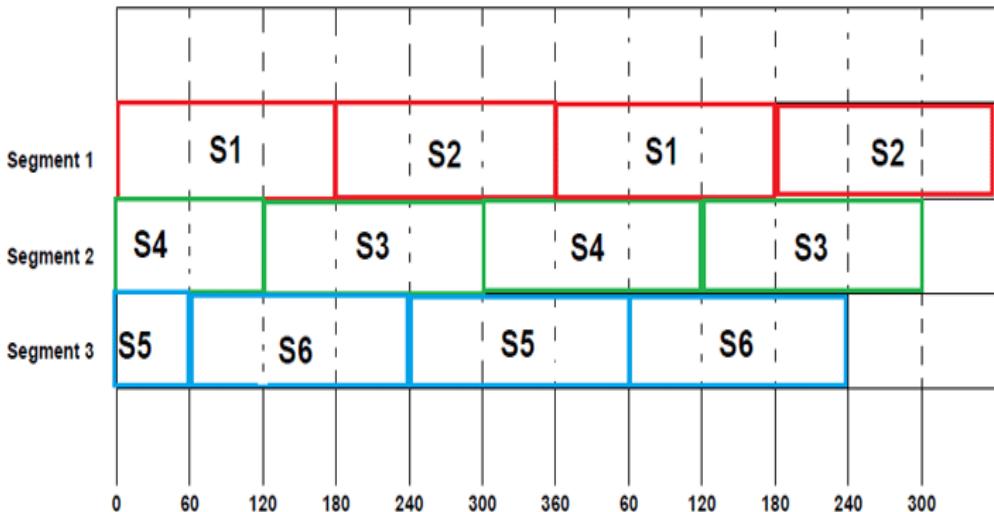


Figure 3.16: 180° Conduction Mode Diagram.

During the first interval, which is ( $0^\circ \leq \omega t \leq 60^\circ$ ), phase-a and phase-b are connected to the positive bus bar via switch S1 and S5, respectively, while phase-c is connected to the negative bus bar via switch S6. We assume a balanced load in a wye-connected circuit. Thus, the output phase voltages are ( $V_{an} = V_{bn} = \frac{V_{dc}}{3}$ ), and  $V_{co} = -\frac{2V_{dc}}{3}$ ), and the output line voltages are obtained using equations 3.14 - 3.16. Figures 3.17-3.18 depict output line-to-neutral and line-to-line voltages in a clear manner. Furthermore, based on the line waveform voltage, we can calculate the root mean square (RMS) values for the line voltage ( $v_{L-RMS} = 0.816V_{dc}$ ) and the phase voltage ( $v_{Ph-RMS} = 0.471V_{dc}$ ) [23]. Consequently, we obtain phase voltages that exhibit a six-step per cycle and quasi-square wave pattern, characterized by one positive pulse and one negative pulse (each lasting for a duration of  $120^\circ$ ), for the line voltages. The three line and phase voltages are out of phase by  $120^\circ$ . In contrast to the  $120^\circ$  mode, the  $180^\circ$  mode yields higher power output [22]. In the  $180^\circ$  mode, three Switches are used per interval, while in the  $120^\circ$  mode, only two Switches are used. This difference in the number of Switches results in a potential short circuit condition in the source for the  $180^\circ$  mode, but not for the  $120^\circ$  mode.

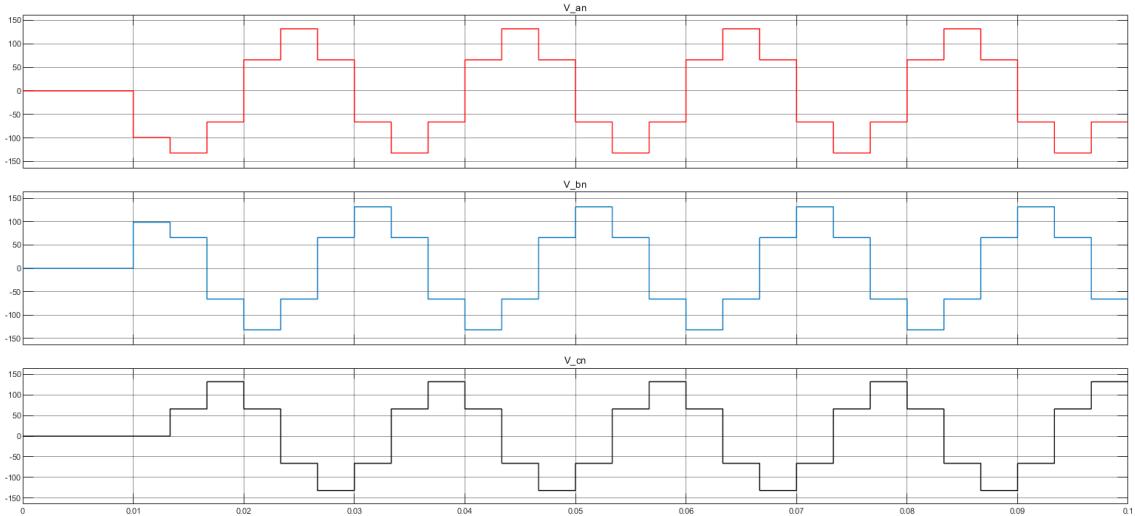


Figure 3.17: Output phase voltages using  $180^\circ$  Conduction Mode Diagram.

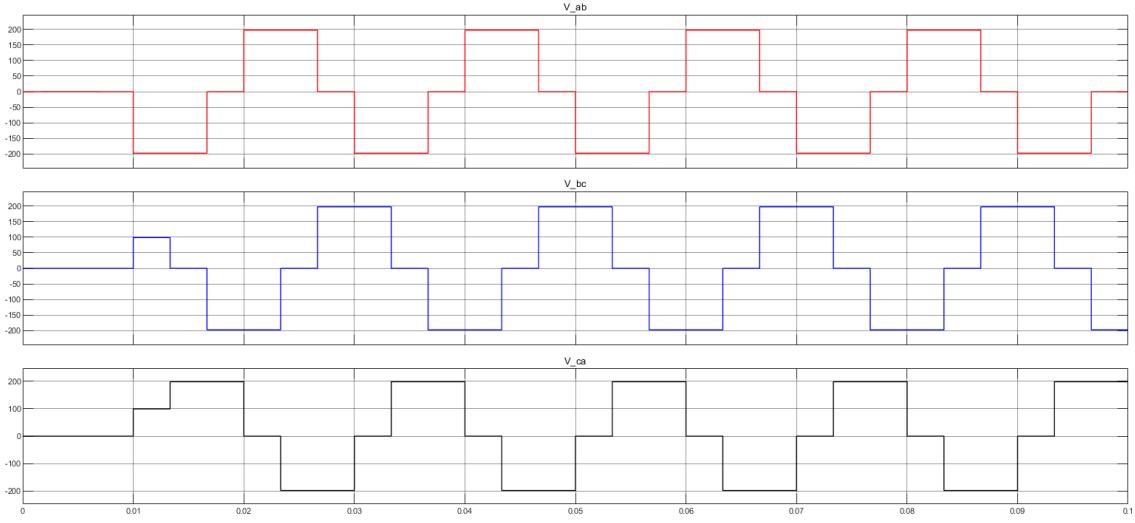


Figure 3.18: Output line voltages using  $180^\circ$  Conduction Mode Diagram.

## 3.4 Power System Harmonics

In an electric power system, a harmonic is a voltage or current at a multiple of the fundamental frequency of the system. Harmonics can best be described as the shape or characteristics of a voltage or current waveform relative to its fundamental frequency. When waveforms deviate from a sine wave shape, they contain harmonics. Harmonic frequencies in the power grid are a frequent cause of power quality problems, resulting in increased heating in the equipment and conductors, misfiring in variable speed drives and torque ripples in motors.[\[24\]](#)

### 3.4.1 Causes of Harmonics

#### 1. Non Linear Loads

A Non Linear Load [NLL] is a load with current consuming characteristics that do not follow the same fundamental shape as the applied voltage waveform. Technically, this situation is examined by conducting a voltage and current harmonic analysis. This data provides details of the predominant current harmonics and the resulting harmonic distortion to the applied voltage waveform [\[25\]](#), Fig3.19 illustrates the effect of the non-linear load on the

consumed current with respect to the input voltage applied.

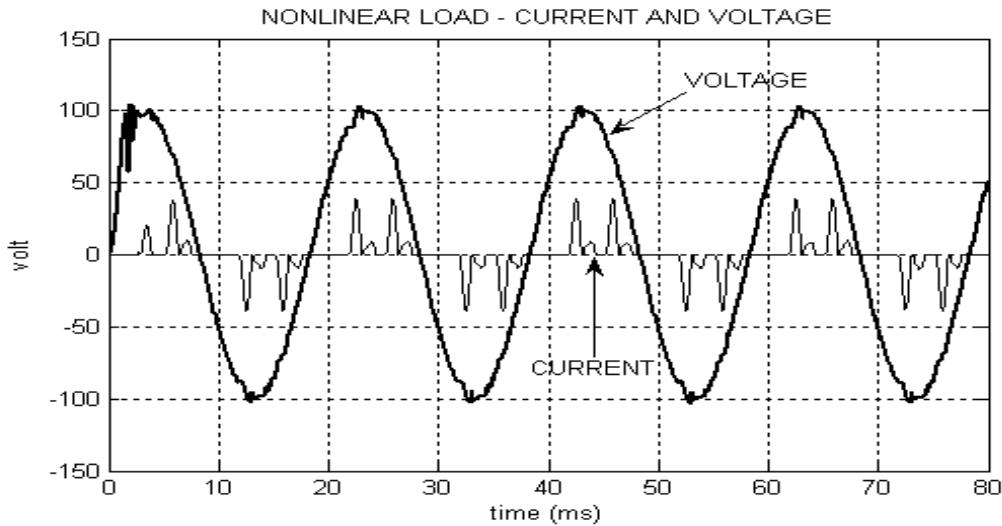


Figure 3.19: Harmonic distortion to the current with respect to the fundamental.

## 2. Purity of the input waveform

The waveform shape of the input signal, such as a square wave, contributes to the presence of harmonics. Unlike a smooth sinusoidal waveform, a square wave with its abrupt transitions contains additional frequency components known as harmonics. These harmonics are integer multiples of the fundamental frequency. When a non-sinusoidal waveform is used in a power system or device, it can generate harmonics that affect the voltage or current waveforms, leading to various issues. Considering the input waveform shape is crucial for understanding and mitigating harmonic's impact on power systems and devices.

### 3.4.2 Fourier Analysis of Square Wave

The Fourier expansion of a square wave can be derived using the concept of Fourier series. A square wave is a periodic waveform that alternates between two levels, typically represented for example as -1 and +1. Let's consider a square wave with a period of  $T$ . The general form of the Fourier series for a periodic function  $f(t)$

with period  $T$  is given by [26]:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left( a_n \cos \left( \frac{2\pi nt}{T} \right) + b_n \sin \left( \frac{2\pi nt}{T} \right) \right) \quad (3.17)$$

In the case of a square wave, the function is odd, meaning it has no cosine terms (since cosine is an even function). Therefore, the Fourier expansion simplifies to:

$$f(t) = \sum_{n=1}^{\infty} b_n \sin \left( \frac{2\pi nt}{T} \right) \quad (3.18)$$

The square wave is defined as -1 for half of the period and +1 for the other half. Mathematically, we can express it as:

$$f(t) = \begin{cases} -1, & \text{if } 0 \leq t < \frac{T}{2} \\ 1, & \text{if } \frac{T}{2} \leq t < T \end{cases} \quad (3.19)$$

To find the coefficient  $b_n$ , we integrate the product of the square wave and the sine function over one period:

$$b_n = \frac{2}{T} \int_0^T f(t) \sin \left( \frac{2\pi nt}{T} \right) dt \quad (3.20)$$

By evaluating the integral over the respective intervals of the square wave, we can compute the coefficients  $b_n$ .

For the square wave, the coefficients  $b_n$  are given by:

$$b_n = \frac{4}{n\pi} (1 - (-1)^n) \quad (3.21)$$

Substituting these coefficients back into the Fourier expansion equation, we get the final expression for the Fourier expansion of a square wave.

$$f(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{1}{2n-1} \sin \left( \frac{2\pi(2n-1)t}{T} \right) \quad (3.22)$$

In this equation, the term  $(2n - 1)$  represents the harmonic frequencies, and the amplitude of each harmonic is inversely proportional to  $(2n - 1)$  which is the order of the harmonic itself.

### 3.4.3 Harmonic Voltage Distortion Factor

The proliferation of converter modulation algorithms that have appeared over the years has created confusion as to the effectiveness of one method over another for comparing various algorithms. One method of comparing the effectiveness of modulation processes is by comparing the unwanted components, i.e., the distortion in the output voltage or current waveform relative to that of an ideal sine wave.

Let's assume that the voltage waveform can be represented by the function  $v(t)$ . The fundamental component of the voltage can be expressed as  $V_1 \cos(\omega t)$ , where  $V_1$  is the amplitude of the fundamental frequency component and  $\omega$  is the angular frequency.

The harmonic components can be represented as a sum of sinusoidal functions with frequencies that are integer multiples of the fundamental frequency. We can write the nth harmonic component as  $V_n \cos(n\omega t + \phi_n)$ , where  $V_n$  is the amplitude of the nth harmonic and  $\phi_n$  is the phase angle of the nth harmonic.

The total voltage waveform can be expressed as the sum of the fundamental and harmonic components [26]:

$$v(t) = V_1 \cos(\omega t) + \sum_{n=2}^{\infty} V_n \cos(n\omega t + \phi_n) \quad (3.23)$$

The RMS value of the voltage waveform can be calculated using the formula:

$$V_{\text{RMS}} = \sqrt{\frac{1}{T_k} \int_0^{T_k} v^2(t) dt} \quad (3.24)$$

where  $T_k$  is the period of the waveform.

To calculate the RMS value of the fundamental component, we square the function  $V_1 \cos(\omega t)$  and integrate it over one period:

$$V_{1\text{RMS}} = \sqrt{\frac{1}{T_k} \int_0^{T_k} (V_1 \cos(\omega t))^2 dt} \quad (3.25)$$

Similarly, to calculate the RMS value of the nth harmonic component, we square the function  $V_n \cos(n\omega t + \phi_n)$  and integrate it over one period:

$$V_{n\text{RMS}} = \sqrt{\frac{1}{T_k} \int_0^{T_k} (V_n \cos(n\omega t + \phi_n))^2 dt} \quad (3.26)$$

The total harmonic distortion (THD) of the voltage can now be defined as

$$\text{THD} = \frac{\sqrt{V_{2\text{RMS}}^2 + V_{3\text{RMS}}^2 + \dots + V_{n\text{RMS}}^2}}{V_{1\text{RMS}}} \quad (3.27)$$

if this equation is applied to the inverter circuit of Figure 3.12, it can be assumed that by proper control, the positive and negative portions of the output wave are symmetrical (no DC or even harmonics). The voltage harmonic distortion factor reduces to

$$THD = \sqrt{\sum_{n=3,5,7,\dots}^{\infty} \left(\frac{V_n}{V_1}\right)^2} \quad (3.28)$$

## 3.5 Dead time

Dead time is the time interval between the turn-off of one switch and the turn-on of another switch in the same leg of a bridge circuit. For example, in a half-bridge circuit, which consists of two switches and a load connected in series, the dead time is the time between the turn-off of the upper switch and the turn-on of the lower switch, or vice versa. The purpose of dead time is to prevent both switches from being on at the same time, which would create a shoot-through condition that can damage the switches and the load. However, the dead time also affects the output voltage and current, as it creates a zero-voltage interval that can reduce the power transfer and introduce harmonics.

### 3.5.1 Effect of the Load type on the Dead Time

The optimal dead time for a bridge circuit depends on the type of load that is connected to it. There are two main types of loads: resistive and inductive. A resistive load is a load that has a constant resistance, such as a heater or a lamp. An inductive load is a load that has a significant inductance, such as a motor or a transformer. The difference between resistive and inductive loads is that resistive loads have a current that is proportional to the voltage, while inductive loads have a current that lags behind the voltage. This means that the output current of

a bridge circuit with an inductive load has a longer zero-crossing interval than with a resistive load. Therefore, the optimal dead time for an inductive load is shorter than for a resistive load, as it reduces the distortion and losses caused by the zero-voltage interval.[27]

### 3.5.2 Measuring and adjustment of the Dead time

To measure and adjust the dead time of a bridge circuit, you need to use an oscilloscope and a signal generator. The oscilloscope is a device that displays the waveform of an electrical signal, such as the output voltage or current of a bridge circuit. The signal generator is a device that produces a periodic electrical signal, such as a pulse-width modulated (PWM) signal that controls the switches of a bridge circuit. To measure the dead time, you need to connect the oscilloscope probes to the output terminals of the bridge circuit, and set the signal generator to produce a PWM signal with a fixed frequency and duty cycle. Then, you need to observe the output waveform on the oscilloscope screen, and measure the time interval between the turn-off of one switch and the turn-on of another switch in the same leg of the bridge circuit. This is the dead time. To adjust the dead time, you need to change the settings of the signal generator, such as the phase shift or the delay time, until you achieve the desired dead time.[27]

### 3.5.3 Dead time optimization

To optimize dead time for different load conditions, you need to consider the trade-off between shoot-through protection and output quality. If the dead time is too short, you risk causing shoot-through, which can damage the switches and the load. If the dead time is too long, you reduce the output power and introduce distortion and harmonics. Therefore, you need to find a balance between these two factors, depending on the type and characteristics of your load. For example, if you have a resistive load, you can use a longer dead time, as it has less impact on the output current. If you have an inductive load, you can use a shorter dead time, as it reduces the zero-voltage interval and improves the output quality. However, also needed to take into account other factors, such as the switching frequency, the load dynamics, and the temperature variations, as they can affect the optimal dead

time. Therefore, you may need to use a feedback control system or an adaptive algorithm to adjust the dead time according to the load conditions.[27]

### 3.5.4 Dead time Control

The dead time can be controlled either by hardware implementation of a electronic circuits or by software delay, however for the hardware implementation by tuning the parameters of the circuit board we can adjust and control the dead time. Figure 3.20 illustrate the hardware implementation of dead time adjustment circuit. However for the software control of the dead time we can delay the transition between the complementary switches on the same leg and control the dead time precisely. After generating the gate signals, we direct each signal to the subsequent

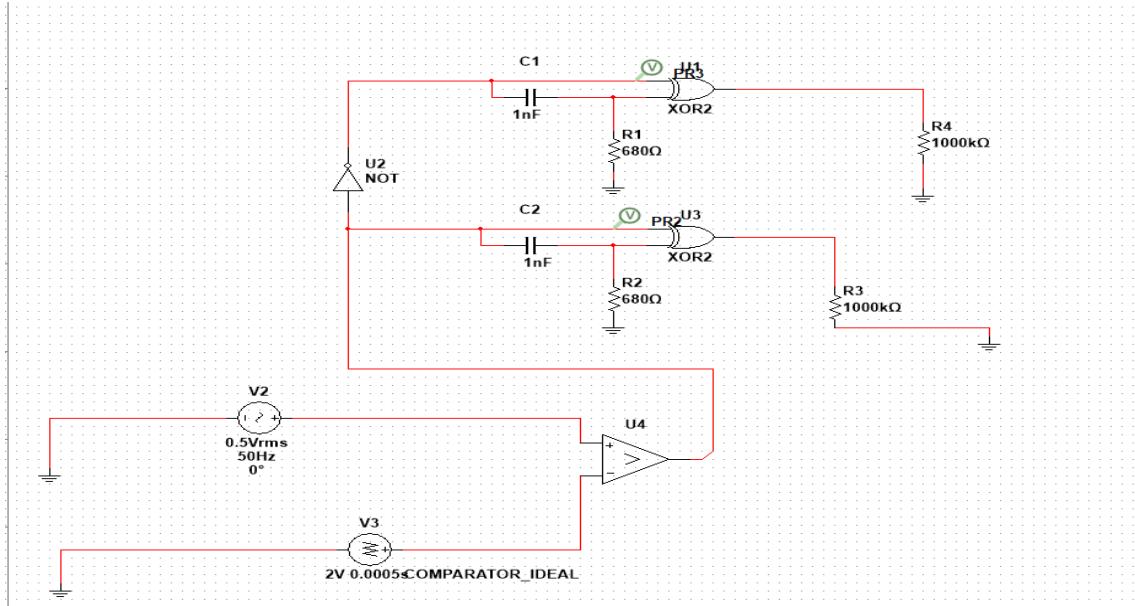


Figure 3.20: Electronic circuit to control the Dead time.

circuit where the XOR logic briefly transitions to a 'LOW' state for a very short period, owing to the presence of a capacitor. This transition persists until the capacitor reaches its steady state and effectively operates as an open circuit. As a result, the logic of the circuit switches to 'HIGH.' Conversely, a similar process occurs for the complementary signal of the lower switch in the leg, leading to a transition from 'HIGH' to 'LOW.' The duration it takes for the capacitor to reach

this transient state is commonly referred to as the dead time. By adjusting the capacitance and resistance of the circuit, we have the ability to control the length of this dead time, allowing us to fine-tune the behavior of the circuit according to our requirements.

### 3.6 Summary

In this chapter, our primary focus was on delving into power electronic switches, elucidating their distinctions, and discerning the most prevalent ones employed in industrial applications, based on their suitability in which present the MOSFETS and the IGBTS. Additionally, we embarked on an exploration of inverters and their variants, encompassing both single and three-phase configurations, along with their mathematical underpinnings. We traversed through the various operational modes of inverters, distinguishing between the 120 and 180 conduction modes. Subsequently, our inquiry delved into the realm of harmonics, delving into their analysis and calculation methodologies. Finally, we concluded by scrutinizing the concept of dead time, unraveling its impact on switching losses, and elucidating optimization strategies.

# Chapter 4

## Sinusoidal Pulse Width Modulation

### 4.1 Introduction

Sinusoidal Pulse Width Modulation (SPWM) is a modulation technique utilized in various types of inverters to generate output signals that approximate sinusoidal waveforms. It achieves this by adjusting the duty cycle of the output signals based on a reference sine wave. The primary objective of SPWM is to reduce low-order harmonics in the output waveform [28], resulting in high quality sinusoidal voltage signals. The core principle of SPWM involves tracking a reference sine wave and comparing it with a carrier signal. Sinusoidal Pulse Width Modulation can be considered as a special case of carrier-based Pulse Width Modulation in which the modulating signal takes the form of a sine wave. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of these pulses are modulated in order to obtain inverter output voltage control and to reduce its harmonic content. SPWM utilizes the average output voltage over each half-cycle to closely resemble the desired sinusoidal waveform. This modulation technique provides control over the output voltage level, although it may have higher switching losses compared to alternative modulation techniques. However, SPWM offers the advantage of being relatively straightforward to implement and producing low harmonic content in the output waveform.

## 4.2 Sampling methods

### 4.2.1 Natural Sampling SPWM

The natural sampling SPWM method for inverters is depicted in Figure 4.2 [7]. It involves comparing a analog real time sinusoidal modulating signal,  $V_r$ , with a higher frequency triangular carrier signal,  $V_c$ . By comparing these signals, a rectangular pulse sequence is generated, where the width of each pulse varies according to the sinusoidal law. This pulse sequence is then power amplified to drive the inverter, resulting in a sinusoidal voltage or current output.

Figure 4.1 provides a closer look at the intersection points between the sine and triangle waveforms. Accurate calculation of these intersection times is crucial for generating the natural SPWM rectangular pulse sequence. Within one period of the triangular carrier waveform  $T_c$ , there are two intersections:  $t_1$  and  $t_2$ . The durations of the ON and OFF states for each SPWM pulse,  $t_{on1}, t_{on2}, t_{off1}$ , and  $t_{off2}$ , are determined based on these intersection times.

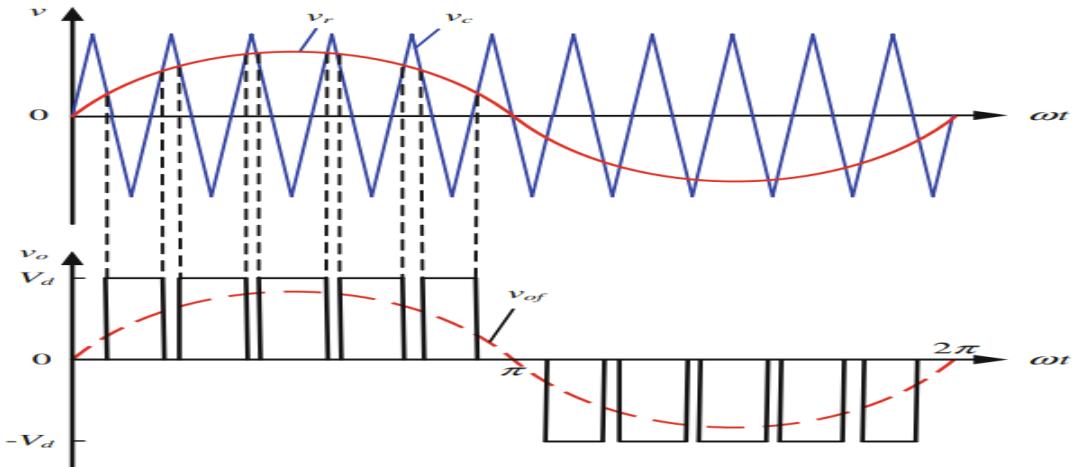


Figure 4.1: Principle of the SPWM waveform generation.[7]

Figure 4.2 illustrates the natural sampling method in which a real time modulated sine wave with a triangular carrier wave at intersection points of time  $t_1$  and  $t_2$  in a total period of carrier wave of  $T_c$  and the ON -OFF time is represented by  $t_{on1}$ ,

$t_{on_2}$ ,  $t_{off_1}$ , and  $t_{off_2}$  Respectively. Where  $M_a$  is the amplitude modulation index and defined as the ratio between the amplitude of the modulating signal to the carrier signal.

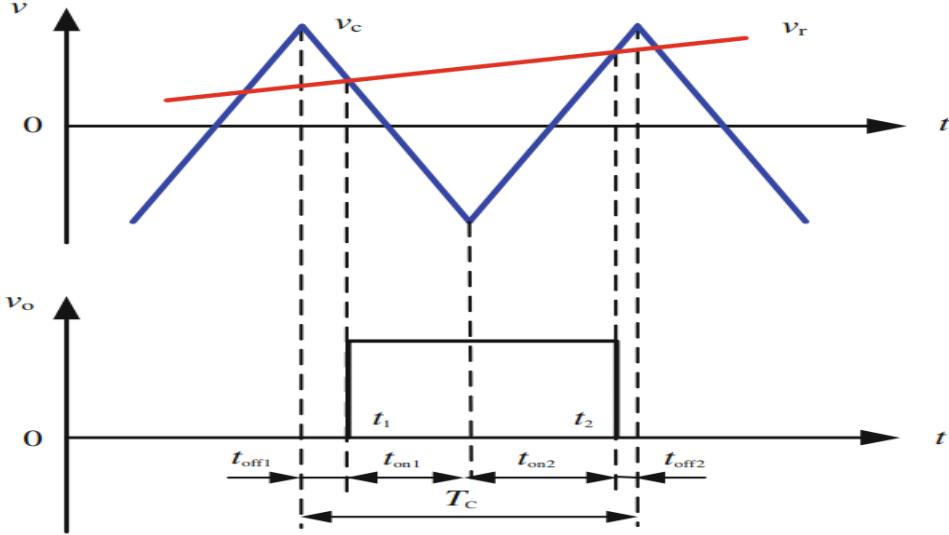


Figure 4.2: Natural sampling SPWM method.[7]

The duration of each SPWM pulse is determined by [7]

$$t_{off_1} = \frac{T_c}{4}(1 - M_a \sin(\omega t_1)) \quad (4.1)$$

$$t_{on_1} = \frac{T_c}{4}(1 + M_a \sin(\omega t_1)) \quad (4.2)$$

$$t_{on_2} = \frac{T_c}{4}(1 + M_a \sin(\omega t_2)) \quad (4.3)$$

$$t_{off_2} = \frac{T_c}{4}(1 - M_a \sin(\omega t_2)) \quad (4.4)$$

The pulse width of the generated SPWM wave in one period is

$$t_{on} = t_{on_1} + t_{on_2} = \frac{T_c}{4}\left(1 + \frac{M_a}{2}(\sin(\omega t_1) + \sin(\omega t_2))\right) \quad (4.5)$$

### 4.2.2 Regular sampling PWM

One major limitation with natural sampling PWM is the difficulty of its implementation in a digital modulation system, because the intersection between the reference waveform and the triangular waveform is defined by a transcendental equation and is complex to calculate. An analogue circuit possesses the advantages of a low cost with a fast dynamic response, but suffers from a complex circuitry to generate complex PWM, limited function ability and difficulty to perform in circuit modifications. To overcome this limitation the modern popular alternative is to implement the modulation system using a regular sampling PWM strategy. This technique was introduced to provide a more flexible way of designing the system. The system offers simple circuitry, software control and flexibility in adaptation to various applications. The two most common regular sampling techniques are regular symmetrical and asymmetrical sampling.

#### Symmetric Regular Sampling SPWM

The symmetric regular sampling method for SPWM involves selecting the time corresponding to the symmetry axis of each triangular wave as the sampling time. It is common practice to use the bottom point of the triangle wave as the symmetry axis. In Figure 4.3, there is a line that passes through the intersection point of the sine wave and the symmetry axis of the triangular wave. This line is parallel to the time axis. The intersection points of this parallel line and the triangular wave are sampled to determine the "ON" or "OFF" moments of the SPWM waveform. Since these two intersections are symmetrical, this method is referred to as the symmetric regular sampling method. Using Figure 4.3, we can establish the following relationship:

$$\frac{T_c}{\delta} = \frac{2}{1 + M_a \sin(\omega t_D)} \quad (4.6)$$

where  $\frac{\delta}{2} = t_{on_1} = t_{on_2}$ . Thus, the pulse width can be defined by

$$\delta = \frac{T_c}{2}(1 + M_a \sin(2n - 1) \frac{\pi}{M_f}) \quad (4.7)$$

where  $n = 1, 2, \dots, M_f$ , Where  $M_f$  is the frequency modulation ratio a, however During one period of the triangular wave, the gap width on both sides of the pulse is

$$\delta' = \frac{1}{2}(T_c - \delta) = \frac{T_c}{4}(1 - M_a \sin(2n - 1) \frac{2\pi}{M_f}) \quad (4.8)$$

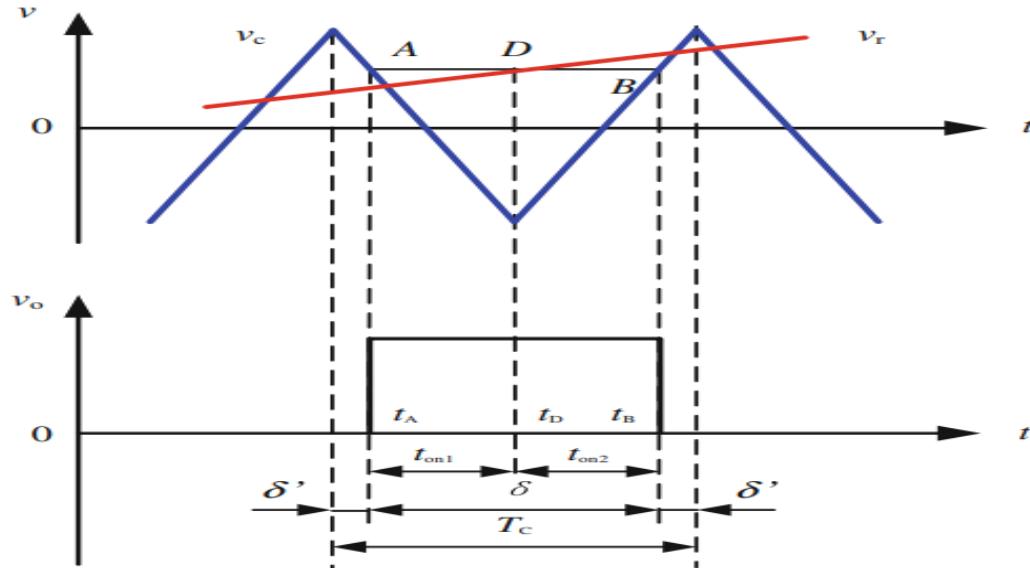


Figure 4.3: Symmetric regular sampling SPWM.[7]

### Asymmetric Regular Sampling SPWM

The asymmetrical modulation is produced when the triangular carrier waveform is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency. Each side of the triangular carrier waveform about a sampling point, intersect the stepped waveform at different step level. The resultant pulse width is asymmetrical about the sampling point as illustrate in Figure 4.4 .using

in this technique the dynamic response can be improved and produces less harmonic distortion of the load current.

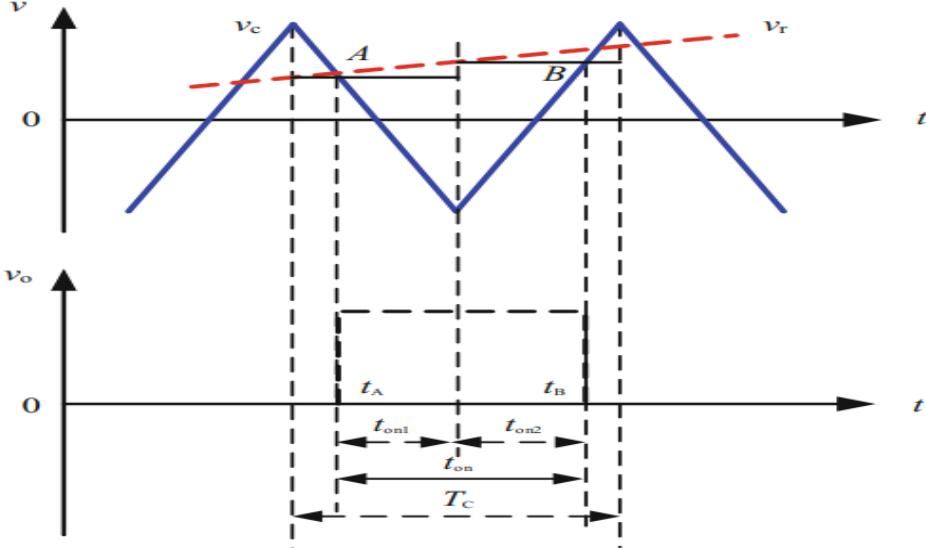


Figure 4.4: Asymmetric regular sampling SPWM.[7]

The ON durations are defined by

$$t_{on_1} = \frac{T_c}{4} \left( 1 + M_a \sin \frac{n\pi}{M_f} \right), \text{ where } n = 0, 2, 4, \dots, 2(M_f - 1) \quad (4.9)$$

$$t_{on_2} = \frac{T_c}{4} \left( 1 + M_a \sin \frac{(n+1)\pi}{M_f} \right), \text{ where } n = 1, 3, 5, \dots, 2(M_f - 1) \quad (4.10)$$

Obviously, when  $n$  is an even number, it represents for the vertex sampling, and when  $n$  is an odd number, it represents for the bottom point sampling. Therefore, the pulse width of the single-phase SPWM wave can be calculated as follows: [7]

$$t_{on} = t_{on_1} + t_{on_2} \quad (4.11)$$

For further exploration of the Asymmetric Regular Sampling Sinusoidal Pulse Width Modulation (SPWM) method, detailed information and in-depth insights can be found in the provided reference [7]. However, to maintain simplicity and

avoid delving too deeply into the topic, we will refrain from discussing it extensively here.

### 4.3 SPWM Switching Techniques

In single-phase full bridge inverters Fig 4.5 with an architecture of IGBTs and with DC voltage source  $V_d = 100V$ , achieving sinusoidal pulse width modulation involves two primary switching techniques: unipolar and bipolar. Each technique can be selected based on specific requirements. Bipolar switching, while capable of meeting certain needs, tends to introduce relatively more harmonics compared to unipolar switching. On the other hand, the unipolar technique, while potentially offering cleaner output, demands an additional modulating signal for implementation. Choosing the preferred one may vary depends on the demand and the complexity of the needs. [29]

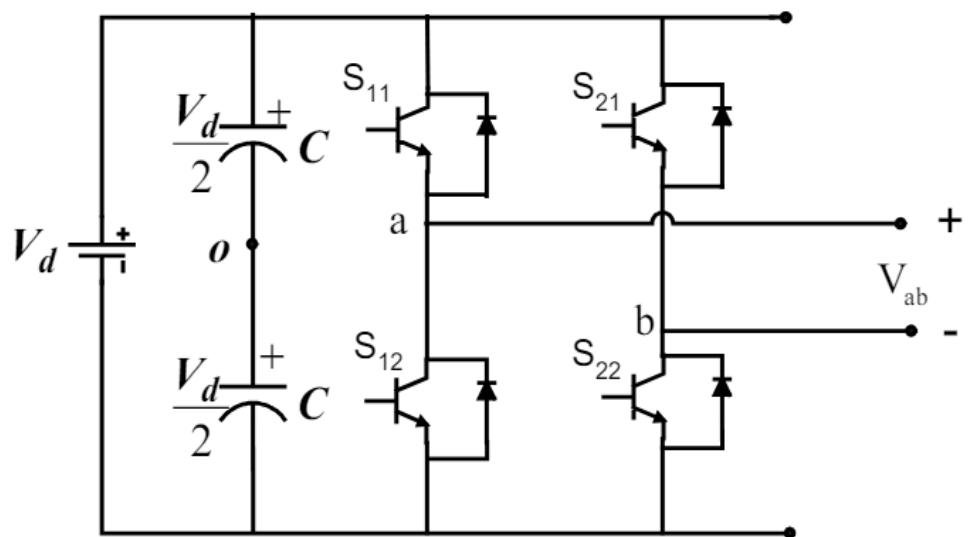


Figure 4.5: Single-phase full-bridge VSI.[4]

### 4.3.1 Bipolar PWM Switching Technique

In this scheme the diagonally opposite transistors  $S_{11}, S_{22}, S_{33}$  and  $S_{44}$  are turned on or turned off at the same time. The output of any leg is equal in magnitude and opposite in polarity to the alternative leg. However the output voltage is determined by comparing the modulated sine wave which is the reference signal  $V_r$ , to the triangular wave which is the carrier signal  $V_c$ , and the switching pattern is as follows.

$$V_r > V_c, \text{ then } S_{11} \text{ is on thus, } V_{ao} = \frac{V_d}{2} \text{ and } S_{22} \text{ is on thus, } V_{bo} = \frac{-V_d}{2} \quad (4.12)$$

$$V_r < V_c, \text{ then } S_{12} \text{ is on thus, } V_{ao} = \frac{-V_d}{2} \text{ and } S_{21} \text{ is on thus, } V_{bo} = \frac{V_d}{2} \quad (4.13)$$

Hence

$$V_{ao} = -V_{bo} \ \& V_{ab} = V_{ao} - V_{bo} \quad (4.14)$$

Fig 4.6 illustrates the control circuit to generate the appropriate gate signals as a result of the comparison between the reference signal and the carrier signal using SPWM bipolar switching implemented using simiulink, Where  $S_1$  is the gate signal for switches  $S_{11}, S_{22}$  and  $S_2$  is the gate signal for switches  $S_{21}, S_{12}$ .

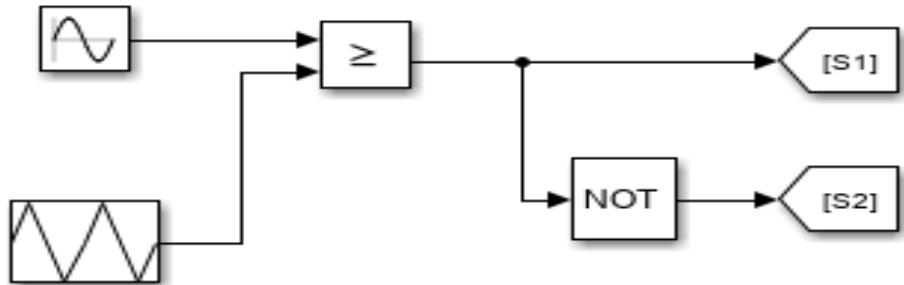


Figure 4.6: SPWM Bipolar Switching control circuit implemented using Simulink.

Fig 4.7 illustrates SPWM generation, showcasing the reference and carrier signals ,however it also demonstrates the resulting signals after comparing the reference and carrier using natural sampling and bipolar switching.

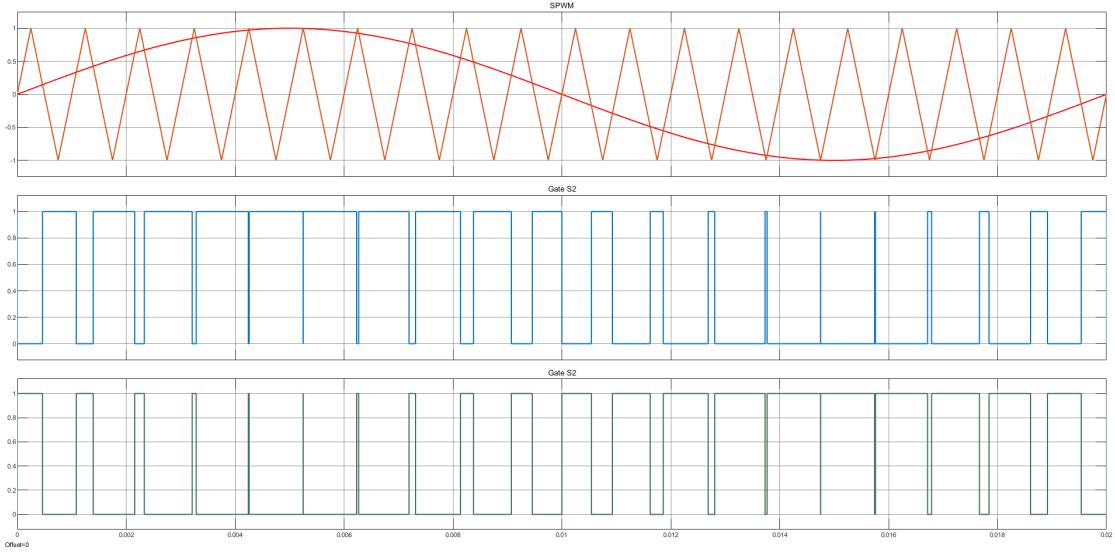


Figure 4.7: SPWM generation using natural sampling and bipolar switching.

The gating signals control the VSI operation: S1 high activates one pair of switches, while S2 high activates the other pair. Deadtime is neglected in the simulation to study the ideal behavior of the VSI.

Figure 4.8 demonstrates the behavior of the output phase voltage when applying bipolar switching into the VSI 4.5, on an inductive load ( $R - L$ ), Where ( $R = 20\Omega$   $L = 20mH$ ). It reveals that the voltage fluctuates between two voltage levels which are ( $V_d$ ) and ( $-V_d$ ), with an absence of the zero voltage level.

Figure 4.9 illustrates the harmonic spectrum of the phase voltage waveform shown in Figure 4.8. The utilization of SPWM bipolar switching eliminates low-order harmonics; however, the harmonics exhibit a notable clustering pattern around the multiples of the frequency modulation ratio  $M_f$ .

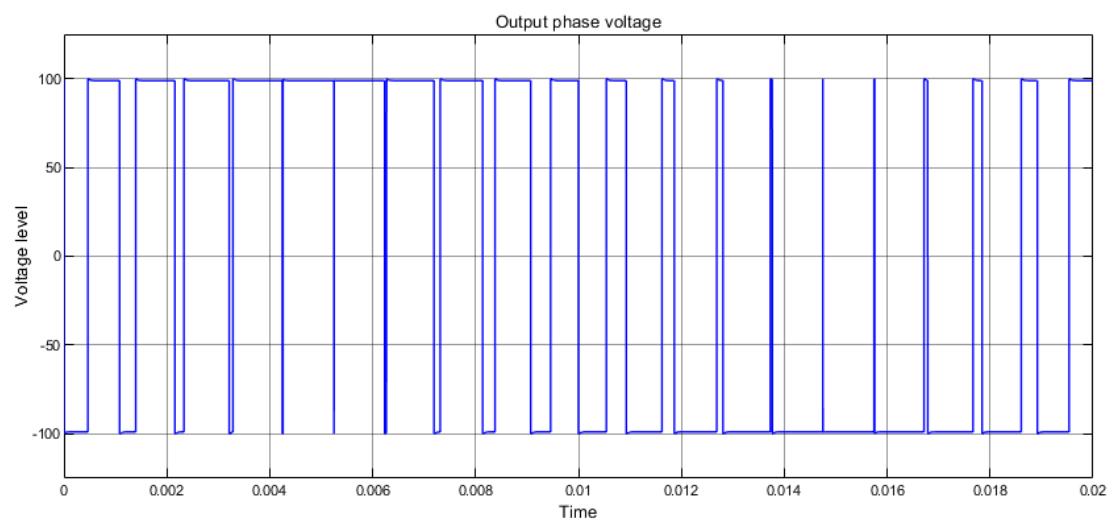


Figure 4.8: Output voltage waveform using bipolar switching.

In Figure 4.10, the output current drawn by the load is demonstrated. Considering the inductive nature of the load , eliminating the high order harmonics, it is possible to model the current behavior using a first-order differential equation 4.15. The response of this differential equation can be described by Equation 4.16.

### KVL loop equation 3.2.3 :

$$V_d + L \frac{di}{dt} + iR = 0 \quad (4.15)$$

Solving equation 4.15 results equation 4.16, however for more information and detailed steps check the reference book. [4]

$$i_{(t)} = \frac{V_d}{R} (1 - e^{-\frac{t}{\tau}}), \text{ where } \tau = \frac{L}{R} \quad (4.16)$$

In the investigation of the bipolar switching SPWM, it is mentioned all the values of the controlling parameters in 4.3, however including all the controlling parameters regarding the modulation index , frequency modulation index and etc.

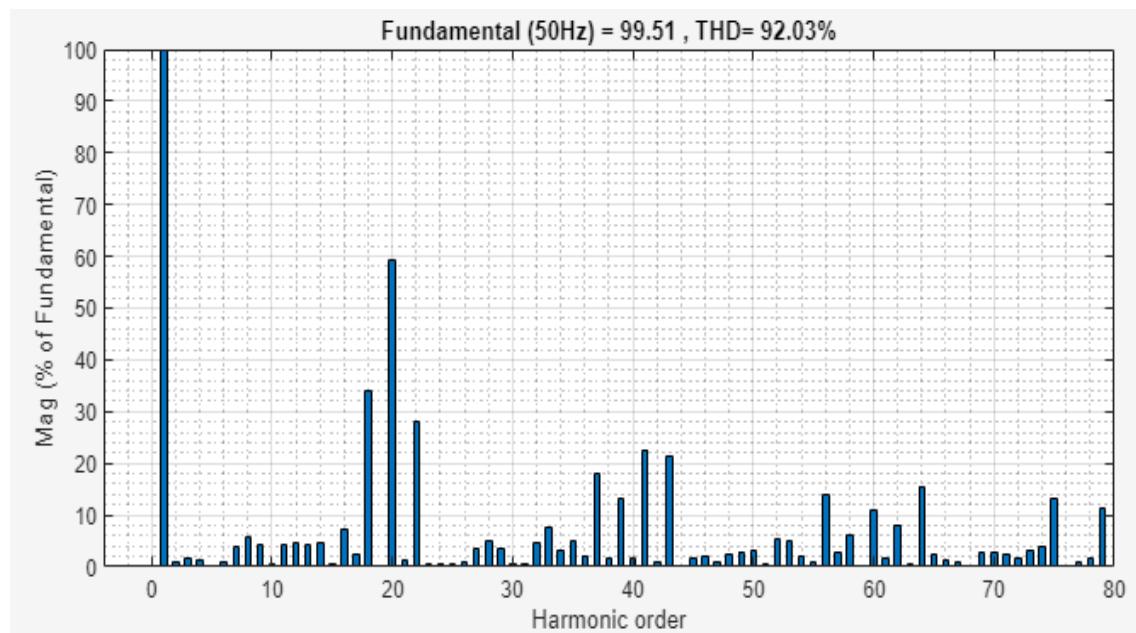


Figure 4.9: Harmonic spectrum of the output voltage using bipolar technique.

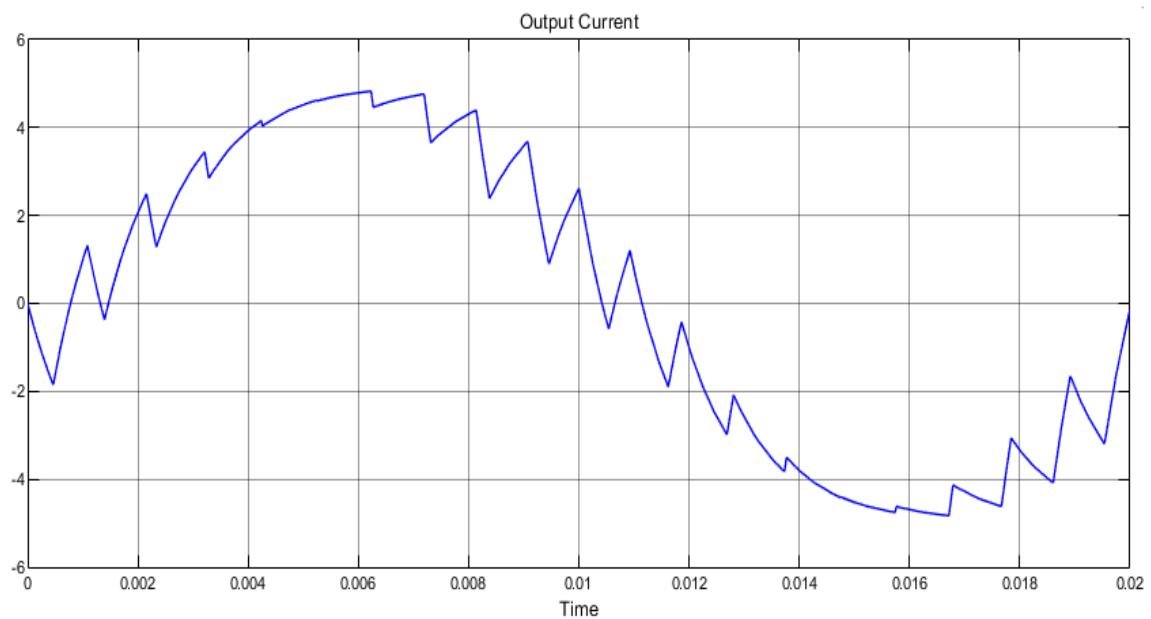


Figure 4.10: Output current waveform using bipolar switching.

Figure 4.11 illustrate the harmonic spectrum of the current using bipolar switching SPWM demonstrated in figure 4.10, and observed that the the harmonics are clustering in a pattern around a multiples of the modulation frequency ratio  $M_f$ .

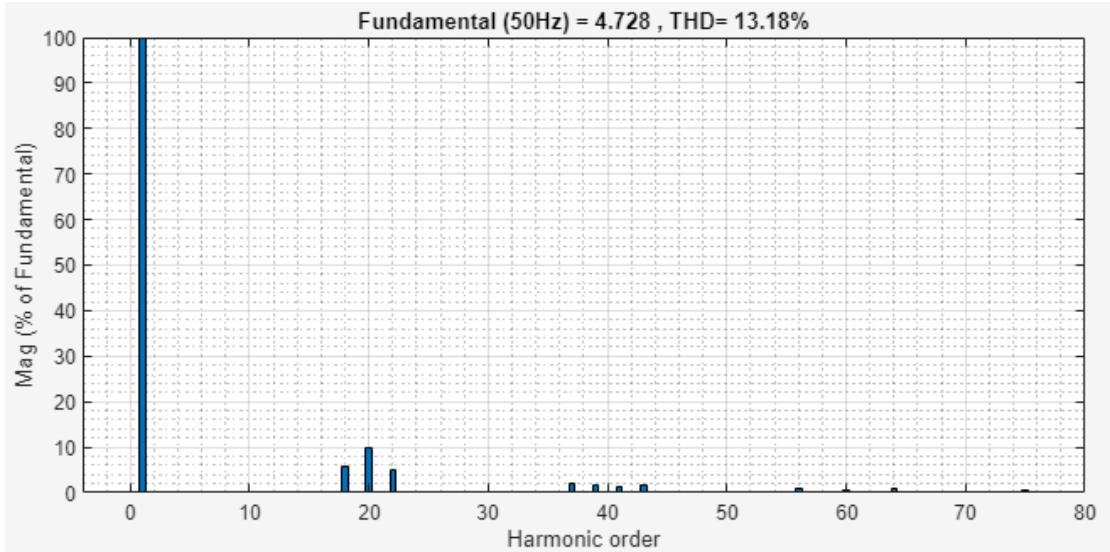


Figure 4.11: Harmonic spectrum of the output current using bipolar SPWM.

### 4.3.2 Unipolar PWM Switching Technique

In this approach, a carrier waveform is compared with two sinusoidal modulating signals: one positive and one negative means they are shifted 180 degree from each other. The concept behind producing Sinusoidal Pulse Width Modulation with Unipolar switching involves comparing the carrier waveform with both positive and negative reference signals. Unlike Bipolar SPWM generators, which use another comparator to compare with the inverse reference waveform, Unipolar voltage level alternates the output voltage between 0 and either  $V_d$  or  $-V_d$ . Consequently, in Unipolar switching, the change in output voltage during each switching event is halved compared to Bipolar switching. This results in a doubled effective switching frequency and a halved voltage pulse amplitude. As a consequence, the harmonic content of the output voltage waveform is reduced in Unipolar switching compared to Bipolar switching [4].The behaviour of the switching can be modeled as follows:

$$V_r > V_c, \text{ then } S_{11} \text{ is on thus, } V_{ao} = \frac{V_d}{2} \quad (4.17)$$

$$V_r < V_c, \text{ then } S_{12} \text{ is on thus, } V_{ao} = -\frac{V_d}{2} \quad (4.18)$$

$$-V_r > V_c, \text{ then } S_{21} \text{ is on thus, } V_{bo} = \frac{V_d}{2} \quad (4.19)$$

$$-V_r < V_c, \text{ then } S_{22} \text{ is on thus, } V_{bo} = -\frac{V_d}{2} \quad (4.20)$$

However, the output voltage described previously in equation 4.14.

Figure 4.12 depicts the control circuit responsible for generating the necessary gate signals by comparing two reference signals and the carrier signal using Sinusoidal Pulse Width Modulation with unipolar switching. In this setup,  $S_1$  represents the gate signal for switch  $S_{11}$ ,  $S_4$  represents the gate signal for switch  $S_{12}$ ,  $S_3$  represents the gate signal for switch  $S_{21}$ , and  $S_2$  represents the gate signal for switch  $S_{22}$ . The modulation index  $M_a$  is set to 1, and the modulation frequency  $M_f$  is set to 20, Where  $V_d$  is Dc power supply of the inverter , $V_r$  reference wave and  $V_c$  carrier wave.

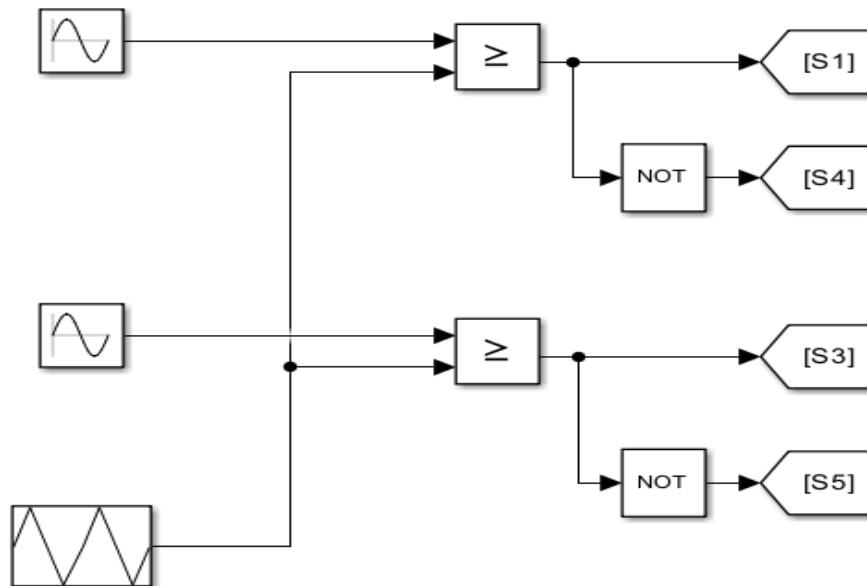


Figure 4.12: SPWM Unipolar Switching control circuit implemented using Simulink.

Figure 4.13 illustrates the generation of SPWM using the unipolar switching technique, incorporating two modulated signals and the carrier signal. Figure 4.14 demonstrates the gating signals sent to the VSI 4.5 following the comparison action event.

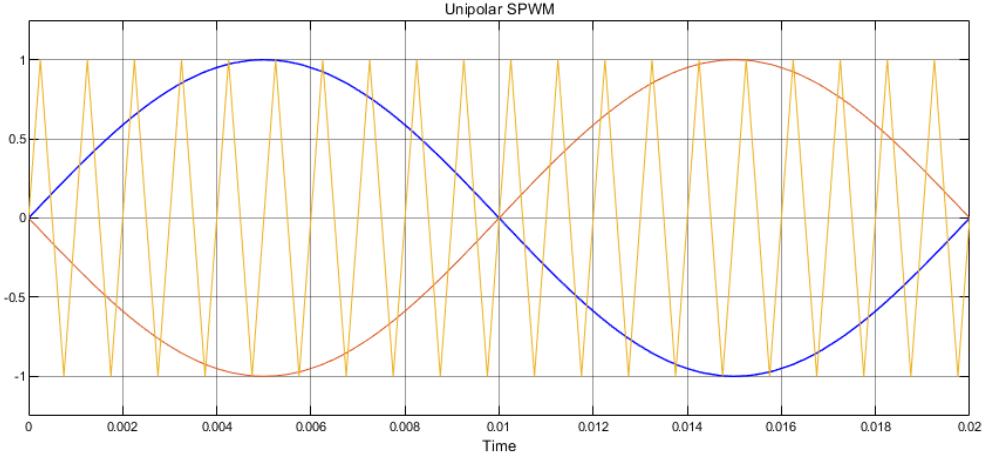


Figure 4.13: SPWM generation using Unipolar Switching and natural sampling.

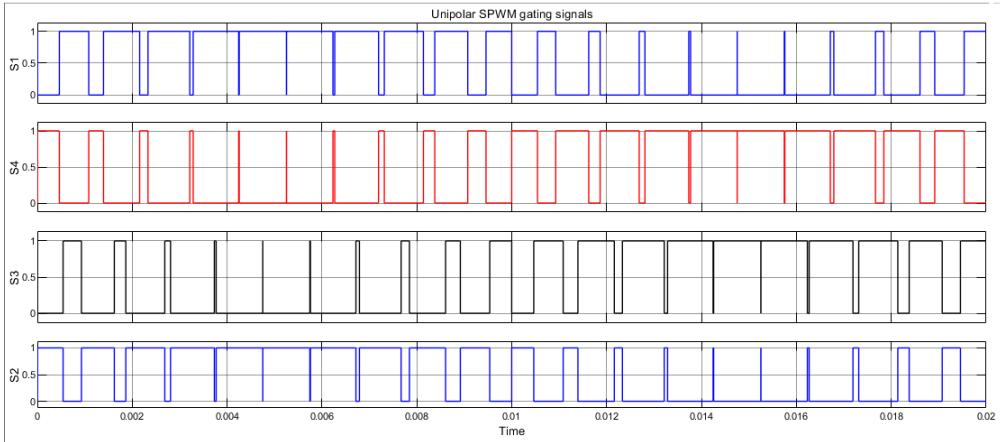


Figure 4.14: Corresponding gate signals of unipolar switching.

When both  $S_1$  and  $S_3$  are set to a HIGH state, it can be observed that both switches  $S_{11}$  and  $S_{21}$  will be activated simultaneously. This results in an absence of potential difference across the load, introducing a zero-level voltage on the output waveform.

Figure 4.15 demonstrates the behavior of the output phase voltage when applying unipolar switching in the VSI 4.5, and it confirms that the unipolar have three voltage levels fluctuating between  $V_d$ , 0 and  $-V_d$ . The parameters and values utilized for the load and other system parameters remain unchanged in the unipolar configuration, as they were in the bipolar setup 4.3.1.

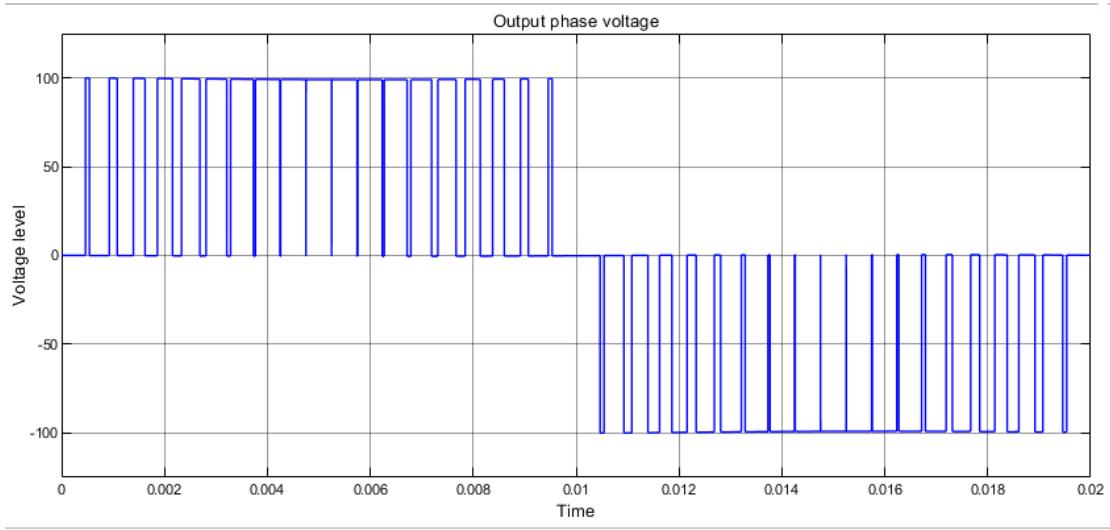


Figure 4.15: Output voltage waveform using unipolar switching

Figure 4.16 illustrates the harmonic spectrum analysis of the phase voltage waveform presented in Figure 4.15. Applying SPWM with unipolar switching effectively eliminates low-order harmonics, and overcoming the performance of the bipolar approach. However, It's observed that from Fig 4.15 the harmonics exhibit a distinctive clustering pattern around the even multiples of the frequency modulation ratio  $M_f$ , which behave to be more effective to the bipolar technique since it effectively eliminates the low order harmonics and shifts the harmonic cluster twice as much as the bipolar results, and resulting to have lower total harmonic distortion ( $THD$ ).

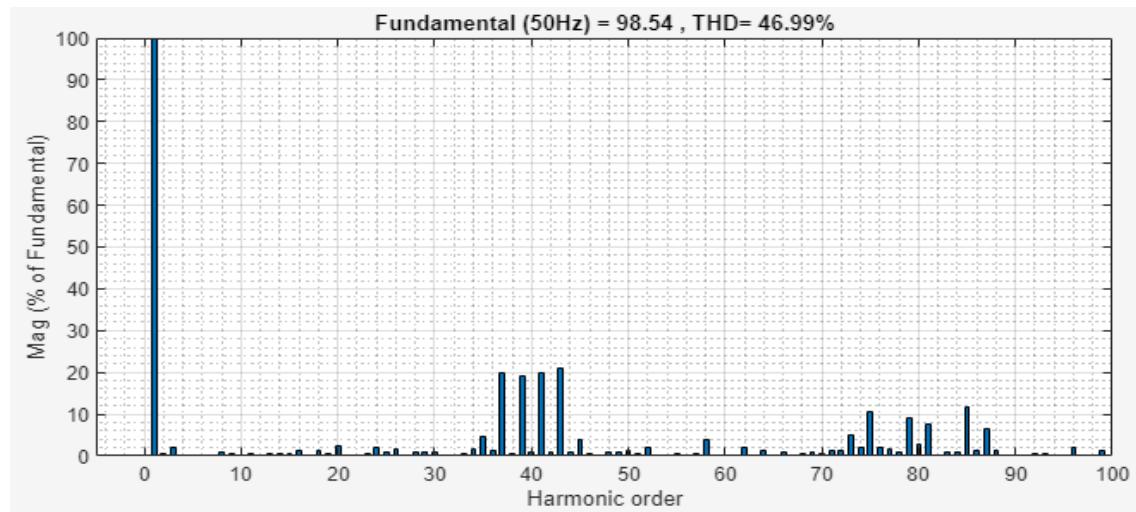


Figure 4.16: Harmonic spectrum of the output voltage using unipolar technique.

Figure 4.17 provides a visual representation of the current drawn by the load. Since the load is inductive, the response of the current is modeled previously using Equation 4.16.

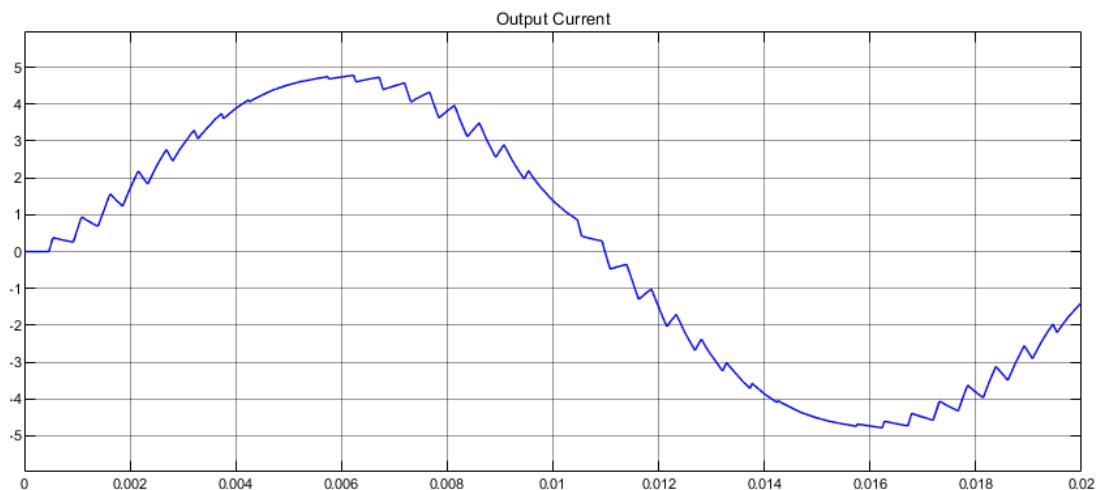


Figure 4.17: Output current waveform using unipolar switching.

It is observed that the output current using unipolar switching smoother and having better approximation to the fundamental component than bipolar scheme.

#### 4.4. THREE PHASE HALF BRIDGE INVERTER USING SPWM 66

Figure 4.18, demonstrates the harmonic spectrum of current using unipolar switching SPWM, as depicted in Figure 4.17. Notably, the harmonics tend to cluster around even multiples of the frequency modulation ratio  $M_f$ .

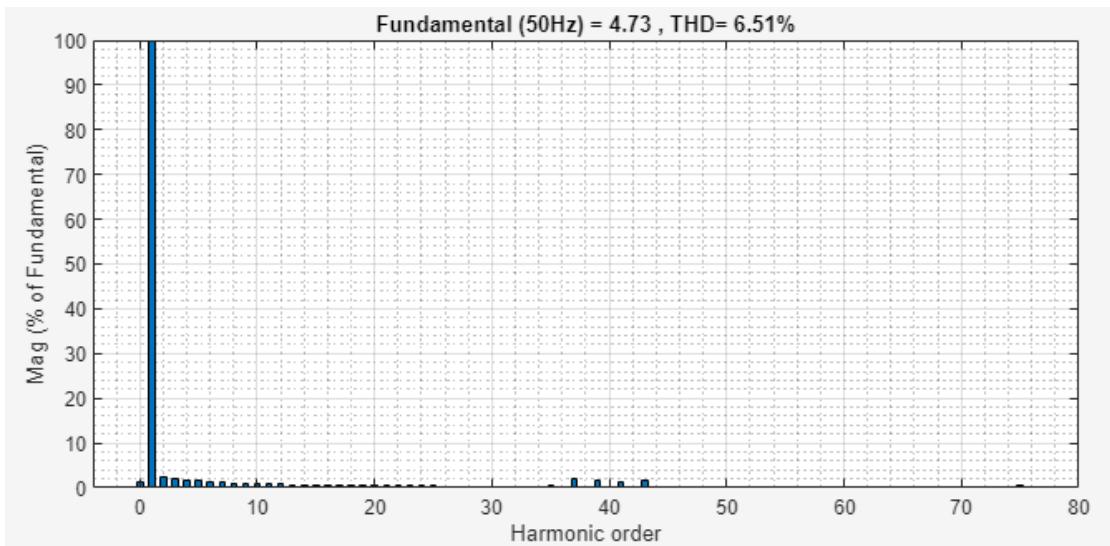


Figure 4.18: Harmonic spectrum of the output current using unipolar SPWM.

## 4.4 Three phase half bridge inverter using SPWM

In a three-phase inverter which explained briefly in subsection 3.2.3, three sinusoidal reference signals are utilized. These reference signals have a phase difference of  $120^\circ$  between each other, and since the architecture of the inverter is half bridge, bipolar switching is the only technique used, however The frequency of these sinusoidal waves is chosen based on the desired output frequency of the inverter, typically 50/60 Hz [30]. The carrier triangular wave, on the other hand, has a higher frequency usually in the several KHz range. By comparing the sinusoidal waves with the triangular wave, a gating signal to the power electronic switches is generated.

Figure 4.19 illustrates the three phase power inverter implemented in simulink for the purpose of the simulation, with three phase balanced inductive load ( $R - L$ ), Where ( $R = 20\Omega$   $L = 20_{mH}$ ), and with Dc voltage source  $V_d = 380v$ .

#### 4.4. THREE PHASE HALF BRIDGE INVERTER USING SPWM 67

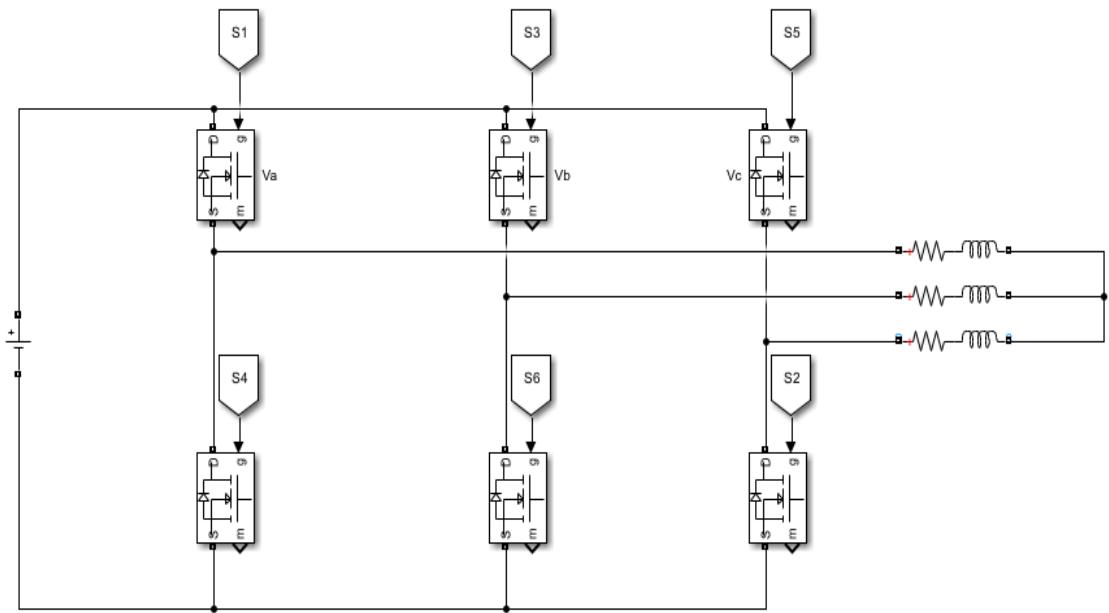


Figure 4.19: Three phase power inverter with 3 phase balanced load.

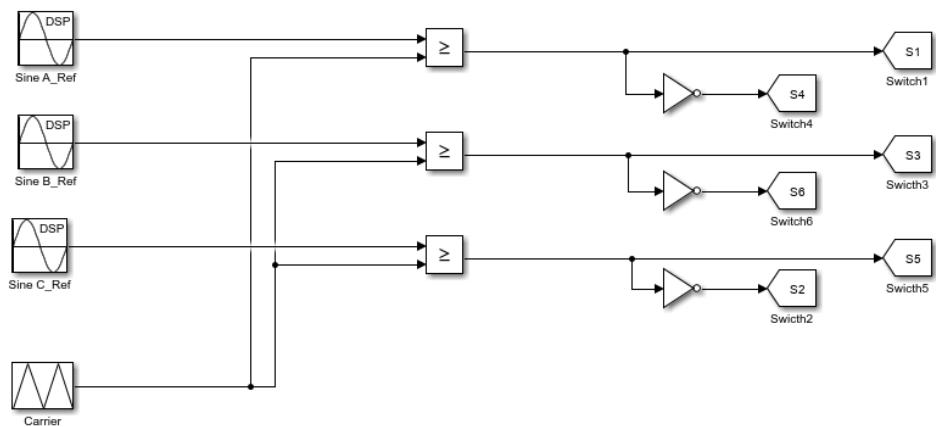


Figure 4.20: Control circuit for three phase SPWM generation.

#### 4.4. THREE PHASE HALF BRIDGE INVERTER USING SPWM 68

Figure 4.21 demonstrate the generation of three phase SPWM with a natural sampling and triangular carrier signal.

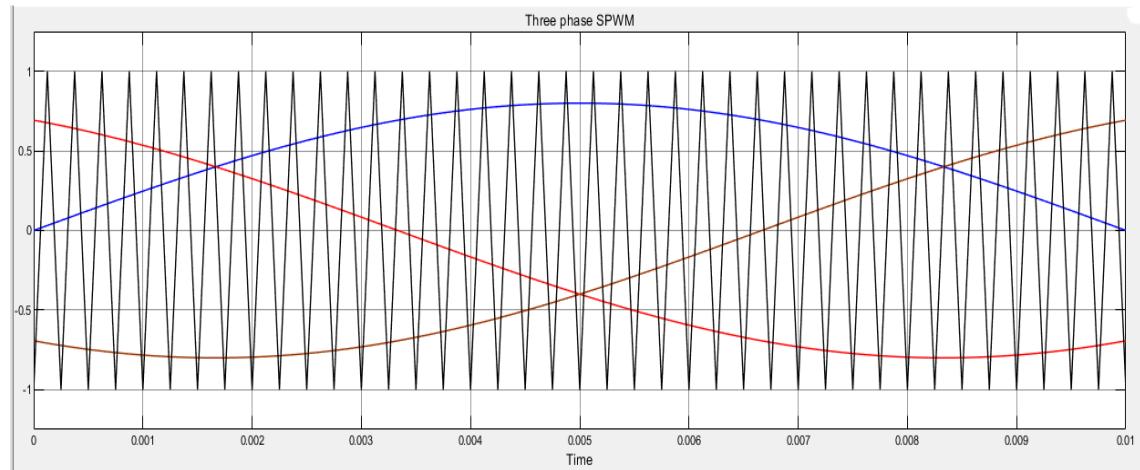


Figure 4.21: Three phase SPWM generation.

Figure 4.22 illustrates the generation of corresponding gate signal for each upper switch ( $S_1, S_3$  and  $S_5$ ) after the sine triangle comparison for each modulated phase signal.

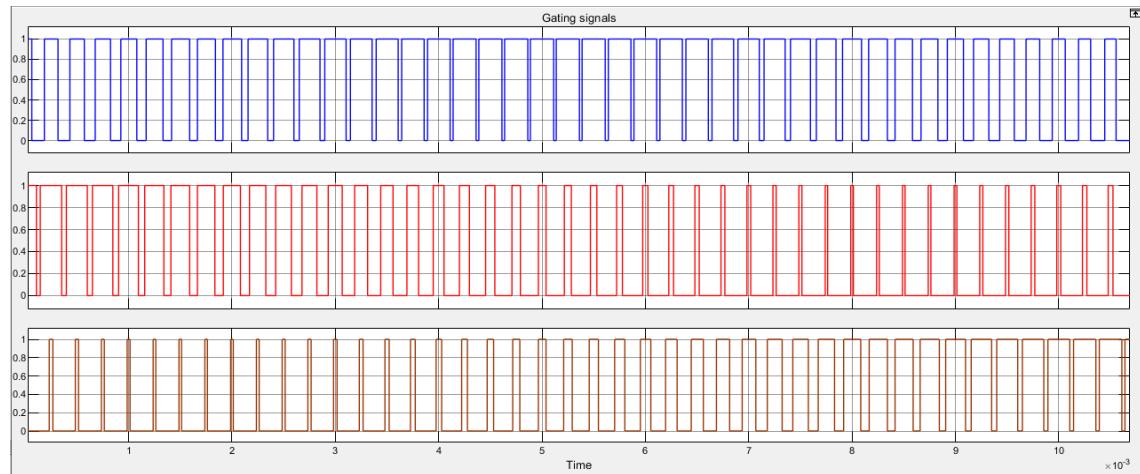


Figure 4.22: Three phase SPWM upper switches gate generation.

## 4.5 Case Studies

In this section, we present a series of case studies and comparisons that encompass various aspects and controlling parameters associated with the generation of Sinusoidal Pulse Width Modulation (SPWM). Our aim is to explore different approaches for achieving enhanced performance in SPWM generation.

### 4.5.1 Sampling Criteria

Previously, we discussed the various techniques for sampling the reference signal in Sinusoidal Pulse Width Modulation (SPWM). These techniques include natural sampling, where a real-time analog reference signal is utilized, and regular sampling, which can be further classified into symmetrical and asymmetrical sampling. The choice of sampling technique affects the characteristics and purity of the output waveform. Each sampling method has its own impact on the resulting waveform and requires careful consideration of the desired output quality.

For this study, we will set  $M_a$  to a value of 0.8 and  $M_f$  to 20. Additionally, an inductive load ( $R - L$ ) is used, where the resistance  $R$  is set to  $20 \Omega$  and the inductance  $L$  is set to 20 mH and the Dc voltage supplier  $V_d = 100v$ .

#### Natural sampling

Natural sampling was discussed briefly in section 4.2.1 and illustrated in the generation of SPWM in three phase system in fig 4.1

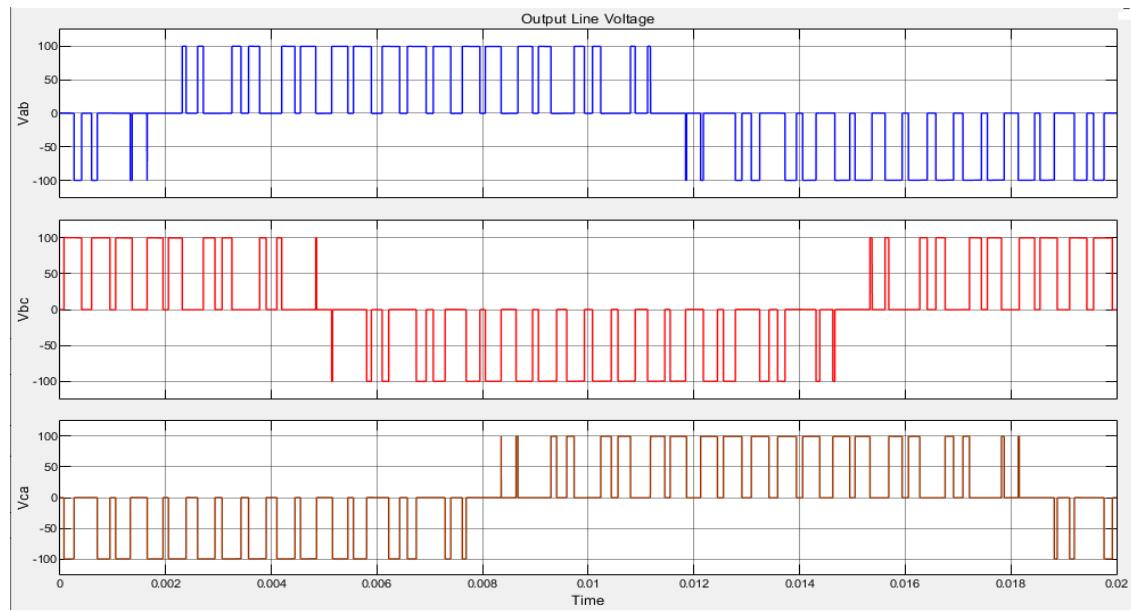


Figure 4.23: Output line voltage waveform using natural sampling.

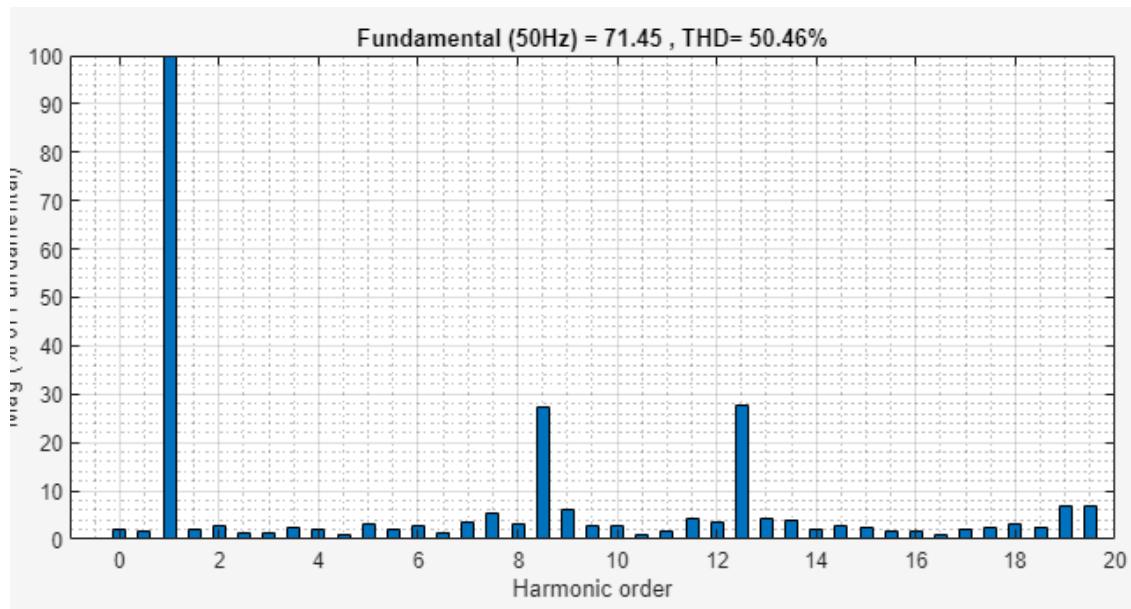


Figure 4.24: Harmonic spectrum of the line voltage waveform using natural sampling.

The harmonic spectrum in fig 4.24 illustrates the output line voltage with magnitude of the fundamental of 39.81v and  $THD = 56.47\%$ .

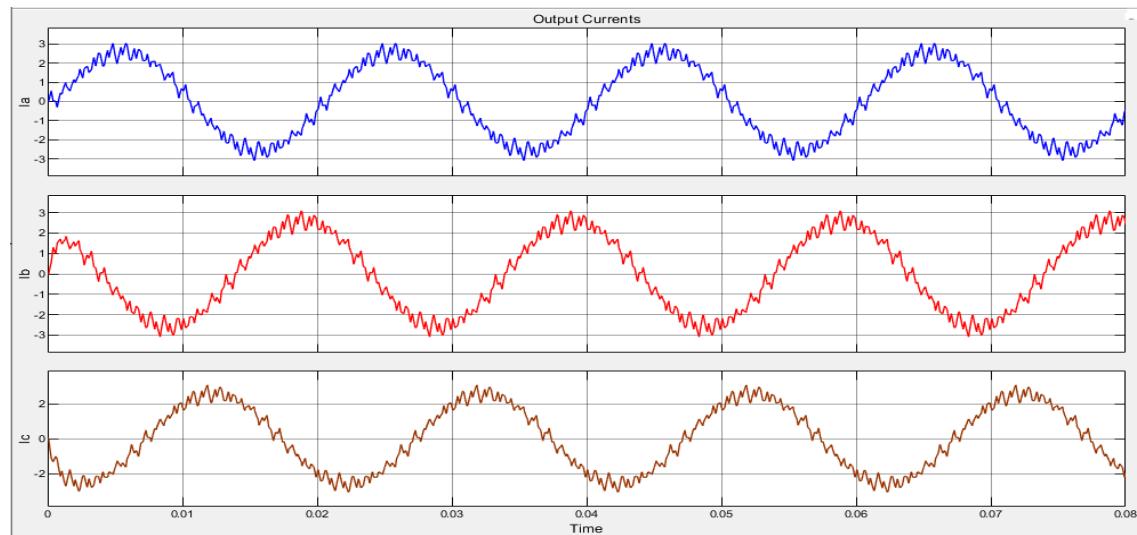


Figure 4.25: Output currents waveform using natural sampling.

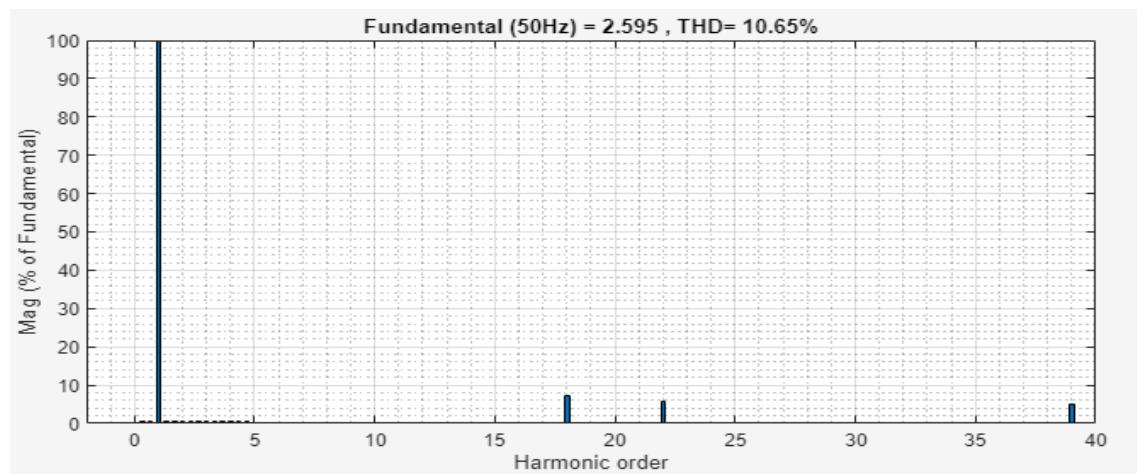


Figure 4.26: Harmonic spectrum of the output current using natural sampling.

The harmonic spectrum in fig 4.27 illustrates the output current with magnitude of the fundamental of 1.973A and  $THD = 30.66\%$ .

### Symmetrical sampling

As mentioned previously the symmetrical sampling may be considered not complex in its implementation, however it is discussed briefly in section 4.2.2. In this case study the sampled time used is  $1ms$ .

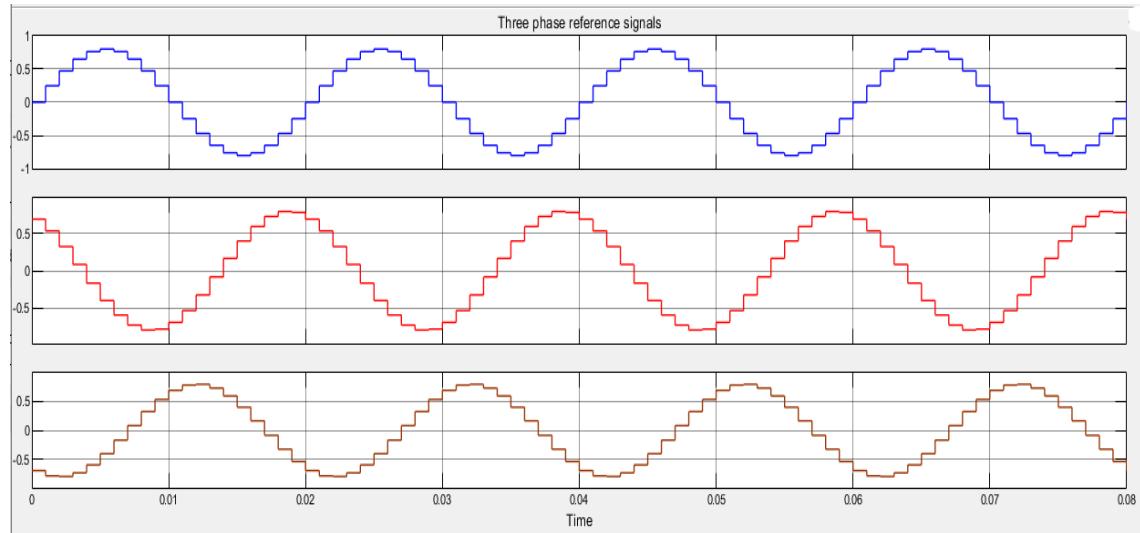


Figure 4.27: Three phase sampled modulating signals.

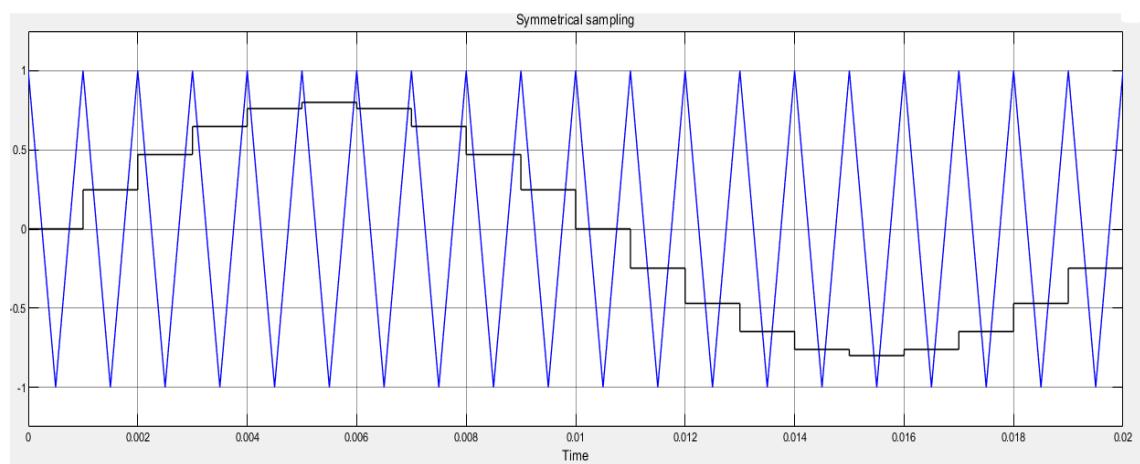


Figure 4.28: Symmetrical sampling SPWM for one of the three modulated waves.

The output line voltage waveform is resulting from Symmetrical sampling SPWM is illustrated in Fig4.29, where its harmonic spectrum is demonstrated in fig 4.30

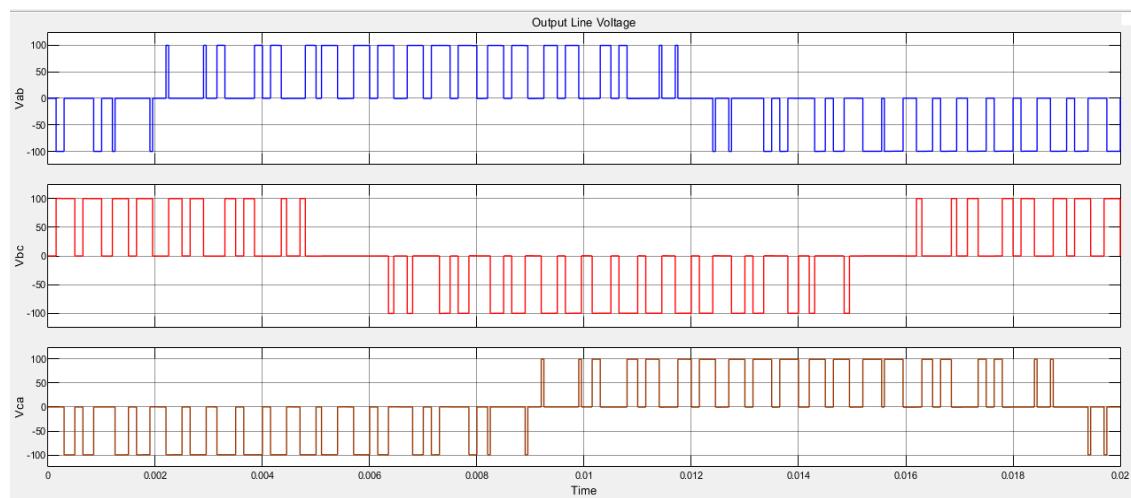


Figure 4.29: Output line voltage using Symmetrical sampling.

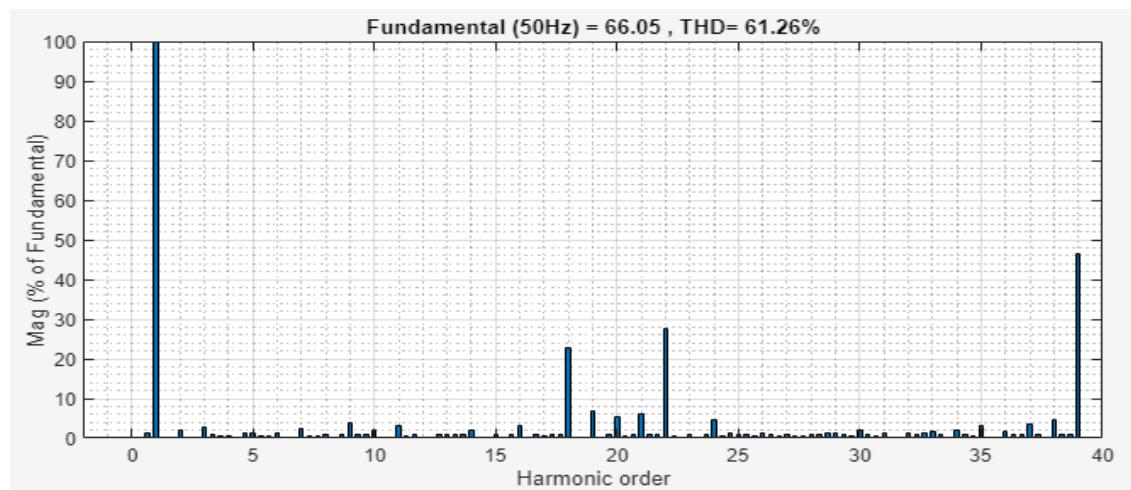


Figure 4.30: Harmonic spectrum for the output line voltage using symmetrical sampling.

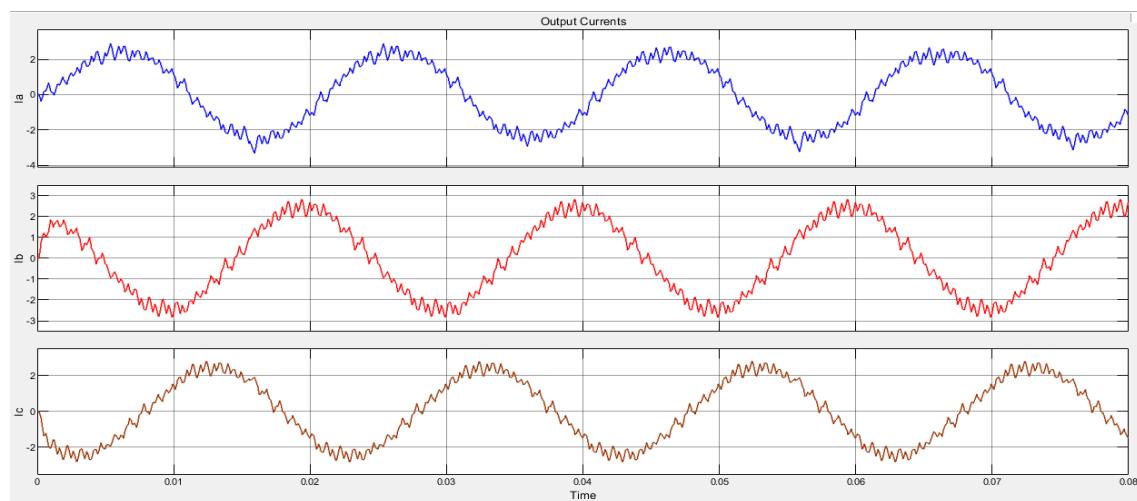


Figure 4.31: Output current using symmetrical sampling.

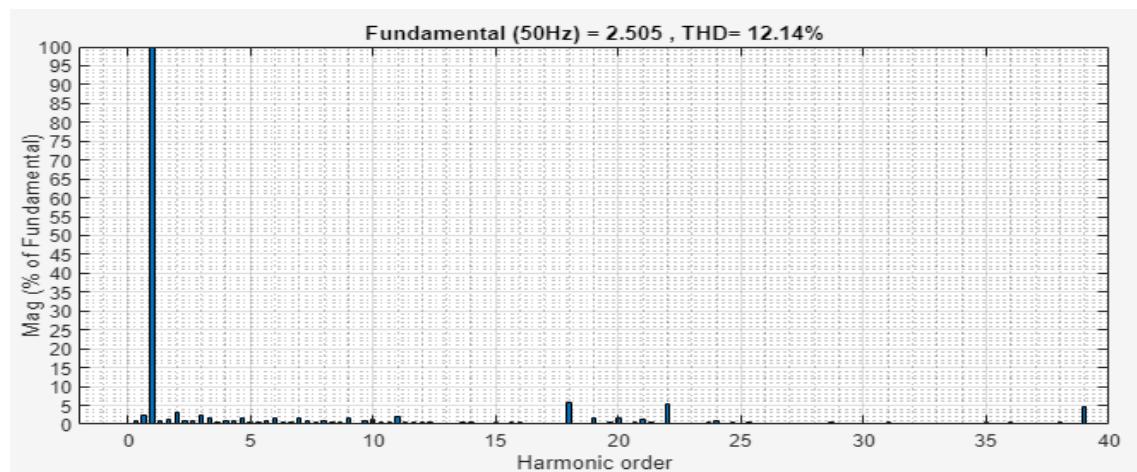


Figure 4.32: Harmonic spectrum for the output current using symmetrical sampling.

The harmonic spectrum in fig 4.32 illustrates the output current with magnitude of the fundamental of 2.505A and  $THD = 12.14\%$ .

### Asymmetrical sampling

Asymmetrical modulation occurs when the triangular carrier waveform is compared with a stepped sine wave generated by sampling and holding at a frequency twice that of the carrier waveform. its implementation considered to be lower in complexity relative to the natural sampling and higher with respect to the symmetrical sampling technique , it is discussed briefly in section 4.2.2.

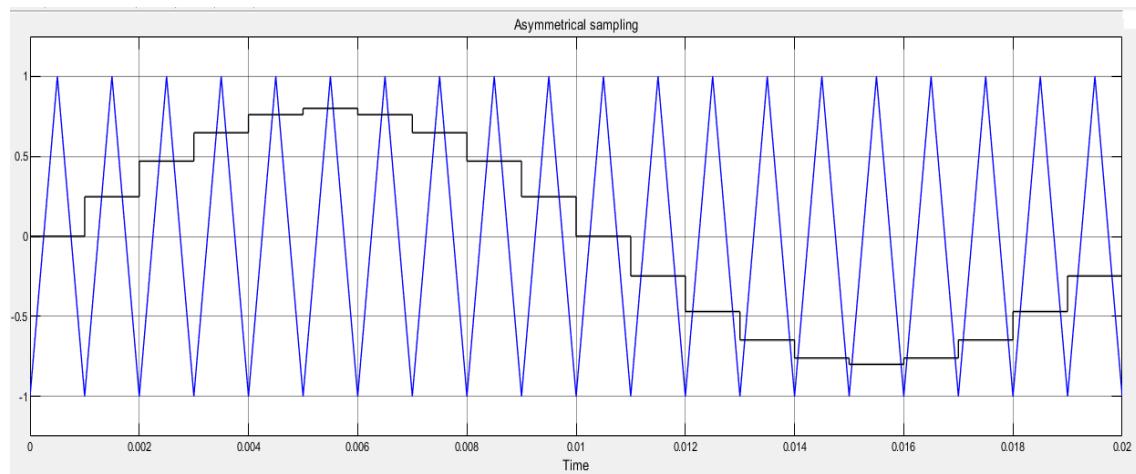


Figure 4.33: Asymmetrical sampling SPWM for one of the three modulated wave.

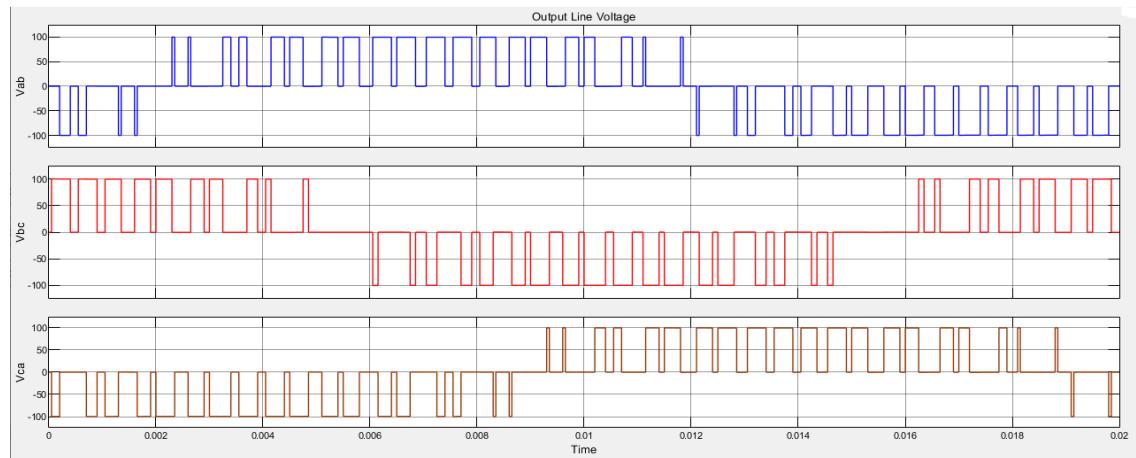


Figure 4.34: Output line voltage using Asymmetrical sampling SPWM.

The harmonic spectrum in fig 4.35 illustrates the output line voltage with magnitude of the fundamental of 70.68v and  $THD = 58.03\%$ .

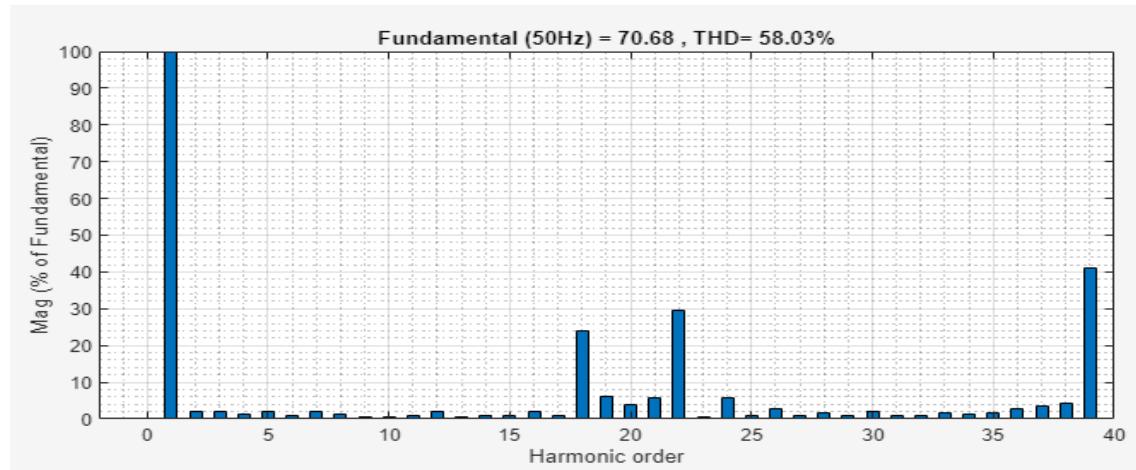


Figure 4.35: Harmonic spectrum of the output line voltage using asymmetrical SPWM.

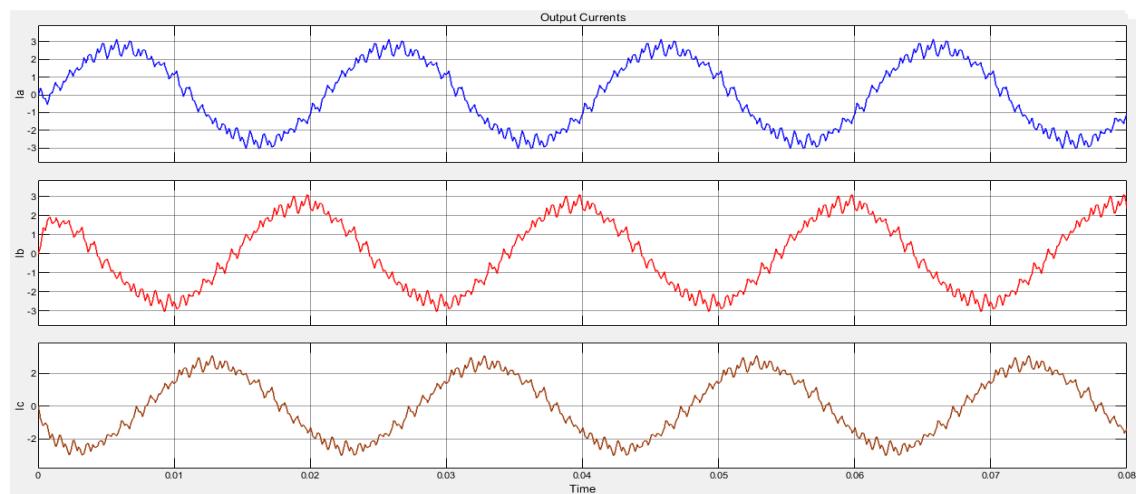


Figure 4.36: Output current using asymmetrical SPWM.

The harmonic spectrum in fig 4.37 illustrates the output current with magnitude of the fundamental of 2.583A and  $THD = 11.54\%$ .

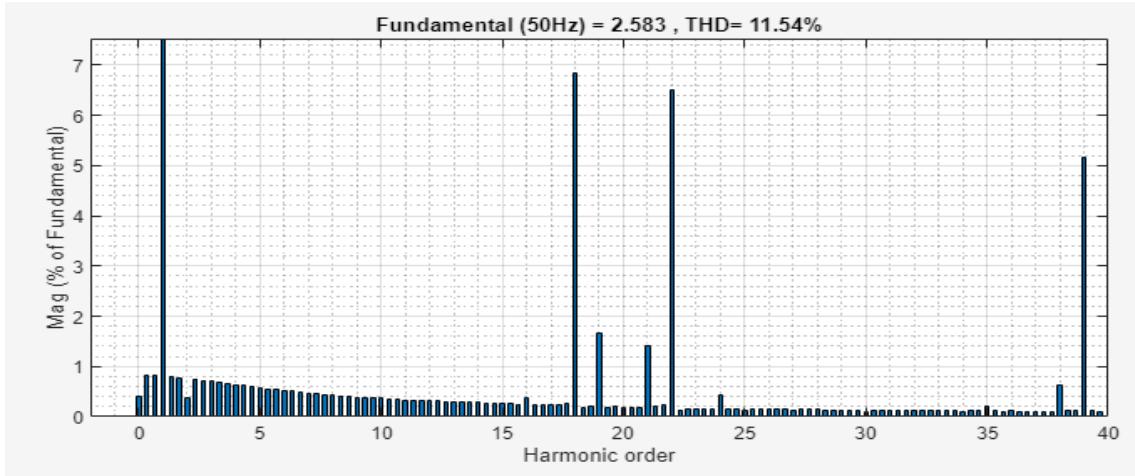


Figure 4.37: Harmonic spectrum of the output current using asymmetrical SPWM.

### Comments on the results of sampling criteria

Upon comparing the three sampling modes of natural, symmetrical, and asymmetrical, it can be observed that natural sampling exhibits the highest performance in terms of the fundamental magnitude and total harmonic distortion in the output waveform. However, the complexity associated with its computational requirements limits its practical implementation, as discussed in Section 4.2.1. On the other hand, when comparing the two regular sampling techniques, symmetrical and asymmetrical, it has been confirmed that asymmetrical sampling outperforms symmetrical sampling in terms of total harmonic distortion and the magnitude of the fundamental component in the output waveform. However, it should be noted that implementing asymmetrical sampling comes with increased complexity compared to its symmetrical counterpart. These observations lead to the conclusion that while natural sampling provides the highest performance, it is challenging to implement due to its computational complexity. Asymmetrical sampling, on the other hand, provides improved performance in terms of harmonic distortion and

fundamental magnitude compared to symmetrical sampling, albeit with increased implementation complexity. [7]

#### 4.5.2 Exploring the Impact of Frequency Modulation Ratio Variations

This case study aims to explore the performance implications of altering the frequency modulation ratio, which is defined as the ratio of the frequency of the carrier signal to the frequency of the reference signal, within the system,. The focus will be on investigating how variations in the frequency modulation ratio affect the performance of the system and it's such as the total harmonic distortion in the output wave form ,the fundamental component in the output and etc,however For this study, we will set  $M_a$  to a value of 0.8 and will use the natural sampling technique.Additionally,an inductive load ( $R - L$ ) is used, where the resistance  $R$  is set to  $20 \Omega$  and the inductance  $L$  is set to 50 mH and the Dc voltage supplier  $V_d = 100v$ .

**Introduce Modulation frequency ratio ( $M_f = 30$ )**

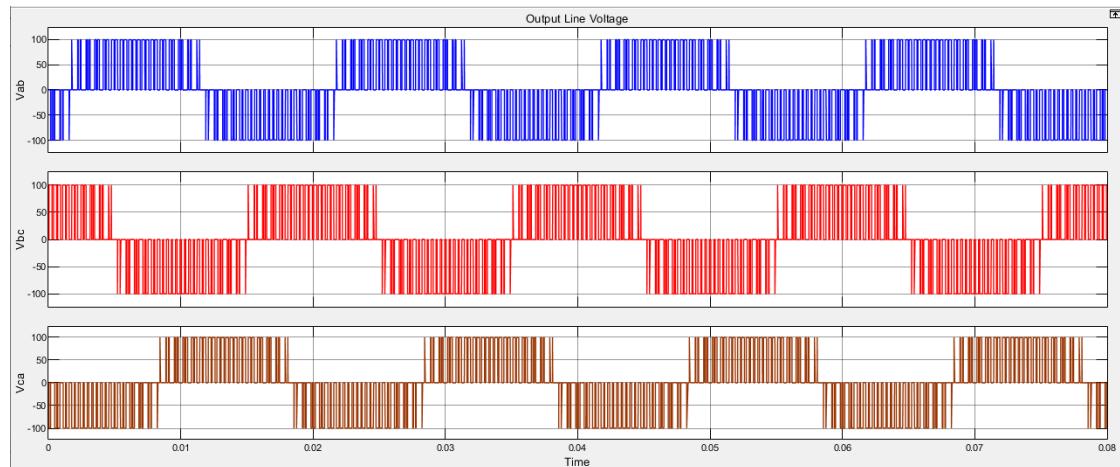


Figure 4.38: Output line voltage using when  $M_f = 30$ .

The harmonic spectrum in fig 4.39 illustrates the line voltage with magnitude of the fundamental of 69.72v and  $THD = 39.55\%$ .

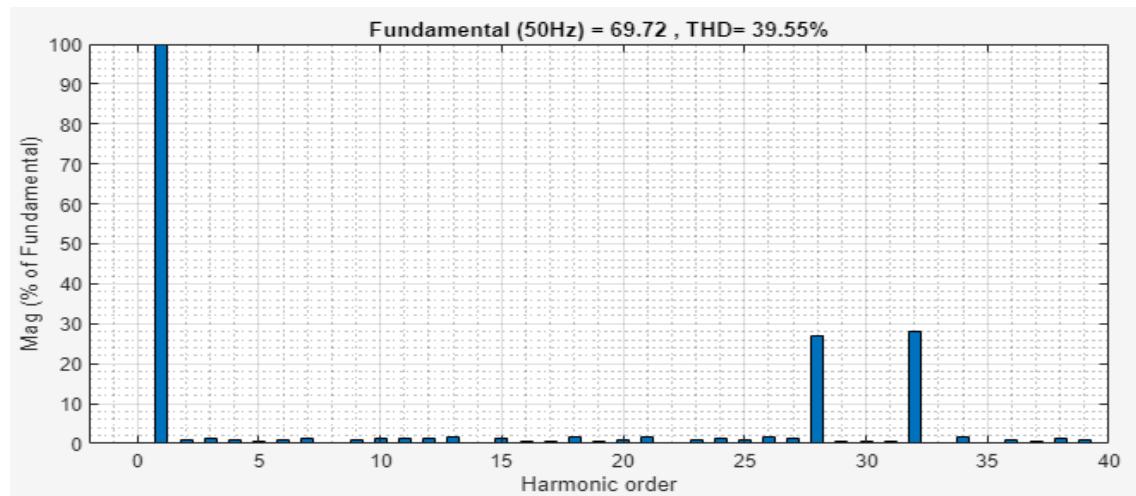


Figure 4.39: Harmonic spectrum of line voltage when  $M_f = 30$ .

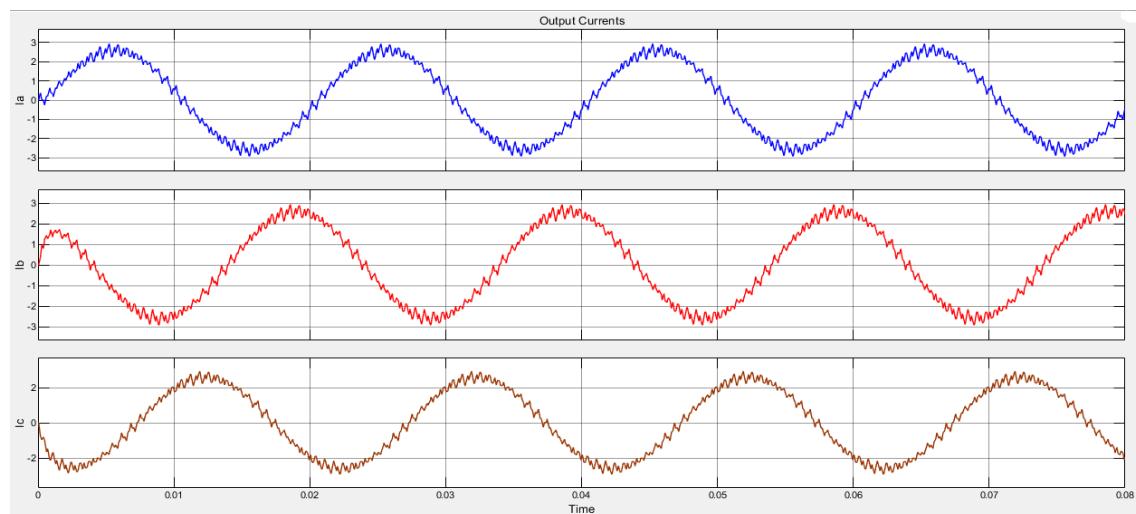


Figure 4.40: Output current when  $M_f = 30$ .

The harmonic spectrum in fig 4.41 illustrates the output current with magnitude of the fundamental of 2.596A and  $THD = 6.67\%$ .

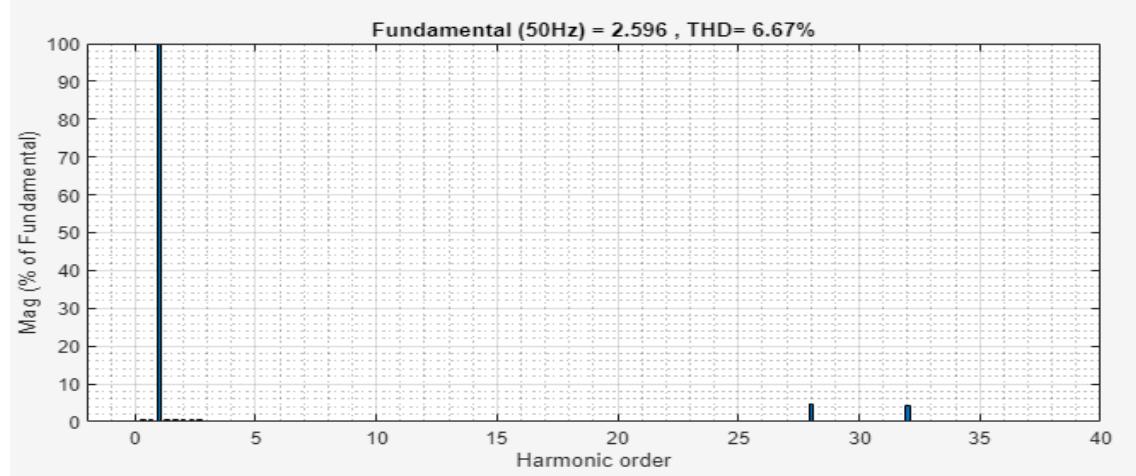


Figure 4.41: Harmonic spectrum of current when  $M_f = 30$ .

In order to align with the high-frequency nature typically seen in microcontrollers or microprocessors, we will enhance the carrier frequency to 20 kHz for this particular case study. As a result, the frequency modulation ratio, represented by  $M_f$ , will be set to 400.

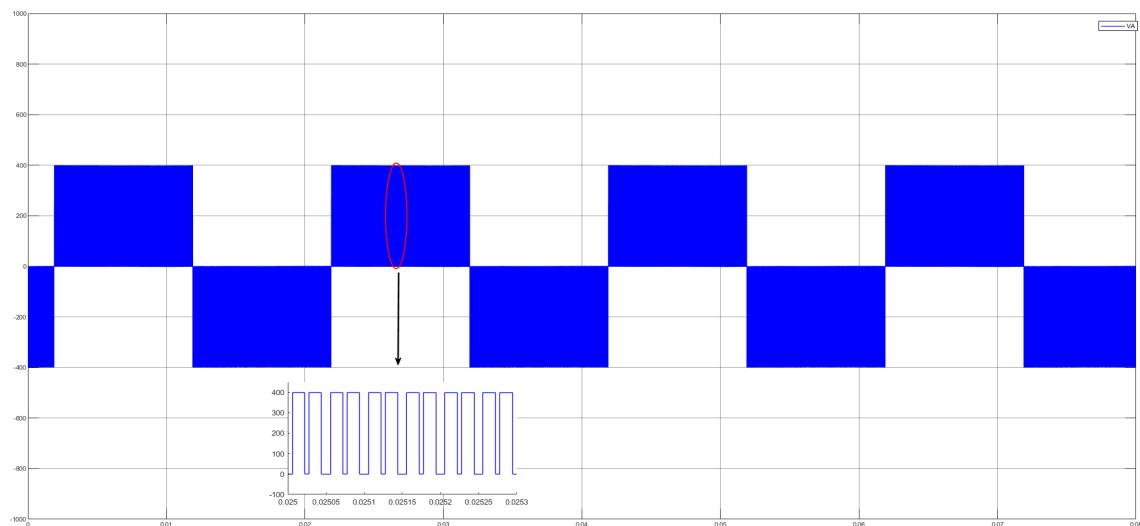


Figure 4.42: Output line voltage when  $M_f = 400$ .

The harmonic spectrum in fig 4.43 illustrates the output line voltage with magnitude of the fundamental of 68.94v and  $THD = 0.75\%$ .

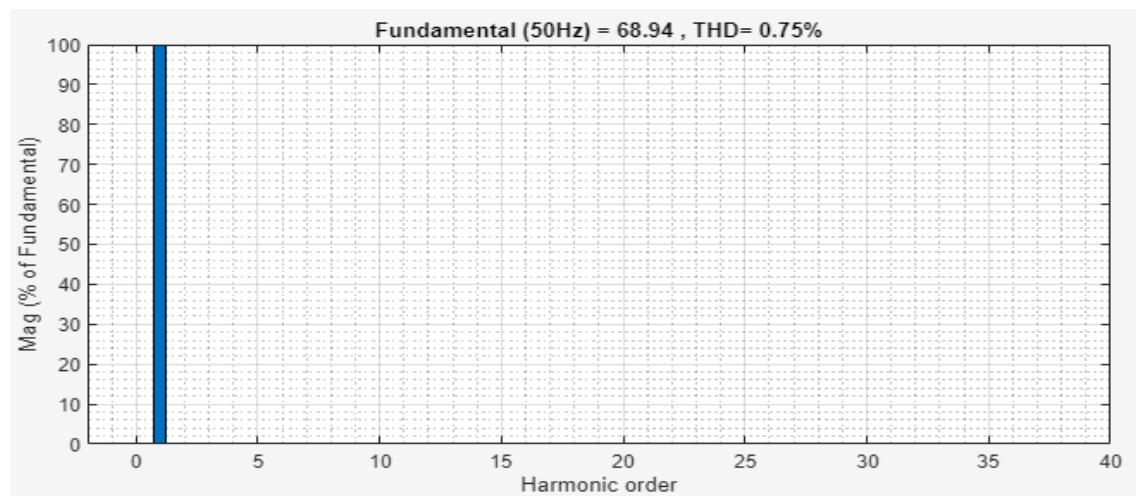


Figure 4.43: Harmonic spectrum of the line voltage when  $M_f = 400$ .

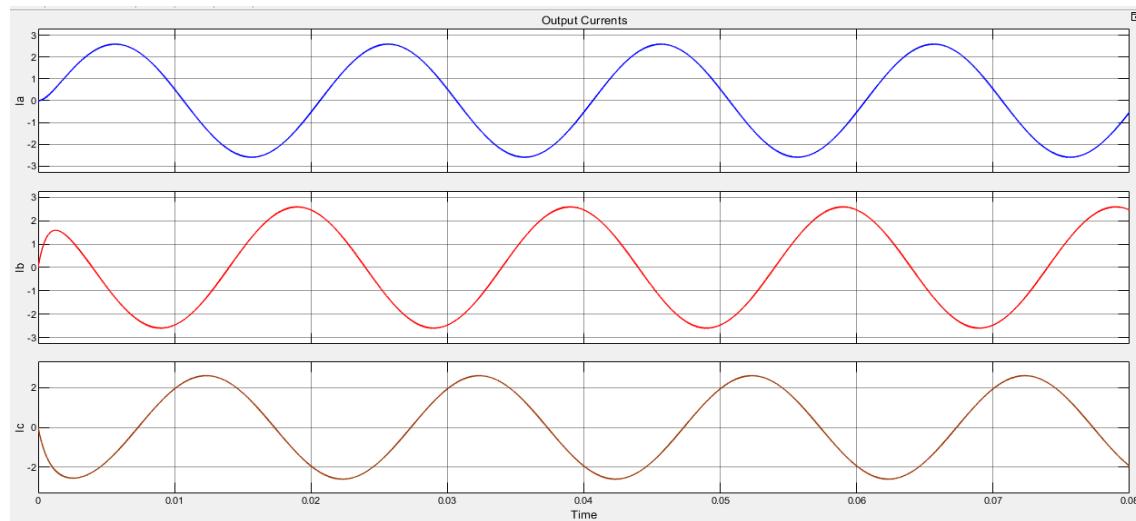


Figure 4.44: Output current when  $M_f = 400$ .

The harmonic spectrum in fig 4.45 illustrates the output current with magnitude of the fundamental of 2.596A and  $THD = 0.01\%$ .

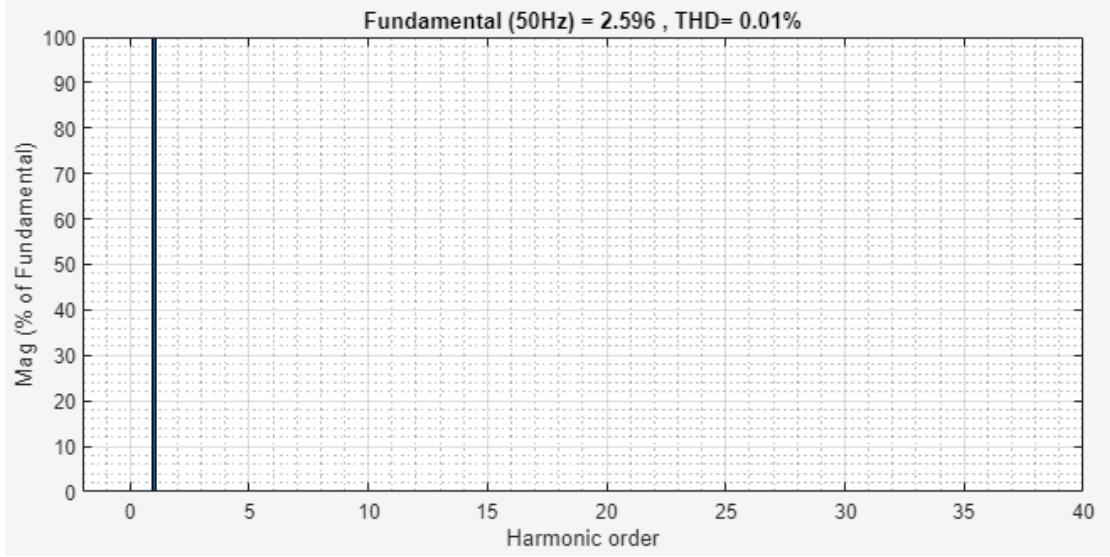


Figure 4.45: Harmonic spectrum of current when  $M_f = 400$ .

### Comments on the results of the Impact of frequency modulation ratio

From the results it becomes clear that increasing the frequency modulation ratio significantly enhances the performance of both the voltage and current output waveform. This improvement is characterized by several notable effects. Firstly, increasing the modulation ratio effectively eliminates low-order harmonics below the value of the modulation ratio, and increasing the fundamental component in the output waveform. This results in a smoother and more refined waveform, free from undesirable distortions and unwanted frequency components. Consequently, the overall quality and accuracy of the output waveform are greatly enhanced. Furthermore, a fascinating observation is that higher-order harmonics tend to cluster around multiples of the modulation ratio  $M_f$  [7].

### 4.5.3 Impact of the modulation index

This case study aims to investigate the performance implications of adjusting the modulation index within the system. The objective is to understand how variations in the modulation index influence the system's performance parameters such as total harmonic distortion in the output waveform and the fundamental component in the output. For this study, we will maintain a frequency modulation ratio ( $M_f$ ) of 30 and utilize the natural sampling technique. Moreover, an inductive load ( $R - L$ ) will be employed, with the resistance (R) set to  $20 \Omega$  and the inductance (L) set to  $50 \text{ mH}$ , alongside a DC voltage supplier ( $V_D$ ) =  $100\text{V}$ .

For SPWM The maximum output phase voltage is a function of the modulation index which is illustrated in Eqs.4.21

$$V_{out} = \frac{M_a}{2} V_{dc} \sin(\omega t + \phi) \quad (4.21)$$

Figure 4.46 illustrate the effect of the modulation index on the total harmonic distortion and how it enhances the performance of the output waveform of both voltages and currents.

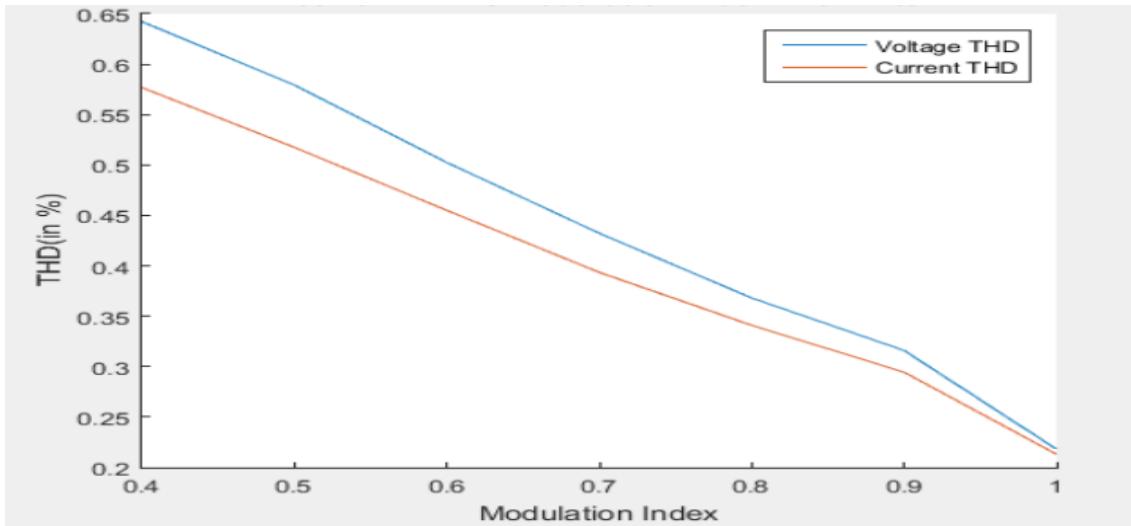


Figure 4.46: Impact of the modulation index on  $THD$ .

By setting the modulation index  $M_a$  to 0.5, it is observed a noticeable impact on the voltage level of the output line waveform at which the duty cycle of each pulse reduced as illustrated in Figure 4.47. This effect occurs because the gate signals experience a reduction in width, attributed to a shorter duration in the on state, consequently resulting in a lower duty cycle. which illustrated in figure 4.48.

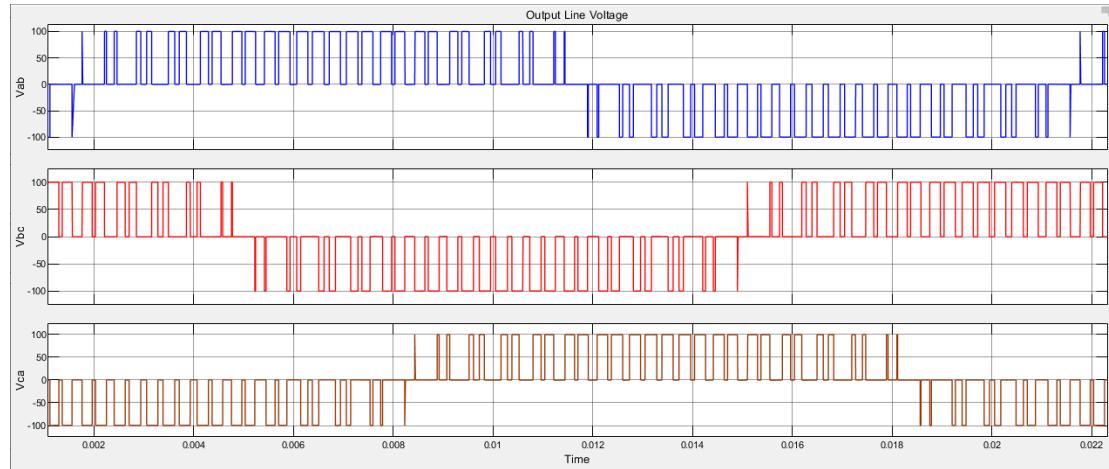


Figure 4.47: Output line voltage when  $M_a = 0.5$ .

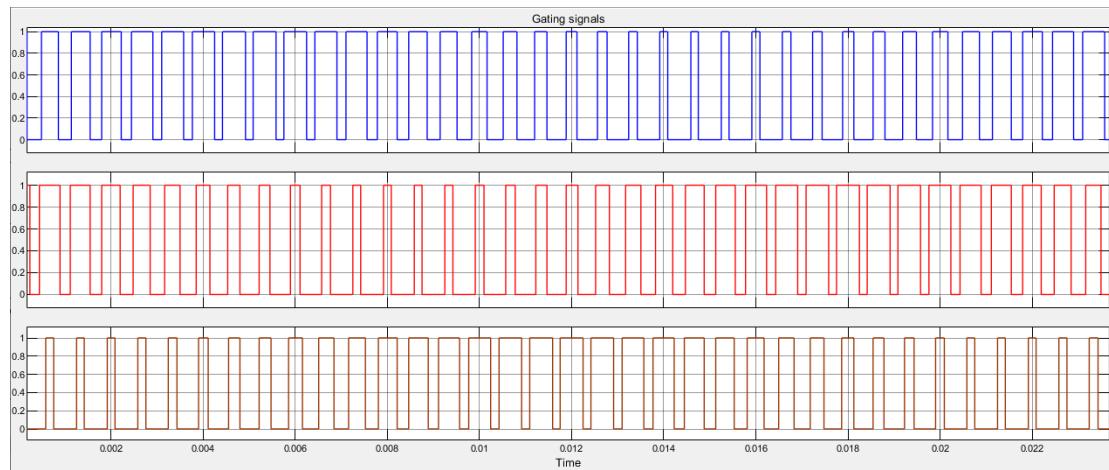


Figure 4.48: Gating Signals to switches  $S_1, S_3$  and  $S_5$  when  $M_a = 0.5$ .

Figure 4.49 depicts the output line voltage when the modulation index is set to 1.3, indicating the modulation technique entering the over modulation region. However the maximum attainable modulation index before entering the overmodulation region is 1.

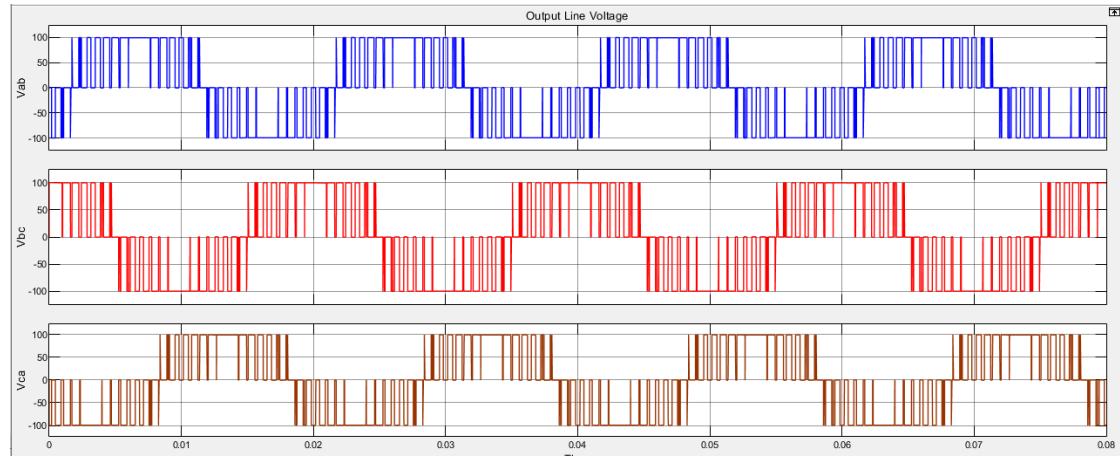


Figure 4.49: Output line voltage with  $M_a = 1.3$ .

Figure 4.50 illustrate the output line voltage's harmonic spectrum when  $M_a = 1.3$  and it can be observed that when entering the over modulation region the output wave form is distort.

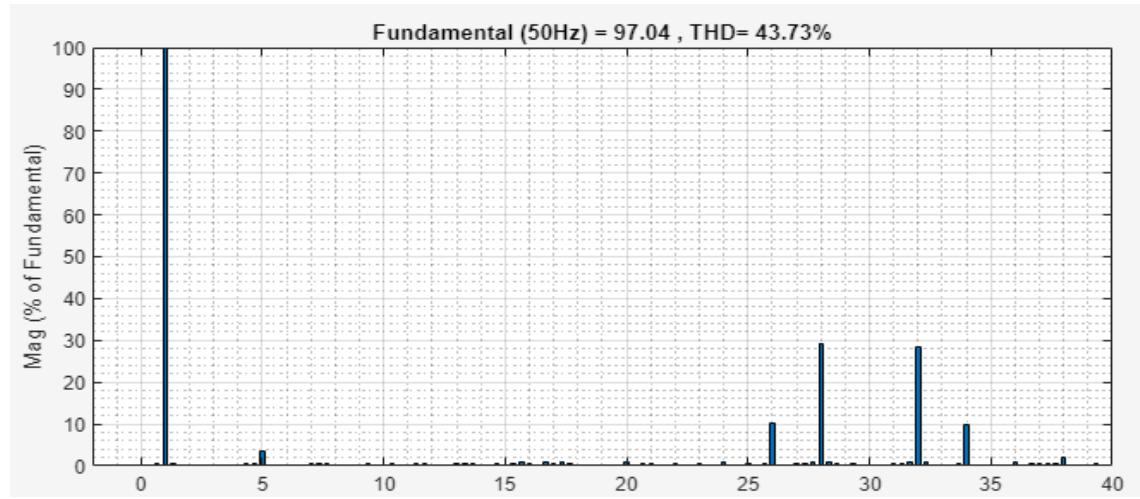


Figure 4.50: Harmonic spectrum of the line voltage when  $M_a = 1.3$ .

### Comments on the results of the impact of modulation index

It is noticed that the modulation index significantly influences the total harmonic distortion of the output waveform. Increasing the modulation index enhances the fundamental component in the output until reaching the threshold of overmodulation. Prior to entering this region, this enhancement tends to decrease distortion in the output waveform. Moreover, adjusting the modulation index enables precise control over the voltage level, highlighting the importance of selecting the appropriate modulation index for desired voltage regulation.

#### 4.5.4 Designing a passive LC low pass filter

Low-pass filters are filter circuits that pass DC and low-frequency signals and cut high-frequency signals. They are the most widely used filter circuits and are mainly used to cut high-frequency noise. In audio, they are also used to cut treble/mid-range sound components of bass speakers. However we will implement it to eliminate the high order harmonics from the output wave form and to enhance the response of the output. Figure 4.51 shows the basic circuit consists of an inductor and capacitor that can operate as a low pass filter.

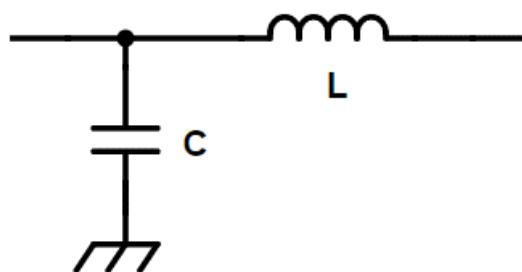


Figure 4.51: Low pass passive LC filter circuit [7].

The designing of a passive LC is just about to select the desirable values for L and C to achieve the targeted cutoff frequency, however the cut off frequency can approximated as  $0.1F_{sw}$ , and the designing criteria is to assume one of the

parameters and to find the other one , however in this case we will select the inductor value  $L=0.01H$  , and using the following relation :[7]

$$F_{cutoff} = \frac{1}{4\pi\sqrt{LC}} \quad (4.22)$$

For switching frequency 15Khz, however this value is an approximation to the average value of the switching frequency of the most of the microcontrollers and could be higher. and from equation 4.22 the capacitance value is about  $1.1258\mu F$ .

After designing the low-pass LC filter to attenuate high-order frequencies, we can employ it to filter the desired output voltage and current of the system. Figure 4.52 illustrates the resulting line voltage after filtration, showcasing its restoration to its fundamental behavior. Additionally, Figure 4.53 shows the corresponding output current,in which  $V_d = 400v$  , $M_a = 1$ ,  $M_f = 300$ . However, it is important to note that passive filters alone are unable to completely eliminate low-order harmonics. While the filter effectively reduces high-order harmonics, the presence of low-order harmonics persists even after filtration.

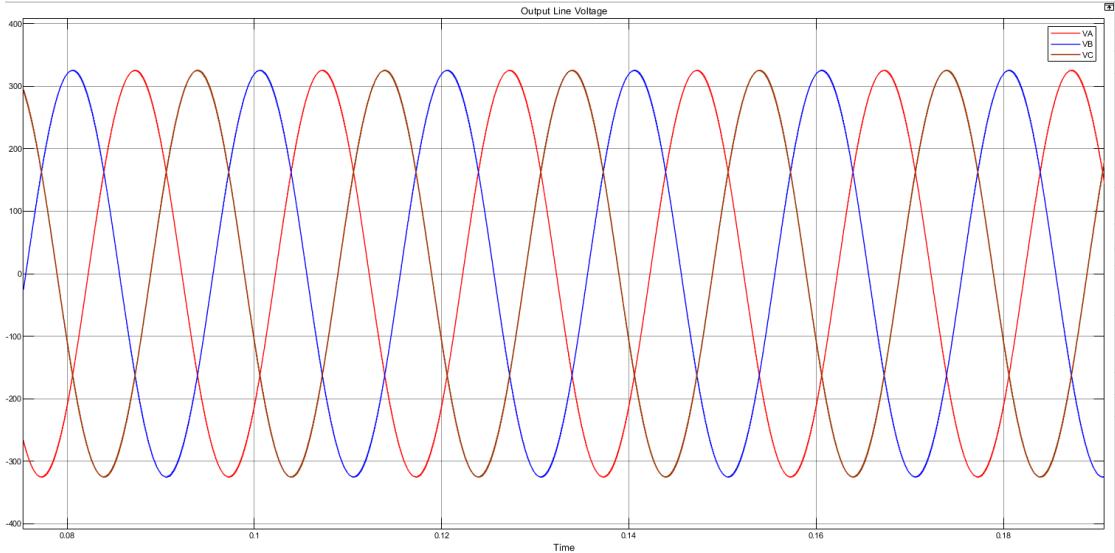


Figure 4.52: Output line voltage after filtering.

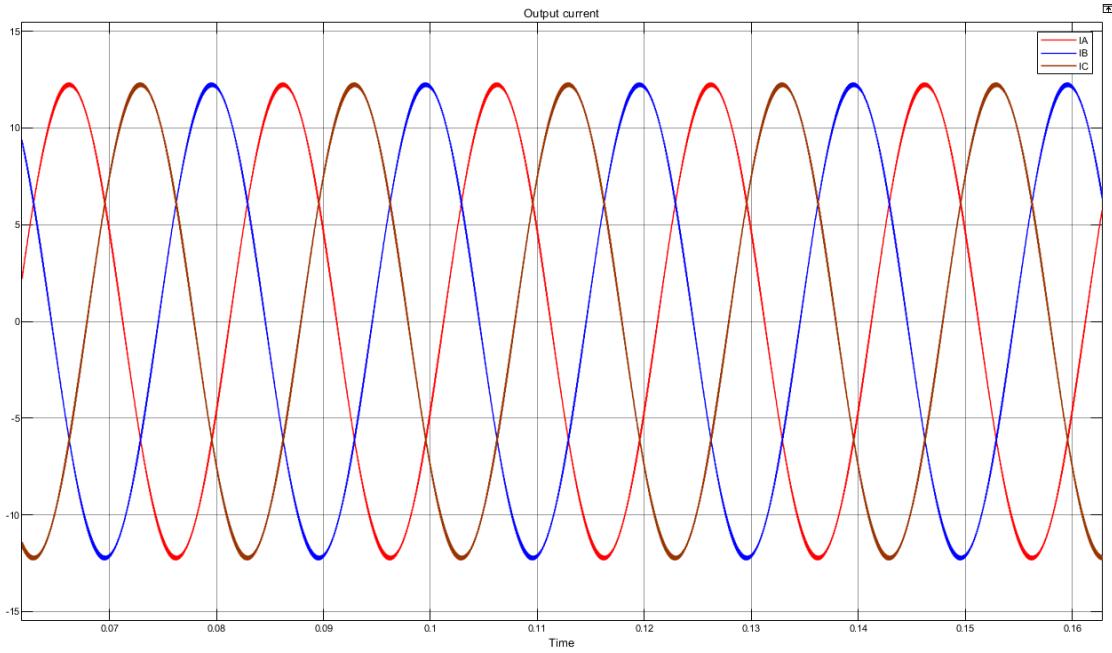


Figure 4.53: Output current after filtering.

The studying of harmonic analysis demonstrates that the application of the filter yields remarkable results. Both the voltage and current in Figure 4.52 Figure 4.53 exhibit an high level of purity, with nearly negligible distortion. The total harmonic distortion for both the voltage and current measures a mere 0.02%, while the fundamental magnitudes remain robust at 325.1V and 12.24A, respectively. With the filter in place, the output showcases a clean sinusoidal AC voltage and current waveform, with distortion levels approaching zero.

## 4.6 Experimental results

In this implementation, a single-phase inverter was controlled using carrier-based Sinusoidal Pulse Width Modulation SPWM with a microcontroller. the microcontroller's timer and counter modules were employed to generate the carrier waveform. A sawtooth waveform was selected as the carrier signal, the frequency of the carrier waveform was set to 20 kHz, ensuring a high-frequency switching pattern for the inverter. The reference was sampled using regular symmetrical sampling with frequency of 50Hz, however unipolar switching is used to achieve better performance. Resistive load is used  $R = 1k\Omega$  with  $M_f = 400$  and  $V_d = 12v$ .

Figure 4.54 illustrate the flowchart of the code for SPWM generation.

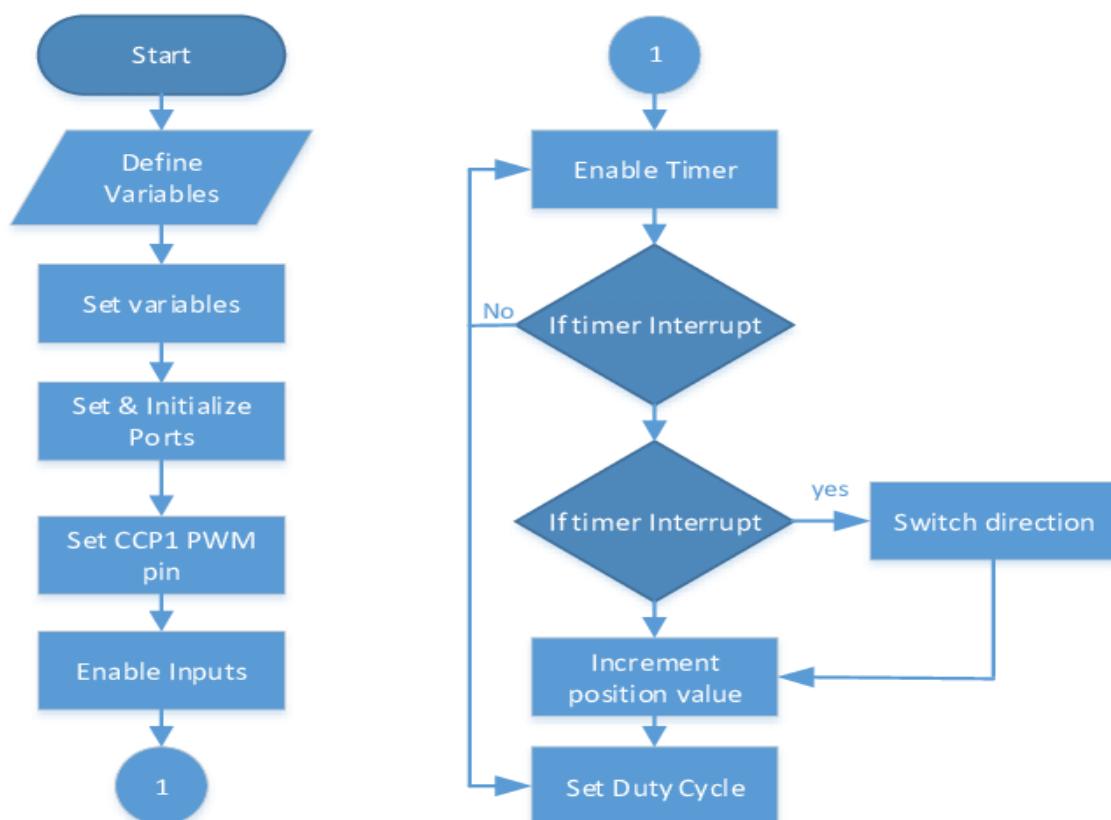


Figure 4.54: Flowchart for SWPM generation.

Figure 4.55 illustrates the output Gating signals of the microcontroller when the modulation index  $M_a$  is set to be 1 using the oscilloscope.

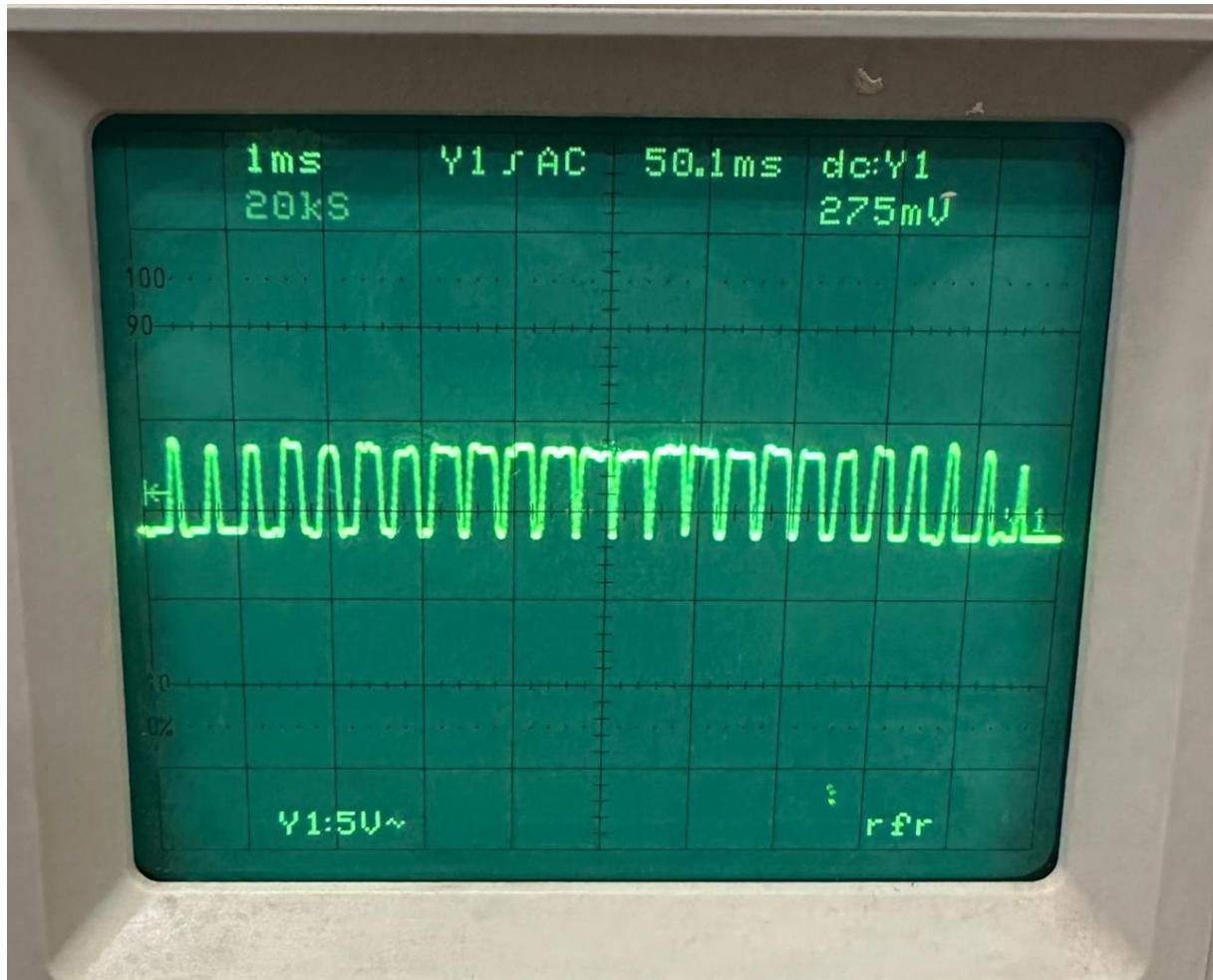


Figure 4.55: Output Gating Signals using oscilloscope  $M_a = 1$ .

Figure 4.55 illustrates the output Voltage of the VSI when the modulation index  $M_a$  is set to be 1 using the oscilloscope.

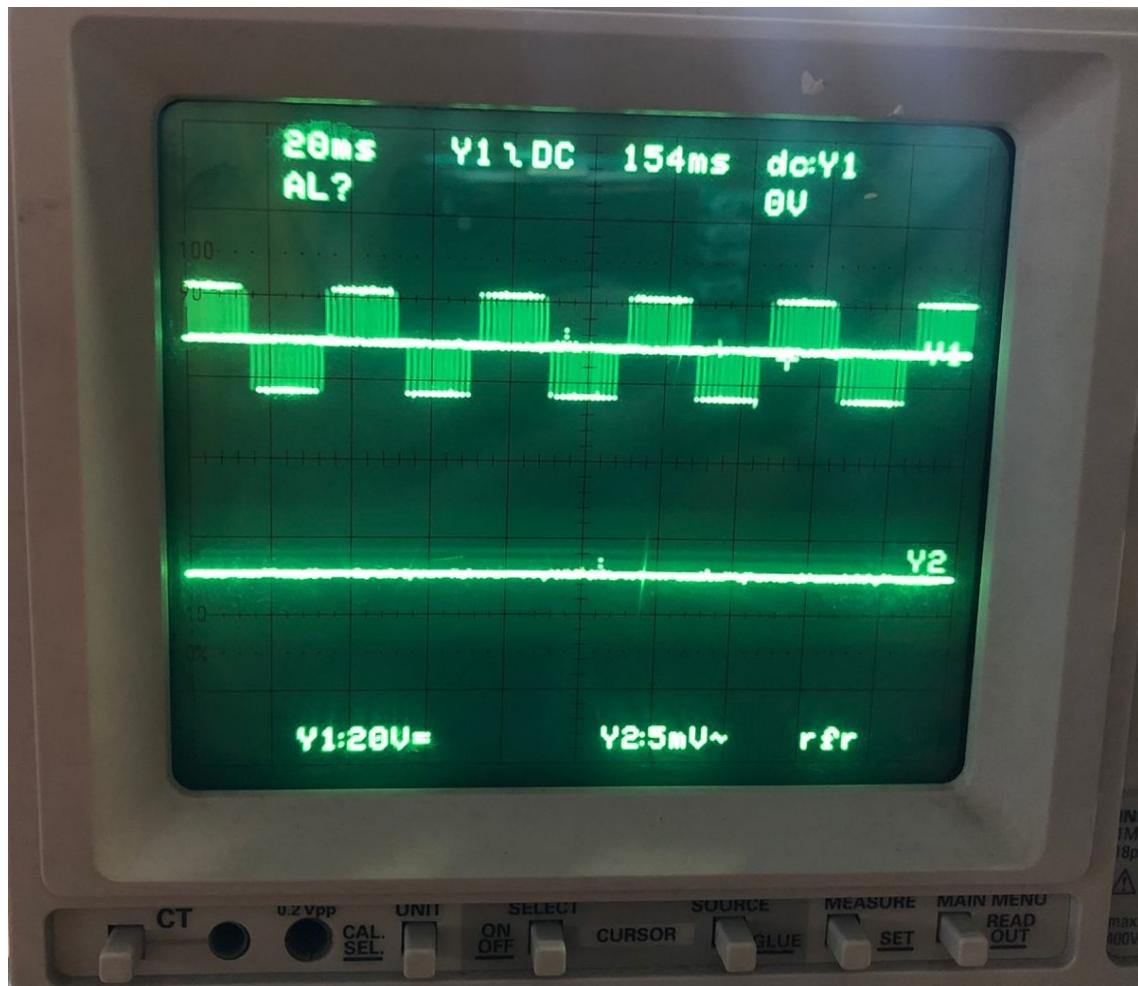


Figure 4.56: Output voltage of VSI using oscilloscope  $M_a = 1$ .

Figure 4.57 illustrates the output voltage of the voltage source inverter when the modulation index  $M_a$  is set to be 1.3 and it can be observed that SPWM enters the over modulation region, which is resulting at the output voltage.

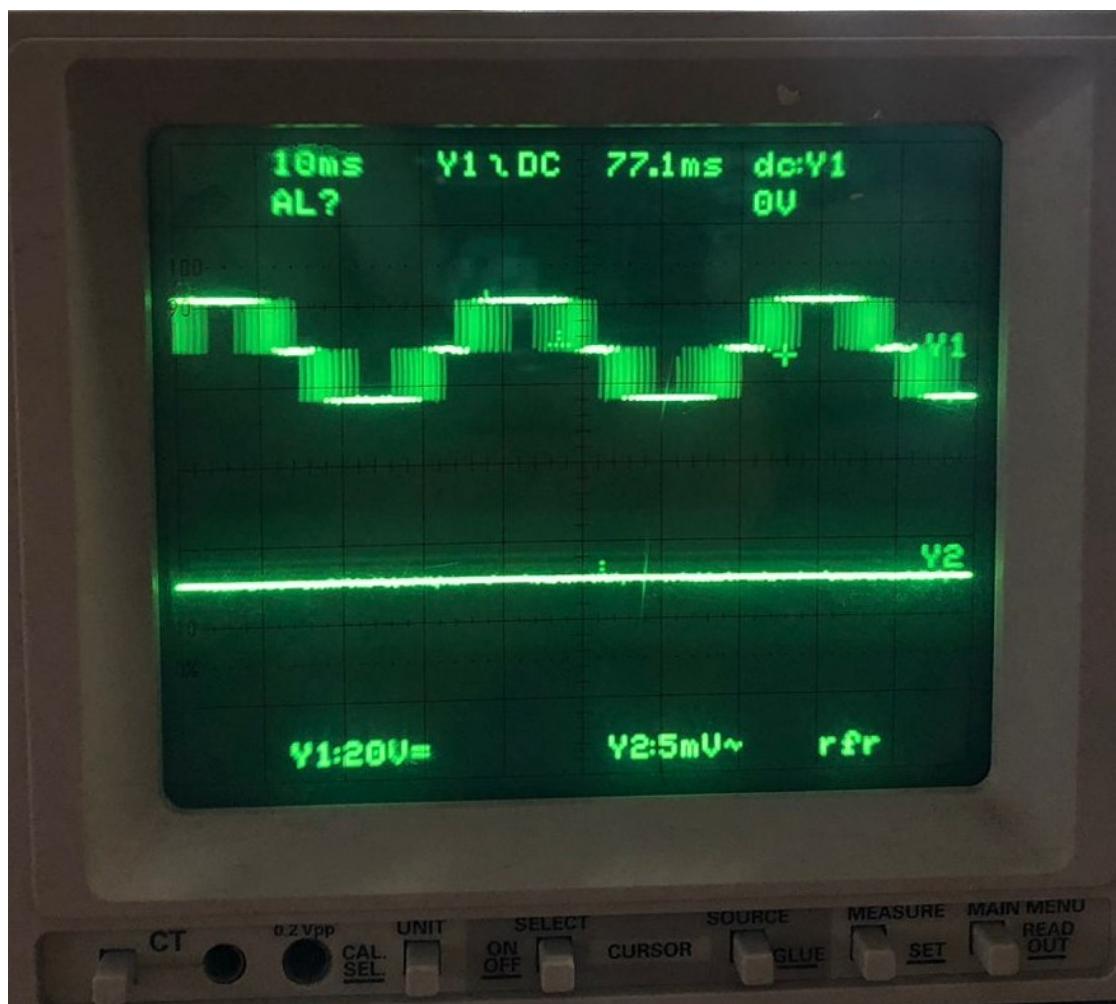


Figure 4.57: Output voltage of VSI using oscilloscope  $M_a = 1.3$ .

Figure 4.58 illustrates the output voltage of the voltage source inverter when the modulation index  $M_a$  is set to be 1 and a low pass LC filter is used, however it can be observed that the usage of the low pass filter turns output voltage to its fundamental component

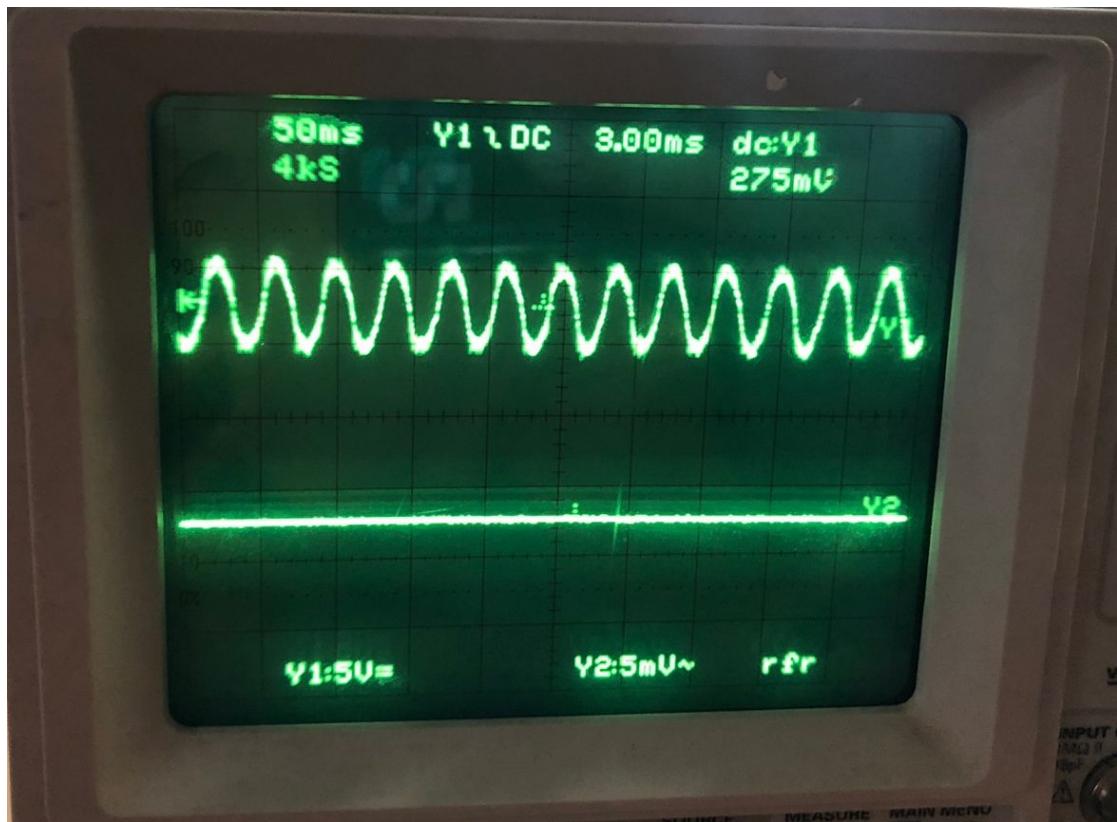


Figure 4.58: Output voltage of VSI using low pass filter on oscilloscope  $M_a = 1$ .

## 4.7 Summary

In this chapter the sinusoidal pulse width modulation technique was illustrated in details, in addition to the case studies of different approaches in its implementation including the sampling criteria ,switching techniques and the controlling parameters of the carrier based which is modulation index and frequency modulation ratio. Moreover investigating methods to enhance the output characteristics

such as using passive filter to eliminate the high order harmonics. Showing how is the simulation related to the practical aspects by implementing the modulation technique on the microcontroller.

#### 4.7.1 Case studies summary

The following tables illustrate the summary of the case studies that implemented and simulated in which the comparisons between the switching techniques either of Bipolar or Unipolar which is illustrated in 4.2, the comparisons between the sampling methods which are Natural ,Symmetrical and Asymmetrical sampling techniques in 4.2 and lastly the effect of the variation in frequency modulation ratio  $M_f$ .

Table 4.1: Comparison of Switching Techniques . Section 4.3

Switching Technique	$V_1v$	$I_1A$	Voltage THD	Current THD
Bipolar Switching	99.51	4.728	92.03%	13.18%
Unipolar Switching	98.54	4.73	46.99%	6.51%

Table 4.2: Comparison of Sampling methods. Section 4.5.1

Sampling Method	$V_1v$	$I_1A$	Voltage THD	Current THD
Natural Sampling	71.45	2.595	56.46%	10.65%
Symmetrical Sampling	66.05	2.505	61.22%	12.14%
Asymmetrical Sampling	70.68	2.58	58.03%	11.54%

Table 4.3: Effect of frequency modulation ratio. Section 4.5.2

Frequency modulation ratio $M_f$	$V_1v$	$I_1A$	Voltage THD	Current THD
30	69.72	2.2596	39.55%	6.67%
400	69.94	2.596	0.75%	0.01%

# Chapter 5

## Space Vector Pulse Width Modulation

Space vector pulse width modulation (SVPWM) is a highly popular modulation approach used in two-level converters and increasingly in the control of multilevel converters, however it is an alternative method for carrier based technique. This advanced technique requires significant computational power but offers numerous benefits. SVPWM enhances the output capability of sinusoidal PWM while ensuring that the line-to-line output voltage waveform remains undistorted. The fundamental principle behind SVPWM involves mapping space voltage vectors to different switching states, enabling the study of their impact on capacitor charge balancing. One notable advantage of SVPWM is its ability to instantaneously control switching states and select vectors to achieve optimal neutral point (NP) balancing. Furthermore, by utilizing the nearest three vectors, SVPWM enables the generation of output voltages with nearly any desired average value, resulting in superior spectral performance. SVPWM stands out as an advanced and computation-intensive PWM technique in which it can generate robust commands to ensure of tracking the reference, making it a highly favorable choice for variable frequency drive applications. Its exceptional performance characteristics have led to its widespread adoption in recent years. When the switching frequency is sufficiently high, the losses attributed to harmonics become negligible. This makes SVPWM an excellent solution in terms of inverter output voltage, harmonic losses, and the number of switching events per cycle [1].

## 5.1 Features of SVPWM

The SVPWM technique is more popular than conventional technique because of the following excellent features:

- i) it achieves the wide linear modulation range associated with PWM, third-harmonic injection automatically and all the triplen harmonics.
- ii) It has lower base band harmonics than regular PWM or other sine-based modulation methods, or otherwise optimizes harmonics [31].
- iii) 15% more output voltage than conventional modulation, i.e. better dc-link utilization.[7]
- iv) More efficient use of dc supply voltage.
- v) Advanced and computation-intensive PWM technique.
- vi) Prevent unnecessary switching hence less commutation losses.
- vii) A different approach to PWM modulation based on space vector representation of the voltages in the  $\alpha - \beta$  plane.

## 5.2 Clarke Transformation

Clarke Transformation is an approach of mapping a three phase voltage system from continuous time domain, “abc”, which are on stationary coordinate frame, to two phase system in the space vector resulting a rotating vector field with constant magnitude and with speed,  $\alpha - \beta$  frame. approach was developed by E. Clarke. Fig. 5.1 shows the Clarke transformation.

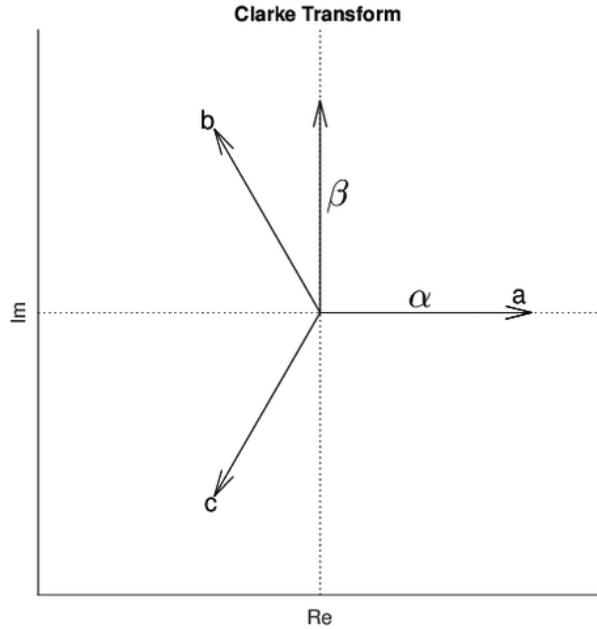


Figure 5.1: Clarke Transformation.

Clarke Transformation and its inverse transformation are given as follows:

$$\begin{aligned} V_{\alpha\beta 0} &= KV_{abc} \\ V_{abc} &= K^{-1}V_{\alpha\beta 0} \end{aligned} \tag{5.1}$$

However ,  $V_{\alpha\beta 0}$  and  $V_{abc}$  are matrices contains space vector and time domain components respectively.

where  $K$  and  $K^{-1}$  are transformation matrix and its inverse [32].

$$K = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{5.2}$$

$$K^{-1} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \tag{5.3}$$

### 5.3 Space vector concept

The space vector concept is derived from the rotating field of ac machine that is used for modulating the inverter output voltage. In this modulation technique, the three phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame or in stationary frame. From this two-phase component, the magnitude of the reference vector can be found and is used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame.

Let the three-phase sinusoidal voltage component be:

$$\begin{aligned} V_a &= V_m \sin(\omega t) \\ V_b &= V_m \sin(\omega t - \frac{2\pi}{3}) \\ V_c &= V_m \sin(\omega t + \frac{2\pi}{3}) \end{aligned} \quad (5.4)$$

When this three-phase voltage is applied to the ac machine, it produces a rotating flux in the air gap of the ac machine. This rotating flux component can be represented as single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's transformation Which it the transforming the three phase-abc time domain to its space vector equivalence  $\alpha - \beta$  frame.

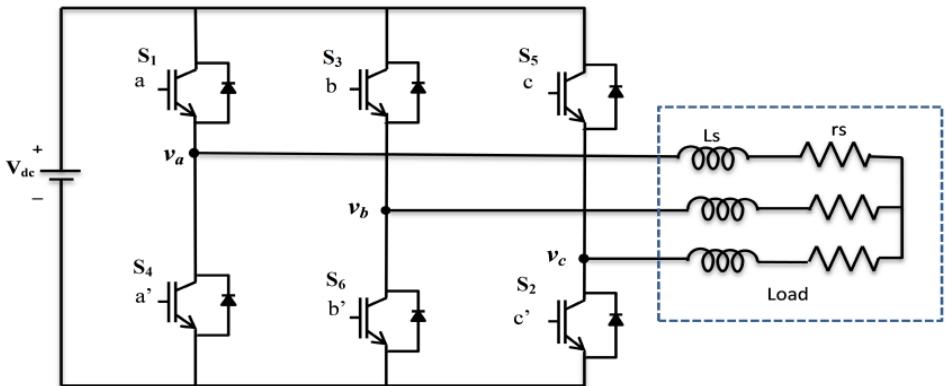


Figure 5.2: VSI With Three Phase Balanced Load, IGBTs are Pictured as Switches (S). [6]

The line-line  $[V_{ab}, V_{bc}, V_{ca}]^T$  and line to neutral  $[V_a, V_b, V_c]^T$  are given by: [32]

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (5.5)$$

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & -1 & -2 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (5.6)$$

Where  $[a, b, c]$  are the gate signals of switches  $S_1, S_3, S_5$  respectively.

Table 5.1 is shown the switching pattern and output voltage of three-phase power inverter.

Table 5.1: Possible switching states of the two-level inverter.[6]

a	b	c	$v_a$	$v_b$	$v_c$	$v_{ab}$	$v_{bc}$	$v_{ca}$
0	0	0	0	0	0	0	0	0
1	0	0	$\frac{2}{3}$	$-\frac{1}{3}$	$-\frac{1}{3}$	1	0	-1
1	1	0	$\frac{1}{3}$	$\frac{1}{3}$	$-\frac{2}{3}$	0	1	-1
0	1	0	$-\frac{1}{3}$	$\frac{2}{3}$	$-\frac{1}{3}$	-1	1	0
0	1	1	$-\frac{2}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-1	0	1
0	0	1	$-\frac{1}{3}$	$-\frac{1}{3}$	$\frac{2}{3}$	0	-1	1
1	0	1	$\frac{1}{3}$	$-\frac{2}{3}$	$\frac{1}{3}$	1	-1	0
1	1	1	0	0	0	0	0	0

## 5.4 Principle of SVPWM

The SVPWM treats the sinusoidal voltage as a constant amplitude vector rotating at a constant frequency. This PWM technique approximates the reference voltage  $V_{ref}$  by a combination of the eight switching patterns. A three-phase voltage vector is transformed into a vector in the stationary  $\alpha - \beta$  coordinate frame, which represents the spatial vector sum of the three-phase voltage. The transformation to the  $\alpha - \beta$  coordinate frame was illustrated in equation 5.1 , however when neglecting the zero component the equation becomes:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (5.7)$$

Table 5.2 shows the eight switching patterns and corresponding  $\alpha - \beta$  voltages with  $V_{ref}$ .

Table 5.2: Switching Pattern of VSI The Output Voltage  $\alpha - \beta$  .[6]

a	b	c	$v_\alpha$	$v_\beta$	$v_{ref}$
0	0	0	0	0	$v_0 = 0$
0	0	1	$-\frac{1}{3}V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$v_1 = \frac{2}{3}V_{dc}$
0	1	0	$-\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$v_2 = \frac{2}{3}V_{dc}$
0	1	1	$-\frac{2}{3}V_{dc}$	0	$v_3 = \frac{2}{3}V_{dc}$
1	0	0	$\frac{2}{3}V_{dc}$	0	$v_4 = \frac{2}{3}V_{dc}$
0	1	0	$\frac{1}{3}V_{dc}$	$\frac{1}{\sqrt{3}}V_{dc}$	$v_5 = \frac{2}{3}V_{dc}$
1	1	0	$\frac{1}{3}V_{dc}$	$-\frac{1}{\sqrt{3}}V_{dc}$	$v_6 = \frac{2}{3}V_{dc}$
1	1	1	0	0	$v_7 = 0$

As shown in Tab. 5.2, there are six non-zero vectors which will form diagonals of a hexagon, and two zero vectors positioned at the origin. The two zero vectors apply zero potential difference on the Output, however the angle between any two adjusted non-zero vectors is 60 degree.

By transferring the reference output voltages vector, which are three sinusoidal voltage with  $120^\circ$  out of phase in the continuous time domain, to the stationary coordinate via Clarke transformation,  $\alpha - \beta$  vector is obtained. Furthermore,  $V_{ref}$  vector becomes a vector rotating around the origin in the  $\alpha - \beta$  coordinate with a frequency that corresponds to the frequency of the reference output voltage. This rotating is represented by a circle inscribed in the vector hexagon which illustrated in Fig 5.3. [32].

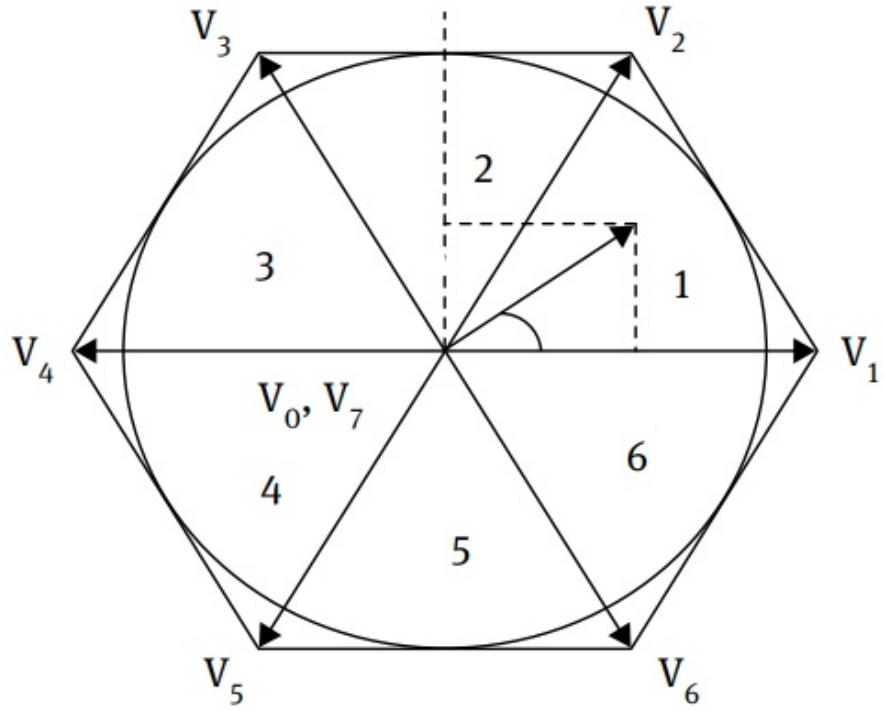


Table 5.3: Basic Switching Vectors, Sectors, and Inscribed Circle.[7]

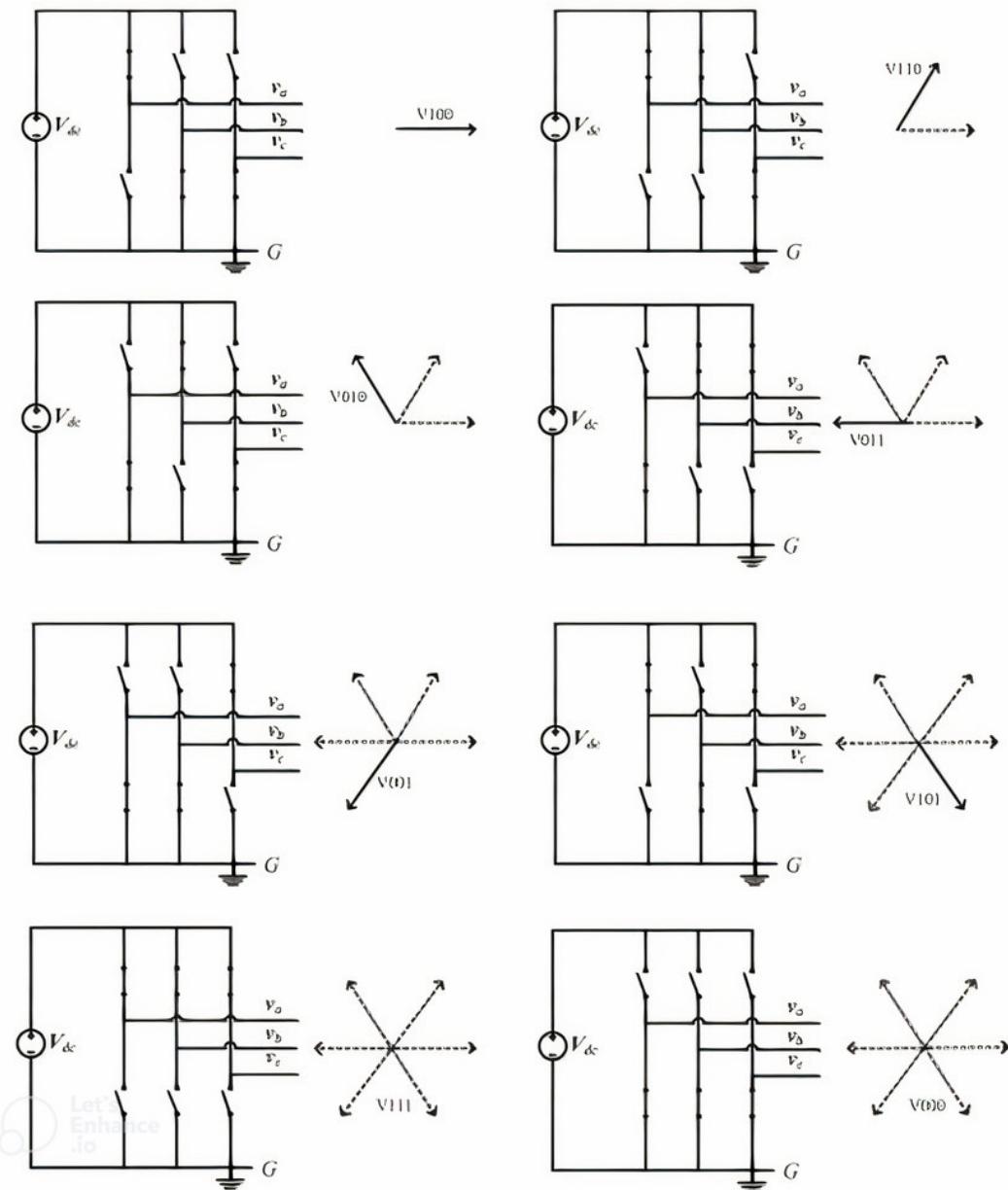


Figure 5.3: Three Phase Output Voltage and Their Projection on Plane  $\alpha - \beta$ .

## 5.5 Implementation of SVPWM

The intention of SVPWM technique is to approximate  $V_{ref}$  vector by using the combination of the eight switching vectors. One method of the approximation is to require the average output voltage of the inverter in small period,  $T$ , to be equal to the average of  $V_{ref}$  vector in the same period. Consequently, there are three steps to implement SVPWM:

1. determine  $V_\alpha$ ,  $V_\beta$ ,  $V_{ref}$ , and the vector reference angle ( $\alpha^\circ$ ), which were illustrated briefly in Fig.5.3.

From (5.1) the  $V_\alpha$ ,  $V_\beta$ ,  $V_{ref}$ , and the angle ( $\alpha^\circ$ ) can be determined as follows:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

$$|V_{ref}| = \sqrt{V_\alpha^2 + V_\beta^2} \quad (5.8)$$

$$\alpha^\circ = \tan^{-1}\left(\frac{V_\alpha}{V_\beta}\right) = \omega t = 2\pi f \quad (5.9)$$

Where  $f$  is the fundamental frequency of the desired output voltage.

2. In the second step, one of the two adjacent active voltage vectors in sector 1,  $V_1$ , is applied first during time  $T_1$ . As a result, an output voltage with the magnitude of  $V_1\left(\frac{T_1}{T_s}\right)$  in the direction of the vector  $V_1$  is generated. Next, another vector  $V_2$  is applied during time  $T_2$  to meet the magnitude and the phase of the voltage reference vector  $V_{ref}$ . Through these two steps, it is possible to generate the same output voltage as the voltage reference vector over the modulation period  $T$ . Lastly, if  $T_1 + T_2 < T_s$ , then one of the zero vectors,  $V_0$  or  $V_7$ , is applied during the remaining time  $T_0 (= T_s - (T_1 + T_2))$ . The duration time ( $T_1$ ,  $T_2$ , and  $T_0$ ) of each voltage vector for generating a given reference vector  $V_{ref}$  in sector 1 can be calculated as follows: [3]

$$\int_{T_0}^{T_s} V_{ref} dt = \int_{T_0}^{T_s} V_4 dt + \int_{T_1}^{T_1+T_2} V_6 dt + \int_{T_1+T_2}^{T_s} V_{0,7} dt \quad (5.10)$$

Assuming a constant DC-link voltage during period  $T_s$  Eq.5.10 can be rewritten as:

$$T_s V_{ref} = T_1 V_4 + T_2 V_6 \quad (5.11)$$

Since the reference vector  $V_{ref}$  is in the first sector,  $0 \leq \alpha \leq 60^\circ$ , it can be decomposed into two components as:

$$T_s |V_{ref}| = \begin{bmatrix} \cos(\alpha) \\ \sin(\alpha) \end{bmatrix} T_1 \frac{2}{3} V_{dc} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \frac{2}{3} V_{dc} \begin{bmatrix} \cos(\frac{\pi}{3}) \\ \sin(\frac{\pi}{3}) \end{bmatrix} \quad (5.12)$$

Note, in Eq.5.12, the values of  $V_4, V_6$  are substituted from Table.5.2.

Hence,

$$T_2 = T_s \frac{3}{2} \frac{|V_{ref}| \sin(\alpha)}{V_{dc} \sin(\frac{\pi}{3})} \quad (5.13)$$

$$T_2 = T_s a \frac{\sin(\alpha)}{\sin(\frac{\pi}{3})} \quad (5.14)$$

$$T_1 = T_s \frac{3}{2} \frac{|V_{ref}| \sin(\frac{\pi}{3} - \alpha)}{V_{dc} \sin(\frac{\pi}{3})} \quad (5.15)$$

$$T_1 = T_s a \frac{\sin(\frac{\pi}{3} - \alpha)}{\sin(\frac{\pi}{3})} \quad (5.16)$$

Where  $a = \frac{|V_{ref}|}{\frac{2}{3} V_{dc}}$  is defined as modulation ratio for space vector modulation.

### Switching time duration in arbitrary sector

To determine the time at sector n, where n ranges from 1 to 6, one can calculate it by substituting the angle of the reference vector within that sector into Equations (5.15) and (5.13) as:

$angle = \alpha - \frac{\pi}{3}(n - 1)$ . Hence,

$$T_1 = T_s \frac{3}{2} \frac{|V_{ref}| \sin(\frac{\pi}{3} - (\alpha - \frac{\pi}{3}(n - 1)))}{V_{dc} \sin(\frac{\pi}{3})} \quad (5.17)$$

$$= \frac{\sqrt{3} T_s |V_{ref}|}{V_{dc}} \sin\left(\frac{n}{3}\pi - \alpha\right) \quad (5.18)$$

then

$$T_1 = \frac{\sqrt{3} T_s |V_{ref}|}{V_{dc}} \left\{ \sin\left(\frac{n\pi}{3}\right) \cos(\alpha) - \cos\left(\frac{n\pi}{3}\right) \sin(\alpha) \right\} \quad (5.19)$$

$$T_2 = T_s \frac{3}{2} \frac{|V_{ref}|}{V_{dc}} \frac{\sin(\alpha - \frac{\pi}{3}(n-1))}{\sin(\frac{\pi}{3})} \quad (5.20)$$

$$\frac{\sqrt{3} T_s |V_{ref}|}{V_{dc}} \sin(\alpha + \frac{\pi}{3}(n-1)) \quad (5.21)$$

$$T_2 = \frac{\sqrt{3} T_s |V_{ref}|}{V_{dc}} \left\{ \cos((n-1)\frac{\pi}{3}) \sin(\alpha) + \cos(\alpha) \sin((n-1)\frac{\pi}{3}) \right\} \quad (5.22)$$

$$T_0 = T_s - (T_1 + T_2) \quad (5.23)$$

To analyze the attainable range of the output voltage through the utilization of the Space Vector Pulse Width Modulation technique, we need to consider a constraint. In SVPWM, it is crucial that the combined duration of the two active voltage vectors does not surpass the modulation period. Mathematically, this can be expressed as  $T_1 + T_2 \leq T_s$ . By employing Equations 5.19 and 5.22, we can determine the necessary magnitude of the voltage reference to satisfy this condition as

$$T_1 + T_2 \leq T_s \rightarrow V_{ref} \leq \frac{V_{dc}}{\sqrt{3}} \frac{1}{\sin(60 + \alpha)} \quad (5.24)$$

This equation indicates that the possible range of the voltage reference vector  $V_{ref}$  is inside the hexagon formed by joining the extremities of the six active vectors as shown in Fig. 5.4. However, for a voltage reference vector over one electrical period, the range of the voltage reference vector should be inside the inscribed circle of the hexagon to obtain the equal magnitude. Therefore the radius of the inscribed circle,  $\frac{V_{dc}}{\sqrt{3}}$ , is the maximum fundamental phase

voltage in the SVPWM technique. This value is about 15.5% larger than that of the SPWM technique and is equal to that of the THIPWM technique. The value corresponds to 90.7% of the output voltage in the six-step operation.[2]

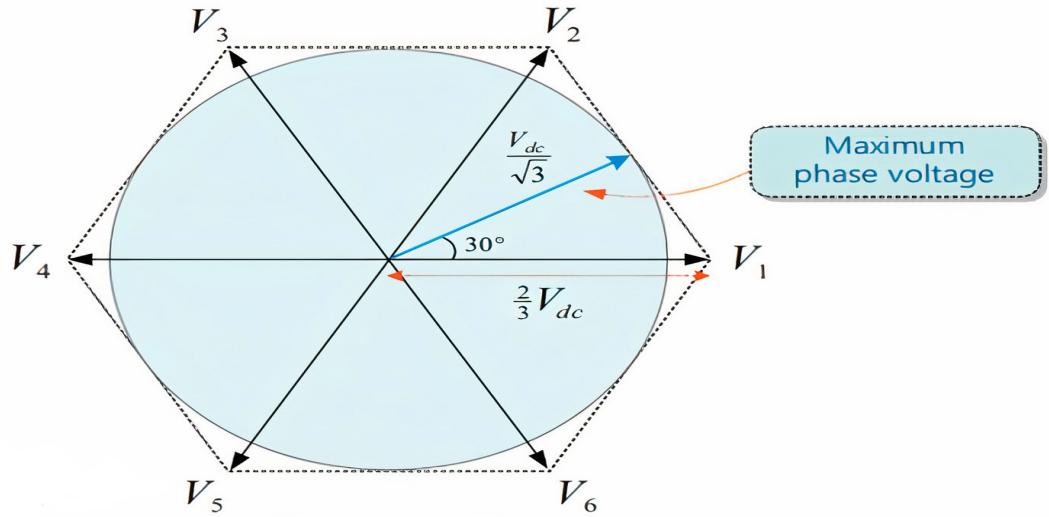


Figure 5.4: Possible range of the voltage reference vector in the SVPWM.[3]

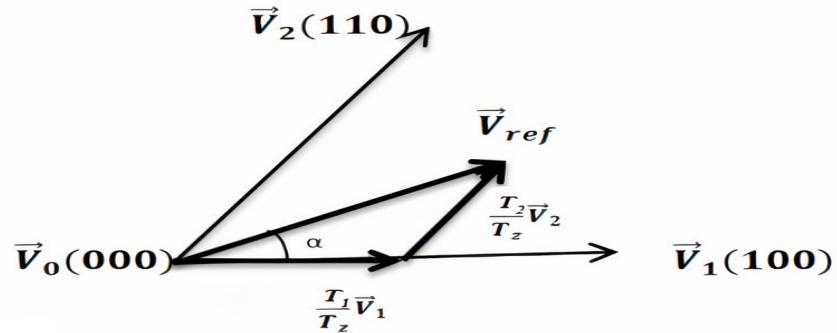


Figure 5.5: The Reference Vector as a Combination of Adjacent Vectors at Sector 1.[6]

### 3. Optimized switching sequence

The aim of SVPWM is to approximate the reference voltage vector ( $V_{ref}$ ) in a sampling period by time averaging the three voltage vectors. In the SVPWM strategy, the total zero voltage vector time is equally distributed between  $V_0$  and  $V_7$ . Further, the zero voltage vector time is equally distributed symmetrically at the start and at the end of the subcycle in a symmetrical manner. Moreover, to minimize the switching frequency and reduce the number of commutations, it is desirable that the switching sequence between the three voltage vectors involves only one commutation when there is a transfer from one state to the other. This requires the use of both zero vectors  $V_0$  and  $V_7$  in a given sector and a reversal of the switching sequence every subcycle. Thus, SVPWM uses a unique switching sequence between the active and the zero vectors depending on the sector of the application, the modulation process for voltage generation is to apply zero vector followed by active vector followed by active vector then followed by zero vector again, for example,  $V_0 - V_1 - V_2 - V_3 - V_4 - V_5 - V_6 - V_7$  in sector I, and so on. Table 5.4 depicts the switching sequence for all sectors.

Table 5.4: Switching sequence of the two-level inverter.[\[1\]](#)

<b>Sector number</b>	<b>ON sequence</b>	<b>OFF sequence</b>
1	$V_0 - V_1 - V_2 - V_7$	$V_7 - V_2 - V_1 - V_0$
2	$V_0 - V_3 - V_2 - V_7$	$V_7 - V_2 - V_3 - V_0$
3	$V_0 - V_3 - V_4 - V_7$	$V_7 - V_4 - V_3 - V_0$
4	$V_0 - V_5 - V_4 - V_7$	$V_7 - V_4 - V_5 - V_0$
5	$V_0 - V_5 - V_6 - V_7$	$V_7 - V_6 - V_5 - V_0$
6	$V_0 - V_1 - V_6 - V_7$	$V_7 - V_6 - V_1 - V_0$

Table 5.5: Switching Pattern of Control Signal by Using SVPWM in Six Different Sectors.[6]

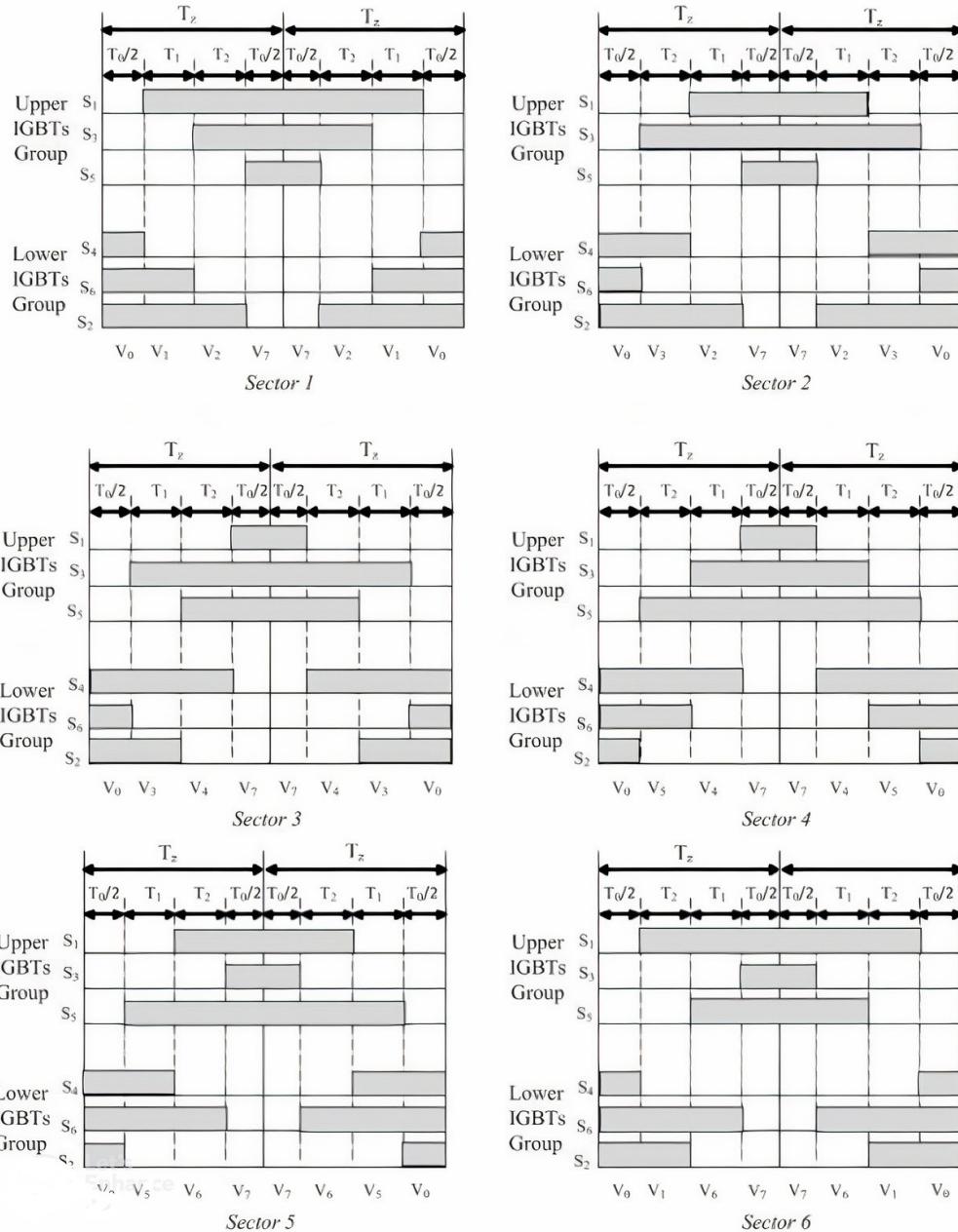


Table 5.6 illustrates the activation time for each switch of the six switches and it is assumed that the architecture of the inverter from IGBTs switches.

Table 5.6: Switching Time of Upper and Lower IGBT Groups in Six Sectors.[6]

Sector	Upper IGBT Groups ( $S_1, S_3, S_5$ )	Lower IGBT Groups ( $S_4, S_6, S_2$ )
1	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_2 + T_0/2$	$S_6 = T_1 + T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
2	$S_1 = T_1 + T_0/2$	$S_4 = T_2 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_0/2$	$S_2 = T_1 + T_2 + T_0/2$
3	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_1 + T_2 + T_0/2$	$S_6 = T_0/2$
	$S_5 = T_2 + T_0/2$	$S_2 = T_1 + T_0/2$
4	$S_1 = T_0/2$	$S_4 = T_1 + T_2 + T_0/2$
	$S_3 = T_1 + T_0/2$	$S_6 = T_2 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
5	$S_1 = T_2 + T_0/2$	$S_4 = T_1 + T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_1 + T_2 + T_0/2$	$S_2 = T_0/2$
6	$S_1 = T_1 + T_2 + T_0/2$	$S_4 = T_0/2$
	$S_3 = T_0/2$	$S_6 = T_1 + T_2 + T_0/2$
	$S_5 = T_1 + T_0/2$	$S_2 = T_2 + T_0/2$

## 5.6 Simulations of SVPWM via Simulink

The implementation pf the space vector pulse width modulation requires the three phase reference voltages to determine the voltage level of the output waveform , the space vector controller which demonstrated in Fig.5.6 to compute the activation time for each switch in the three phase voltage source inverter, and lastly the actuator to produce the desired sinusoidal output waveform which is the power three phase voltage source inverter.

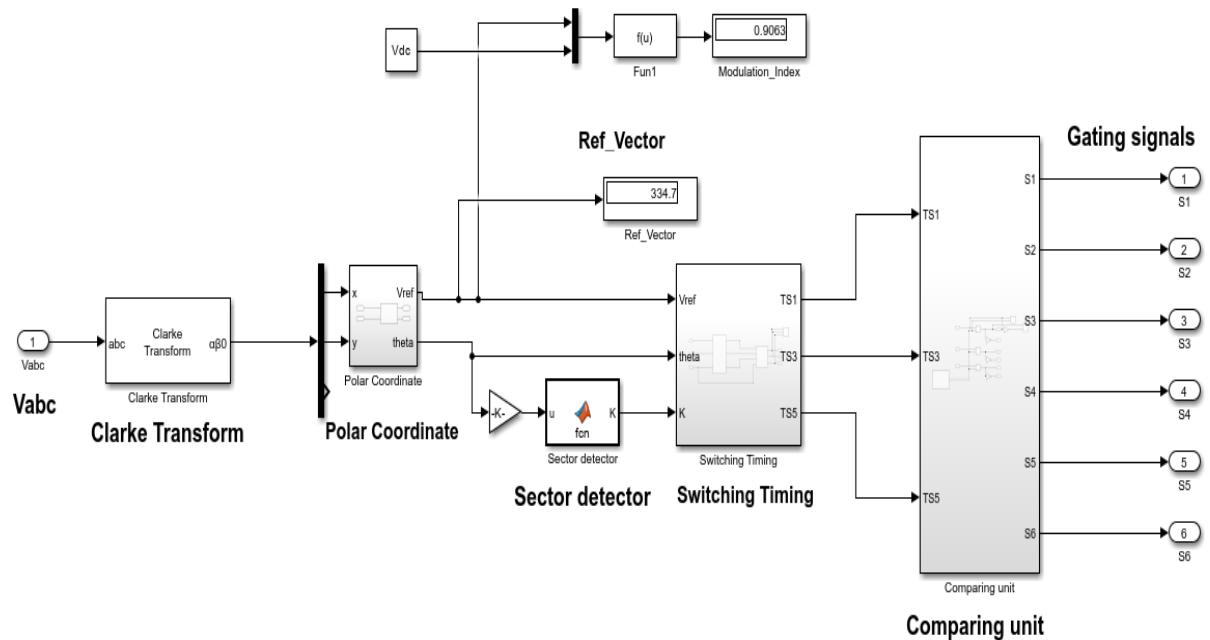


Figure 5.6: Space vector pulse width modulation controller.

After computing the reference voltage vector as a magnitude and angle in the space vector plane , the dwell times  $T_1, T_2, T_0$  are also computed for a list of parameters shown in table.5.7

Table 5.7: Parameters and their values in the SVPWM simulations.

Parameters	Value
Modulation period $T_s$	0.0002s
Dc voltage source $V_{dc}$	80v
Input voltage reference $V_R$	290v
Switching frequency $F$	2.5Khz
R	$10\Omega$
L	15mH

Figure.5.7 illustrates the sector detection in the space vector plane , however each  $60^\circ$  the sector is updated to generate the appropriate switching sequence which discussed previously in Fig.5.5.

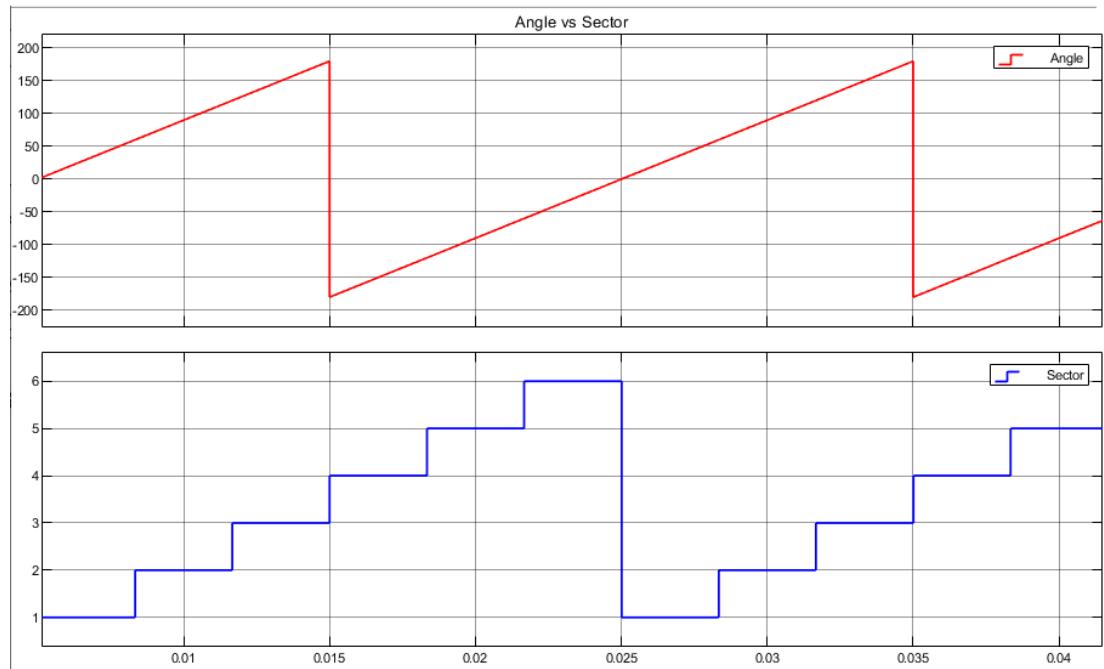


Figure 5.7: Waveforms of the reference vector angle and its corresponding sector.

Then computing the dwell times  $T_1, T_2, T_0$  for the given parameters Tab.5.7. Figure.5.8 illustrate the output waveforms for the dwell times.

As it can be seen from Fig.5.8 the timing wave from for each active vector and the zero vector could be expressed in Eqs.5.19 5.22 5.23, however after finding the sector number the corresponding timing for each active and zero vector will be defined. One can observe that the wave form of the timing of the zero vector construct unique which could be used in the generation of different forms of modulating signals.

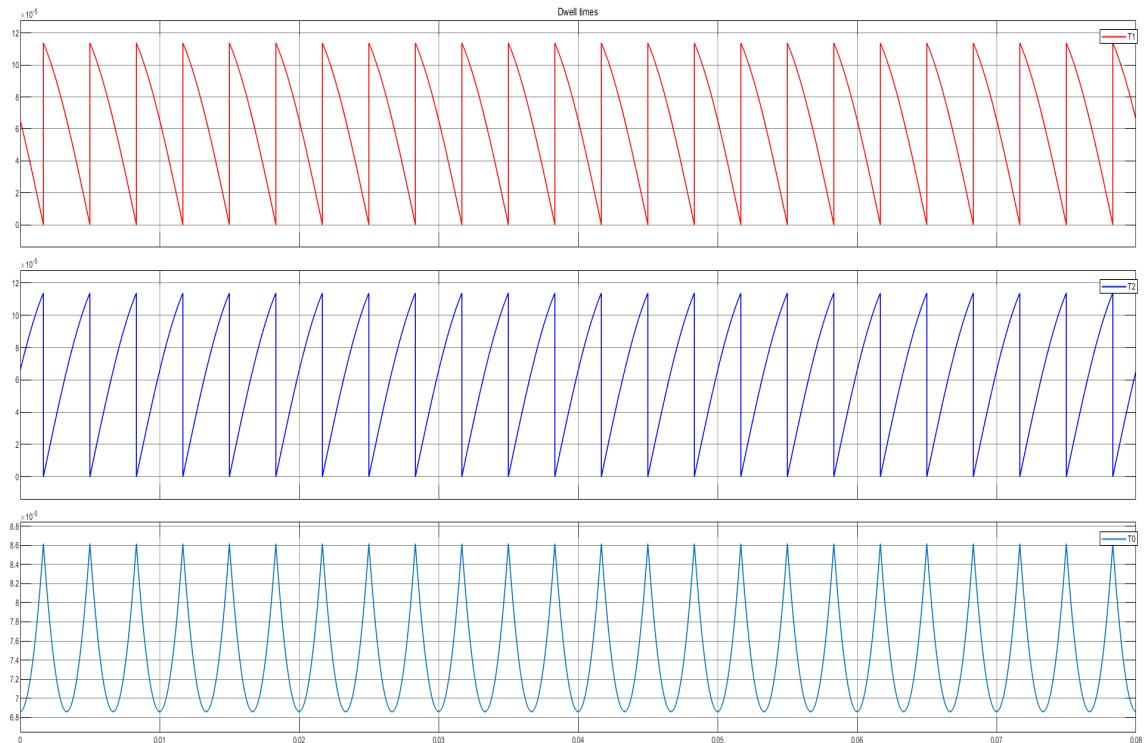


Figure 5.8: Waveforms of the Dwell times  $T_1, T_2, T_0$ .

Then apply the switching sequence depending on the sector number and the dwell times, in such a way to switch between zero vector, active vector , another active vector then followed by the zero vector, then apply the symmetry to ensure that we achieve the switching with the minimum switching losses as discussed previously[3]. Figure.5.9 illustrate the time for each upper switch in the voltage source inverter which illustrated in fig.3.12. One can notice that the waveform is not purely sinusoidal, however this due the equal distribution of the  $T_0$  among the two zero vectors  $V_0$  and  $V_0'$ ,the modulating signal named by the double humped shape, which able to offer higher range of linear region of the modulation index  $M_a$  resulting in higher utilization of the Dc voltage.

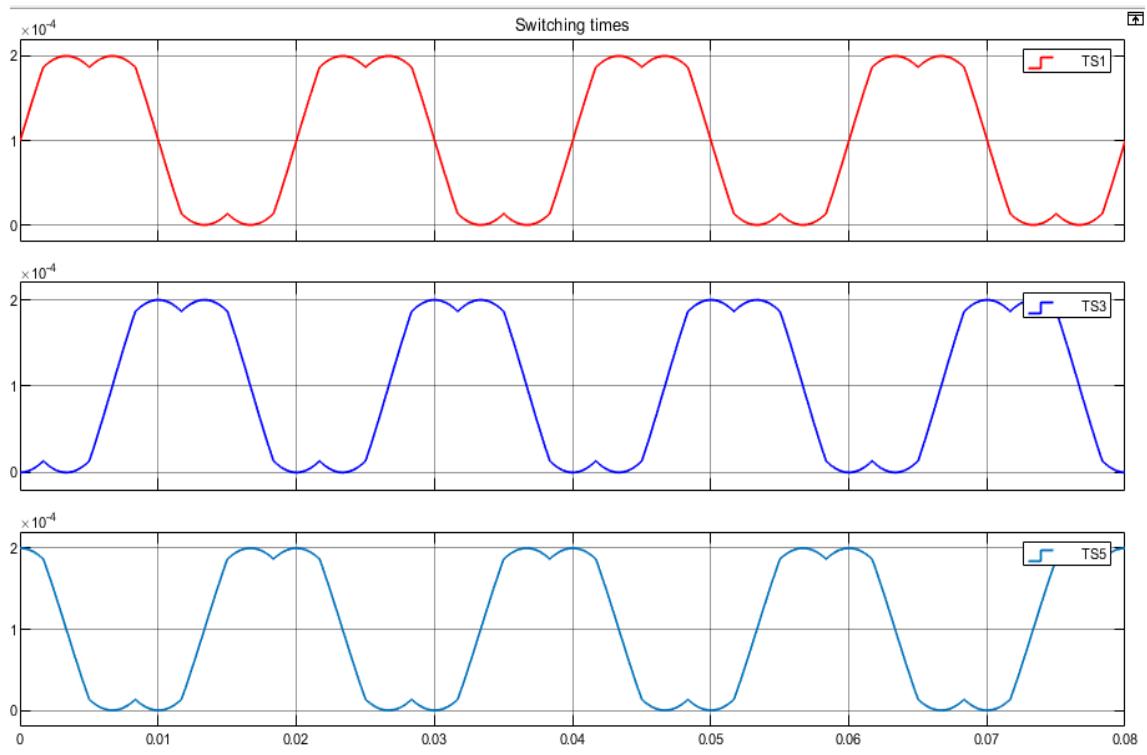


Figure 5.9: Waveforms of time for each switch  $Ts_1, Ts_3, Ts_5$ .

Figure 5.10 illustrates the corresponding gating signal for each switch after comparing each modulated signal in fig.5.9 with triangle waveform, where fig.5.11 demonstrate the gate signal for each upper switch in VSI.

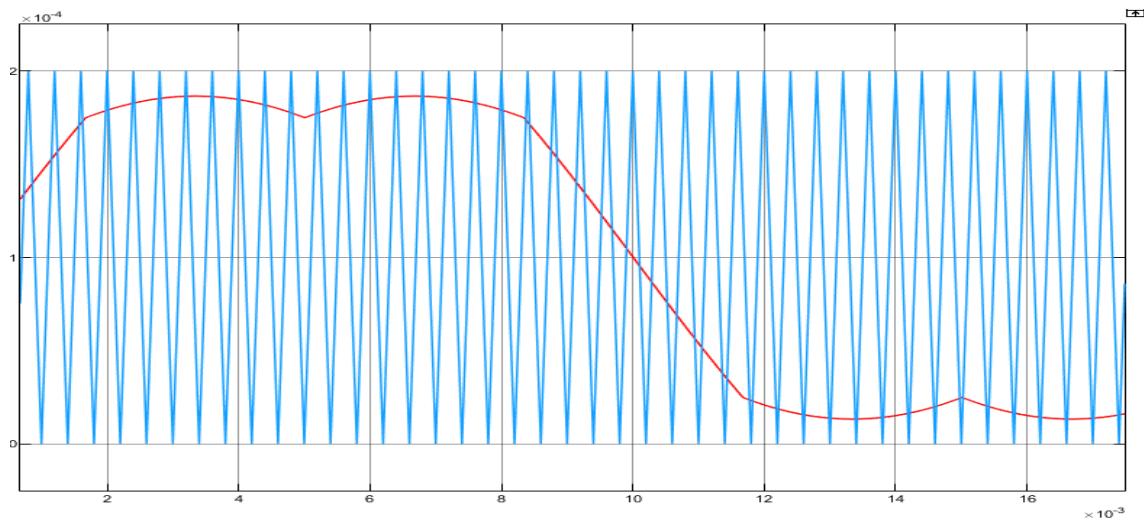


Figure 5.10: Modulated wave compared to triangle wave.

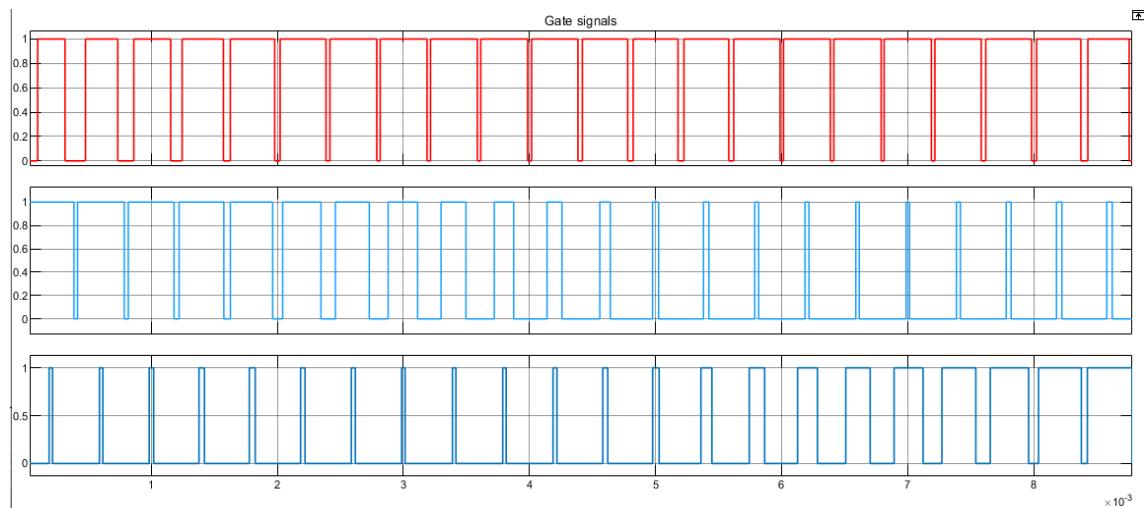


Figure 5.11: Corresponding gate signal for each upper switch  $Ts_1, Ts_3, Ts_5$ .

after feeding the gate signals which illustrated in fig.5.11 to the three phase voltage source inverter an output wave forms of line voltage and current is illustrated in fig.5.12 and fig5.13 respectively.

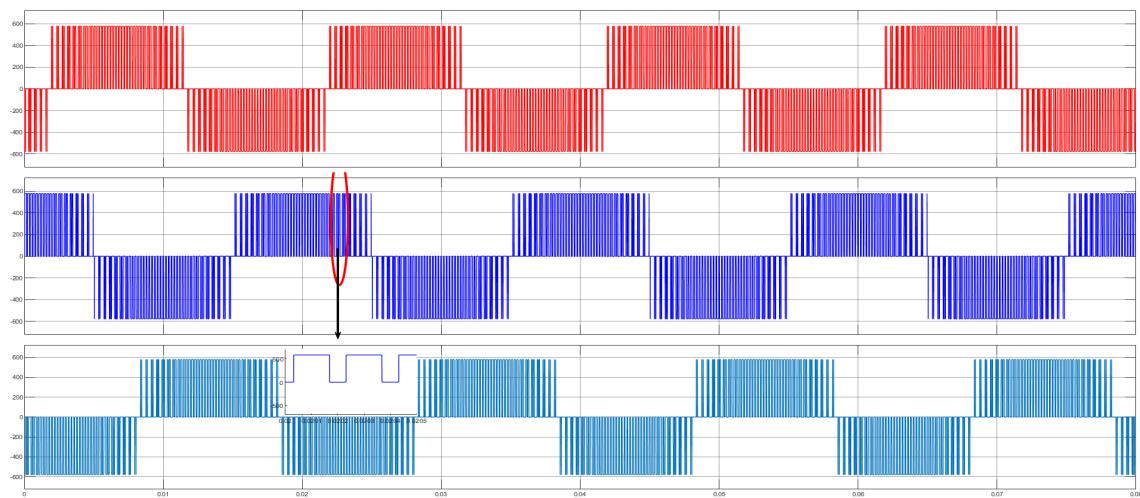


Figure 5.12: Output line voltage waveforms using SVPWM.

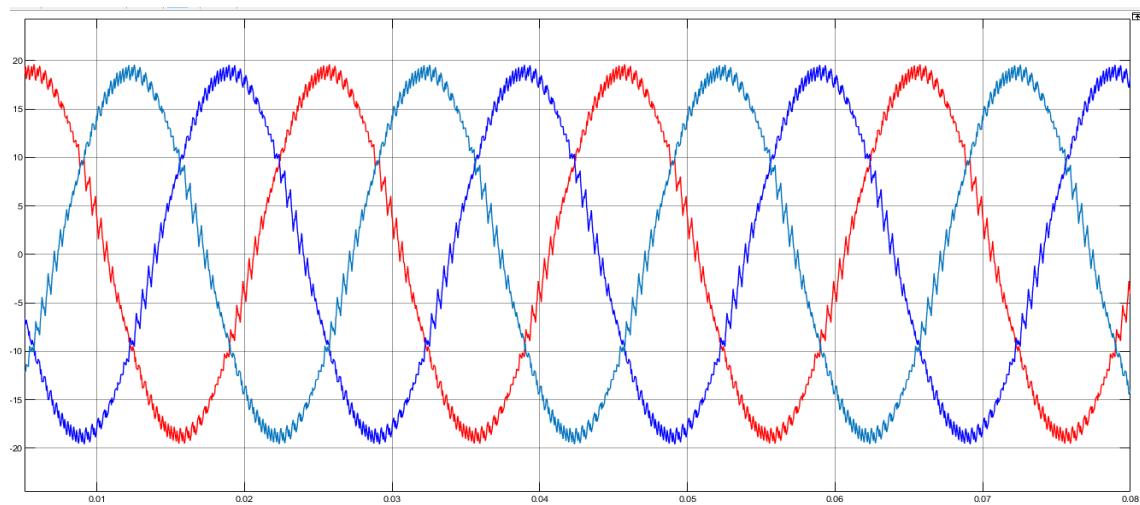


Figure 5.13: Output Current waveforms using SVPWM.

After obtaining the output wave forms, one can measure the performance of the output using the total harmonic distortion factor, however the harmonic spectrum for the output line voltage and current are illustrated in fig.(5.15)(5.15) respectively.

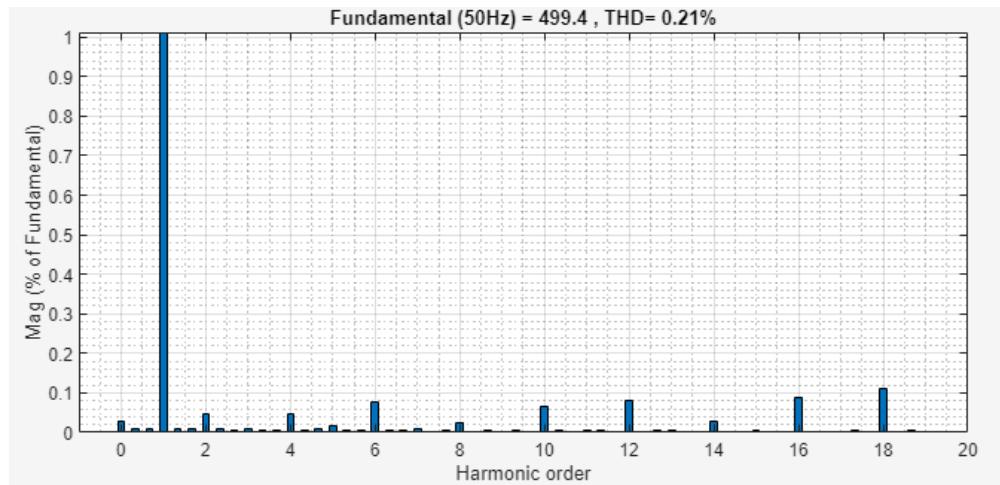


Figure 5.14: Harmonic spectrum for the output line voltage using SVPWM.

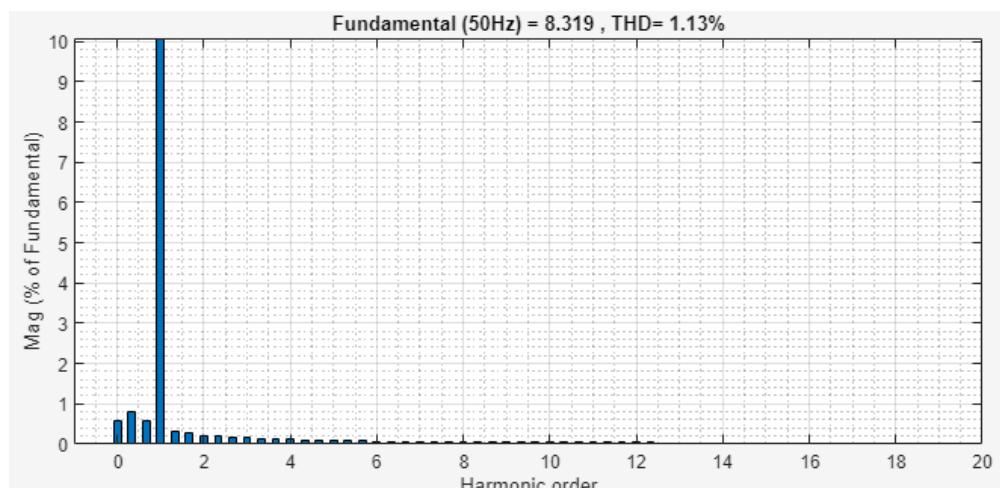


Figure 5.15: Harmonic spectrum for the output current using SVPWM.

As discussed previously in Section 4.5.4 the performance of the output waveform can be enhanced using low pass passive filter ( $L - C$ ), however following the same steps for designing filter criteria, figs.(5.16)(5.17) illustrate the output line voltage and current in the presence of low pass LC passive filter.

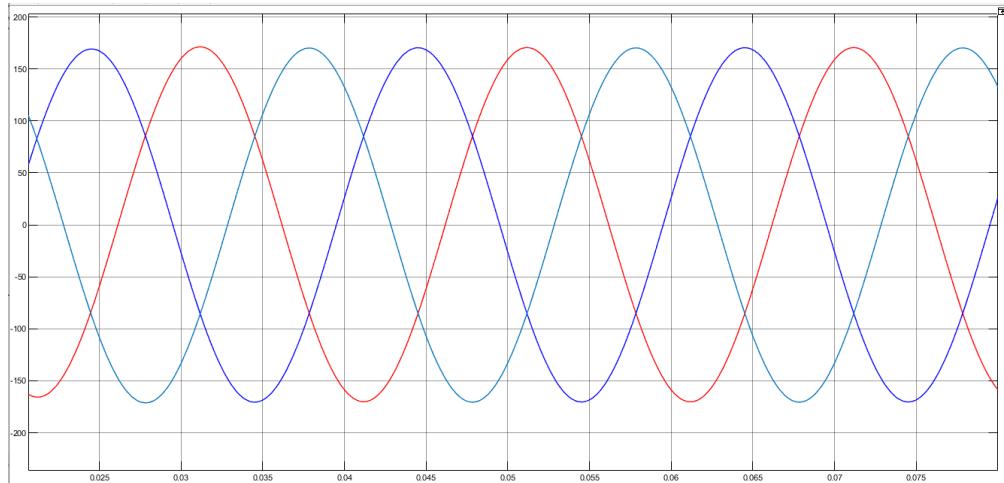


Figure 5.16: Output line voltage after filtration using SVPWM.

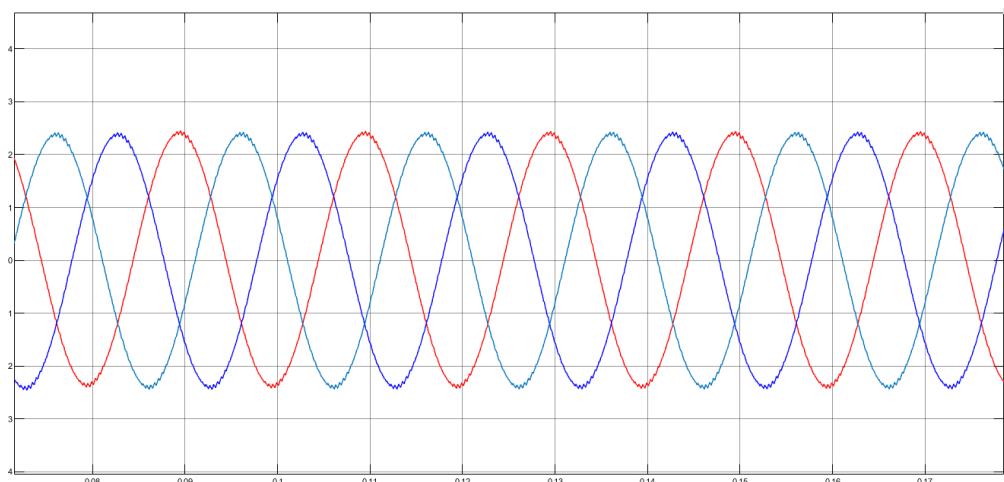


Figure 5.17: Output current after filtration using SVPWM.

## 5.7 Zero sequence component in the power systems

The zero sequence represents the component of the unbalanced phasors that is equal in magnitude and phase (Triplen harmonics). Because they are in phase, zero sequence currents flowing through an n-phase network will sum to n times the magnitude of the individual zero sequence. However their sum does not affect the rotation of the rotating reference vector but it affects its average value along the half cycle. If the inverter is connected to a load with a grounded star connection, the distortion of the phase voltages is propagated to the line-to-line voltages, as shown below in Fig.5.18 (a). As a result, the load currents are also distorted, and SVPWM is not a suitable modulation scheme in terms of harmonic content. Fortunately, it is possible to suppress the distortions in the line-to-line voltages by using different wiring of the load. If the star connection is floating – see Fig.5.18 (b) – the triplen harmonics of the zero-sequence will cancel each other out, and the line-to-line voltages remain unaffected. The situation is similar in the case of a delta-connected load – see Fig.5.18 (c) – since the phase voltages of the load are equal to the line-to-line voltages produced by the inverter. Thus, for delta or floating star connections, SVPWM allows increasing the maximum line-to-line voltage without distortion of the load currents.

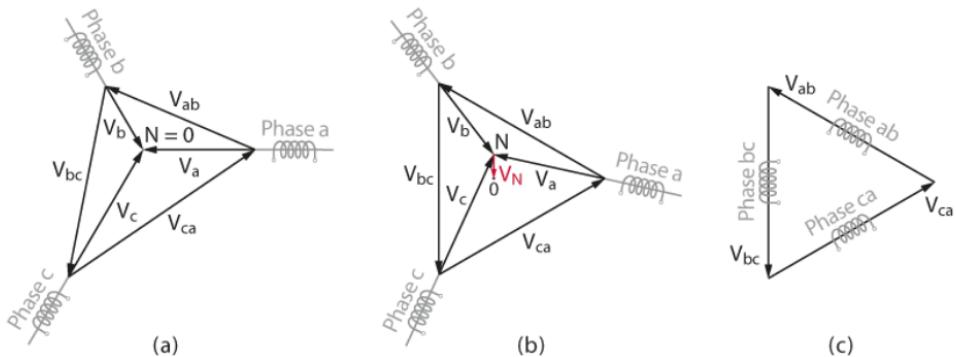


Figure 5.18: (a) Distortion of the line-to-line voltages when the star is grounded; (b) the triplen harmonics cancel each other out when the star is floating; (c) no triplen harmonics neither with a delta connection.

## 5.8 Equivalent carrier based implementation

The two main pulse width modulation (PWM) techniques are space vector pulse width modulation (SVPWM) and carrier-based pulse width modulation (CBPWM). Although SVPWM guarantees a more straightforward understanding of the modulation theory, it has been outcompeted by the implementation simplicity of CBPWM in both analog and digital systems. One of their main differences is the way they employ their degrees of freedom. In space vector modulation (SVM), it corresponds to the criterion used for sharing two ‘zero’ states. On the other hand, in the carrier-based (CB) implementation, it corresponds to the additive common-mode injection (pattern of zero sequence) into the modulating signals. It has been demonstrated that SVPWM leads to the identical CBPWM gate signals pattern, and therefore, their performances are coinciding. In the current paper, CB methodology has been employed, although the same results could have been obtained with the SVM approach as well.

### 5.8.1 Carrier-Based Common-Mode Injection

In the carrier-based implementation, it is possible to achieve multiple optimizations for a considered modulation method, some of them are higher dc-link utilization (maximization of the modulation index) and reduction of commutations in each fundamental period. This procedure consists of injecting into all sine-like modulating signals the common-mode component  $\gamma(\phi)$ , as:

$$\begin{aligned} V_{ra}^* &= V_{ra} + \gamma(\phi) \\ V_{rb}^* &= V_{rb} + \gamma(\phi) \\ V_{rc}^* &= V_{rc} + \gamma(\phi) \end{aligned} \quad (5.25)$$

Where  $V_{ra}^*, V_{rb}^*, V_{rc}^*$  are the modulating signals after the injection.

However  $V_{ra}, V_{rb}, V_{rc}$  is the reference modulated signals before the zero sequence injection.

However in SPWM, the common-mode component is kept equal to zero in the whole fundamental cycle. Despite the simplicity of the implementation, it does not provide any benefits neither in dc-bus voltage utilization nor in minimization of switching losses. Equation (5.27) shows the SPWM common-mode injection.

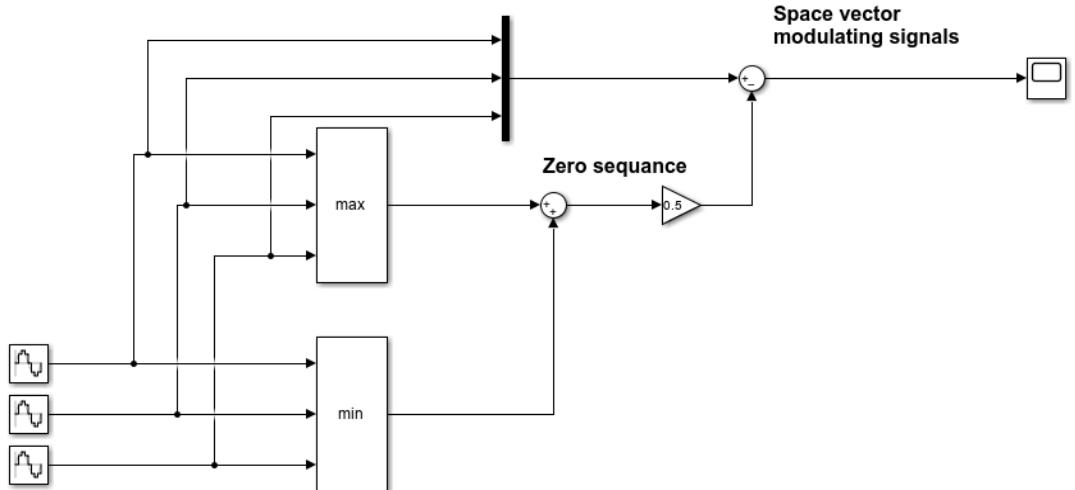
$$\gamma(\phi)|_{SPWM} = 0 \quad (5.26)$$

On the other hand, it is feasible to maximize the dc-link voltage utilization by means of the zero sequence injection. It can be considered as the carrier-based implementation of the space vector PWM (SVPWM), and it shares the same benefits of a +15% bus utilization improvement. Its mathematical definition can be derived from the following

$$\gamma(\phi)|_{SVPWM} = -\frac{1}{2}\{Max[V_{ra}, V_{rb}, V_{rc}] + Min[V_{ra}, V_{rb}, V_{rc}]\} \quad (5.27)$$

Hence,

$$\begin{aligned} V_{ra}^* &= V_{ra} + \gamma(\phi)|_{SVPWM} \\ V_{rb}^* &= V_{rb} + \gamma(\phi)|_{SVPWM} \\ V_{rc}^* &= V_{rc} + \gamma(\phi)|_{SVPWM} \end{aligned} \quad (5.28)$$



**Reference signals**

Figure 5.19: SPWM with Min/Max injection.

Figure 5.21 illustrate the three reference signals before the Min/Max injection with the Min/Max zero sequence, where fig.5.20 illustrate the output modulating signals after the injection of the specified zero sequence component.

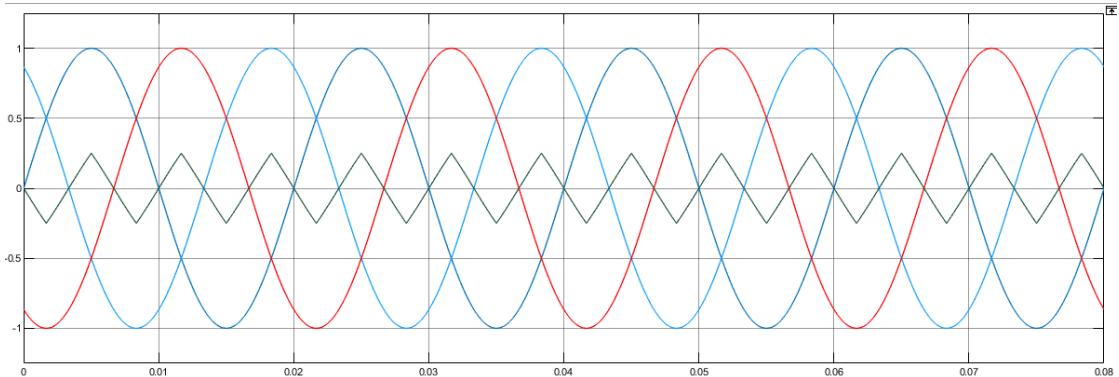


Figure 5.20: Reference signals with Min/Max zero sequence.

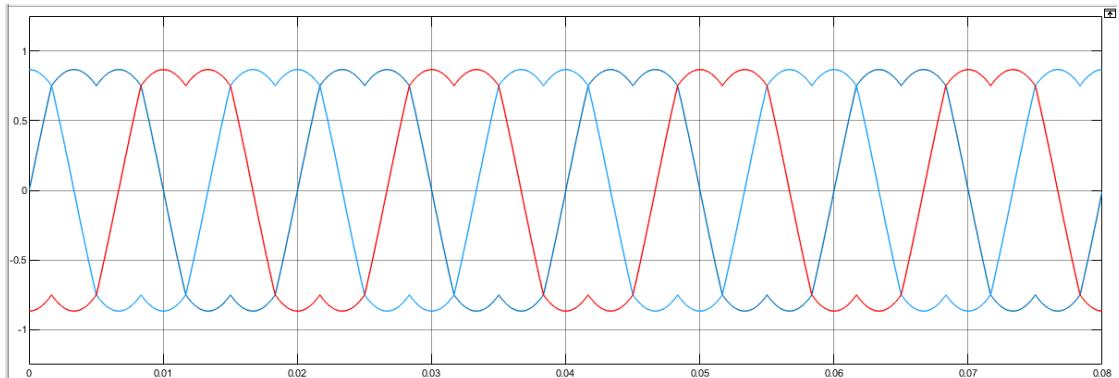


Figure 5.21: Reference signals after zero sequence for SVPWM CB injection.

It can be observed that the direct implementation of the carrier based method for the output modulating of the space vector pulse width modulation is identical to the its implementation in the space vector plane. However the CB implementation requires lower order of computations and processing with same characteristics of the output waveform, however note to mention that the space vector technique is very powerful in the analysis scheme and able to generate multiple and different modulating signals.

## 5.9 Third harmonic injection

A good way to improve the performance of the sinusoidal pulse width modulation (SPWM), in the form of the DC-bus utilization that is the third harmonic injection which has output modulated signal seems to be similar in such a way to the output modulated signal of the space vector pulse width modulation, however it extends the modulation index of the reference wave up  $1.12$   $M_a = 1.12$  [33]. The two most popular injections of this kind are THIPWM1/6 and THIPWM1/4, which respectively have a magnitude of one-sixth and one-quarter of the fundamental component. They can be analytically described as

$$\gamma(\phi)|_{THIPWM1/6} = -\frac{M_a}{6} \sin(3\omega t) \quad (5.29)$$

$$\gamma(\phi)|_{THIPWM1/4} = -\frac{M_a}{4} \sin(3\omega t) \quad (5.30)$$

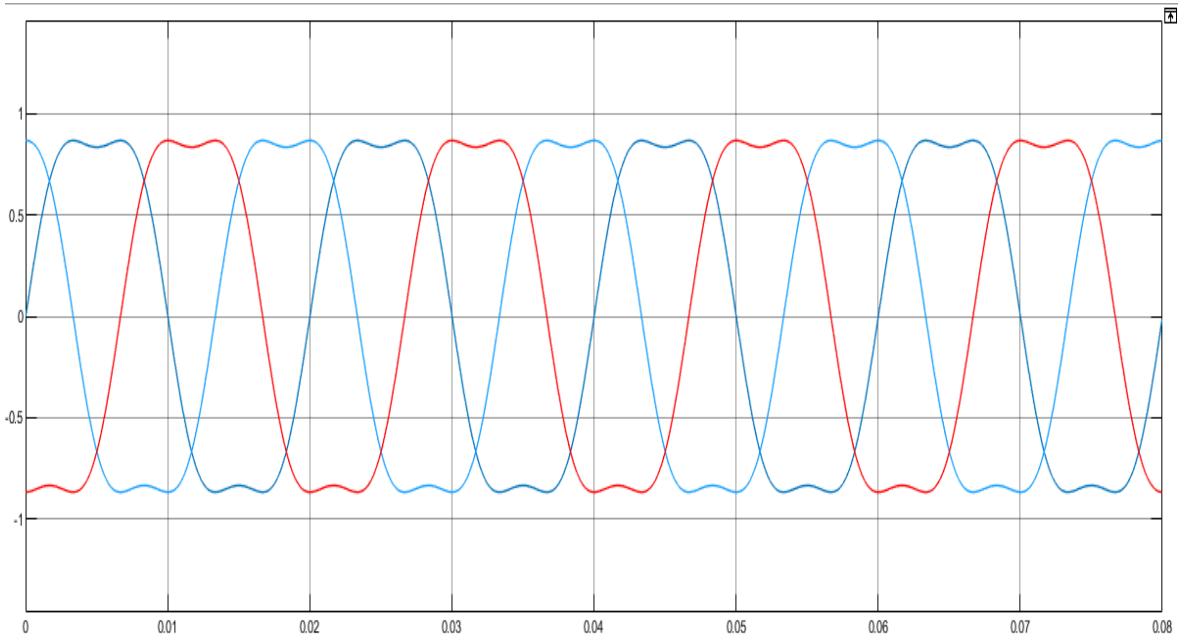


Figure 5.22: Reference signals after TWIPWM1/6 at  $Ma = 1$ .

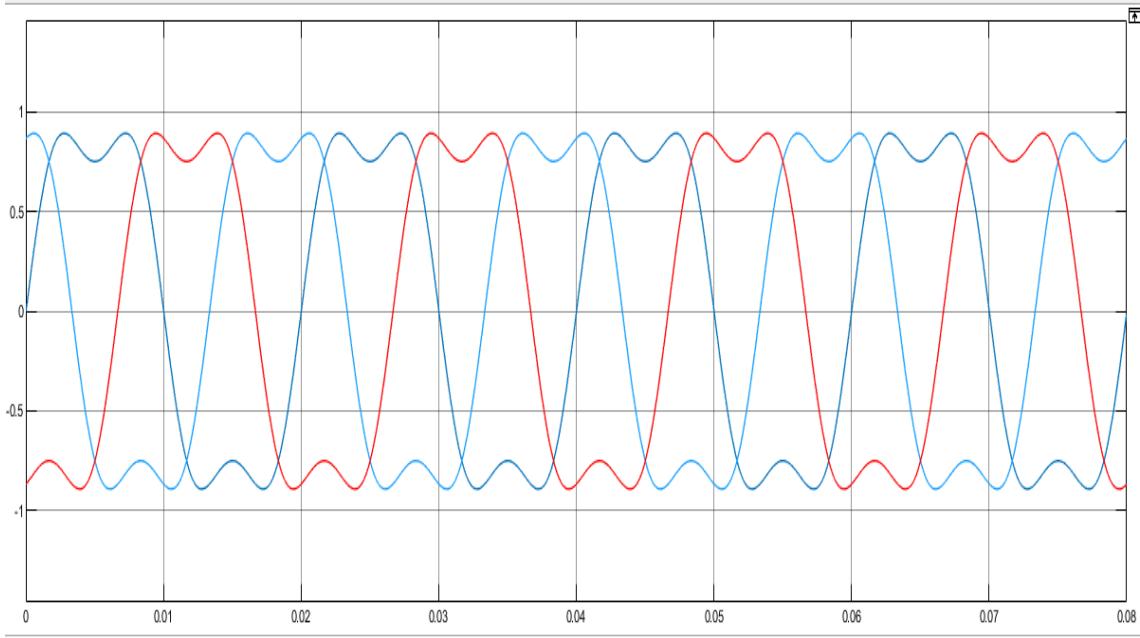


Figure 5.23: Reference signals after TWIPWM1/4 at  $Ma = 1$ .

## 5.10 Comparison between SPWM and SVPWM

Based on the information provided, we can conclude that space vector modulation offers higher direct current (DC) utilization compared to traditional sinusoidal pulse width modulation (SPWM) techniques. The increased utilization is attributed to the broader range of modulation index available in space vector modulation, which exceeds that of SPWM by approximately 15%. While the maximum modulation index for SPWM is 1, space vector modulation allows for a modulation index of up to 1.15. It's worth noting that exceeding a modulation index of 1 in SPWM can result in waveform distortion. In Figure 5.24, the effect of the modulation index on the modulated wave using SPWM is demonstrated. Before the injection of the zero sequence, the wave behaves according to the conventional SPWM modulation index limitations. However, after the injection of the zero sequence, the modulation index can surpass 1, leading to altered characteristics in the modulated wave.

When the modulation index is  $M_a = 1.15$ , the SPWM technique is in its overmodulation region. As a result, the output currents are flattened at their maximum, as shown in the figure below between  $t = 0ms$  and  $t = 60ms$ . However, the currents are undistorted if the SPWM is used in combination with a min/max injection, as observed after  $t = 120ms$ . The absence of distortion at  $M_a = 1.15$  with min/max

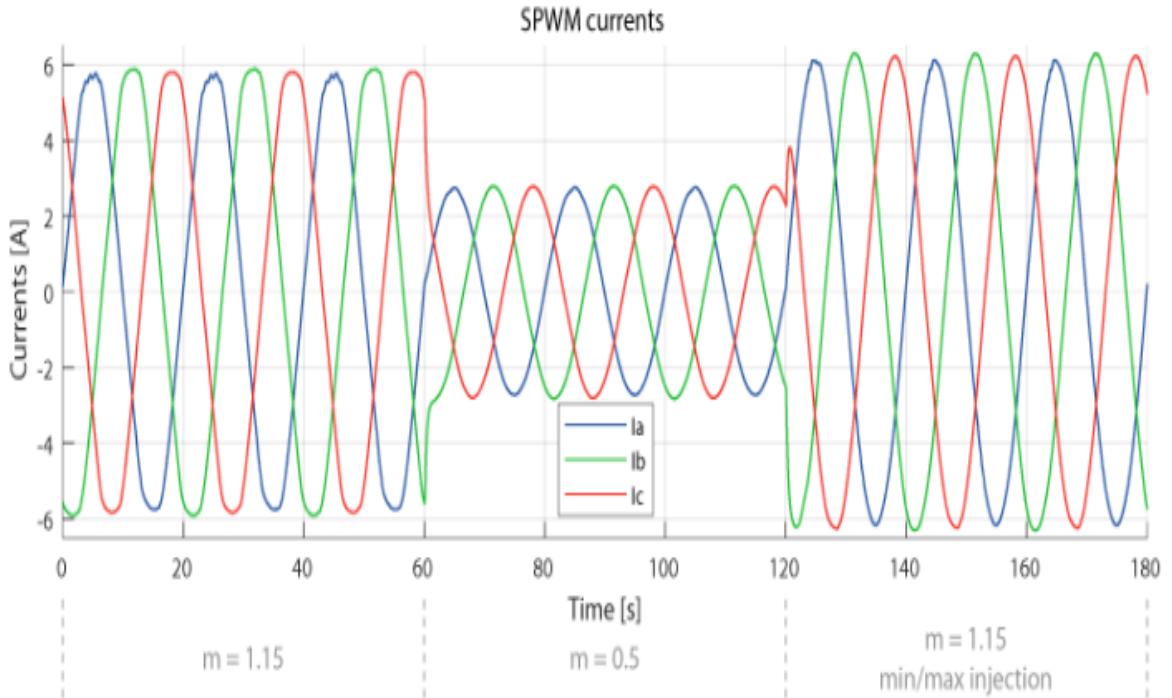


Figure 5.24: Simulation results of the SPWM modulation with or without min-/max injection.

injection – or SVPWM, since the methods are equivalent – is easier to observe by superimposing the currents obtained with SPWM and SVPWM, as shown below Fig5.25. For  $M_a = 0.5$  though, the output voltages are within the capabilities of the DC bus with both modulation techniques, and the currents are identical regardless of the zero-sequence injection.

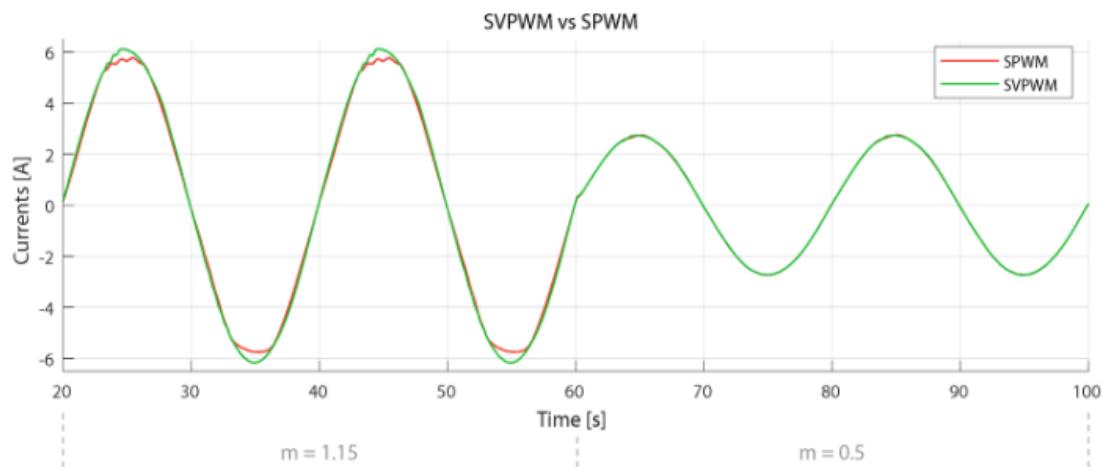


Figure 5.25: Simulation results illustrating the absence of distortion with SVPWM at  $m = 1.15$ , when compared to SPWM

The equivalence between SVPWM and SPWM with min/max injection was also verified experimentally, by using both methods with  $M_a = 1.15$  and superimposing the measured currents, as shown below Fig 5.26.

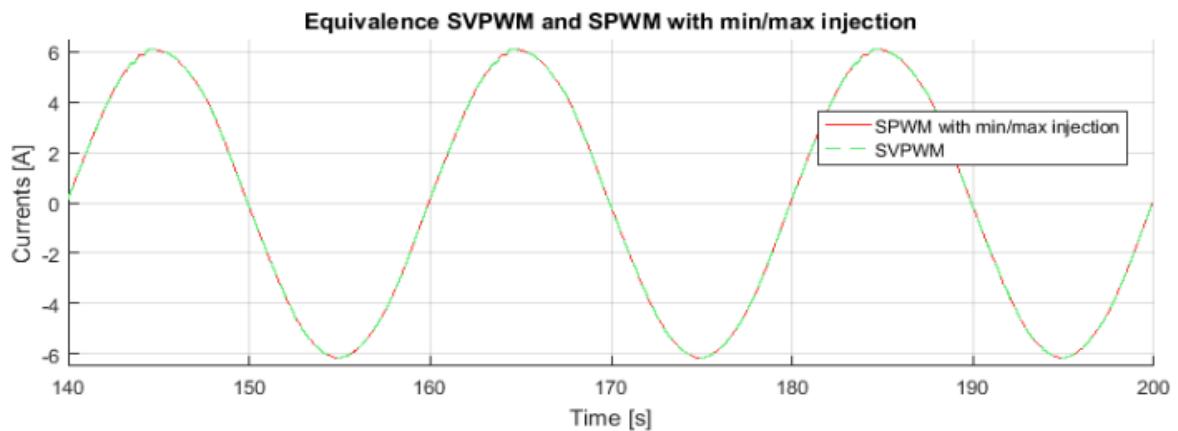


Figure 5.26: Simulation results illustrating the equivalence between SVPWM and SPWM with min/max injection.

## 5.11 Experimental Results

The Arduino Uno is a microcontroller board based on the ATmega328. It has 14 digital input/output pins (of which 6 can be used as PWM outputs), 6 analog inputs, a 16 MHz crystal oscillator, a USB connection, a power jack, an ICSP header, and a reset button as shown in Fig.5.27. Simply connect it to a computer with a USB cable or power it with a AC-to DC adapter or battery to get started. The Arduino can do standard mathematical operations. While floating point numbers are allowed if declared as floats.

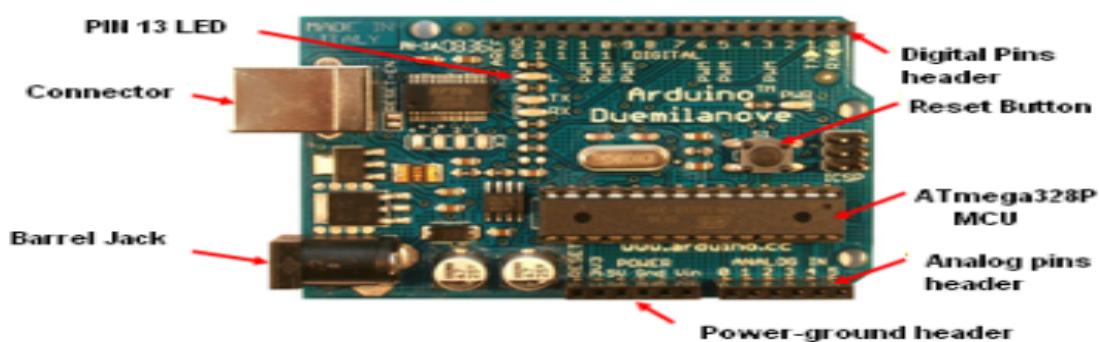


Figure 5.27: Arduino Board.

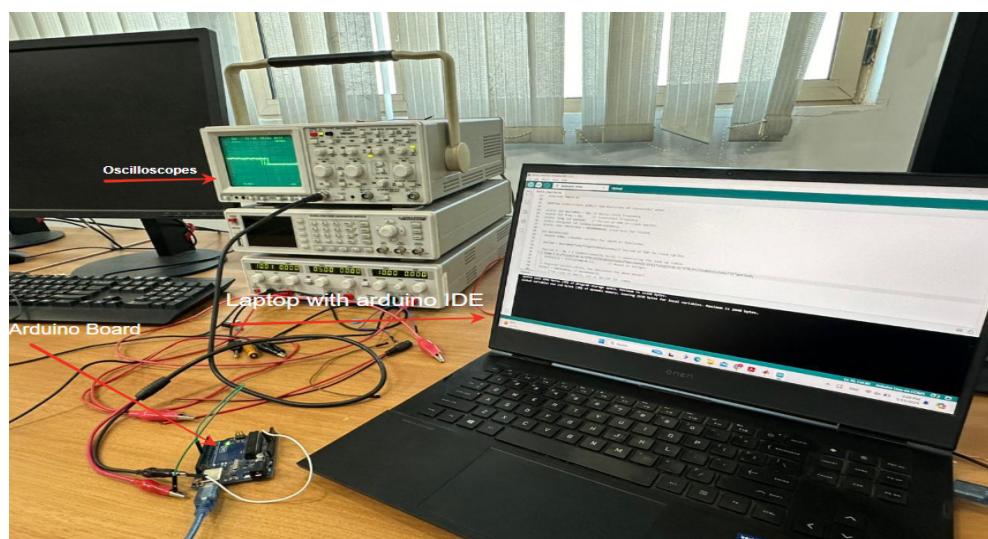


Figure 5.28: Experiment Setup.

### 5.11.1 SVPWM Code Flowchart

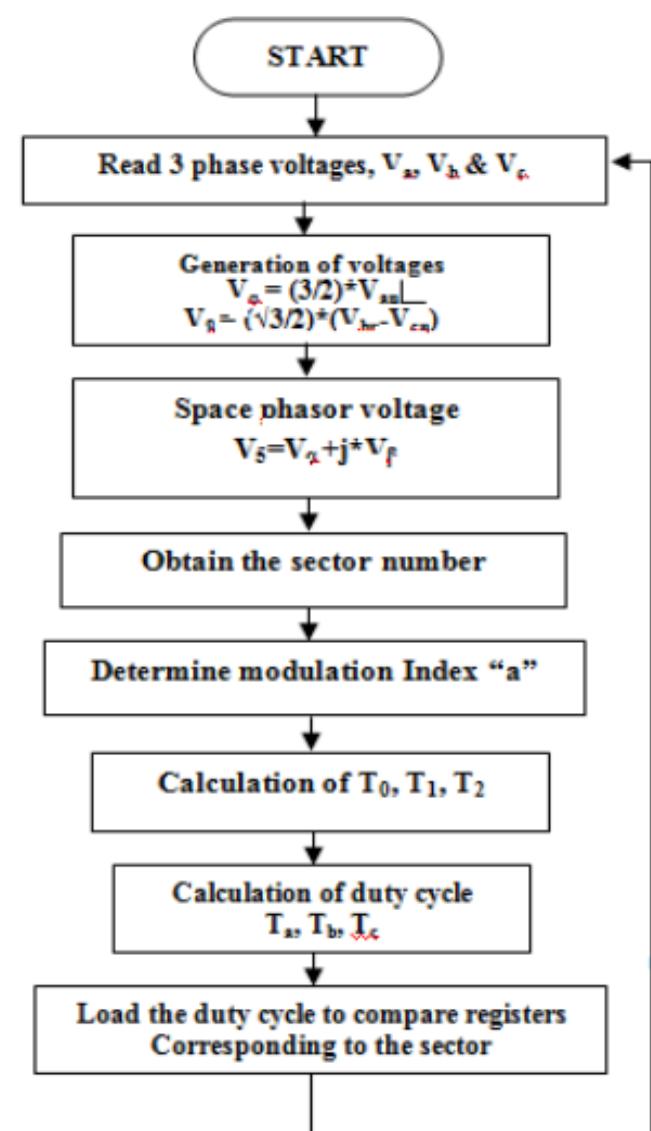


Figure 5.29: SVPWM Microcontroller Code Flowchart.

### 5.11.2 SVPWM Output Gating signals

In space vector pulse width modulation (SVPWM), the generation of output gating signals plays a crucial role in controlling the inverter switches to achieve the desired output voltage waveform. The output gating signals determine the switching states of the inverter legs, which ultimately regulate the magnitude and phase of the output voltage. However it can be observed that it is confirmed with simulations as it has the same output waveform. Which is illustrated in Fig 5.30.

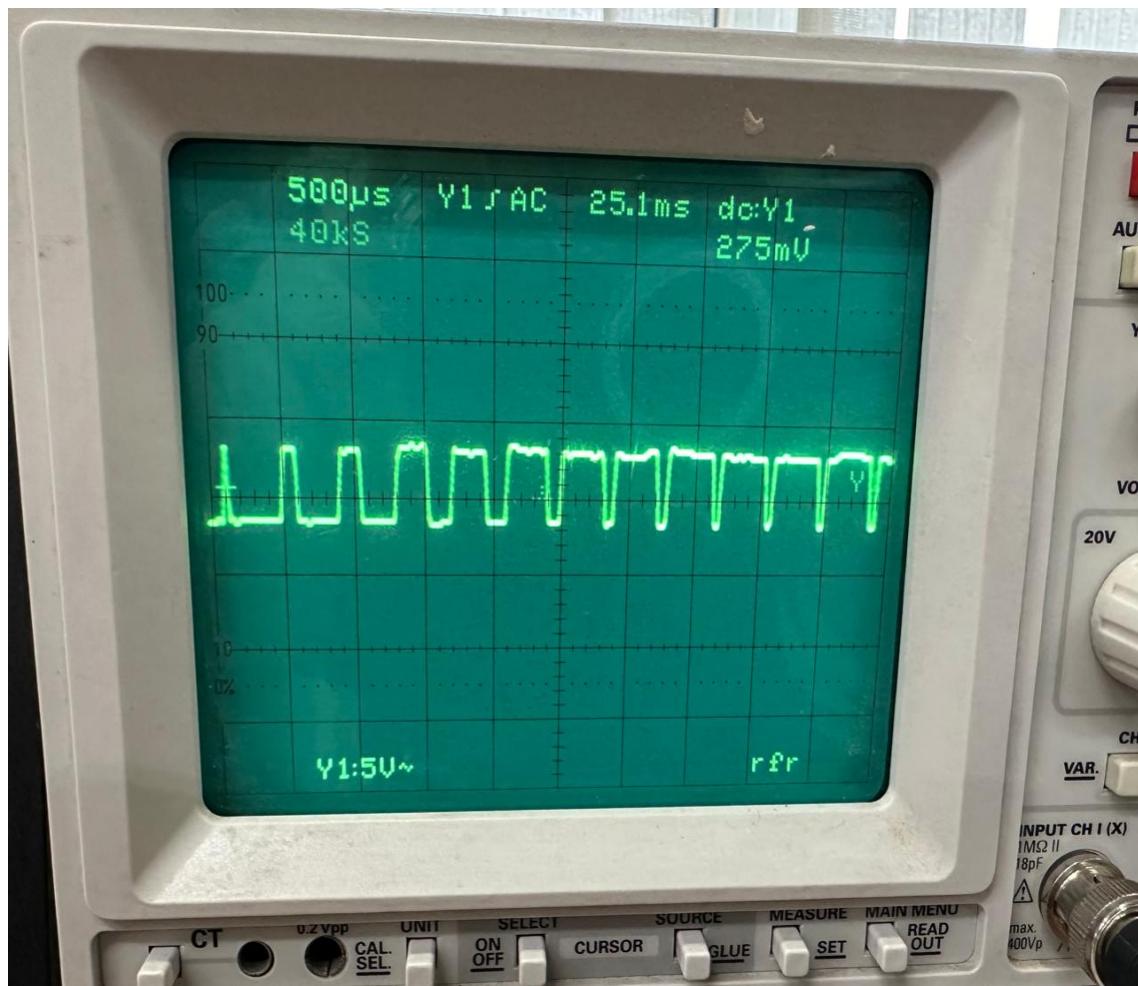


Figure 5.30: SVPWM Microcontroller Output Gating Signals.

## 5.12 Summary

This chapter delves into the intricacies of Space Vector Pulse Width Modulation (SVPWM), presenting its key features and transformation from the time domain to the space vector domain. The chapter provides a comprehensive overview of SVPWM simulations, accompanied by a brief exploration of alternative techniques such as third harmonic injection and Carrier-based implementation of SVPWM. Additionally, it discusses the fundamental principle of zero sequence and compares SVPWM with traditional Sinusoidal Pulse Width Modulation (SPWM), particularly focusing on hardware implementation aspects. Through these discussions and analyses, the chapter aims to provide insights into the practical application and comparative performance of SVPWM in various power electronics systems.

# Chapter 6

## Discontinuous Pulse Width Modulation

The previously discussed PWM techniques employ continuous modulation, where switching actions occur across all three poles of an inverter. In contrast, discontinuous modulation (or two-phase modulation) reduces the switching frequency by limiting switching actions to only two of the three poles. While the primary objective of discontinuous modulation is to decrease the switching frequency, certain characteristics, such as switching losses, harmonics, and voltage linearity, vary depending on the location of the inactive interval (referred to as the unmodulated section) within the switches. Consequently, several discontinuous PWM (DPWM) techniques exist based on the placement of the unmodulated section. Six popular DPWM techniques will be described.[3]

In a three-phase system, for symmetry purposes, the maximum scope for modulation cessation is  $120^\circ$  per fundamental cycle. Therefore, by utilizing the unmodulated section fully, the effective switching frequency can be reduced to 66.7% of the frequency employed in continuous PWM (CPWM) methods. Although the unmodulated section can be positioned at any location, it is typically placed around the peak of the phase current to effectively minimize switching losses. This choice is motivated by the fact that switching losses are proportional to the current magnitude. Consequently, the placement of unmodulated sections needs to be adjusted according to the power factor of the load.

## 6.1 Principle of Generation

### 1. Equivalent Carrier-Based Implementation with Specific Zero Sequence Injection:

This concept involves generating DPWM through an equivalent carrier-based implementation, where specific zero sequence injection is applied to the reference modulated signals. The DPWM waveform is created by utilizing carrier signals to determine the switching instants, and additional zero sequence injection is introduced to achieve the desired DPWM waveform.[8]

### 2. Implementation in the Space Vector Plane:

This concept involves implementing DPWM in the space vector plane. The DPWM waveform is generated by manipulating the space vectors in the space vector plane. By appropriately modulating the magnitude and angle of the space vectors, the desired DPWM waveform can be achieved. However due to its high order of complexity and computation , this technique is not preferred in the implementation of DPWM, however its importance in the analysis.

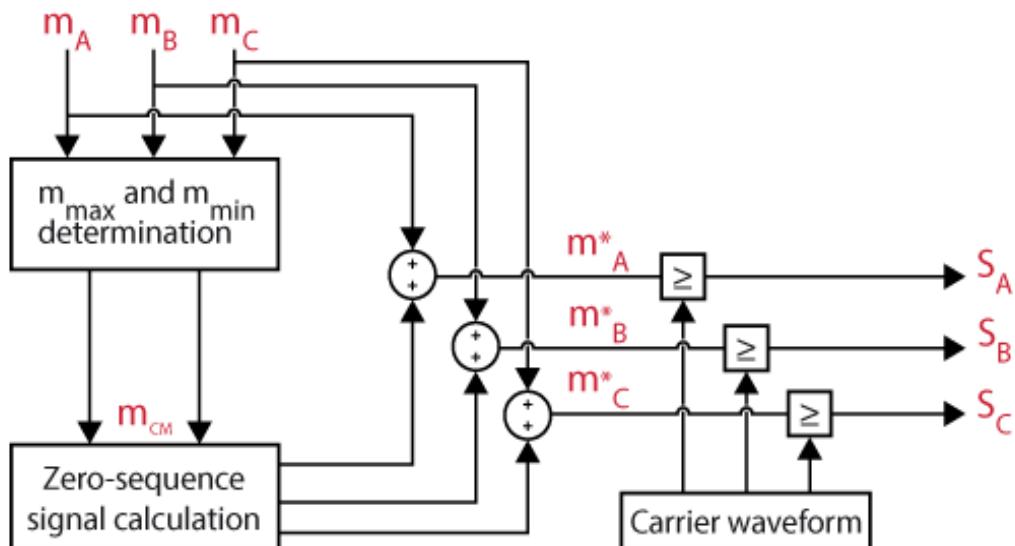


Figure 6.1: Zero-sequence injection principle for Discontinuous PWM.

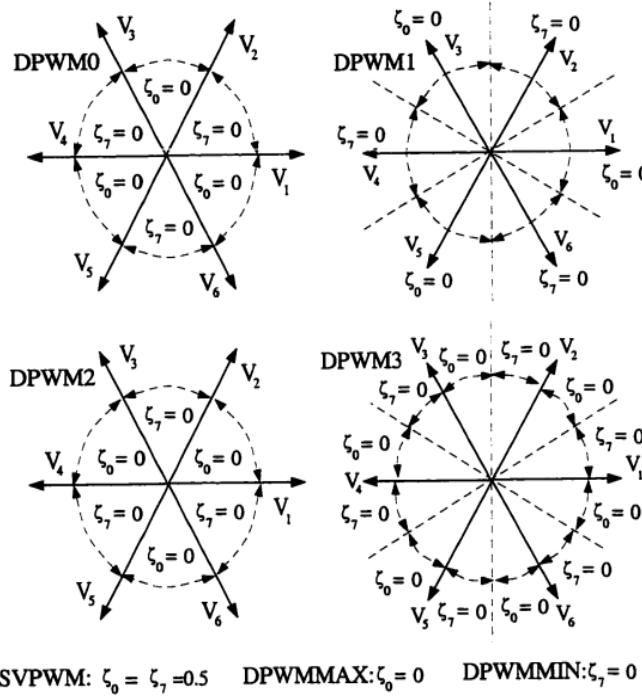


Figure 6.2: Zero state partitioning of the modern PWM methods. DPWMMIN, DPWMMAX, and SVPWM have space invariant partitioning. Where  $\zeta$  is the time for the zero state.[8]

## 6.2 DPWM Modes

Similarly to SVPWM, DPWM enlarges the voltage utilization range up to  $M_a = \frac{1}{\sqrt{3}}$ . However, the main feature of this modulation class is in switching losses reduction. All the DPWM injections here studied, decrease by one third in the number of switching operations in each fundamental cycle. This feature is achieved by the injection of a proper common-mode signal  $\gamma(\phi)$ , which can “shift” the modulating signals in a position that guarantees, at any switching instance, at least one non-commutating leg.

### 6.2.1 DPWMMAX and DPWMMIN

The two most popular DPWM injections are DPWMMAX and DPWMMIN, represented by the equations and figures labeled as DMAX and DMIN, respectively. They consistently clamp one of the modulating signals to the maximum (0.5) or minimum (-0.5) value, respectively. The common-mode injection can be obtained through:

$$\gamma(t)|_{\text{DMAX}} = \frac{1}{2} - \max[V_{ra}(\theta), V_{rb}(\theta), V_{rc}(\theta)] \quad (5.31)$$

$$\gamma(t)|_{\text{DMIN}} = -\frac{1}{2} - \min[V_{ra}(\theta), V_{rb}(\theta), V_{rc}(\theta)] \quad (5.32)$$

Assuming a balanced system (with a unique modulation index for all phases), Equations (5.31) and (5.32) can be explicitly rewritten as:

$$\gamma(\phi)|_{\text{DMAX}} = \frac{1}{2} - \begin{cases} M_a \cos\left(\theta + \frac{2\pi}{3}\right), & -\pi \leq \theta \leq -\frac{\pi}{3} \\ M_a \cos(\theta) - \frac{\pi}{3}, & -\frac{\pi}{3} \leq \theta \leq \frac{\pi}{3} \\ M_a \cos\left(\theta - \frac{2\pi}{3}\right), & \frac{\pi}{3} \leq \theta \leq \pi \end{cases} \quad (5.33)$$

$$\gamma(\phi)|_{\text{DMIN}} = -\frac{1}{2} - \begin{cases} M_a \cos\left(\theta + \frac{2\pi}{3}\right), & 0 \leq \theta \leq \frac{2\pi}{3} \\ M_a \cos(\theta), & \frac{2\pi}{3} \leq \theta \leq \frac{4\pi}{3} \\ M_a \cos\left(\theta - \frac{2\pi}{3}\right), & \frac{4\pi}{3} \leq \theta \leq 2\pi \end{cases} \quad (5.34)$$

Both DPWMMAX and DPWMMIN are depicted in Figures 6.3, 6.4. It is visible that, for one-third of the fundamental period, modulating signals  $V_{rn}^*$  do not intersect the carrier Waveform and therefore do not cause commutations.

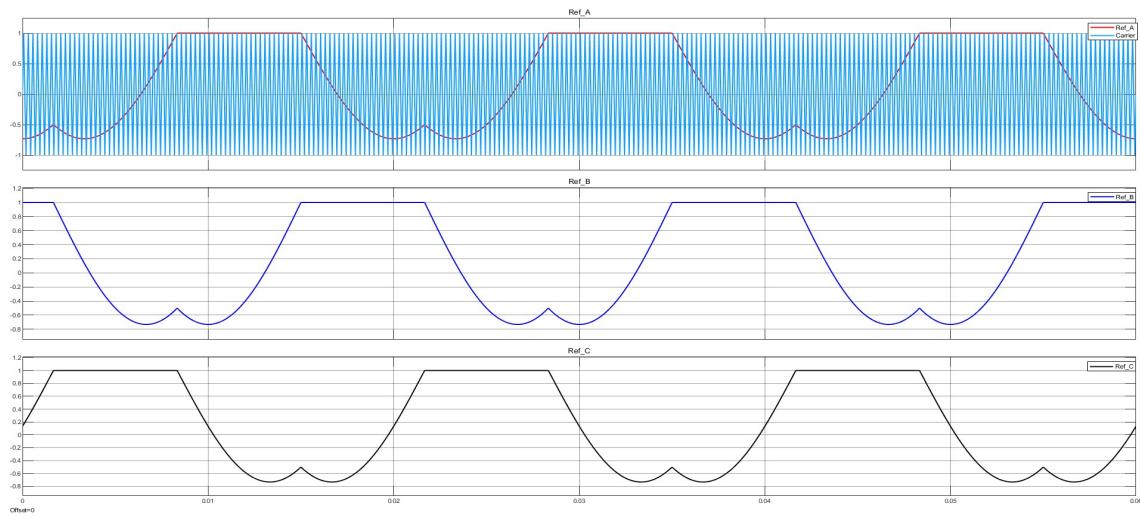


Figure 6.3: Three phase modulated references using DPWMMAX.

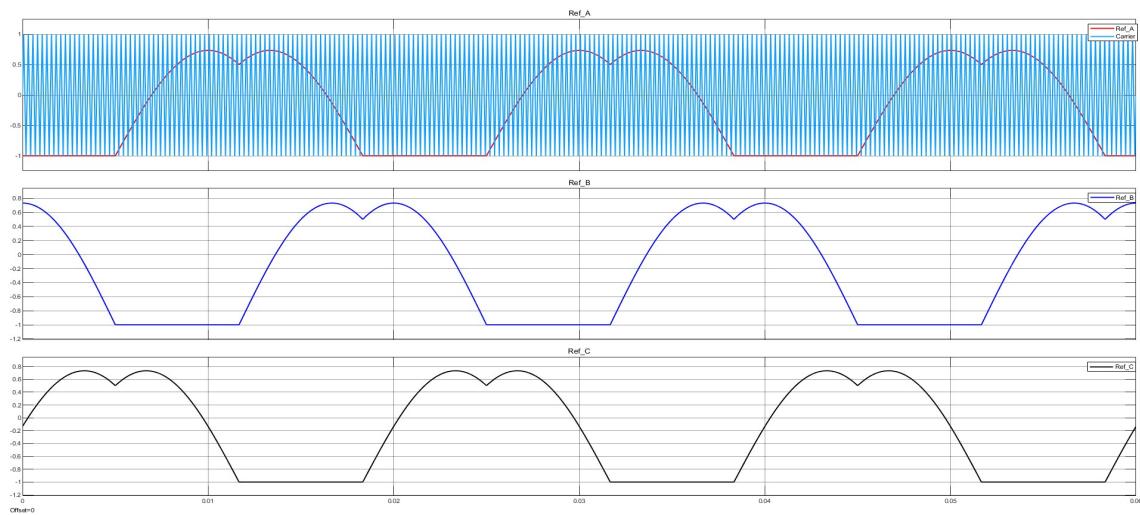


Figure 6.4: Three phase modulated references using DPWMMIN.

Figure 6.5 depicts the gate signals of the upper switches within the inverter for generating DPWMMAX. Notably, the figure showcases the presence of a DC clamp for each phase.

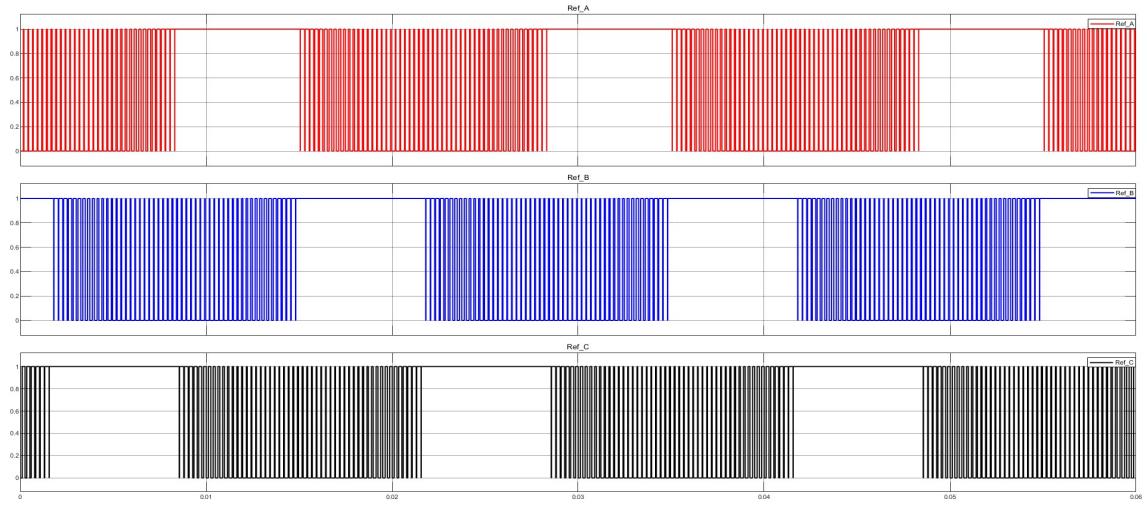
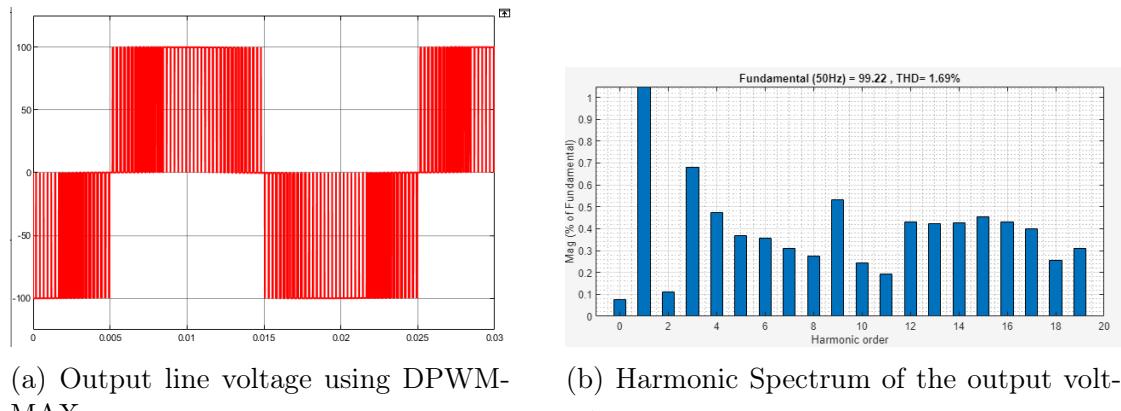


Figure 6.5: Gate signals of the upper switches using DPWMMAX.



(a) Output line voltage using DPWM-MAX.

(b) Harmonic Spectrum of the output voltage.

Figure 6.6: DPWMMAX Outputs.

Since the Presence of the zero-sequence component in the reference modulated waves , the distortion of the references is not affecting the output voltage.

### 6.2.2 DPWM0

The DPWM0 Modulation technique is implemented when there is a phase-shift between the voltage and current about  $-30^\circ$ , Meaning the load can be capacitive load in which the current leads the voltage. The DC clamping is conducted in which we shift it by  $-30$  and conducts for 60 degree for each half cycle.

The zero sequence component to achieve the specified modulated waves can be formed in such a way of: [8]

$$\gamma(\phi)|_{\text{DPWM1}} = \begin{cases} \gamma(\phi)|_{\text{DMAX}}, & -\pi \leq \phi \leq -\frac{2\pi}{3} \\ \gamma(\phi)|_{\text{DMIN}}, & -\frac{2\pi}{3} \leq \phi \leq -\frac{\pi}{3} \\ & -\frac{\pi}{3} \leq \phi \leq 0 \\ & 0 \leq \phi \leq \frac{\pi}{3} \\ & \frac{\pi}{3} \leq \phi \leq \frac{2\pi}{3} \\ & \frac{2\pi}{3} \leq \phi \leq \pi \end{cases} \quad (5.35)$$

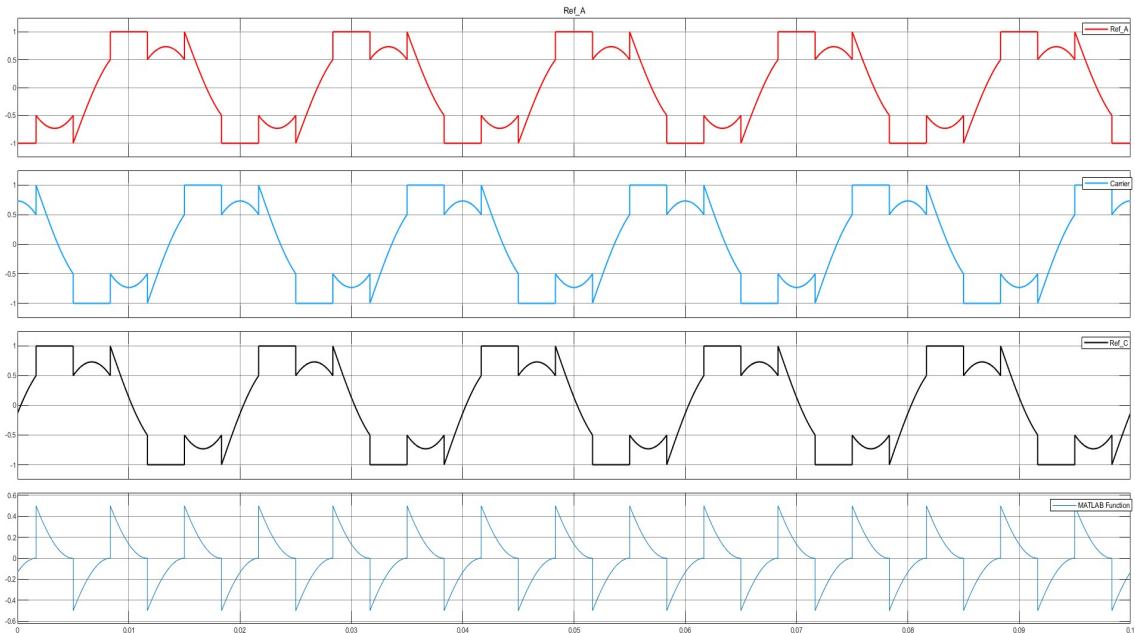


Figure 6.7: Three phase modulated references and their zero sequence using DP-WMM0.

### 6.2.3 DPWM1

The DPWM1 is a discontinuous pulse width modulation which applied when we ensure that we are having a unity power factor in the circuit to clamp the reference waves for 60 degree for each half cycle around the maximum current to achieve lower switching losses.[3]

The zero sequence component to achieve the specified modulated waves can be formed in such a way of:

$$\gamma(\phi)|_{\text{DPWM1}} = \begin{cases} \gamma(\phi)|_{\text{DMAX}}, & -\frac{5\pi}{6} \leq \phi \leq -\frac{\pi}{2} \\ \gamma(\phi)|_{\text{DMIN}}, & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \quad \frac{\pi}{6} \leq \phi \leq \frac{\pi}{2} \quad \frac{5\pi}{6} \leq \phi \leq \frac{7\pi}{6} \end{cases} \quad (5.36)$$

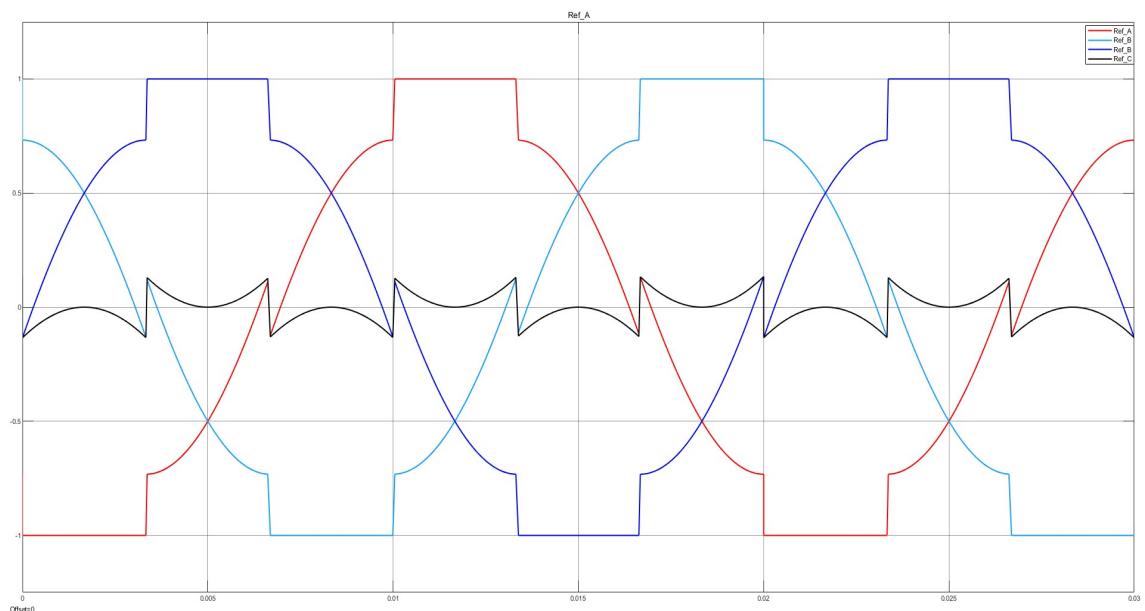


Figure 6.8: Three phase modulated references and their zero sequence using DP-WMM1.

### 6.2.4 DPWM2

The DPWM2 is a discontinuous pulse width modulation which applied when we have lagging power factor in the circuit to clamp the reference waves for 60 degree for each half cycle around the maximum current to achieve lower switching losses. Specifically for inductive loads with 30° phase-shift between the voltage and current to ensure that the clamping and the absence of the switching occurs around the maximum current values.

The zero sequence component to achieve the specified modulated waves can be formed in such a way of:

$$\gamma(\phi)|_{\text{DPWM1}} = \begin{cases} \gamma(\phi)|_{\text{DMIN}}, & -\pi \leq \phi \leq -\frac{2\pi}{3} \\ \gamma(\phi)|_{\text{DMAX}}, & -\frac{2\pi}{3} \leq \phi \leq -\frac{\pi}{3} \end{cases} \quad \begin{cases} -\frac{\pi}{3} \leq \phi \leq 0 \\ 0 \leq \phi \leq \frac{\pi}{3} \\ \frac{2\pi}{3} \leq \phi \leq \pi \end{cases} \quad (5.37)$$

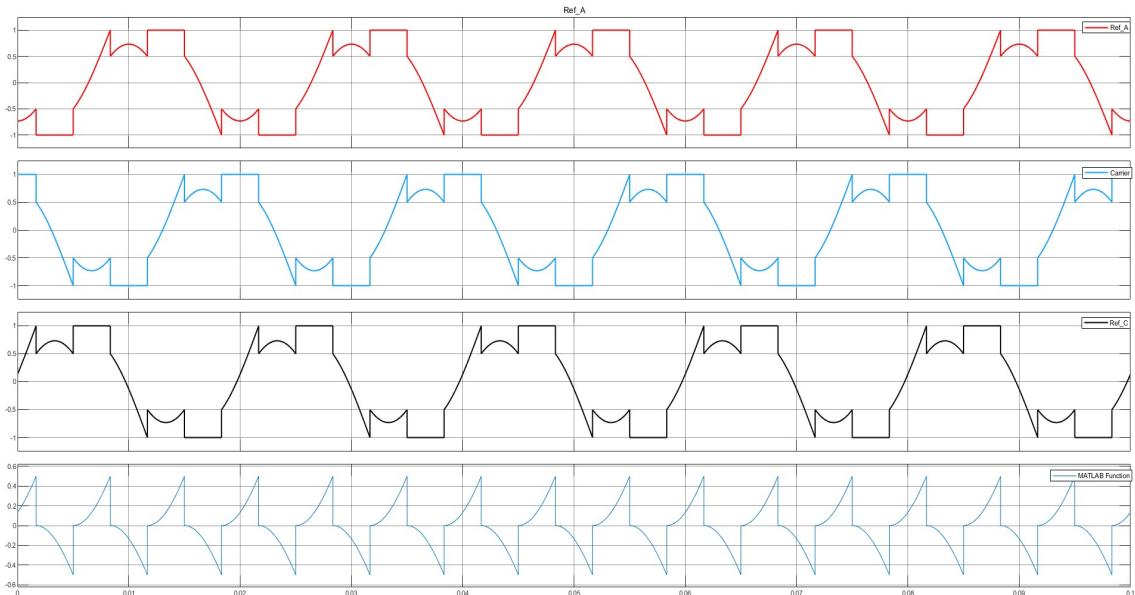


Figure 6.9: Three phase modulated references and their zero sequence using DP-WMM2.

### 6.2.5 Generalized Discontinuous Pulse Width Modulation

The generalized discontinuous pulse width modulation (GDPWM) technique is widely used to generate discontinuous reference signals by adjusting the DC rail clamp based on the power factor of the circuit. This approach aims to minimize switching losses. The implementation of GDPWM in the space vector plane can be described as illustrated in Figure 6.10. [8]

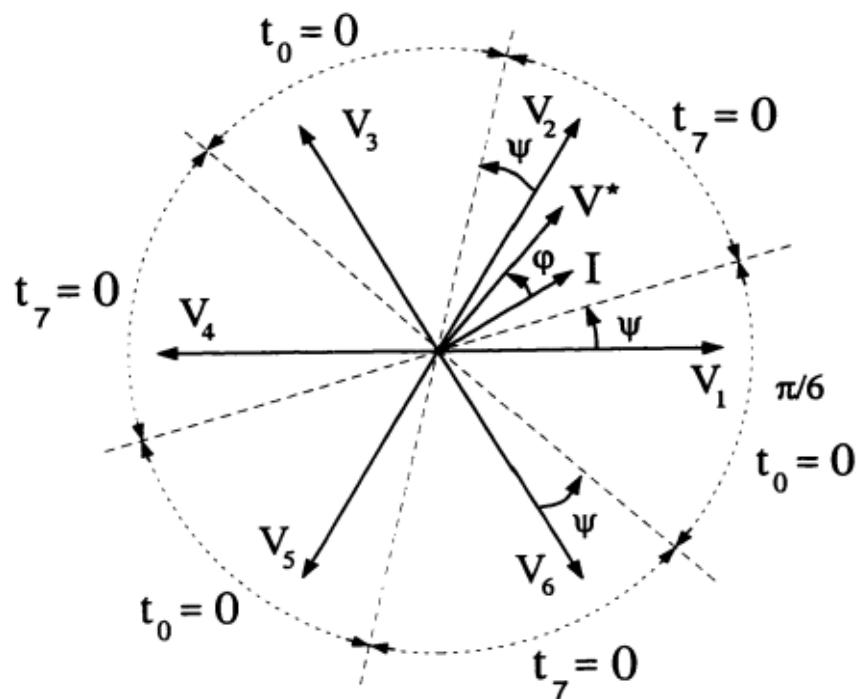


Figure 6.10: The GDPWM method space vector illustration. Where  $\psi$  is voltage current phase shift angle.[8]

### GDPWM equivalent carrier based implementation

GDPWM injection can be obtained throughout the magnitude test Equation which is :

$$\gamma(\phi, \psi_m)_{\text{GDPWM}} = \begin{cases} \frac{1}{2}[\text{sign}(V_{ra}(\phi))] - V_{ra}(\phi) & \text{if } V_{ra}(\phi, \psi) \geq |V_{rb}(\phi, \psi), V_{rc}(\phi, \psi)| \\ \frac{1}{2}[\text{sign}(V_{rb}(\phi))] - V_{rb}(\phi) & \text{if } V_{rb}(\phi, \psi) \geq |V_{ra}(\phi, \psi), V_{rc}(\phi, \psi)| \\ \frac{1}{2}[\text{sign}(V_{rc}(\phi))] - V_{rc}(\phi) & \text{if } V_{rc}(\phi, \psi) \geq |V_{rb}(\phi, \psi), V_{ra}(\phi, \psi)| \end{cases}$$

As it can be observed from Fig.6.11 after applying the step input as a variable

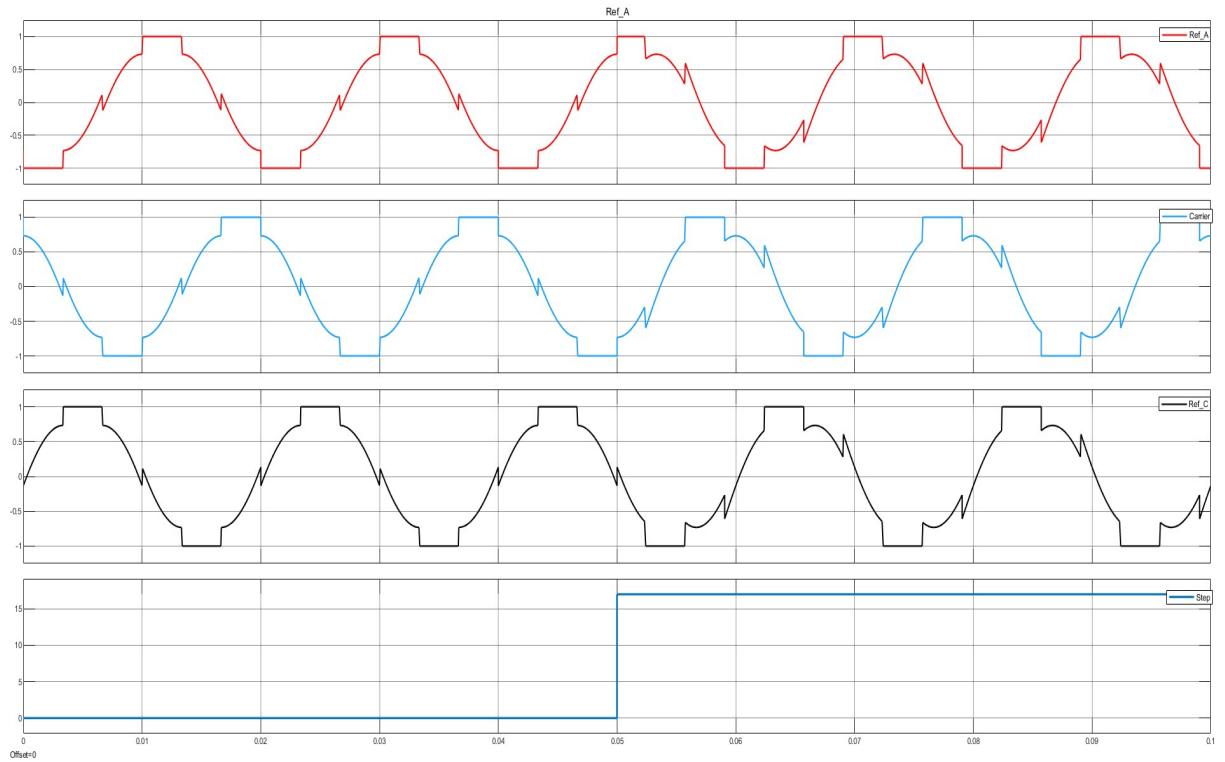


Figure 6.11: The GDPWM method under applying step input of phase shift angle from  $0^\circ$  to  $17^\circ$ .

power factor, the system respond to shift the rail clamped Dc to be surrounded with the maximum current to ensure that we are achieving the minimum switching losses.

## 6.3 Summary

This chapter explores the application of an advanced modulation technique which is Discontinuous Pulse Width Modulation (DPWM) for inverter control. The primary objective of this technique is to generate a pure sinusoidal waveform with lower harmonics with minimizing switching losses compared to traditional modulation methods. The effectiveness of DPWM relies on the power factor of the circuit to achieve optimal system performance. DPWM is further classified into three categories: DPWM0, DPWM1, and DPWM2, each tailored to specific power factor requirements based on the load characteristics. It is important to note that these classifications are special cases derived from the more generalized form known as Generalized Discontinuous Pulse Width Modulation (GDPWM). The chapter delves into the intricacies of DPWM and its variations, shedding light on their advantages and limitations within practical applications.

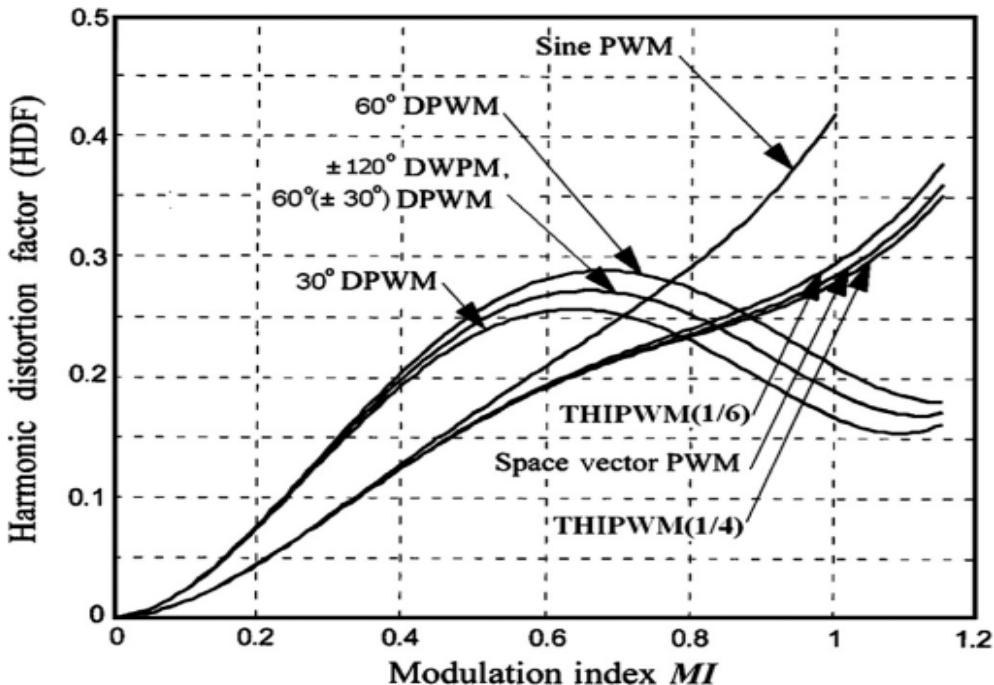


Figure 6.12: HDF comparison with different voltage modulation techniques.

# Chapter 7

## Conclusion and Future Work

### 7.1 Conclusion

In conclusion, when selecting an inverter architecture, the specific requirements of the application play a crucial role. MOSFETs are well-suited for low-power applications due to their high switching frequencies, enabling precise control and efficient operation. On the other hand, IGBTs are preferred for medium to high-power applications due to their acceptable switching frequencies, robustness, and reliability.

Modulation techniques are essential for shaping the output characteristics of three-phase inverters, including dual inverter drives. Among various modulation methods, THISPWM and SVM outperform SPWM in terms of voltage control and harmonic reduction. THISPWM offers straightforward control through modulation index and phase angle adjustments, allowing for precise customization of the output waveform. SVM excels in minimizing switching losses and leakage current flow, ensuring efficient energy conversion, particularly in high-power applications. Additionally, the incorporation of an inductance filter can further mitigate leakage currents, especially in scenarios with intermittent or absent grid connections. This additional filtering enhances system reliability and performance by effectively managing residual currents that could cause disturbances or inefficiencies.

Furthermore, within the realm of modulation techniques, Discontinuous Pulse Width Modulation (DPWM) stands out as an advanced approach that aims to produce a pure sinusoidal waveform with minimal switching losses. DPWM is

categorized into DPWM0, DPWM1, and DPWM2, which correspond to specific power factor requirements based on load characteristics. These classifications are derived from the more generalized form known as Generalized Discontinuous Pulse Width Modulation (GDPWM). DPWM, alongside other modulation techniques, contributes to achieving smooth and efficient operation in various applications. Overall, by carefully considering the specific requirements and characteristics of the application, selecting the appropriate inverter architecture, and employing suitable modulation techniques, it is possible to optimize the performance, efficiency, and reliability of the system.

## 7.2 Future Work

### 1. Hysteresis Control of Dual Inverter

hysteresis controllers aim to obtain effective control over the voltage or the current. They typically set a hysteresis band ( $h$ ) which allows the switches to change their state to adapt for the current condition. If the variable reaches its upper limit, the regulator will switch off to decrease the value. If the variable reaches the lower limit, the regulator will turn on to increase the value of the variable.

### 2. Space Vector Pulse Width Modulation for Multilevel Inverter

In the field of high-power, high-performance applications, multilevel inverters seem to be the most promising alternative. In this chapter, the application of SVPWM control strategy on three-level inverter has been proposed and analyzed. The proposed SVPWM algorithm provides high-safety voltages with less harmonic components compared to two-level structures and reduces the switching losses by limiting the switching to two thirds of the pulse duty cycle. On the one hand, the latter aimed to prove the effectiveness of SVPWM in the contribution of switching power losses reduction and to show the advantage of the three-level inverter that carry out voltages with contents of less harmonic injection than the two-level inverter. On the other hand, the simulation results show that as modulation index increases, the THD decreases and the fundamental RMS value increases linearly. In the first proposed method, the obtained THD for the two- and three-level inverters.

### 3. Proportional resonant controller

In AC applications, Proportional Resonant Controllers (PRCs) offer an alternative to conventional PI controllers, providing precise voltage control directly in the stationary reference frame. With inherent resonance at specific frequencies, PRCs, when coupled with modulation techniques, enable efficient and robust voltage regulation without the need for coordinate transformations, enhancing performance in AC systems. Integrating PRCs into future works promises improved voltage control capabilities and responsiveness, particularly in applications requiring high precision and efficiency.

### 4. Field Oriented Control with different modulation techniques

FOC provides good control capability over the full torque and speed ranges. Using appropriate modulation technique for FOC could enhance the performance of the used motor with reduction of the torque ripples.

### 5. Selective Harmonic Elimination

Incorporating Selective Harmonic Elimination (SHE) techniques presents a promising avenue for enhancing power quality in inverters. By selectively eliminating specific harmonics from the output voltage waveform, SHE methods offer improved efficiency and reduced harmonic distortion, leading to cleaner power delivery and minimized electromagnetic interference. Integrating SHE techniques into modulation strategies can enhance the performance and reliability of power electronics systems, making them more suitable for a wide range of applications, from renewable energy integration to motor drive systems.

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## Appendices

# **Appendix A**

## **SIMULINK MODELS**

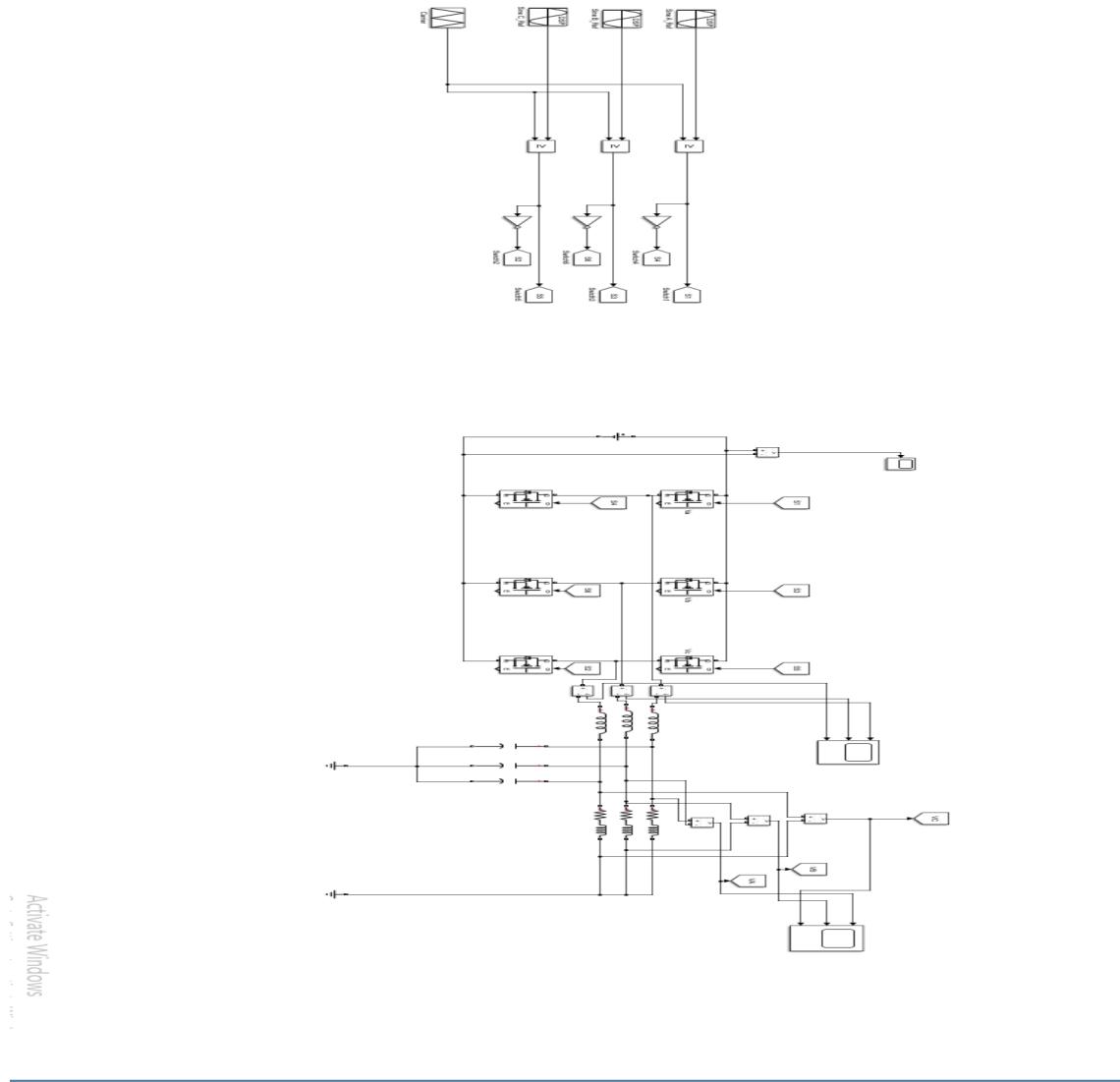


Figure A.1: SIMULINK model of SPWM with LC filter

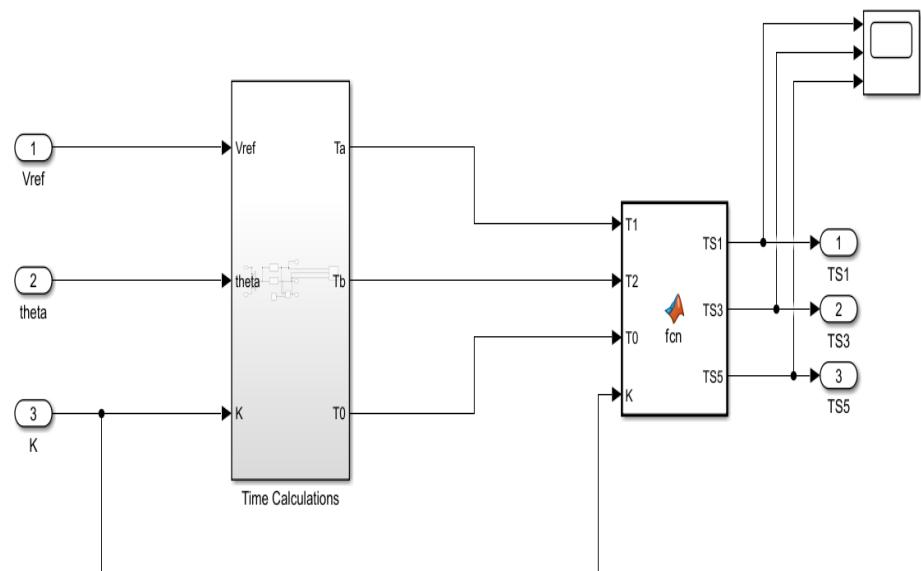
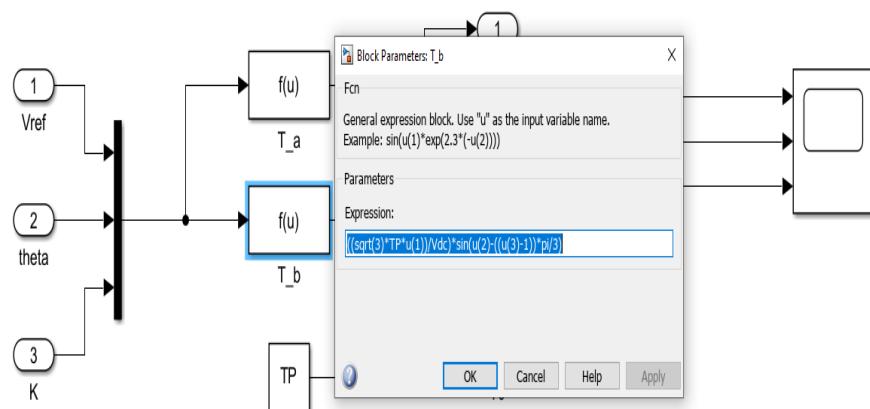


Figure A.2: Switching times in SVM block diagram.



Activate Window

Figure A.3: Timing T2 of the SVM.

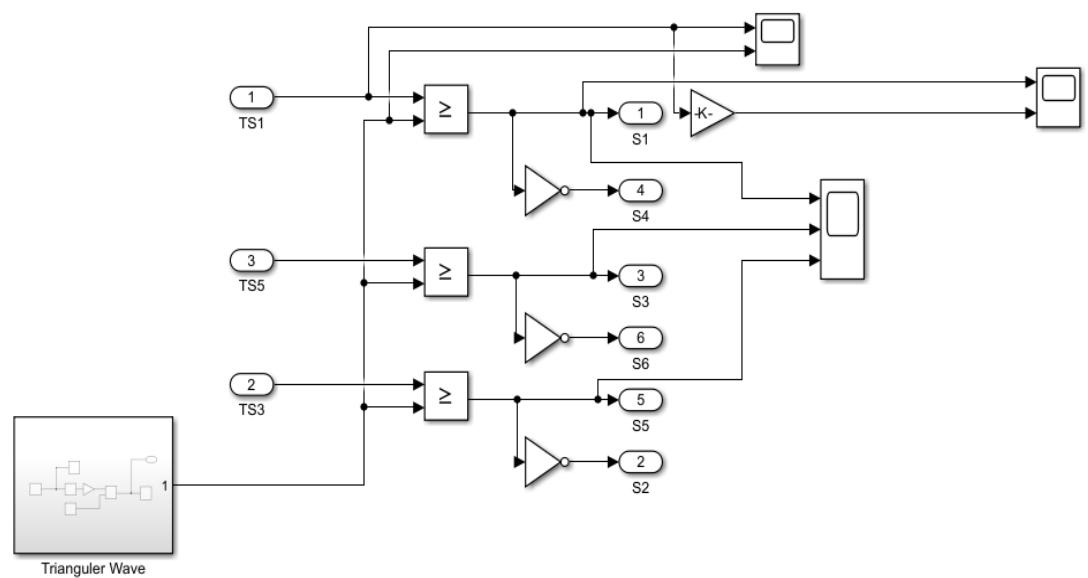


Figure A.4: SVM signal generation.

# Appendix B

## MATLAB CODES

### Sector Detector in Space Vector Modulation

```
function K = fcn(u)
Sector=0;
if (u>=0&&u<60)
    Sector=1;
elseif (u>=60&&u<120)
    Sector=2;
elseif (u>=120&&u<180)
    Sector=3;
elseif (u>=-180&&u<-120)
    Sector=4;
elseif (u>=-120&&u<-60)
    Sector=5;
elseif (u>=-60&&u<0)
    Sector=6;
end
K = Sector;
```

## Time Duration of Each Upper Switch in VSI using SVM

```
function [TS1, TS3, TS5] = fcn(T1, T2, T0, K)
switch K

    case 1
        TS1=T1+T2+T0/2;
        TS3=T2+T0/2;
        TS5=T0/2;

    case 2
        TS1=T1+T0/2;
        TS3=T1+T2+T0/2;
        TS5=T0/2;

    case 3
        TS1=T0/2;
        TS3=T1+T2+T0/2;
        TS5=T2+T0/2;

    case 4
        TS1=T0/2;
        TS3=T1+T0/2;
        TS5=T1+T2+T0/2;
        TS4=T1+T2+T0/2;
        TS6=T2+T0/2;
        TS2=T0/2;

    case 5
        TS1=T2+T0/2;
        TS3=T0/2;
        TS5=T1+T2+T0/2;
```

```
case 6
    TS1=T1+T2+T0/2;
    TS3=T0/2;
    TS5=T1+T0/2;

otherwise
    TS1=0;
    TS3=0;
    TS5=0;

end
end
```

# Appendix C

## C Codes

### SPWM Code

```
#include <stdio.h>
#include <math.h>
#include <avr/io.h>
#include <avr/interrupt.h>

#define TABLE_SIZE 200
#Modulation_index=1
int counter = 0;
double sine_table[TABLE_SIZE];
void setup(){
    pinMode(A0,INPUT);}
int main() {
    sei();
    Serial.begin(9600);
    DDRB |= (1 << DDB1); // Set pin 9 (PB1) as output

    int i;
    double step = M_PI / 200;
```

```
for (i = 0; i < TABLE_SIZE; i++) {
    sine_table[i] = Modulation_index*sin(step * i) * 799;
}

ICR1 = 799;
TCCR1B |= (1 << WGM13) | (1 << WGM12)|(1<<CS10);
TIMSK1 |= 1 << TOIE1;
TCCR1A |= (1 << COM1A1) | (1 << WGM11) ;
TCNT1 = 0;
OCR1A = 0;

while(1){ }
    return 0;

}

ISR(TIMER1_OVF_vect) {
    if (counter == 200)
        counter = 0;
    OCR1A = (int)sine_table[counter];
    counter++;
}
```