Design

Computer Architecture

12-27-2014

1-CPU

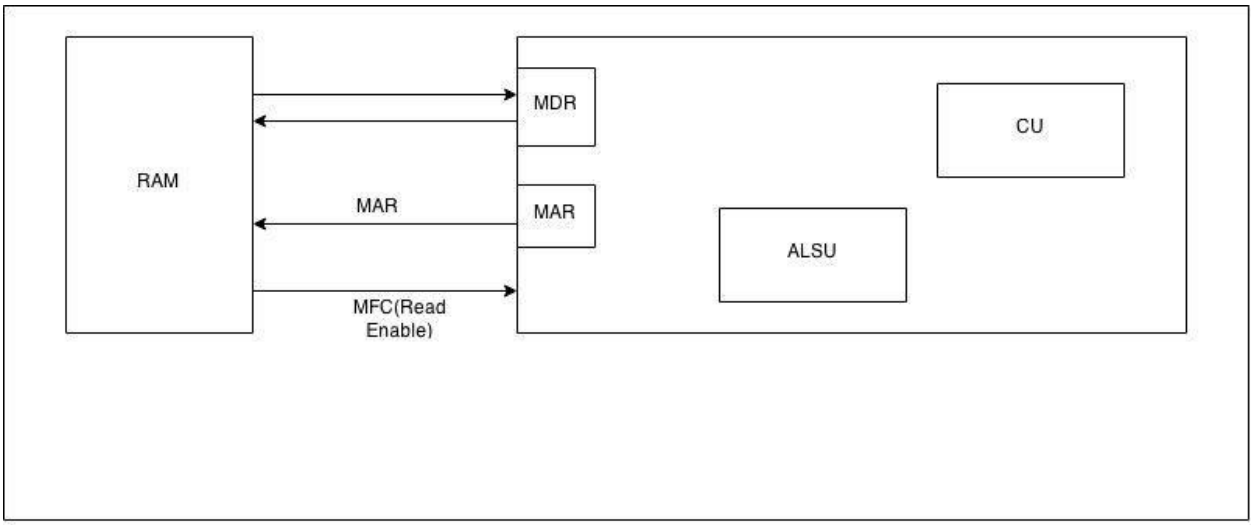

Figure 1: CPU Diagram

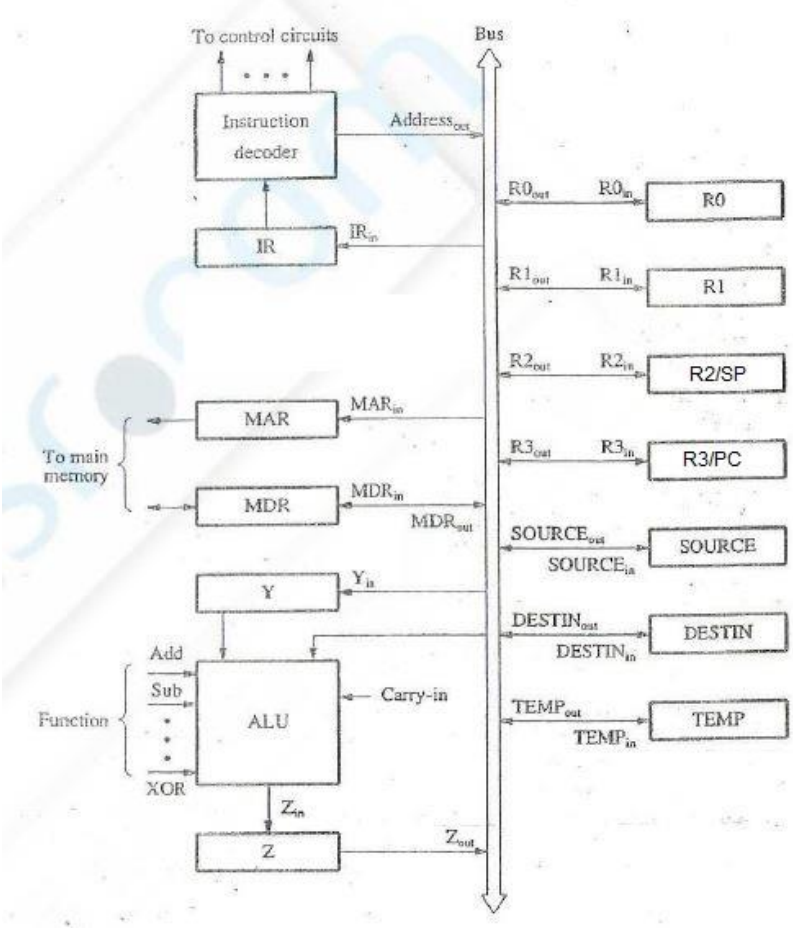

Figure 2: CPU Circuit

2- ALSU Functions

	S_3	S_2	S_1	S_0	Cin =0	Cin = 1
Part A	0	0	0	0	F = A	F = A+1
	0	0	0	1	F = A + B	F = A+ B+1
	0	0	1	0	F = A-B-1	F = A-B
	0	0	1	1	F= A- 1	F = 0
Part B	0	1	0	0	F = A and B	
	0	1	0	1	F = A or B	
	0	1	1	0	F = A xor B	
	0	1	1	1	F = Not A	
Part C	1	0	0	0	F=Logic shift right A	
	1	0	0	1	F=Rotate right A	
	1	0	1	0	F=Rotate right A with Carry	
	1	0	1	1	F=Arithmatic shift right A	
Part D	1	1	0	0	F=Logic shift left A	
	1	1	0	1	F=Rotate left A	
	1	1	1	0	F=Rotate left A with Carry	
	1	1	1	1	F = Arithmatic shift left A	

Figure 3: ALSU Functions

3-CU

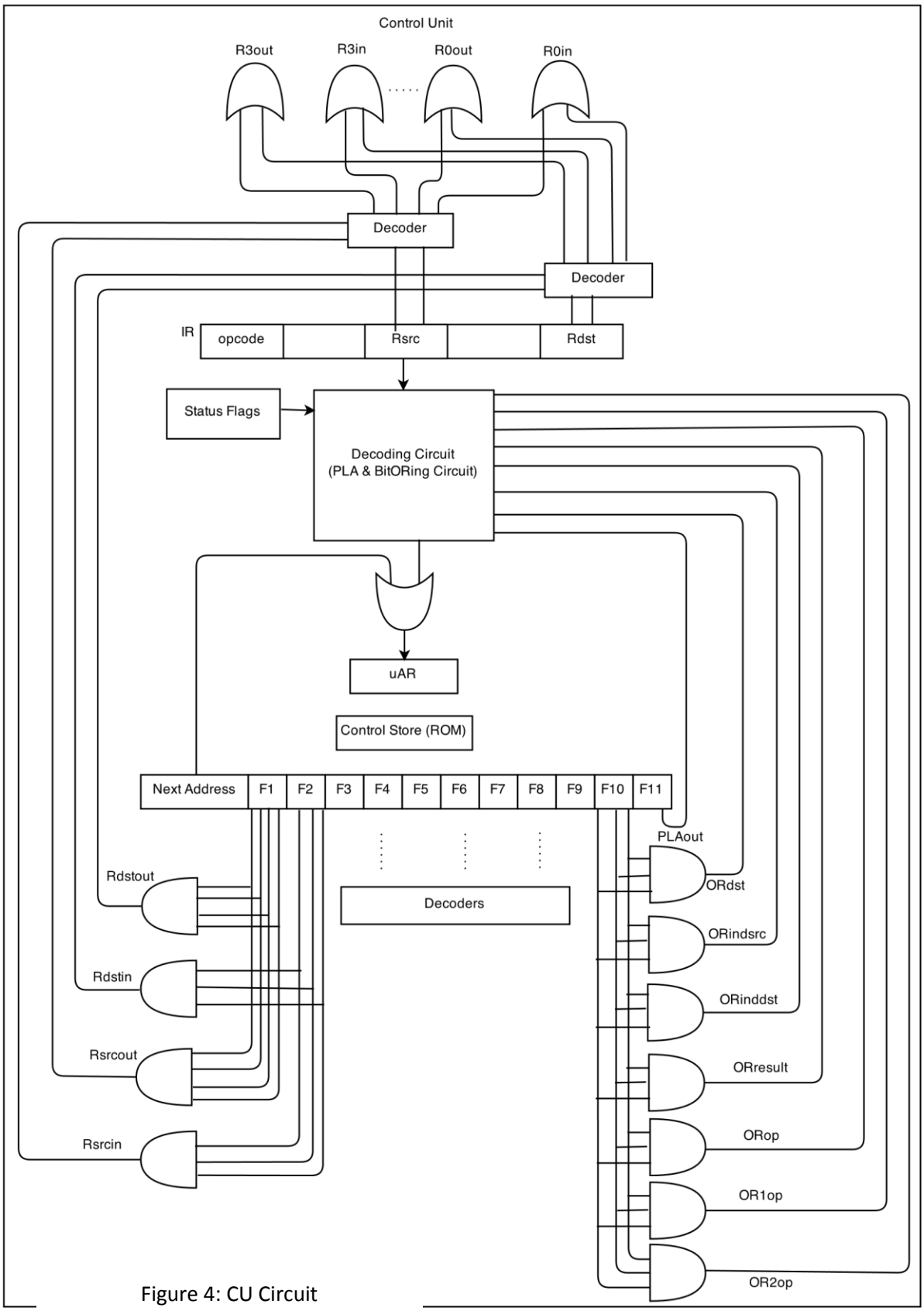

Figure 4: CU Circuit

4-CW functions

F0	F1	F2	F3
F0 (8 bits)	F1 (4 bits)	F2 (3 bits)	F3 (2 bits)
Address of next microinstruction	0000: No transfer 0001: PC_{out} 0010: MDR_{out} 0011: Z_{out} 0100: $Rsrc_{out}$ 0101: $Rdst_{out}$ 0110: SPout 1000: $SOURCE_{out}$ 1001: $DESTIN_{out}$ 1010: $TEMP_{out}$ 1011: Addressout	000: No transfer 001: PC_{in} 010: IR_{in} 011: Z_{in} 100: $Rsrc_{in}$ 101: $Rdst_{in}$ 110: SPin	00: No transfer 01: MAR_{in} 10: MDR_{in} 11: $TEMP_{in}$

F4	F5	F6	F7
F4 (2 bits)	F5 (4 bits)	F6 (2 bits)	F7 (1 bit)
00: No transfer 01: Y_{in} 10: $SOURCE_{in}$ 11: $DESTIN_{in}$	in ALSU file	00: No action 01: Read 10: Write 11: HLT	0: No action 1: Clear Y

F8	F9	F10	F11
F8 (1 bit)	F9 (1 bit)	F10 (3 bits)	F11 (1 bit)
0: Carry-in = 0 1: Carry-in = 1	0: No action 1: FLAGS_E	000: No action 001: OR_{dst} 010: OR_{indsrc} 011: OR_{inddst} 100: OR_{result} 101: OR2op 110: ORop 111: OR1op	0: No action 1: PLA_{out}

Figure 5: CW Functions

5-BitOring Circuit

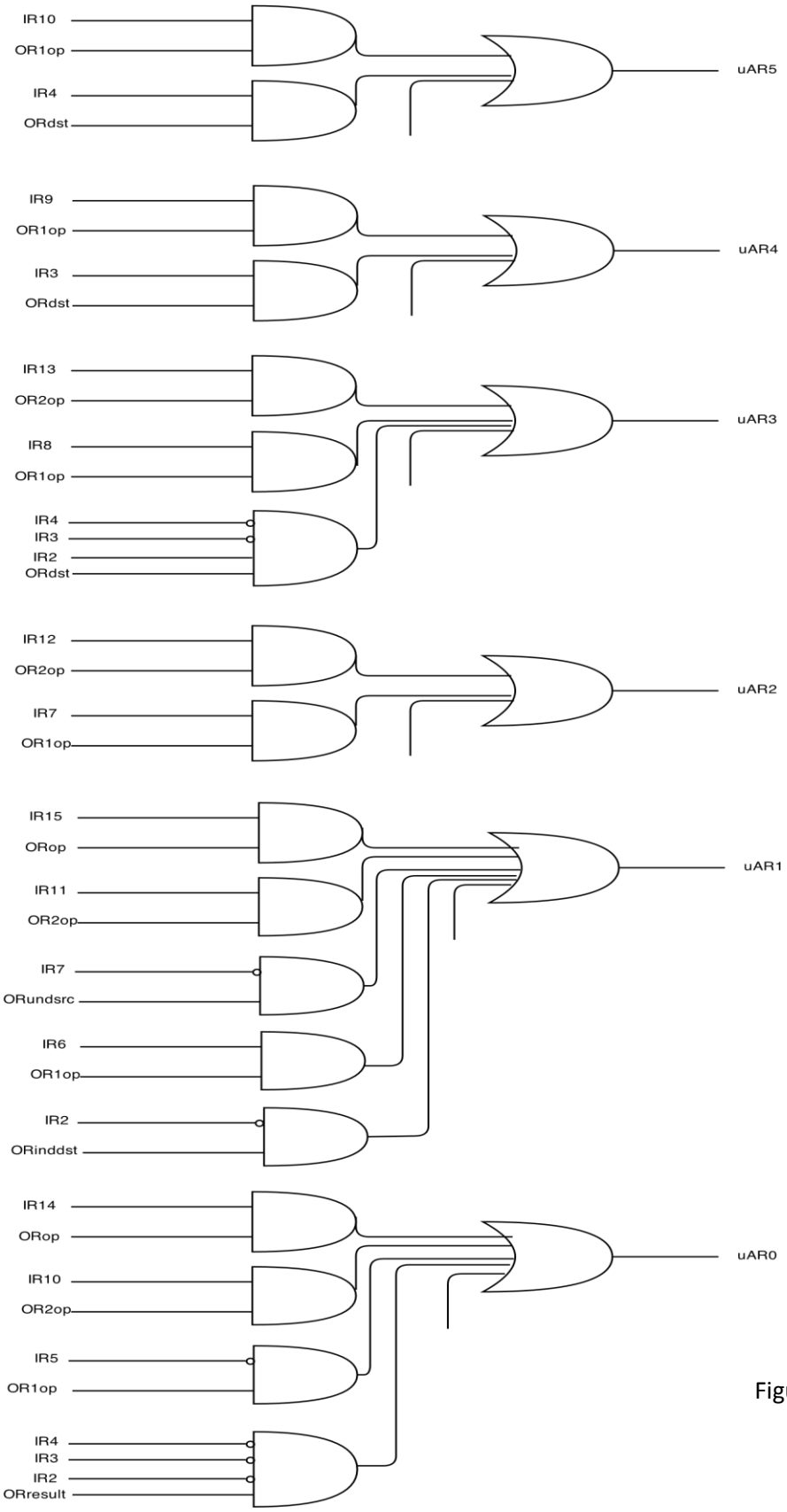

Figure 6: BitORing Circuit

6- ROM instructions

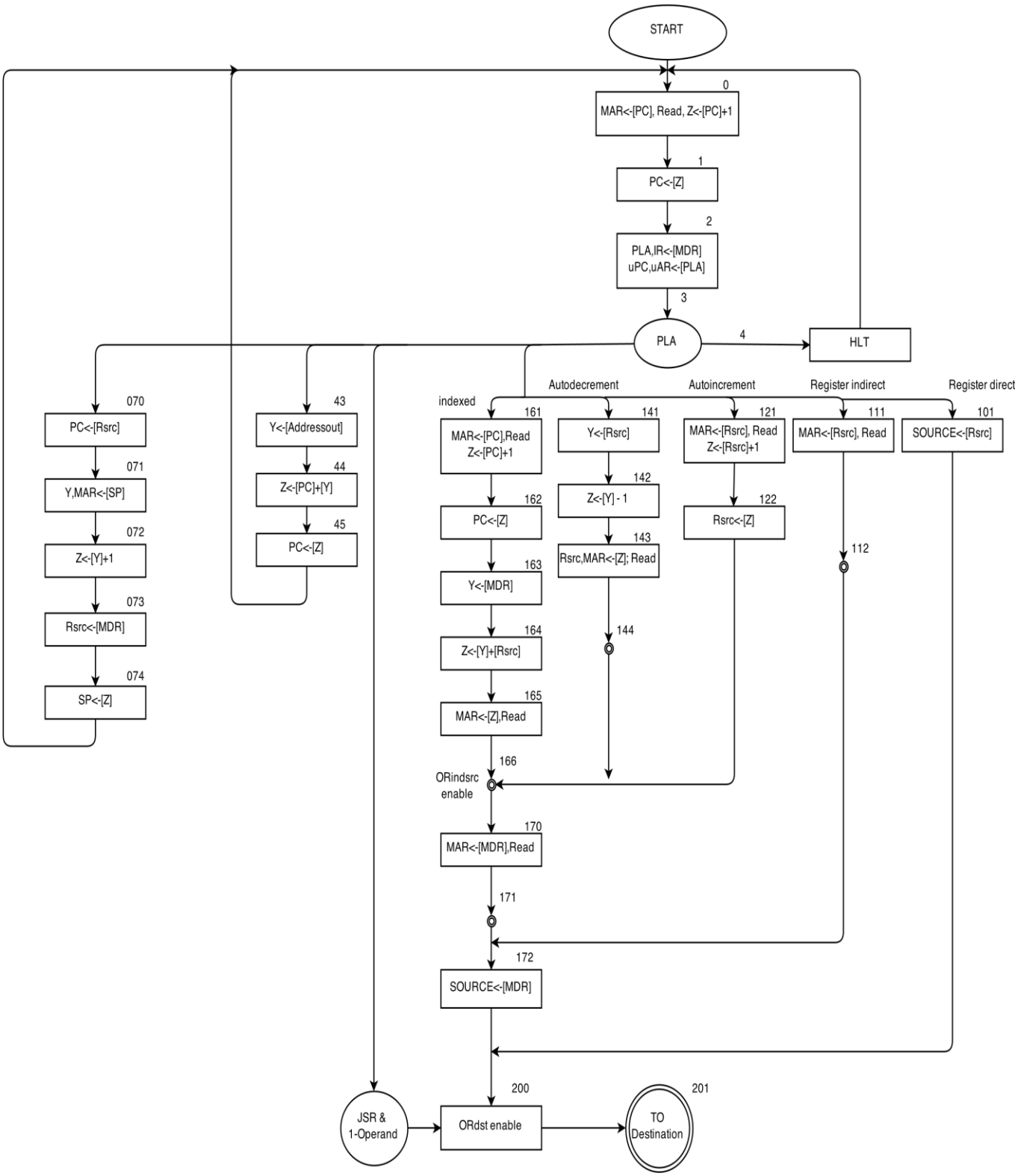

Figure 7: fetching Source & Branch operations & RTS

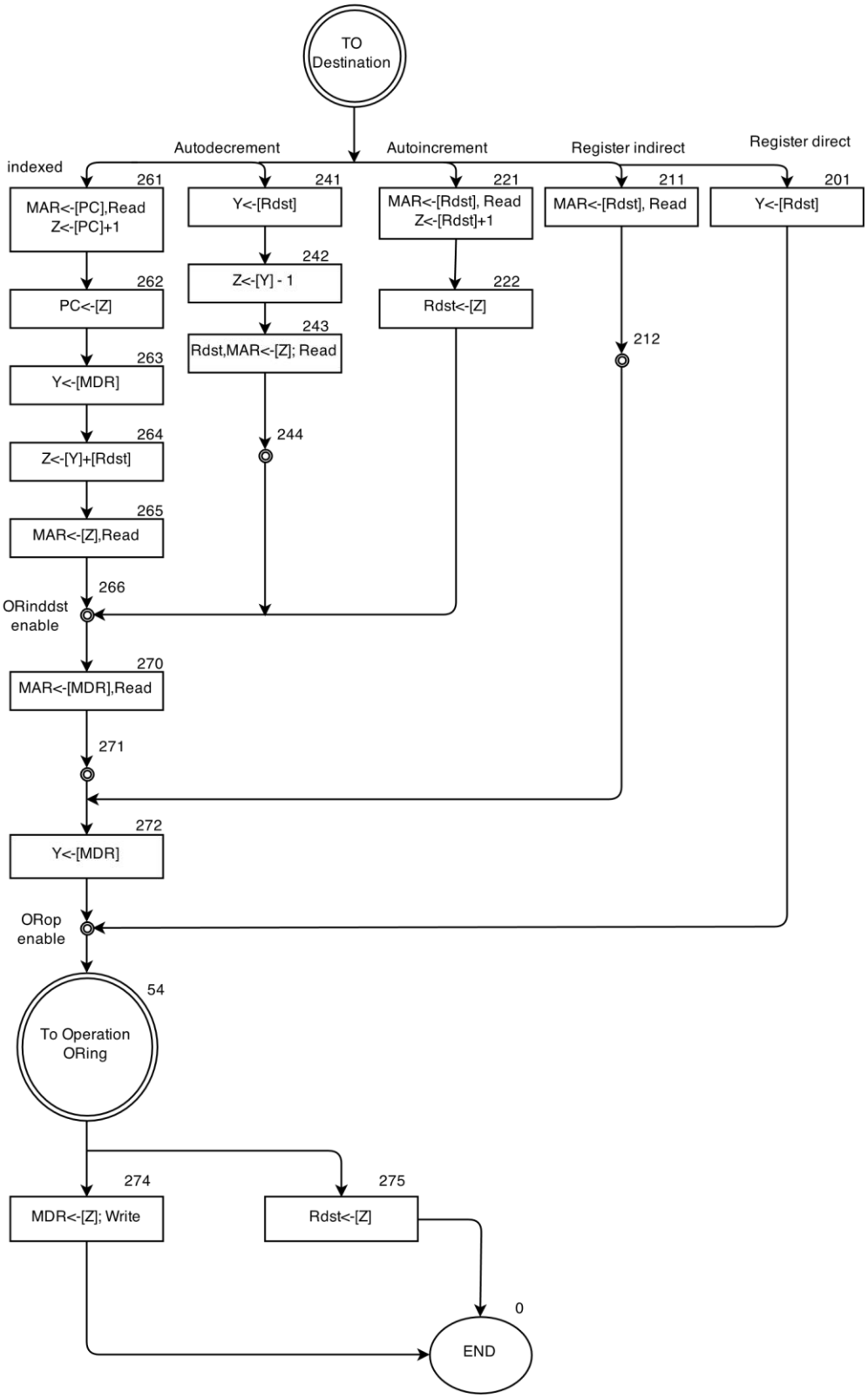

Figure 8: fetching Destination

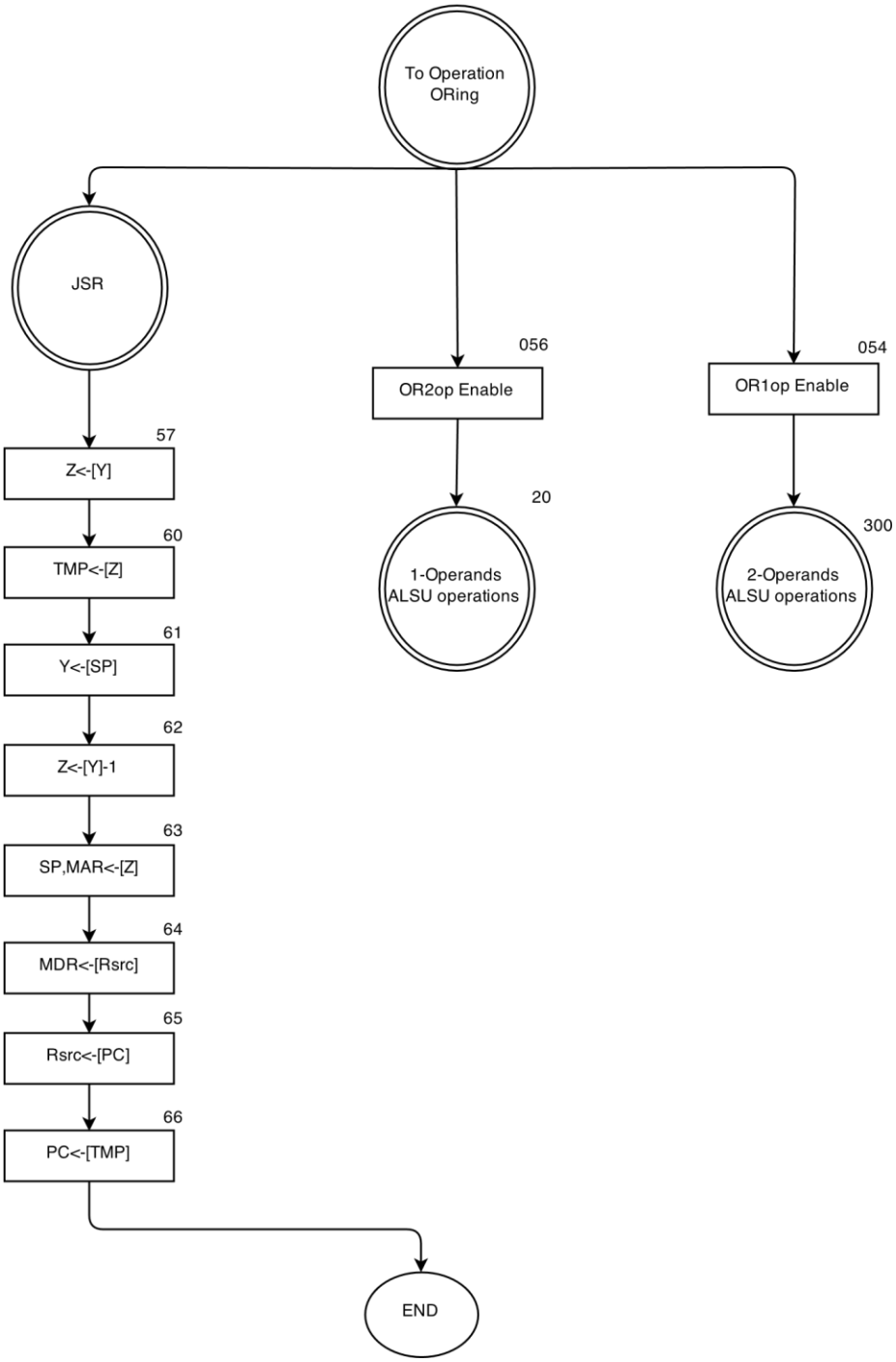

Figure 9: Operation ORing & JSR

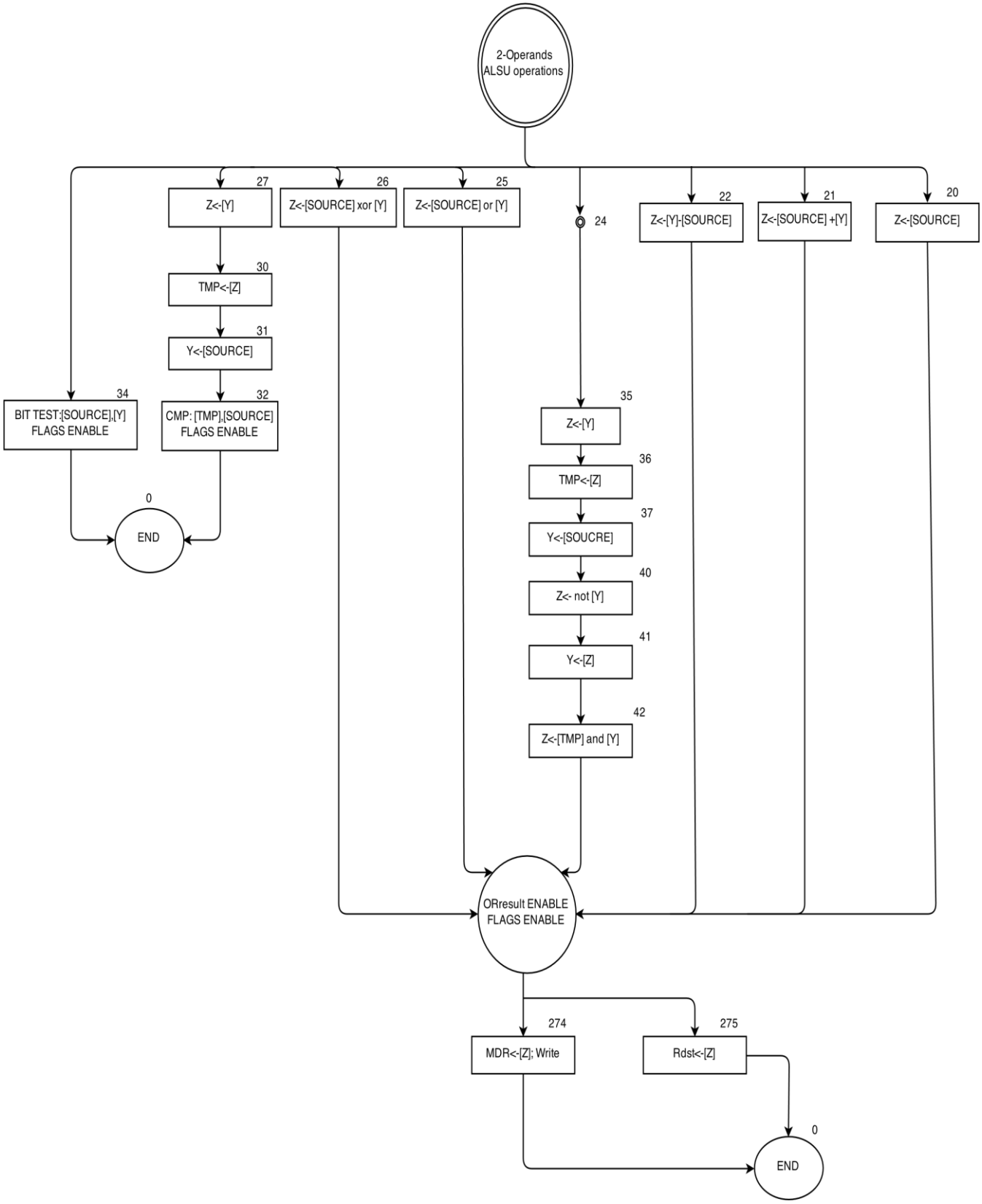

Figure 10: 2-Operand operations

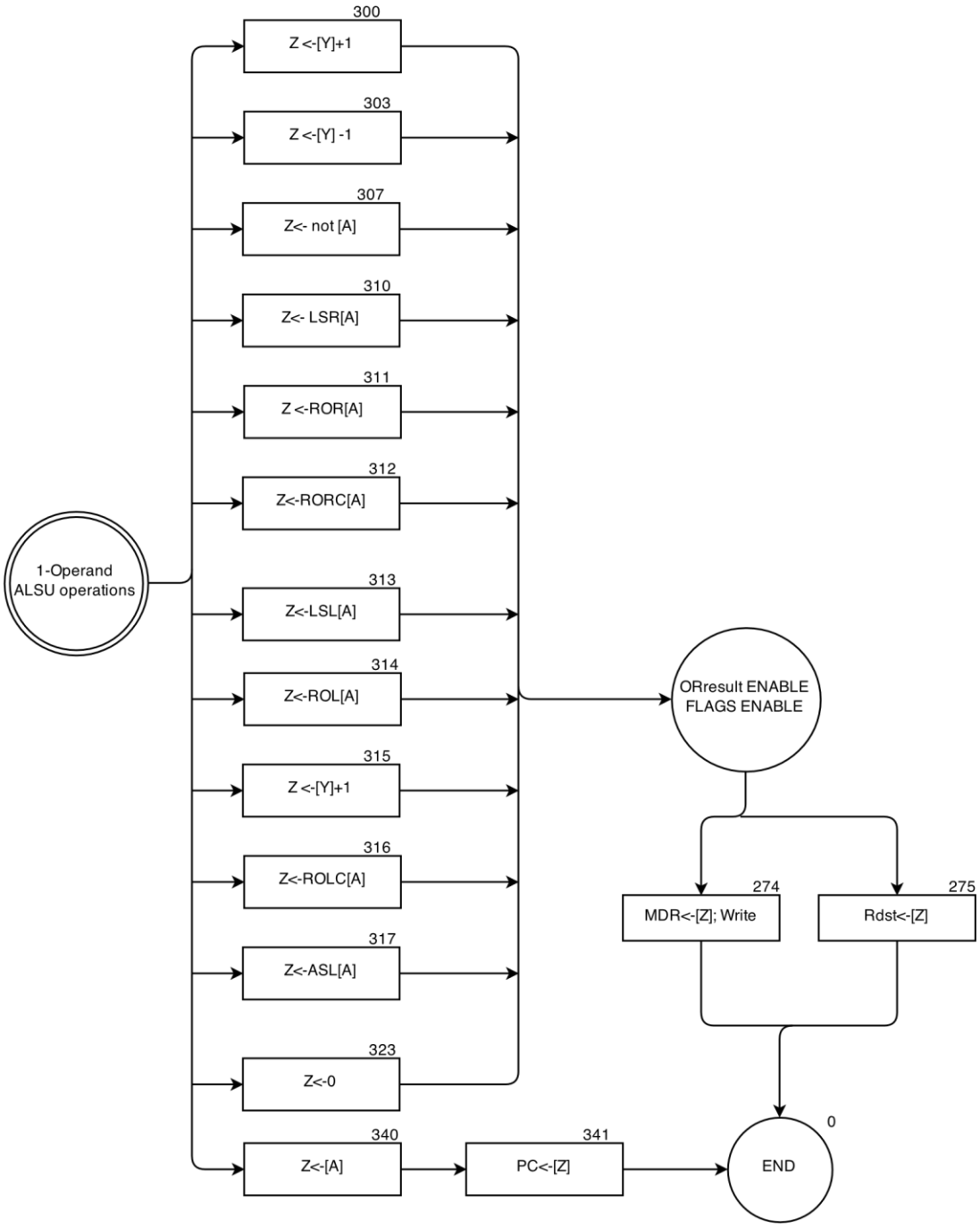

Figure 11: 1-Operand operations