Practical 3 FIFO

Code

```
architecture Behavioral of fifo1234 is
signal WPTR,RPTR:STD_LOGIC_VECTOR(3 downto 0);
type fifo is array(15 downto 00) of std_logic_vector(7 downto 00);
signal MEM:fifo;
begin
PROCESS(clk,rst)
begin
IF rst ='1' THEN
WPTR <="0000";
RPTR<="0000";
red <= '0';
ELSIF(clk'EVENT AND clk='1') THEN
IF (EN='1')THEN
IF (w='1') THEN
IF(WPTR<"1111")THEN
MEM(CONV_INTEGER(WPTR))<= datain;
WPTR<=WPTR+1;
END IF;
ELSE
IF(RPTR<WPTR)THEN
red <='0';
dataout<=MEM(CONV_INTEGER(RPTR));
RPTR <= RPTR+1;
ELSE
red<='1';
dataout<="00000000";
END IF;
END IF;
END IF;
END IF;
```

```
END PROCESS;
end Behavioral;
```

Test Bench FIFO

```
BEGIN
wait for 100 ns;
rst<='1';
wait for 10 ns;
rst<='0';
en<='1';
w<='1';
datain<="00010100";
wait for 10 ns;
rst<='0';
en<='1';
w<='0';
wait for 10 ns;
wait; -- will wait forever
END PROCESS;
END;
```