**Mini Project**
Report

# UART Implementation on FPGA

*EC806 Digital Design Using FPGA*

**Masters of Technology**
**in**
**Electronics and Communication Engineering**

Submitted by Group 5


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**Abstract**

The design and implementation of parallel communication are discussed in this study. As more data bits are transmitted simultaneously, the cost and complexity rise. Serial communication does away with this problem and produces successful long-distance communication outcomes. Serial communication protocols are sometimes referred to as UARTs (Universal Asynchronous Receiver Transmitters). The implementation of UART at various baud rates is included in this study. Baud rate generator, transmitter, and receiver are the three primary components of UART. Additionally, FPGA hardware boards are used for testing. Since the Altera Cyclon soc DE1 board meets the requirements for our project, we used it for the UART testing. Verilog, a hardware descriptive language, and Quartus with tool are used to create UARTs and modelsim for RTL verification.

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# Chapter 1

# Introduction

Serial communication methods are becoming and more common because they can send data over great distances with little expense and complexity. A popular serial communication protocol for transmitting and receiving data across various devices is called Universal Asynchronous Receiver Transmitter (UART). There are many benefits to using FPGA to create UART, including flexibility, fast communication, and low power usage.

An FPGA will be used in this project to design and construct a UART communication interface. The project focuses on the use of UART at various baudrates, including the creation and use of the transmitter, receiver, and baud rate generator. The main objective of the project is to validate the functionality of the UART implementation on an FPGA hardware board.The Altera DE01 SOC Development Kit was selected for testing because it could fulfil the needs of the project. The UART modules were created and implemented using Verilog, a common hardware description language.The success of the project will depend on the UART modules' precise design, implementation, testing, and functional verification. A solid grasp of digital system design, Verilog programming, and FPGA implementation are prerequisites for this project.

This project's overall goal is to show how beneficial FPGA is for implementing UART communication interfaces and how versatile it can be in many digital system applications. The project's results will offer important new perspectives on the development of UARTs and their potential for usage in next communication systems.

## 1.1 Motivation

UART (Universal Asynchronous Receiver and Transmitter) is one of the most commonly used serial communication protocols in embedded systems and digital electronics. While most microcontrollers already provide built-in UART peripherals, implementing UART on an FPGA helps in understanding how the protocol actually works at the hardware level.

The main motivation for this project is to design and implement UART communication using FPGA logic blocks instead of using predefined modules. This allows a deeper understanding of data framing, baud-rate generation, sampling, synchronization, and error checking.

Furthermore, implementing UART on an FPGA provides complete control over how the communication protocol is structured and executed. Instead of relying on fixed hardware features, the designer can modify or extend the UART architecture depending on system requirements. This flexibility is especially useful in applications where non-standard baud rates or custom data frames are required.

Another important motivation is that FPGA-based UART design helps in understanding how hardware and timing constraints affect serial communication. It encourages the designer to think about clock domains, metastability, sampling accuracy, and synchronization issues, all of which are critical in real-time communication circuits.

In addition, creating a UART module from scratch strengthens problem-solving skills. It requires breaking down the protocol into functional blocks such as baud rate generators, state machines, serializers, deserializers, and buffers. This modular approach helps in building a structured mindset which is essential for larger FPGA and ASIC projects.

Finally, this project serves as a strong foundation for learning more complex communication protocols like SPI, I2C, CAN, or even high-speed interfaces. By understanding UART at the hardware level, it becomes easier to approach and design other digital communication modules in future embedded or FPGA-based projects.

# Chapter 2

# Work Done

## 2.1 Universal Synchronous Asynchronous Transmitter and Receiver Protocol

This chapter provides a detailed explanation of the UART communication protocol and its implementation using FPGA hardware. The first section presents an overview of the protocol, including its frame structure, data transmission method, and the role of baud-rate generation in reliable serial communication. The following section focuses on the FPGA-based implementation, where we design the UART transmitter and receiver modules using Verilog HDL. It also covers the RTL simulation process used to verify the design's functionality, followed by synthesis and hardware implementation on the FPGA board. Together, these sections offer a complete understanding of both the theoretical aspects of the protocol and its practical realization in digital hardware.

### 2.1.1 Overview

UART (Universal Asynchronous Receiver and Transmitter) is a widely used serial communication protocol designed for point-to-point data transfer between digital devices. It operates asynchronously, meaning it does not require a separate clock signal; instead, both the transmitter and receiver must agree on a common baud rate. UART transmits data in the form of frames, typically consisting of a start bit, data bits, an optional parity bit, and one or more stop bits. The start bit indicates the beginning of transmission, while the stop bit marks its end, allowing the receiver to properly sample the incoming data. UART communication is simple, low-cost, and reliable for short-distance data exchange, making it highly popular in microcontrollers,

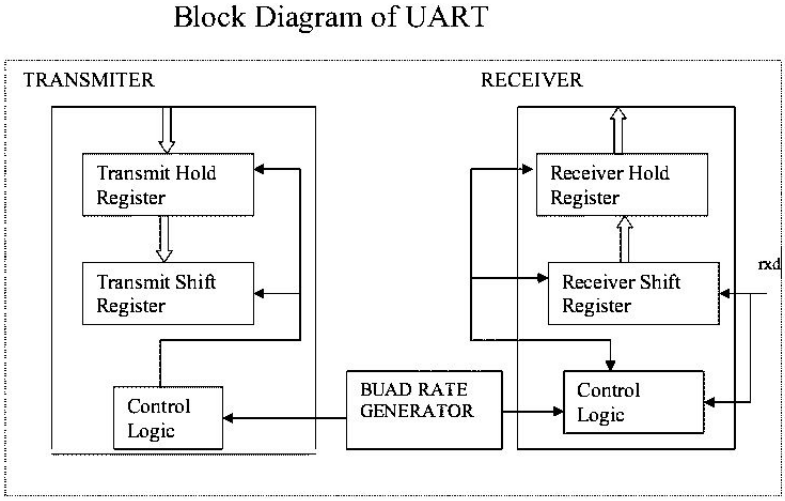


Figure 2.1: UART Block Diagram

sensors, embedded systems, and computer interfaces. Despite its simplicity, UART supports configurable parameters like baud rate, frame format, and parity, which gives flexibility for different applications.

### 2.1.2 Baud rate generation

**Table 19-1. Equations for Calculating Baud Rate Register Setting**

| Operating Mode | Equation for Calculating Baud Rate[1] | Equation for Calculating UBRRn Value |
|---|---|---|
| Asynchronous normal mode (U2Xn = 0) | $BAUD = \frac{f_{OSC}}{16(UBRRn + 1)}$ | $UBRRn = \frac{f_{OSC}}{16BAUD} - 1$ |
| Asynchronous double speed mode (U2Xn = 1) | $BAUD = \frac{f_{OSC}}{8(UBRRn + 1)}$ | $UBRRn = \frac{f_{OSC}}{8BAUD} - 1$ |
| Synchronous master mode | $BAUD = \frac{f_{OSC}}{8(UBRRn + 1)}$ | $UBRRn = \frac{f_{OSC}}{2BAUD} - 1$ |

Note: 1. The baud rate is defined to be the transfer rate in bit per second (bps)

**BAUD** Baud rate (in bits per second, bps)

$f_{OSC}$ System oscillator clock frequency

**UBRRn** Contents of the UBRRnH and UBRRnL registers, (0-4095)

Some examples of UBRRn values for some system clock frequencies are found in Table 19-9 on page 163.

Figure 2.2: UART Baud rate

A baud rate generator is an important block in UART communication that creates the timing signal required for sending and receiving data at a fixed speed. Because UART works without a shared clock, both the transmitter and receiver must operate at the same baud rate for correct data

sampling. The baud rate generator divides the main system clock to produce a lower frequency pulse that matches the selected baud rate, such as 9600 or 115200 bits per second. This pulse controls when each bit is transmitted or read. Many UART designs also use oversampling, such as 8x or 16x sampling, to improve accuracy and reduce errors caused by noise or timing variations. In this way, the baud rate generator ensures proper timing and reliable asynchronous communication between devices.

### 2.1.3 Data Frame format

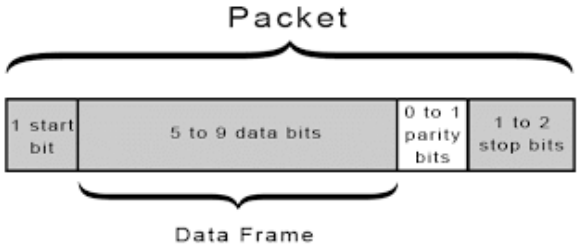


Figure 2.3: UART Data frame

A UART frame is the basic structure used to transmit data serially from the sender to the receiver. Since UART communication is asynchronous and does not use a shared clock, each frame contains specific bits that help the receiver identify the start, content, and end of the transmitted data. A typical UART frame consists of a start bit, a set of data bits, an optional parity bit, and one or more stop bits.

The frame begins with a start bit, which is always a logic low. This bit indicates to the receiver that a new data byte is about to arrive. After the start bit, the data bits are transmitted, typically ranging from 5 to 9 bits depending on the configuration. These bits carry the actual information, with the least significant bit (LSB) sent first. An optional parity bit may follow the data bits to provide simple error detection. The parity can be even, odd, or disabled based on system requirements. The frame ends with one or more stop bits, which are logic high. These stop bits allow the receiver to detect the end of the frame and prepare for the next byte of data.

This structured format ensures reliable communication between devices operating at the same baud rate, even without a shared clock, and makes UART a simple yet robust method for serial data transmission.

### 2.1.4 Data Reception and Transmission

In UART communication, data transmission and reception occur asynchronously through two dedicated signal lines: TX (transmit) and RX (receive). The transmitter converts parallel data from the system into a serial bitstream, while the receiver performs the reverse process. Because no common clock signal is shared between the devices, both ends must be configured with the same baud rate to ensure proper synchronization.

During data transmission, the UART transmitter first sends a start bit to signal the beginning of a new frame. It then shifts out the data bits one by one, starting from the least significant bit (LSB). If parity is enabled, the transmitter appends a parity bit generated according to the selected parity mode. Finally, one or more stop bits are sent to mark the end of the frame. Internally, the transmitter uses a shift register and a baud-rate clock to control the timing of each bit, ensuring that the data is output at a consistent and accurate rate.

In data reception, the receiver continuously monitors the RX line for a transition from high to low, which indicates the arrival of a start bit. Once detected, the receiver begins sampling the incoming data at specific intervals determined by its baud-rate generator. The sampled bits are reconstructed into a byte and checked for parity errors if parity is used. After receiving the stop bit(s), the reconstructed data is transferred to a buffer or register for use by the system. The receiver typically employs oversampling techniques to improve accuracy and reduce the chances of misinterpreting noisy signals.

Together, the transmission and reception processes ensure reliable, bidirectional communication between digital devices using the UART protocol. Their simple structure, minimal hardware requirements, and flexibility make UART a widely used interface in embedded systems and serial communication applications.

## 2.2 Implementation on FPGA

Implementing UART on an FPGA involves designing the transmitter and receiver modules using hardware description languages such as Verilog or VHDL. Instead of relying on built-in peripherals, the UART logic is created using components like state machines, counters, shift registers, and baud-rate generators. The FPGA fabric allows complete customization of the UART features, including frame format, baud rate, and error-checking mechanisms. Once the design is written, it is verified through RTL simulation to ensure correct timing and functionality. After successful simulation, the UART mod-

ule is synthesized and programmed onto the FPGA board, enabling real-time serial communication with external devices. This implementation provides a deeper understanding of digital communication and flexible hardware design.

### 2.2.1 Verilog Module Structure

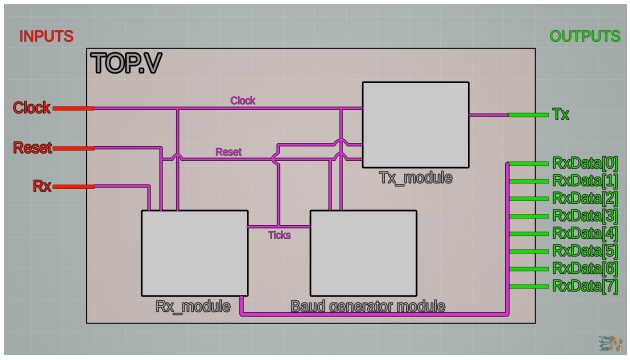


Figure 2.4: UART Module Structure

UART on an FPGA is implemented by dividing the design into separate modules: a Baud Generator, a Transmitter (Tx), and a Receiver (Rx). The Baud Generator creates timing ticks based on the system clock to ensure accurate serial data rate. The Tx module sends data bits serially according to the UART frame format, while the Rx module samples the incoming serial data and reconstructs the 8-bit parallel output. All modules are connected inside the TOP module with shared clock, reset, and baud ticks signals. The design allows reliable full-duplex UART communication on FPGA hardware.

### 2.2.2 Test Bench

The test bench is designed to verify the UART implementation by simulating clock generation, reset conditions, data transmission, and reception. A loopback mechanism is used in which the transmitted data (Tx) is directly fed back to the receiver input (Rx), allowing complete end-to-end validation without external hardware. The test bench sends multiple bytes sequentially and waits for both transmission and reception to complete before sending the next byte. It also monitors internal handshaking signals like `TxDone` and `RxDone` to ensure accurate timing with the baud generator.

Listing 2.1: UART Test Bench Code

```
`timescale 1ns/1ps

module TOP_tb;

    reg Clk;
    reg Rst_n;
    reg [7:0] TxData;
    reg TxEn;
    wire Tx;
    wire [7:0] RxData;
    reg Rx;

    // Instantiate TOP
    TOP uut (
        .Clk(Clk),
        .Rst_n(Rst_n),
        .Rx(Rx),
        .Tx(Tx),
        .RxData(RxData),
        .TxData(TxData),
        .TxEn(TxEn)
    );

    // Clock generation: 50MHz
    initial Clk = 0;
    always #10 Clk = ~Clk;  // 20ns period

    // Loopback TX -> RX
    always @(posedge Clk) begin
        Rx <= Tx;
    end

    // Test procedure
    initial begin
        Rst_n = 0;
        TxData = 8'h00;
        TxEn = 0;
        #100;
        Rst_n = 1;
        #100;

        // Send bytes one by one
```

```
43          send_byte(8'h25);
44          send_byte(8'h3A);
45          send_byte(8'h5F);
46          send_byte(8'h71);
47
48          #5000000;  // wait for last byte
49          $finish;
50      end
51
52      // Task to send a byte respecting UART timing
53      task send_byte(input [7:0] data);
54          integer wait_cycles;
55          begin
56              @(posedge Clk);
57              TxData <= data;
58              TxEn <= 1'b1;
59              @(posedge Clk);
60              TxEn <= 1'b0;
61
62              // Wait until TX is done
63              wait(uut.I_RS232TX.TxDone == 1);
64
65              // Wait until RX is done
66              wait(uut.I_RS232RX.RxDone == 1);
67
68              // Extra delay before next byte
69              wait_cycles = 1000;
70              repeat(wait_cycles) @(posedge Clk);
71
72              // Display result
73              $display("TX: %h, RX: %h at time %0t",
74                       data, RxData, $time);
75          end
76      endtask
77
78  endmodule
```

### 2.2.3 RTL Simulation Waveforms

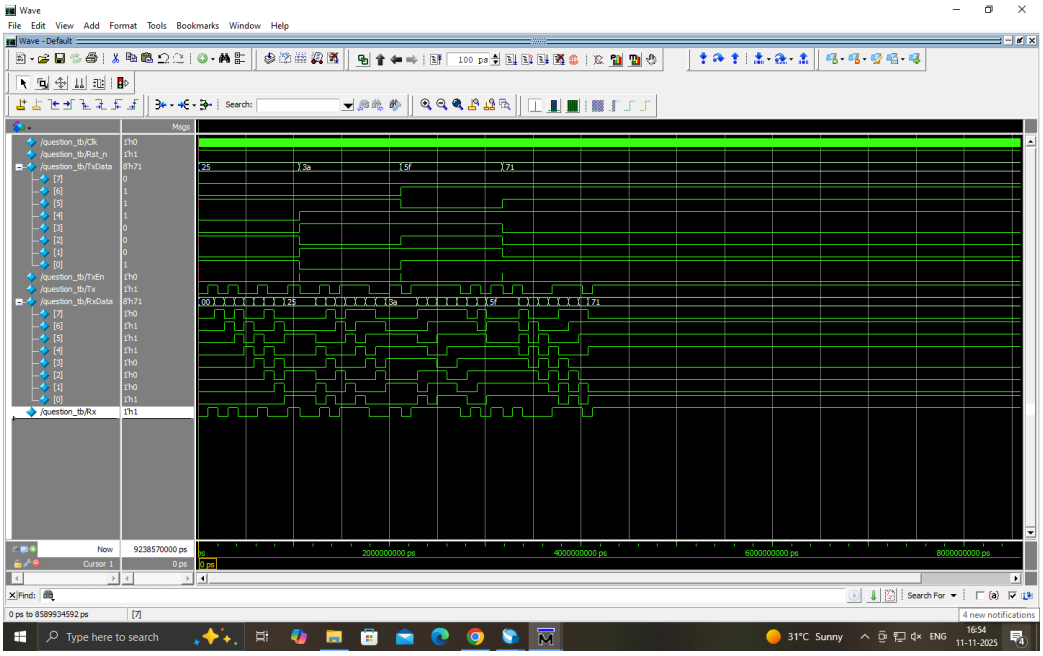

Figure 2.5: Simulation Waveform

#### Observation

During simulation, it was observed that transmitting one bit at 9600 baud takes approximately 104 us for a complete 10-bit UART frame, which includes the start bit, 8 data bits, and the stop bit. For a sequence of 10 such frames, the total transmission time measured from the waveform was approximately 1040 us. This matches closely with the theoretically expected duration, confirming that the baud-rate generator and UART timing are functioning accurately at 9600 baud.

### 2.2.4 Synthesis on Altera DE01 SOC Board

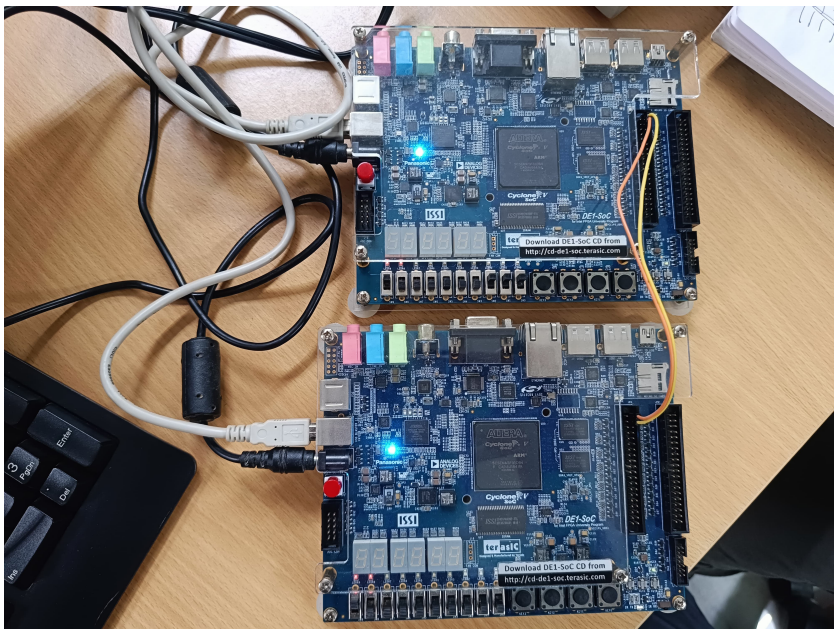


Figure 2.6: Zero Data

In Figure 2.6, the waveform displays the transmission of the byte `0x00` from the transmitter and its correct reception at the receiver.

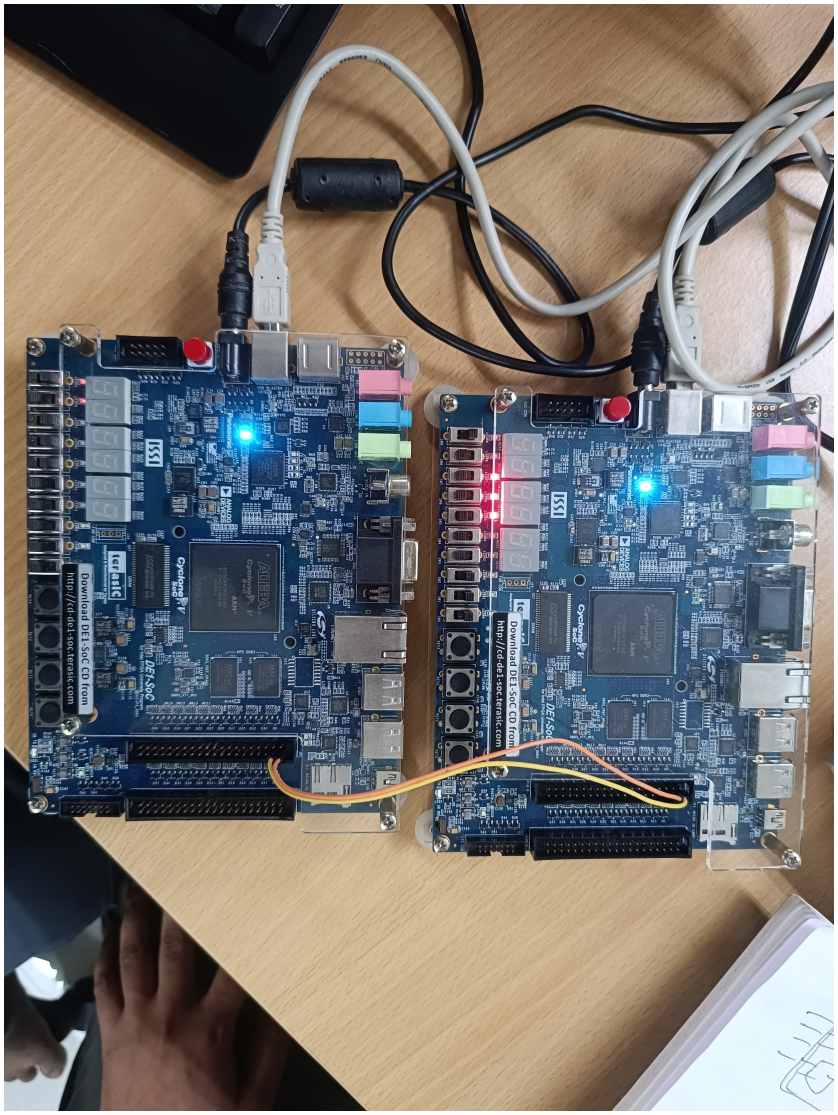

Figure 2.7: E0h Data

In Figure 2.7, the waveform displays the transmission of the byte `0xE0` from the transmitter and its correct reception at the receiver.

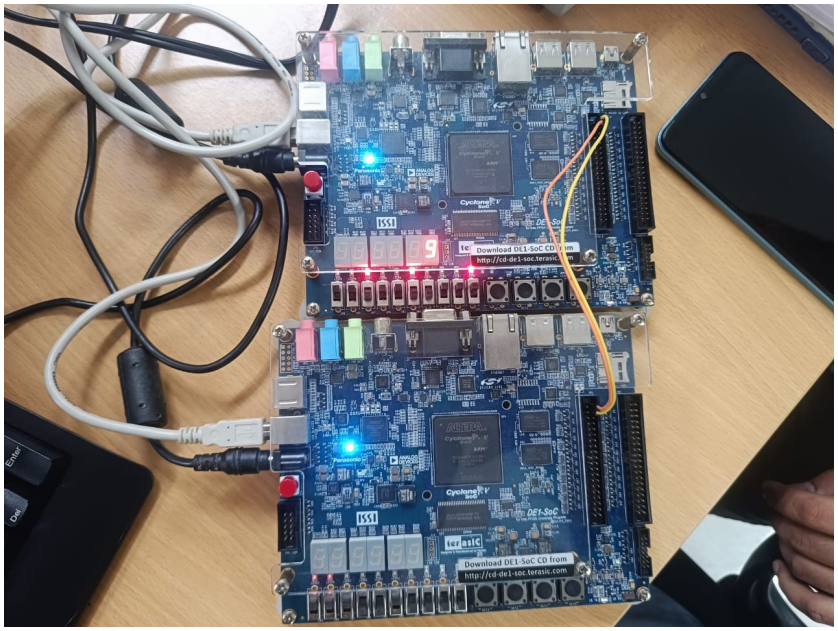


Figure 2.8: Nine Data

In Figure 2.8, the waveform displays the transmission of the byte `0x90` from the transmitter and its correct reception at the receiver.

# Chapter 3

# Future Work

In the future, the UART module can be extended to support more advanced communication architectures. One promising direction is implementing master–multiple-slave UART communication by integrating an address-based framing mechanism. This would allow the master device to selectively communicate with different slave modules on the same serial line, reducing wiring complexity and enabling scalable system expansion. Additionally, features such as multi-drop RS-485 support, error detection (parity/CRC), configurable baud-rate generation, and FIFO buffering can be incorporated to improve reliability and performance in larger embedded networks.

Another potential area for future improvement is increasing the communication speed of the UART module. Although the current implementation operates at lower baud rates such as 9600 bps for reliability, the system can be enhanced to support higher baud rates like 115200 bps or beyond. This would significantly improve data throughput and reduce transmission latency. Achieving higher speed may require optimizing the baud-rate generator, improving timing accuracy, and integrating oversampling techniques to maintain stability. With these enhancements, the UART system can handle faster data exchange while still ensuring robust and error-free communication.

# Chapter 4

# Conclusion

- The project involved designing and implementing a complete UART communication system using FPGA hardware.
- Initial study focused on understanding the UART protocol, including the transmitter (TX), receiver (RX), and baud-rate generator modules.
- RTL simulations were performed to verify correct data framing, sampling accuracy, timing behavior, and proper transmission and reception of data.
- The UART design was synthesized and implemented on FPGA boards for practical validation.
- Two separate FPGA boards were used—one configured as the transmitter and the other as the receiver—to establish real point-to-point communication.
- Hardware results confirmed that all transmitted data from the TX FPGA were correctly received by the RX FPGA without errors.
- These results demonstrate the correctness, stability, and reliability of the implemented UART system.
- The project successfully covered the full workflow, from protocol study and Verilog design to simulation, synthesis, and hardware verification.

# References


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