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Amirali Sharifian

Education

2017– **Ph.D. in Computing Science**, *Simon Fraser University*, Canada.
Supervisor: Dr. Arrvindh Shriraman

2014–2016 **M.Sc. in Computing Science**, *Simon Fraser University*, Canada, *3.72/4*.
Supervisor: Dr. Arrvindh Shriraman
Thesis: Specialized Macro-Instructions for Von-Neumann Accelerators
Courses: Machine Learning, Computer Architecture, VLSI system design.

2009–2014 **B.Sc. in Computer Engineering**, *Isfahan University of Technology*, Iran, *17.49/20*.
Supervisor: Dr. Shadrokh Samavi
Thesis: Fast Watermarking for Digital Content Protecting using GPUs

Publications

2016 **CHAINSAW: Creating Von-Neumann Accelerators with Fused Instruction Chains** .
Amirali Sharifian, Snehasish Kumar, Apala Guha, and Arrvindh Shriraman, In Proc. of the 49th Intl. Symposium on Microarchitecture, (MICRO) , 2016.

Peruse and Profit : Estimating the Accelerability of Loops .
Snehasish Kumar, Vijayalakshmi Srinivasan, Amirali Sharifian, Nick Sumner and Arrvindh Shriraman, In Proceedings of the 30th ACM International Conference on Supercomputing , ICS 2016.

2013 **An Energy-Efficient Clustering Algorithm for Large Scale Wireless Sensor Networks**.
Maryam Soleimani, Amirali Sharifian, and Ali Fanian, The 21st Iranian Conference on Electrical Engineering (ICEE 2013).

Research Projects

2016 • **Specialized Macro-Instructions for Von-Neumann Accelerators**
My research focuses on improving resource utilization in hardware accelerators using specialized macro-instructions. The proposed architecture uses fetching and decoding macro-instructions from the instruction buffer to reuse function units. However, the macro-instructions can adapt themselves to different program behaviors by varying the length and type of the instructions that are fused into macro-instruction. Overall energy consumption was reduced with comparable performance. We realsed *CHAINSAW* simulator and LLVM framework to extract macro-instructions as an open-source project.
Publication: ***MICRO'16***

2016 • **Peruse and Profit : Estimating the Accelerability of Loops**
Peruse is an LLVM-based static program analysis framework, to characterize key accelerator-oriented featureswithin the loop nests of applications. My responsibility included demonstrating the extensibility of Peruse by using LegUp (LLVM frame-work translating C to Verilog targeting FPGAs) to generate synthesizable Verilog. Additionally, I analyzed workloads to find target functions, collected and extend workloads data and also I analyzed the whole infrastructure. The entire workflow was automated using Python and shell scripting in Bash.
Publication: ***ICS'16***

2015 • **Vertical Hamming Distance**
Vertical Hamming Distance (VHD) is an SIMD friendly approach exploiting the parallelism available at the bit level while aligning DNA sequencing.
For this project I used a well-known fast aligner, MrsFAST, which is based on seed-and-extend algorithm and I replaced aligning function with VHD-SIMD. The results show performance improvement in computing mismatches between sequences.

2015 • **Specialized Hardware for Data Partitioning Algorithms**
For this project I looked at various approaches to improve performance and energy of state-of-the-art accelerators used for data partitioning algorithms, and propose various accelerator micro architecture, using data dependence graphs to manage data locality in caches, and improve scheduling.

2014 • **Fast Watermarking for Digital Content Protecting using GPUs**
The project involved improvement of image watermarking algorithms performance using GPU. Image watermarking uses image transformations such as DCT, DWT and Contourlet to extract the information from a source image and then embedding the information into a target image. The project consists parallel implementation of both steps on GPU. For the first step I implemented mentioned image transformations on GPU and then for the second step I improved embedding run-time performance using parallel algorithms.

2013 • **Designing Xilinx In-System Programming board**
The project involved the development of an Embedded Micro-controller for programming CPLD, FPGA, and configuration PROM families
In this project I used an embedded processor to program CPLDs and FPGAs from an onboard RAM or EPROM. Using this board designers can easily upgrade, modify, and test designs, even in the field.

Work Experience

2016 Teaching Assistance: Parallel and Distributed Systems, Operating Systems

2014–2016 Research Assistance: SYNAR Group, Simon Fraser University

Summer 2012 Research Intern: HDIP Lab, IUT University

Awards

2017 • Computing Science Graguate Fellowship, Simon Fraser University.

2016 • Graduate Fellowship, NSERC.
• Computing Science Travel Award, Simon Fraser University.

2015 • Graduate Fellowship, Simon Fraser University
• Graduate Fellowship, NSERC
• Travel and Minor Research Award, Simon Fraser University

Technical skills

Languages C/C++11, Scala, Python, Verilog/VHDL

Kernel Linux, Android

Infrastructure LLVM Compiler Infrastructure, Intel Pin

Design Tools Modelsim, Vivado, Design Compiler