NI 6731/6733 Specifications

このドキュメントの日本語版については、ni.com/manuals を参照してください。 (For a Japanese language version, go to ni.com/manuals.)

This document lists the specifications for the NI 6731/6733 analog output devices. The following specifications are typical at 25 °C unless otherwise noted.



Note With NI-DAQmx, National Instruments has revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ terminal names and their NI-DAQmx equivalents, refer to the *Terminal Name Equivalents* section of Chapter 2, *I/O Connector*, of the *Analog Output Series User Manual*.

Analog Output

Output Characteristics

Number of channels

NI 6731	. 4 voltage outputs
NI 6733	. 8 voltage outputs

Max update rate

	Max Update Rate		
Number of Channels	Using Local FIFO (kS/s)*	Using Host PC Memory (kS/s) [†]	
1	1,000	1,000	
2	1,000	1,000	
3	1,000	1,000	
4	1,000	1,000	
5	1,000	1,000	
6	952	1,000	

	Max Update Rate			
Number of Channels	Using Local Using Host PC FIFO (kS/s)* Memory (kS/s)†			
7	833	869		
8	740	769		

* These numbers apply to continuous waveform generation, which allows for the time it takes to reset the FIFO to the beginning when cycling through it. This additional time, about 200 ns, is not incurred when using host PC memory for waveform generation. Max update rate in FIFO mode does not change regardless of the number of devices in the system.

[†] These results were measured using a PCI-6711/6713 device with a 90 MHz Pentium machine. These numbers may change when using more devices or when other CPU or bus activity occurs.

Type of DAC	Double-buffered, multiplying
FIFO buffer size	
NI 6731	8,192 samples
NI 6733	16,384 samples
DMA channels	3
Data transfers	DMA, interrupts, programmed I/O

DMA modesScatter-gather



Accuracy Information

	Absolute Accuracy				
Nominal Range at	% of Reading				
Full Scale (V)	24 Hours	90 Days	1 Year	Offset (mV)	Temp Drift (%/°C)
±10	0.0044%	0.0052%	0.0061%	±1.027	0.0006%

Absolute accuracy = $(\% \text{ of Reading} \times \text{Voltage}) + \text{Offset} + (\text{Temp Drift} \times \text{Voltage})$

Note: Temp drift applies only if ambient is greater than ± 10 °C of previous external calibration.

Transfer Characteristics

Relative accuracy (INL)

After calibration±2.2 LSB max
Before calibration±2.2 LSB max

DNL

After calibration±1.0 LSB max
Before calibration±1.0 LSB max

Offset error

After calibration±168 µV max Before calibration±40 mV max

Gain error (relative to internal reference)

After calibration±30 ppm of output max

Before calibration±9,000 ppm of output

max

Gain error (relative to

external reference)......+0.1% of output max, not adjustable

Voltage Output

Ranges±10 V, ±EXT REF

Output coupling......DC

Current drive.....±5 mA max

Output stabilityAny passive load, up to

Protection.....Short-circuit to ground

1,500 pF

Power-on state $0 \text{ V } (\pm 200 \text{ mV})$

External Reference Input

Range.....±11 V

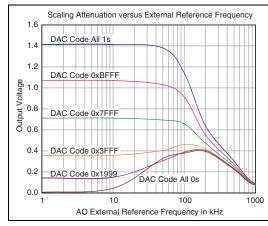
Overvoltage protection±25 V powered on, ±15 V powered off 

Figure 1. Scaling Attenuation versus External Reference Frequency

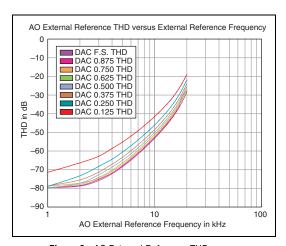


Figure 2. AO External Reference THD versus External Reference Frequency

Dynamic Characteristics Slew rate	•		Output buffer Timing I/O	2,000 bytes
Noise	•		Number of channels	2 up/down
		ating a 10 V,		counter/timers, 1 frequency scaler
10		he reference	Resolution Counter/timers	24 bits
Settling time	,	0 LSB	Frequency scaler	
	curacy	O LOD	Compatibility	TTL/CMOS
		oint, 750 Hz	Base clocks available Counter/timers	
9	harmonics)		Frequency scaler	
Stability			Base clock accuracy	±0.01% over operating temperature
Offset temperature coefficient ±	35 μV/°C		Max source frequency	•
Gain temperature coefficient			Min source pulse duration	10 ns, edge-detect mode
Internal reference± External reference±			Min gate pulse duration	10 ns, edge-detect mode
Onboard calibration reference			Data transfers	DMA, interrupts,
Level5.				programmed I/O
va Temperature coefficient±		n EEPROM)	DMA modes	Scatter-gather
Long-term stability ±			Triggers	
Digital I/O			Digital Trigger	
Number of channels 8	input/outpu	ıt	Purpose	Start triagger gate algebr
CompatibilityT	TL/CMOS		Analog output Counter/timers	
Digital logic levels			Source	PFI <09>
Level	Min	Max	Compatibility	TTL
Input low voltage	0 V	0.8 V	Response	Rising or falling edge
Input high voltage	2.0 V	5.0 V	Pulse width	10 ns min
Input low current $(V_{in} = 0 V)$	_	–320 μΑ	RTSI Bus (PCI Only)	
Input high current $(V_{in} = 5 V)$	_	10 μΑ	Trigger lines <06>	7
Output low voltage ($I_{OL} = 24 \text{ mA}$)	_	0.4 V	RTSI clock	1
Output high voltage ($I_{OH} = -13 \text{ mA}$)	4.35 V	_	PXI Trigger Bus (PXI Only)	
Power-on stateIr	put (high-i	mpedance)	Trigger lines <05>	6
Data transfers D	1		Star trigger	1
	ogrammed		Clock	1

Input buffer2,000 bytes

Bus Interface

NI PCI-6731/6733	5 V PCI master, slave
NI PXI-6733	PXI/CompactPCI master,
	slave

Power Requirement

NI	673	1

+5 VDC (±5%)	0.80 A typ, 1.25 A max
+3.3 VDC (±5%)	125 mA typ, 250 mA max
Power available at	
I/O connector	+4.65 to +5.25 VDC at
	1 A
NI 6733	
+5 VDC (±5%)	1.25 A typ, 1.8 A max
+3.3 VDC (±5%)	125 mA typ, 250 mA max
Power available at	
I/O connector	+4.65 to +5.25 VDC at
	1 A

Physical

Dimensions (not including connectors)

NI PCI-6731/6733	17.5 × 10.7 cm
	$(6.87 \times 4.2 \text{ in.})$
NI PXI-6733	16 × 10 cm
	$(6.3 \times 3.9 \text{ in.})$
I/O connector	68-pin male SCSI-II type

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth	±11 V, Installation
	Category I
Channel-to-channel	±22 V, Installation
	Category I

Environmental

Pollution Degree2



Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label, or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A



Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)



Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

Device Pinouts

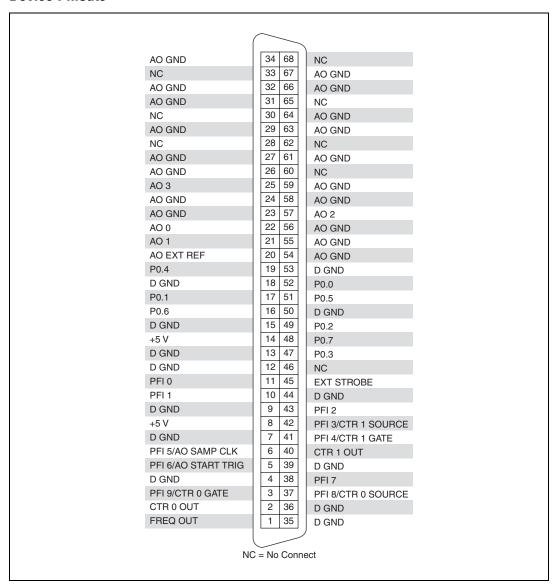


Figure 3. NI 6731 68-Pin AO I/O Connector Pin Assignments

		_		
AO OND	[24		NO	
AO GND	34	-	NC ACCUR	
NC AC OND	33	\vdash	AO GND	
AO GND	32		AO GND	
AO GND	31	_	AO 7	
AO 6	30	_	AO GND	
AO GND	29	-	AO GND	
AO 5	28	_	NC	
AO GND	27	_	AO GND	
AO GND	26	_	AO 4	
AO 3	25	59	AO GND	
AO GND	24	58	AO GND	
AO GND	23	57	AO 2	
AO 0	22	56	AO GND	
AO 1	21	55	AO GND	
AO EXT RE	F 20	54	AO GND	
P0.4	19	53	D GND	
D GND	18	52	P0.0	
P0.1	17	51	P0.5	
P0.6	16	50	D GND	
D GND	15	49	P0.2	
+5 V	14	48	P0.7	
D GND	13	47	P0.3	
D GND	12	46	NC	
PFI 0	11	45	EXT STROBE	
PFI 1	10	44	D GND	
D GND	9	43	PFI 2	
+5 V	8	42	PFI 3/CTR 1 SOURCE	
D GND	7	41	PFI 4/CTR 1 GATE	
PFI 5/AO S	AMP CLK 6	40	CTR 1 OUT	
PFI 6/AO S		39	D GND	
D GND	4	38	PFI 7	
PFI 9/CTR		37	PFI 8/CTR 0 SOURCE	
CTR 0 OUT		36	D GND	
FREQ OUT		35	D GND	
. ALG OUT		رتت		
	NC = No	Conn	ect	

Figure 4. NI 6733 68-Pin AO I/O Connector Pin Assignments

National Instruments, NI, ni.com, and LabVIEW are trademarks of National Instruments Corporation. Refer to the *Terms of Use* section on ni.com/legal for more information about National Instruments trademarks. Other product and company names mentioned herein are trademarks or trade names of their respective companies. For patents covering National Instruments products, refer to the appropriate location: **Help»Patents** in your software, the patents.txt file on your CD, or ni.com/patents.