		GENERAL BUS LAYOUT						
A-row				C-row				
1		GND		1		GND		
2		GND		2		GND		
3		AUX#1		3		AUX#2		
4		$\overline{\text{B\_SYS}}$		4		$\overline{\text{XFEXX}}$		
5		DATA 0		5		DATA 1		
6		DATA 2		6		DATA 3		
7		DATA 4		7		DATA 5		
8		DATA 6		8		DATA 7		
9		ADDRESS 0		9		ADDRESS 1		
10		ADDRESS 2		10		ADDRESS 3		
11		ADDRESS 4		11		ADDRESS 5		
12		ADDRESS 6		12		ADDRESS 7		
13		ADDRESS 8		13		ADDRESS 9		
14		ADDRESS 10		14		ADDRESS 11		
15		ADDRESS 12		15		ADDRESS 13		
16		ADDRESS 14		16		ADDRESS 15		
17		ADDRESS 16		17		ADDRESS 17		
18		ADDRESS 18		18		ADDRESS 19		
19		GND		19		GND		
20		E CLOCK		20		R/$\overline{\text{W}}$		
21		$\overline{\text{RESET}}$		21		$\overline{\text{VMA}}$		
22		BS		22		BA		
23		Q CLOCK		23		AUX#5		
24		R/$\overline{\text{W}}$ DMA(IN)		24		MRDY		
25		$\overline{\text{HALT}}$		25		$\overline{\text{BREQ}}$		
26		$\overline{\text{FIRQ}}$		26		$\overline{\text{IRQ}}$		
27		$\overline{\text{NMI}}$		27		$\overline{\text{VMA}}$_DMA(IN)		
28		AUX#6		28		AUX#7		
29		SIGNAL#1		29		SIGNAL#1		
30		SIGNAL#2 (SIG30)		30		SIGNAL#2 (SIG30)		
31		+5V		31		+5V		
32		+5V		32		+5V		
Note:		SIGNAL#1 and SIGNAL#2 may be used to pass +12V/-12V/+3V3						
		or master BAUD clock over the bus						
		Signals Aux#x are per backplane slot defineable						
		Be careful when you have a mix of these signals on the backplane!!						

		BOARD SPECIFIC wiring					
		CPU CARD					
A-row				C-row			
4		B_SYS	X	4		XFEXX	
				23		RESET_IN	
		MONITOR CARD					
3		SELECT_F100-F17F(DIV5)		3		SELECT_F180-F1FF(DIV6)	
4		B_SYS		4		XFEXX	
				23		SELECT_F080-F0FF(DIV4)	
28		SELECT_F008-F07F(DIV3)	X	28		SELECT_F200-F3FF(DIV7)	
30		SIGNAL#2 (614.4kHz)		30		SIGNAL#2 (614.4kHz)	
		IDE CARD					
				23		SELECT_IN	
		4 PORT SERIAL					
				23		SELECT_IN	
30		SIGNAL#2 (614.4kHz)		30		SIGNAL#2 (614.4kHz)	
		SPI INTERFACE					
		IOP					
				23		SELECT_IN	
29		SIGNAL#1		29		SIGNAL#1	
30		SIGNAL#2 (614.4kHz)		30		SIGNAL#2 (614.4kHz)	
		TIMER CARD					
				23		SELECT_IN	
30		SIGNAL#2 (614.4kHz)		30		SIGNAL#2 (614.4kHz)	