Quick guide for “nut8nt_8chs”

For this project you need to use Vivado 2018.3 version.

The project consists of three main parts: top.v, ads5292_interface, design_1_wrapper.

top.v – the main top file of the project. It unites module of input interface of ads and block design module.

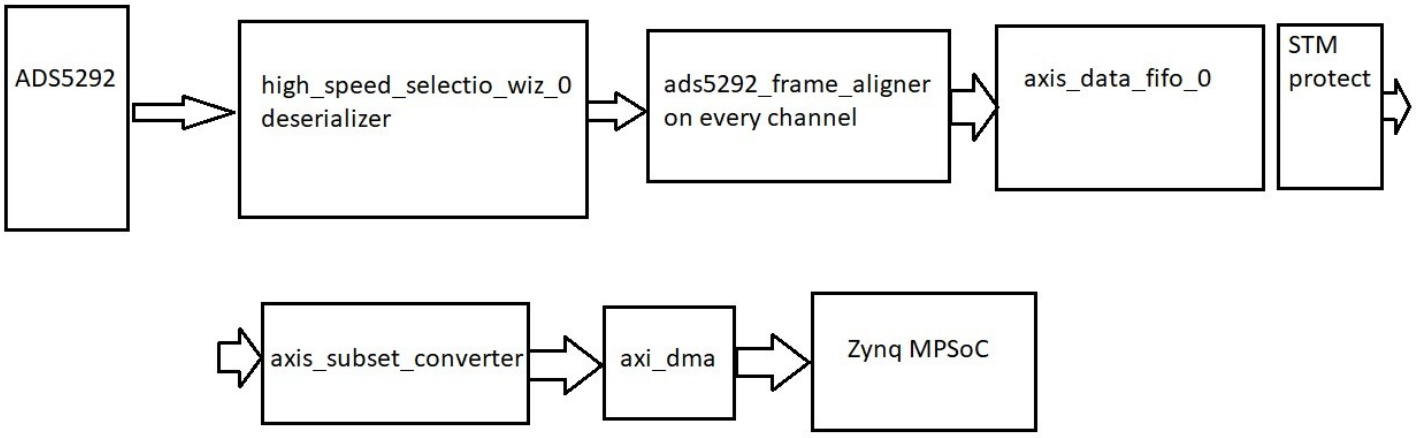
ads5292_interface.v – the module that include first stage interface for input data from ads.

design_1_wrapper.v – the module that include block design of processor and other peripherals ip cores.

The Data flow

Data go to next stages:

pic. 1



The data come from adc and go to high_speed_selectio_wiz_0 ip core. Then it goes to ads5292_frame_aligner, where the data lines will be synchronized. When the synchronization is completed, axis_data_fifo will begin to accumulate data. Next stages depend on soft application on Zynq. App should make read operation through DMA channel and receive data packet from fifo.

Implementation project

If you want to make changes in the project or test your new project you should do next:

1. Make change and save the project
2. You should do “run synthesis”, “run implementation” and “generate bitsteam”. Project need to complete without errors!
3. Next you need export file project to “hdf” format. Go to “File > Export > Export hardware”. Check “include bitstream” and click “Ok”.
4. In your project, open folder “sdk” (for example: nut8nt_amga_8chs\nut8nt_amga.sdk). You can see hdf file of current project (top.hdf). It file is needed for build petalinux project.