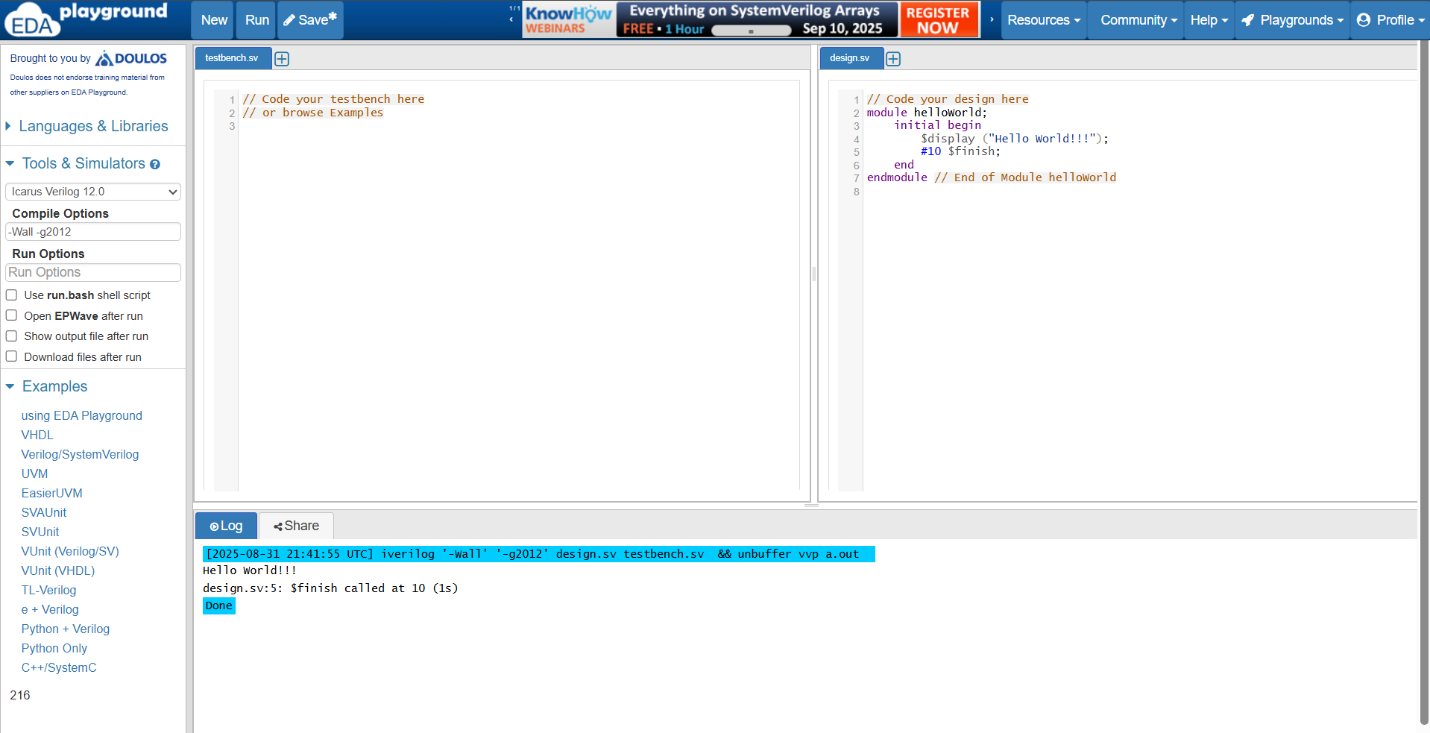
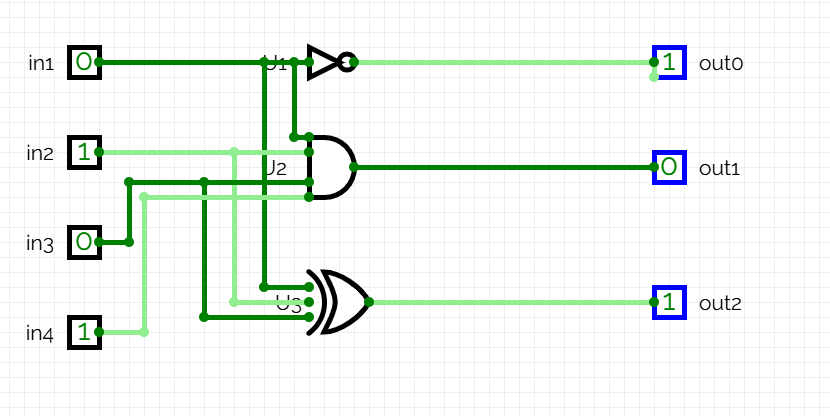
Assignment 1

Ashmitha Murali

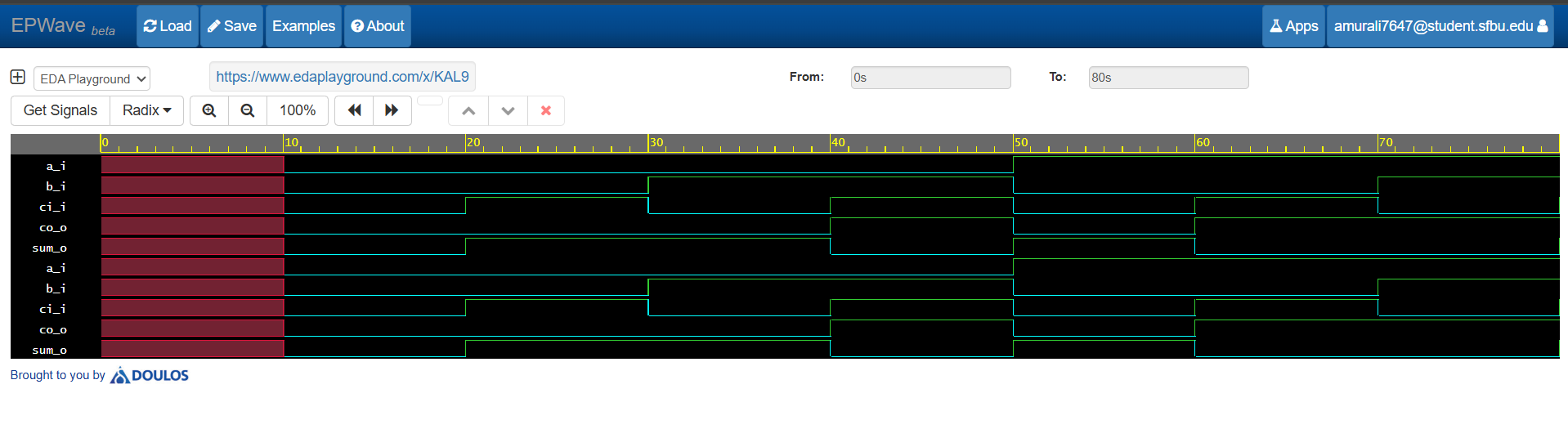
Prof. Alex Yang

Verilog HDL Lab E461L

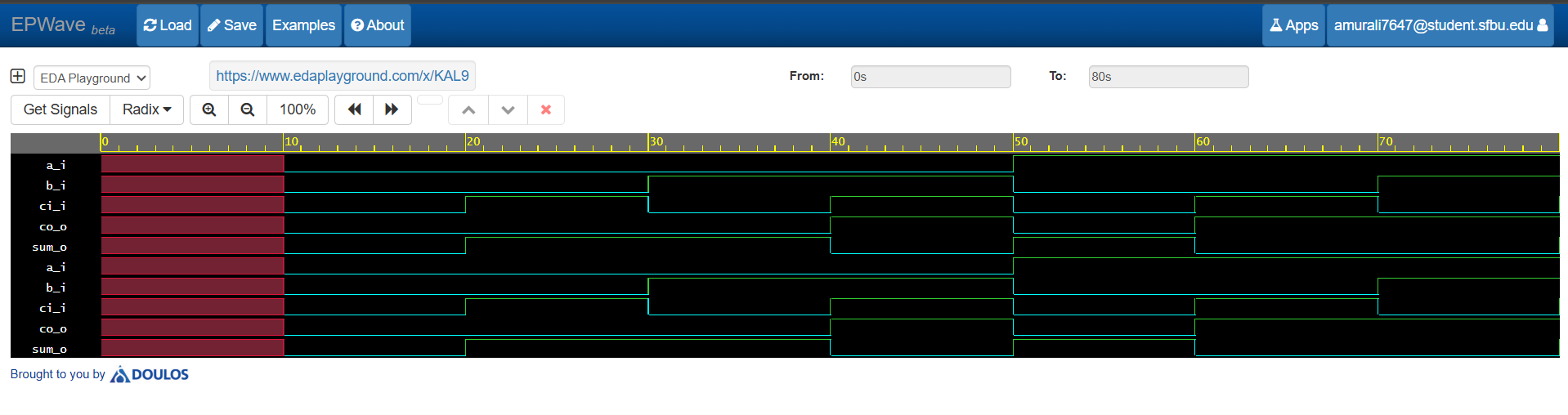
2nd September 2025

1. Directly run the module helloWorld in the online compiler  
   
2. Based on the module gates, draw the digital circuit schematic.  
   
3. Create the testbench first, and then simulate the design modules oneBitFA1,  
   oneBitFA2, DFFSynch, and DFFAsynch

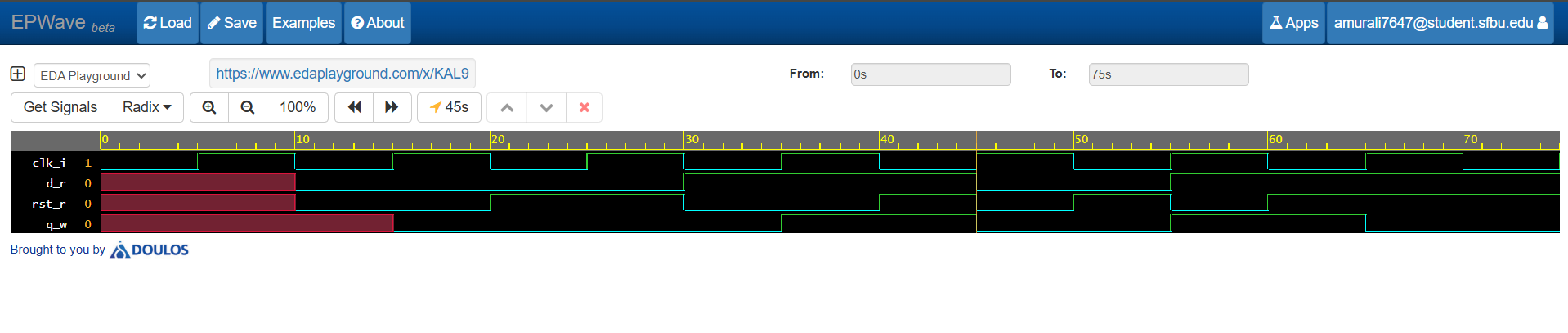
* I have uploaded the Testbench files to GIT. Below are the waveforms for the Testbench simulations:
  + oneBitFA1



* + oneBitFA2



* + DFFSynch



* + DFFAsynch

