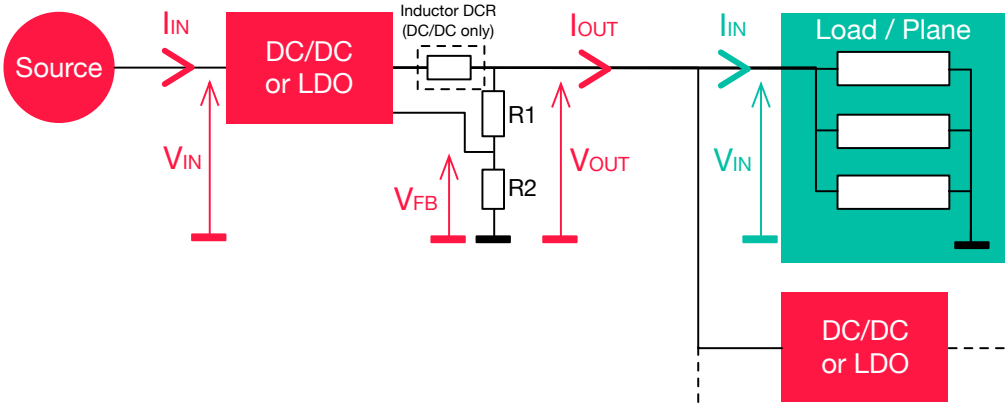
Summary of equations for electrical characteristics of DC/DC, LDO and power planes (loads).

Characteristic	LDO	DC/DC (step down)	Perfect	Dummy	Resistive Element	Power plane / Load
V_{IN}	$V_{OUT\ SOURCE}$					
I_{IN}	$I_{OUT} + I_Q$	$\frac{P_{IN}}{V_{IN}}$		I_{OUT}		$\sum_{PART}^{PART} I_{PART}$
P_{IN}[1]	$V_{IN} \times I_{IN}$	$\frac{P_{OUT}}{Efficiency}$	P_{OUT}	$V_{IN} \times I_{IN}$		
$V_{OUT\ (FIXED)}$	V_{OUT}			V_{IN}	$V_{IN} - I_{OUT} \times R$	N/A
$V_{OUT\ TYP\ (ADJ)}$	$V_{REFTYP} \cdot \left(1 + \frac{R_{1\ TYP}}{R_{2\ TYP}}\right)$		N/A			
$V_{OUT\ MAX\ (ADJ)}$	$V_{REFMAX} \cdot \left(1 + \frac{R_{1\ MAX}}{R_{2\ MIN}}\right)$					
I_{OUT}	$\sum_{CHILD}^{CHILD} I_{IN\ CHILD}$					
P_{OUT}[1]	$V_{OUT} \times I_{OUT}$					
PLOSS	$P_{IN} - P_{OUT}$		0		$R \times I_{OUT}^2$	N/A
Efficiency[2]	$\frac{P_{OUT}}{P_{IN}}$	$f(I_{OUT})$	1		$\frac{P_{OUT}}{P_{IN}}$	N/A



(1) Input and output maximum power are computed with maximum voltage and maximum current. Special attention should be paid when components and loads current are only expressed with typical voltage in their datasheet. In some case, higher voltage may result in a lower current. This wont be

(2) Planes and wires/nets are considered as perfect. In reality, a voltage drop should be considered between the regulator output and the load because of the copper resistance. Especially if the current is hight (CPU cores, for example) and the feedback is close to the regulator. DC/DC inductors also have a parasitic resistance. All of those reduce the efficiency.