PrimeTime® Suite Quick Reference

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SYNOPSYS®

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Contents

Getting Help

PrimeTime provides various forms of online help.

- The help command provides you with quick help for one or more commands or procedures.
- The man command displays the man page.

You can use a wildcard pattern as the argument for the help command. The wildcard characters are

*	Matches n characters.
?	Matches exactly one character.

Accessing Brief Help

Use this command to list all commands by function group:

```
pt_shell> help
```

Use this command to display all commands that end with the word clock:

```
pt_shell> help *clock
```

Use this command to get syntax help for one or more commands:

```
pt_shell> help -verbose cmd_name_pattern
```

Use this command to get syntax help for a specific command:

```
pt_shell> command_name -help
```

Man Page Viewing Instructions

The following sections describe how to set up your environment and the syntax to use to view man pages.

Setting Up the UNIX Environment

Edit your .cshrc file to contain these lines:

```
setenv pt_MAN_DIR synopsys_root/doc/pt/man
setenv MANPATH ${MANPATH}:${pt_MAN_DIR}
```

pt_MAN_DIR is a variable that contains the path to the man page directories, and *synopsys_root* represents the specific path to the Synopsys software directory at your site.

Viewing Man Pages From UNIX

Command

```
% man command_name
```

Variable

```
% man variable_name
```

Error, warning, or information message

```
% man message_id
```

Viewing Man Pages From pt_shell

Command

```
pt_shell> man command_name
```

Variable

```
pt_shell> man variable_name
```

Error, warning, or information message

```
pt_shell> man message_id
```

User Commands

Invoke user commands from a UNIX shell.

primetime

Runs the PrimeTime GUI.

```
primetime
[-f file_name]
[-no_init]
[-version]
```

pt_shell

Runs the PrimeTime command shell.

```
pt_shell
[-f file_name]
[-gui]
[-display display_env_var]
[-x command_string]
[-no_init]
[-version]
```

transcript

Runs transcript, which translates dc_shell scripts to PrimeTime scripts.

```
transcript
dc_script pt_script
[-source_for_include]
[-no_script_warnings]
[-no_init]
```

PrimeTime Commands

Invoke these commands from within the PrimeTime tool.

add_distributed_hosts

Add one or more distributed hosts for distributed jobs.

```
int add_distributed_hosts
[-32bit]
-farm lsf | grd | generic | now
[-setup_path setup_path]
[-num_of_hosts count]
[-options string]
[-submission_script submission_script]
[hostname]
```

add_to_collection

Adds objects to a collection, resulting in a new collection. The base collection remains unchanged.

```
collection add_to_collection
base_collection
object_spec
[-unique]
```

add_variation

Sums two or more variations. Returns a collection that corresponds to this sum variation.

```
collection add_variation
variation_list
```

alias

Creates a pseudo-command which expands to one or more words, or lists current alias definitions.

```
string alias [name] [def]
```

all_clocks

Creates a collection of all clocks in the current design. You can assign these clocks to a variable or pass them into another command.

```
collection all_clocks
```

all_connected

Creates a collection of objects connected to a net, pin, or port object. You can assign this collection to a variable or pass it into another command.

```
collection all_connected
object_spec
[-leaf]
```

all_correlations

Creates a collection of all correlations in the current design. You can assign these correlations to a variable or pass them into another command.

```
collection all_correlations
```

all_fanin

Creates a collection of pins/ports or cells in the fanin of specified sinks.

```
collection all_fanin
-to sink_list
[-flat] [-only_cells]
[-startpoints_only]
[-levels level_count]
[-pin_levels pin_count]
[-trace_arcs arc_types]
[-step_into_hierarchy]
```

all_fanout

Creates a collection of pins/ports or cells in the fanout of the specified sources.

```
collection all_fanout
-from source_list
-clock_tree [-flat]
[-only_cells] [-endpoints_only]
[-levels level_count]
[-pin_levels pin_count]
[-trace_arcs arc_types]
[-step_into_hierarchy]
```

all_inputs

Creates a collection of all input ports in the current design. You can assign these ports to a variable or pass them into another command.

```
collection all_inputs [-level_sensitive]
[-edge_triggered]
[-clock clock_name]
```

all_instances

Creates a collection of all instances of a specific design or library cell in the current design, relative to the current instance. You can assign the resulting collection of cells to a variable or pass it into another command.

```
collection all_instances
[-hierarchy]
object_spec
```

all_outputs

Creates a collection of all output ports in the current design. You can assign these ports to a variable or pass them into another command.

```
collection all_outputs
[-level_sensitive]
[-edge_triggered]
[-clock clock_name]
```

all_registers

Creates a collection of register cells or pins. You can assign the resulting collection to a variable or pass it into another command.

```
collection all_registers
[-clock clock_name]
[-rise_clock rise_clock_name]
[-fall_clock fall_clock_name]
```

all_variations

Creates a collection of all variations in the current design. You can assign these variations to a variable or pass them into another command.

```
collection all_variations
```

append_to_collection

Add objects to a collection. Modifies variable.

```
collection add_to_collection
var_name
object_spec
[-unique]
```

apropos

Searches the command database for a pattern.

```
string apropos
[-symbols_only]
pattern
```

cell_of

Creates a collection of cells of the given pins. The cell_of command is a DC Emulation command provided for compatibility with Design Compiler.

```
string cell_of
object_list
```

change_selection

Changes the selection in the GUI.

```
int change_selection
[-name slct_bus]
[-replace (default) ]
[-add ]
[-remove ]
[-toggle ]
[-type object_type]
[-clock_trees clock_tree_list]
[collection]
```

characterize_context

Captures the timing context of a list of instances.

```
string characterize_context
[-timing] [-environment]
[-design_rules]
[-constant_inputs]
[-no_boundary_annotations]
cell_list
```

check_block_scope

Checks the scope of hierarchical blocks that were replaced with timing models during the top-level analysis.

```
int check_block_scope
-instances instance_list
[-scope_scenario scenario_name]
[-check_types chk_types]
[-significant_digits digits]
[-absolute_clock_arrival]
[-nosplit]
[-verbose]
file_name
```

check_level_shifter

Alias for the check_timing -override_defaults {signal level}.

```
int check_level_shifter [-verbose]
```

check_noise

Performs checking whether there are necessary data available to run the update_noise command.

```
int check_noise
[-verbose]
[-nosplit]
[-beyond_rail]
[-include check_options]
```

check_power

Shows possible power problems for design.

```
string check_power
[-verbose]
[-significant_digits digits]
[-override_defaults check_list]
[-include check_list]
[-exclude check_list]
```

check_timing

Shows possible timing problems for design.

```
string check_timing
[-verbose]
[-significant_digits digits]
[-ms_min_separation delta]
[-override_defaults check_list]
[-include check_list]
[-exclude check_list]
```

compare_collections

Compares the contents of two collections. If the same objects are in both collections, the result is "0" (like string compare). If they are different, the result is nonzero. The order of the objects can optionally be considered.

```
int compare_collections
[-order_dependent]
collection1 collection2
```

compare_interface_timing

Compares two write_interface_timing reports.

```
int compare_interface_timing
ref_timing_file
cmp_timing_file
[-output file_name]
[-absolute_tolerance atol_list]
[-percent_tolerance ptol_list]
[-capacitance_tolerance ctol_list]
[-noise_tolerance ntol_list]
[-ignore ign_list]
[-include cmp_list]
[-quiet]
[-nosplit]
[-sort_by_worst]
[-session session_name]
[-significant_digits digits]
```

complete_net_parasitics

Completes partial parasitics annotated on all nets of the current design.

```
string complete_net_parasitics
 [-complete_with completion_type]
```

connect_net

Connects a net to specified pins or ports.

```
int connect_net
net object_spec
```

connect_power_domain

Connects power net information for the specified power domains.

```
int connect_power_domain
power_domains
[-primary_power_net power_net]
[-primary_ground_net ground_net]
[-backup_power_net power_net]
[-backup_ground_net ground_net]
[-internal_power_net internal_power_net]
[-internal_ground_net internal_ground_net]
```

connect_power_net_info

Connects the specified power net information to the specified power pins.

```
int connect_power_net_info
object_list
-power_pin_name power_pin_name
-power_net_name power_net_name
```

connect_supply_net

Connect the supply_net to specified supply_ports/pins. The command is part of UPF definition of virtual power and ground network.

UPF mode:

```
int connect_supply_net
supply_net_name
[-ports list]
```

copy_collection

Duplicates the contents of a collection, resulting in a new collection. The base collection remains unchanged.

```
collection copy_collection
collection1
```

cputime

Retrieves the overall user time associated with the current pt_shell process.

```
float cputime
[format]
```

create_clock

Creates a clock object.

```
string create_clock
-period period_value
[-name clock_name]
[-waveform edge_list]
[-add]
[source_objects]
```

create_command_group

Creates a new command group.

```
string create_command_group
group_name
```

create_correlation

Creates a new correlation type.

```
int create_correlation
-name correlation_name
[-constant constant_value |
-cross_correlations {float_list} |
-physical_distance {float_list}]
```

create_distributed_farm

Create a virtual distributed farm made up of hosts specified using the add_distributed_hosts command.

```
int create_distributed_farm
[-timeout seconds]
[-min_hosts num_hosts]
```

create_eco_astro_constraints

Creates ECO Astro constraints to fix crosstalk delay, static timing, or static noise.

```
int create_eco_astro_constraints
```

create_generated_clock

Creates a generated clock object.

```
string create_generated_clock
[-name clock_name]
-source master_pin
[-divide_by divide_factor | -multiply_by
multiply_factor |
 -edges edge_list ]
[-combinational]
[-duty_cycle percent]
[-invert]
[-edge_shift edge_shift_list]
[-add]
[-master_clock clock]
[-pll_output output_pin]
[-pll_feedback feedback_pin]
source_objects
```

create_ilm

Extracts interface logic model and writes it to a new directory. Also, sets the is_interface_logic_pin attribute on pins of the current design that are part of its interface logic model.

```
int create_ilm
[-script_format format]
[-instances instance_list]
[-ignore_ports port_list]
[-auto_ignore]
[-verbose]
[-ignore_boundary_pins pin_list]
[-include incl_list]
[-verification_script]
[-latch_level levels]
[-context_borrow]
[-keep_ignored_fanout]
[-include_pins pin_list]
[-critical_pins]
[-traverse_disabled_arcs]
[-parasitics_options para_options]
[-sdf_options sdf_options]
[-block_scope]
[-block_scope_only]
[-scope_scenario scenario_name]
```

create_lcd_operating_condition

Creates an LCD operating condition by using different operating conditions in the library.

```
int create_lcd_operating_condition
-op_worst
worst_case_operating_condition_name
-mult_worst worst_case_multiplier
-op_nominal nominal_operating_condition_name
-mult_nominal nominal_multiplier
-op_best best_case_operating_condition_name
-mult_best best_case_multiplier
-library library_name
name
```

create_net

Creates nets in the current design.

```
int create_net
[-exact]
net_list
```

create_operating_conditions

Creates a new set of operating conditions in a library.

```
int create_operating_conditions
-name name -library library_name
-process process_value -temperature
temperature_value
-voltage voltage_value
[-tree_type tree_type]
[-calc_mode calc_mode]
[-rail_voltages rail_value_pairs]
```

create_power_domain

Creates a power domain at the specified scope, which provides a power supply distribution network.

```
string create_power_domain
domain_name
[-elements element_list]
[-include_scope]
[-scope instance_name]
```

create_power_group

Creates a power group of cells in the current design.

```
int create_power_group
-name name
[object_list]
[-default]
```

create_power_net_info

Creates a power net.

```
int create_power_net_info
power_net_name
-power
-gnd
[-switchable]
[-nominal_voltages nominal_voltage_list]
[-voltage_ranges voltage_range_list]
```

create_power_rail_mapping

Map the power rails defined in the libraries to the physical power rails existing in the design.

```
create_power_rail_mapping
design_rail
[-lib_rail_name <rail_name>]
[-cells cell_list]
[-off_condition condition]
[-default]
```

create_power_switch

Creates a power switch at the specified power domain. This command is supported only in UPF mode.

```
string create_power_switch
switch_name
-domain domain_name
-output_supply_port {port_name
supply_net_name}
-input_supply_port {port_name
supply_net_name}
{-control_port {port_name net_name}
-on_state {state_name input_supply_port
{boolean_function}}
[-off_state {state_name {boolean_function}}*
]
[on_partial_state {state_name
input_supply_port {boolean_function}}]
[-error_state {state_name
{boolean_function}}]
[-ack_port {port_name net_name
[{boolean_function} }]}]
[-ack_delay {port_name delay}]
```

create_qtm_constraint_arc

Creates a constraint arc for a quick timing model.

```
string create_qtm_constraint_arc
[-name arc_name]
[-setup] [-hold]
-from port_name [-to port_spec]
-edge triggering_edge
[-path_type name]
[-path_factor multiplication_factor]
[-value constraint_value]
```

create_qtm_delay_arc

Creates a delay arc for a Quick Timing Model (QTM).

```
string create_qtm_delay_arc
[-name arc_name]
-from port_spec
-to port_spec
[-edge triggering_edge]
[-path_type path_type]
[-path_factor multiplication_factor]
[-value delay_value]
```

create_qtm_drive_type

Creates a drive type in a Quick Timing Model (QTM) description.

```
string create_qtm_drive_type
-lib_cell lib_cell_name
[-input_pin pin_name]
[-output_pin pin_name]
[-input_transition_rise rtrans]
[-input_transition_fall ftrans]
drive_type_name
```

create_qtm_generated_clock

Creates a QTM generated_clock.

```
string create_qtm_generated_clock
-source master_clock_name
[-divide_by divide_factor | -multiply_by
multiply_factor]
[-invert]
generated_clock_name
```

create_qtm_load_type

Creates a load type for a Quick Timing Model (QTM) description.

```
string create_qtm_load_type
-lib_cell name
[-input_pin pin_name]
<load_type name>
```

create_qtm_model

Begins the definition of a Quick Timing Model (QTM) description.

```
string create_qtm_model model_name
```

create_qtm_path_type

Creates a path type in a Quick Timing Model (QTM) description.

```
string create_qtm_path_type
-lib_cell name
[-input_pin pin_name]
[-output_pin pin_name]
[-fanout count]
<path_type name>
```

create_qtm_port

Creates a QTM port.

```
string create_qtm_port
-type port_type
port_list
```

create_scenario

Creates a scenario for multi-scenario analysis.

```
Boolean create_scenario
```

create_si_context

Generates an SI context for selected blocks of the design. A top level design and full chip binary parasitics can also be generated.

```
Boolean create_si_context
[-include include_list]
[-instances instance_list]
[-parasitics_options para_options]
[-top_inst instance_name]
[-no_design_parasitics]
```

create_supply_net

Creates a supply net defined for the specified power domain. The supply net is created in the logic hierarchy at the same scope as specified power_domain.

create_supply_port

Creates a supply port in specified power domain or in current scope if no power domain is specified.

create_variation

Creates a new variation.

```
collection create_variation
[-name variation_name]
[-parameter_name parameter_name]
-type distribution_type
-values values_list
[-unknown_type]
[-lower_bound lower_bound]
[-upper_bound upper_bound]
```

current_design

Sets or gets the current design in PrimeTime.

```
string current_design
[design_name]
```

current_instance

Sets the working instance object in pt_shell and enables other commands to be used relative to a specific instance in the design hierarchy.

```
string current_instance
[instance]
```

current_power_rail

Sets or gets the power rails in a multi-rail design to be included in power analysis. As default (if not specified), all the power rails in the design are included in power analysis. This command has no effect on single rail design.

```
int current_power_rail
[rail_name_list]
```

current_scenario

Selects a subset of the scenarios in the current session for analysis.

```
int current_scenario
[-all]
[scenario_list]
```

current_session

Selects a set of scenarios for analysis.

```
string current_session
[scenario list]
[-all]
```

date

Returns a string containing the current date and time.

```
string date
```

define_design_mode_group

Defines a design mode group with a set of design modes.

```
string define_design_mode_group
[-group_name name]
mode_list
```

define_proc_attributes

Defines attributes of a Tcl procedure, including an information string for help, a command group, a set of argument descriptions for help, and so on. The command returns the empty string.

```
string define_proc_attributes
proc_name
[-info info_text]
[-define_args arg_defs]
[-command_group group_name]
[-hide_body]
[-hidden]
[-dont_abbrev]
[-permanent]
```

define_qtm_attribute

Defines a new user-defined attribute for a class of QTM objects.

```
string define_qtm_attribute
-type data_type
-class obj_class
attr_name
```

define_scaling_lib_group

Defines a group of libraries to support voltage and/or temperature scaling.

```
string define_scaling_lib_group
library_list
```

define_user_attribute

Defines a new user-defined attribute.

```
string define_user_attribute
-type data_type
-classes class_list
[-range_min min]
[-range_max max]
[-one_of values]
[-import]
[-quiet]
attr_name
```

derive_clocks

Creates clocks on source pins in design.

```
string derive_clocks
-period period_value
[-waveform edge_list]
```

disconnect_net

Disconnects a net from specified pins or ports, or from all pins and ports.

```
int disconnect_net
net object_spec | -all
```

drive_of

Determines the drive resistance of the specified library cell pin. The drive_of command is a DC Emulation command provided for compatibility with Design Compiler.

```
float drive_of
[-rise] [-fall]
[-wire_drive]
[-piece val]
lib_cell_pin
```

echo

Echos arguments to standard output.

```
string echo
[-n] [argument...]
```

error_info

Prints extended information on errors from last command.

```
string error_info
```

estimate_clock_network_power

Virtually generate a clock tree and estimate its power.

```
string estimate_clock_network_power
 lib_cell
 [-max_fanout fanout]
 [-wire_load_model wire_load_name]
 [-library lib_name]
 [-input_transition transition]
 [-clocks clock_list]
 [-include_registers]
 [-ignore_clock_gating]
```

estimate_eco

Estimate delay changes for the size_cell and insert_buffer commands.

```
int estimate_eco
[-max]
[-min]
[-rise]
[-fall]
[-type size_cell | insert_buffer]
[-sort_by area|stage_delay|arrival|slack]
[-verbose]
[-nosplit]
[-significant_digits]
[-inverter_pair]
[-lib_cells lib_cell_list]
object_list
```

exit

Terminates the application.

```
string exit
[exit_code]
```

extract_model

Generates a timing/power model for a design from its gate-level netlist.

```
string extract_model
[-context_borrow]
[-latch_level levels]
-output file_name
[-format format_list]
[-parasitic_format format_list]
[-library_cell]
[-remove_internal_arcs]
[-ignore_boundary_parasitics]
[-test_design]
[-arc_types arc_list]
[-noise]
[-power]
[-block_scope]
[-block_scope_only]
[-scope_scenario scenario_name]
```

filter

The filter command, a synonym for the filter_collection command, is a Design Compiler emulation command provided for compatibility between PrimeTime and Design Compiler. You use the filter_collection command to filter an existing collection, resulting in a new collection. The base collection remains unchanged.

filter_collection

Filters an existing collection, resulting in a new collection. The base collection remains unchanged.

```
collection filter_collection
base_collection expression
[-regexp]
[-nocase]
```

find

The find command, used to create a collection of design objects, is a DC Emulation command provided for compatibility with Design Compiler.

```
string find
[-hierarchy]
[-flat]
type
[object_list]
```

fix_eco_timing

Improves or fixes timing violations through engineering change order (ECO) changes.

```
string fix_eco_timing
[-type fixing_type]
[-slack_lesser_than slack_limit]
[-slack_greater_than slack_limit]
[-group group]
[-pba_mode effort]
[-from from_list]
[-to to_list]
[-setup_margin margin]
[-hold_margin margin]
[-buffer_list buffer_list]
[-verbose]
```

foreach_in_collection

Iterates over the elements of a collection.

```
string foreach_in_collection
itr_var collections body
```

get_alternative_lib_cells

Creates a collection of library cells that can be used to replace or size a specified cell in the current design.

```
string get_alternative_lib_cells
[-current_library]
[-libraries lib_spec]
[-base_names]
cell
```

get_app_var

Gets the value of an application variable.

```
string get_app_var
[-default | -details | -list]
[-only_changed_vars]
var
```

get_attribute

Retrieves the value of an attribute on an object.

```
string get_attribute
[-class class_name]
[-quiet]
[-value_list]
object_spec
attr_name
```

get_cells

Creates a collection of cells from the current design relative to the current instance. You can assign these cells to a variable or pass them into another command.

```
collection get_cells
[-hierarchical]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
[patterns | -of_objects objects]
```

get_clock_network_objects

Returns a collection of objects that belong or relate to the direct clock network.

```
collection get_clock_network_objects
-type object_type
[clock_list]
[-include_clock_gating_network]
```

get_clocks

Creates a collection of clocks from the current design. You can assign these clocks to a variable or pass them into another command.

```
collection get_clocks
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_command_option_values

Queries current/default option values.

```
get_command_option_values
[-default | -current]
-command command_name
```

get_correlations

Creates a collection of correlations. You can assign these correlations to a variable or pass them into another command.

```
collection get_correlations
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_current_power_domain

Gets the power domains that are included in the power analysis.

This command works only in UPF mode.

```
string get_current_power_domain
```

get_current_power_net

Gets the power nets that are included in the power analysis.

This command works in UPF mode only.

```
string get_current_power_net
```

get_designs

Creates a collection of one or more designs loaded into PrimeTime. You can assign these designs to a variable or pass them into another command.

```
collection get_designs
[-hierarchical]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-filter expression]
patterns
```

get_distributed_variables

Gets Tcl variables from slaves and creates an array at the master indexed by the scenario name.

```
Boolean get_distributed_variables
```

get_generated_clocks

Creates a collection of generated clocks.

```
collection get_generated_clocks
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_ilm_objects

Returns a collection of nets, cells, or pins that are part of the interface logic for the current design.

```
collection get_ilm_objects
[-type {net | pin | cell}]
```

get_lib_cells

Creates a collection of library cells from libraries loaded into PrimeTime. You can assign these library cells to a variable or pass them into another command.

```
collection get_lib_cells
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns | -of_objects objects
```

get_lib_pins

Creates a collection of library cell pins from libraries loaded into PrimeTime. You can assign these library cell pins to a variable or pass them into another command.

```
collection get_lib_pins
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
patterns | -of_objects objects
```

get_lib_timing_arcs

Creates a collection of library arcs for custom reporting and other processing. You can assign these library arcs to a variable and get the desired attribute for further processing.

```
string get_lib_timing_arcs
[-to to_list]
[-from from_list]
[-of_objects object_list]
[-filter expression]
[-quiet]
```

get_libs

Creates a collection of libraries loaded into PrimeTime. You can assign these libraries to a variable or pass them into another command.

```
collection get_libs
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[patterns | -of_objects objects]
```

get_license

Obtains a license for a feature.

```
int get_license feature_list
```

get_message_info

Returns information about diagnostic messages.

```
Integer get_message_info
 [-error_count | -warning_count |
-info_count |
 -limit l_id | -occurrences o_id |
-suppressed s_id]
```

get_nets

Creates a collection of nets from the netlist. You can assign these nets to a variable or pass them into another command.

```
collection get_nets
[-hierarchical]
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-top_net_of_hierarchical_group]
[-segments]
[-boundary_type btype]
[patterns | -of_objects objects]
```

get_noise_violation_sources

Creates a collection of noise violation sources for custom reporting and other processing. You can assign these timing arcs to a variable and get the desired attribute for further processing.

```
int get_noise_violation_sources
[-above]
[-below]
[-low]
[-high]
[-nworst_endpoints pin_count]
[-max_sources_per_endpoint pin_count]
[-slack_type slack_type]
[object_list]
```

get_object_name

Gets the name of the object in a collection of exactly one object.

```
string get_object_name
collection
```

get_path_groups

Creates a collection of path groups from the current design. You can assign these path groups to a variable or pass them into another command.

```
collection get_path_groups
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

get_pins

Creates a collection of pins from the netlist. You can assign these pins to a variable or pass them into another command.

```
collection get_pins
[-hierarchical]
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[-leaf]
[patterns | -of_objects objects]
```

get_ports

Creates a collection of ports from the current design. You can assign these ports to a variable or pass them into another command.

```
collection get_ports
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[-exact]
[patterns | -of_objects objects]
```

get_power_domains

Create a collection of power domains in the current design.

```
string get_power_domains
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
[-of_objects cells]
```

get_power_group_objects

Return a collection of cells in a power group.

```
collection get_power_group_objects
group_names
```

get_power_switches

Create a collection of UPF power_switches in the current design.

```
string get_power_switches
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
```

get_qtm_ports

Creates a collection of QTM ports. You can assign these QTM ports to a variable or pass them into another command.

```
collection get_qtm_ports
[-filter expression]
pattern
```

get_random_numbers

Generates a list of random numbers for a specified variation.

```
list get_random_numbers
-sample_size sample_size
-seed seed
variation_object Variation object
```

get_selection

Returns the list of objects currently selected in the GUI or information about the selected objects.

```
collection get_selection
[-type object_type]
[-design design]
[-more_than more]
[-fewer_than fewer]
[-count]
[-num num]
[-name slct_bus]
[-slct_targets target_slct_bus]
[-slct_targets_operation operation]
[-create_slct_buses]
```

get_si_bottleneck_nets

Identify the crosstalk bottlenecks in the design. This is useful when the major sources of violations come from crosstalk effects.

```
int get_si_bottleneck_nets
-cost_type type
[-slack_lesser_than slack_limit]
[-max_nets count]
[-significant_digits digits]
[-nosplit]
[-include_clock_nets]
[-minimum_active_aggressors
active_aggressor_count]
[-min]
[-max]
```

get_supply_nets

Create a collection of UPF supply_nets in the current design.

```
string get_supply_nets
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
```

get_supply_ports

Create a collection of UPF supply_ports in the current design.

```
string get_supply_ports
[-filter expression]
[-quiet]
[-regexp]
[-nocase]
[patterns]
```

get_switching_activity

Gets switching activity annotation on nets, pins, ports and cells of the current design.

```
int get_switching_activity
[-toggle_rate]
[-glitch_rate]
[-static_probability]
[-state_condition state]
[-path_sources name_list]
[-average_activity]
[-exclude exclusion_group]
[-include_only inclusion_group]
[-toggle_limit limit]
[-only_related_clock clock_name
[-rise]
[-fall]
object_list
```

get_timing_arcs

Creates a collection of timing arcs for custom reporting and other processing. You can assign these timing arcs to a variable and get the desired attribute for further processing.

```
string get_timing_arcs
[-to to_list]
[-from from_list]
[-of_objects object_list]
[-filter expression]
[-quiet]
```

get_timing_paths

Creates a collection of timing paths for custom reporting and other processing. You can assign these timing paths to a variable or pass them into another command.

```
string get_timing_paths
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-exclude exclude_list
 | -rise_exclude rise_exclude_list
 | -fall_exclude fall_exclude_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-delay_type delay_type]
[-nworst paths_per_endpoint]
[-max_paths max_path_count]
[-group group_name]
[-true]
[-unique_pins]
[-true_threshold path_delay]
[-slack_greater_than greater_slack_limit]
[-slack_lesser_than lesser_slack_limit]
[-ignore_register_feedback
feedback_slack_cutoff]
[-include_hierarchical_pins]
[-justify]
[-trace_latch_borrow]
[-start_end_pair]
[-dont_merge_duplicates]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
[-path_type format]
[-pba_mode effort]
[path_collection]
```

get_unix_variable

This is a synonym for the getenv command.

get_variation_attribute

Returns a collection of one or more values associated with a variation's attribute.

```
list get_variation_attribute
[-class class_name]
[-quiet]
variation
attribute
value
```

get_variations

Creates a collection of variations from the current design. You can assign these variations to a variable or pass them into another command.

```
collection get_variations
[-quiet]
[-regexp]
[-nocase]
[-filter expression]
patterns
```

getenv

Returns the value of a system environment variable.

```
string getenv
variable_name
```

group_path

Groups paths for cost function calculations and reporting.

```
Boolean group_path
-name group_name | -default
[-weight weight_value]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
```

gui_start

Starts the Primetime GUI.

```
string gui_start
[-file name_of_script_file]
[-no_windows]
```

gui_stop

Stops the Primetime GUI.

```
string gui_stop
```

help

Displays quick help for one or more commands.

```
string help
[-verbose] [-groups] [pattern]
```

history

Displays or modifies the commands recorded in the history list.

```
string history
[-h] [-r] [args...]
```

identify_interface_logic

Sets the is_interface_logic_pin attribute on pins of the current design that are part of its interface logic.

```
int identify_interface_logic
[-ignore_ports port_list | -auto_ignore]
[-latch_level levels | -context_borrow]
[-keep_ignored_fanout]
[-include_pins pin_list]
[-critical_pins]
[-include_all_net_pins]
[-traverse_disabled_arcs]
```

index_collection

Creates a single element collection. I.e. Given a collection and an index into it, if the index is in range, extracts the object at that index and creates a new collection containing only that object. The base collection remains unchanged.

```
collection index_collection
collection1 index
```

insert_buffer

Inserts a buffer at one or more pins.

```
[-libraries lib_spec]
[-inverter_pair]
[-new_net_names new_net_names]
[-new_cell_names new_cell_names]
pin_or_port_list
lib_cell
```

is_false

Tests the value of a specified variable, and returns a 1 if the value is 0 or the case-insensitive string *false*; returns a 0 if the value is 1 or the case-insensitive string *true*.

```
int is_false
value
```

is_true

Tests the value of a specified variable, and returns a 1 if the value is 1 or the case-insensitive string *true*; returns a 0 if the value is 0 or the case-insensitive string *false*.

```
int is_true
value
```

license_users

Lists the current users of the Synopsys licensed features.

```
license_users
[feature_list]
```

link

The link command, a synonym for the link_design command, exists in PrimeTime for compatibility with Design Compiler.

link_design

Resolves references in a design.

```
string link_design
[-verbose]
[-remove_sub_designs]
[-keep_sub_designs]
[-force]
[design_name]
```

list_attributes

Lists currently defined attributes.

```
string list_attributes
[-application]
[-class class_name]
[-nosplit]
```

list_designs

Lists designs that have been read into PrimeTime.

```
string list_designs
[-all]
[-only_used]
```

list_key_bindings

Displays all the key bindings and edit mode of current shell session.

```
int list_key_bindings
[-nosplit]
```

list_libraries

Lists all libraries that are read into PrimeTime.

```
string list_libraries
[-only_used]
```

list_licenses

Shows the licenses which are currently checked out.

```
string list_licenses
```

lminus

Removes one or more named elements from a list and returns a new list.

```
list lminus
[-exact] the_list elements
```

load_of

Gets the capacitance of a library cell pin. It is a DC Emulation command provided for compatibility with Design Compiler.

```
float load_of lib_pin
```

load_upf

Reads in a script in Unified Power Format (UPF) format.

```
int load_upf
upf_file_name
[-scope instance_name]
[-version upf_version]
```

ls

Lists the contents of a directory.

```
string ls
[filename ...]
```

man

Displays reference manual pages.

```
string man
topic
```

map_design_mode

Maps specified design modes to cell modes and/or paths

```
string map_design_mode
design_mode
[-from from_pin_list]
[-to to_pin_list]
[-through through_pin_list]
[cell_mode_list]
[instance_list]
```

max_variation

Takes the maximum of two or more variations. Returns a collection (that corresponds to this max variation).

```
collection max_variation
variation_list
```

mem

Retrieves the total memory allocated by the current pt_shell process.

```
int mem
```

merge_models

Merges multiple timing models (in LIB format) together to be one.

```
string merge_models
[-lib_files lib_files]
-mode_names mode_names
[-group_name mode_group_name]
-output output_file_name
[-formats format_list]
[-tolerance merge_tolerance]
[-single_mode]
[-keep_all_arcs]
```

merge_saif

Reads a list of SAIF files with their corresponding weights, annotates switching activity attributes with merged toggle_rate, glitch_rate and merged static_probability for nets, pins, ports, and power arcs in the current instance, and generates a merged output SAIF file.

```
int merge_saif
-input_list saif_file_and_weight_list
[-strip_path inst_name]
[-path prefix]
[-output merged_saif_name]
[-simple_merge]
[-ignore ignore_name]
[-exclude exclude_file_name]
[-derate_glitch value]
[-quiet]
```

min_variation

Takes the minimum of two or more variations. Returns a collection (that corresponds to this min variation).

```
collection min_variation
variation_list
```

parse_proc_arguments

Parses the arguments passed into a Tcl procedure.

```
string parse_proc_arguments
-args arg_list
result_array
```

print_message_info

Prints information about diagnostic messages which have occurred or have been limited.

```
string print_message_info
[-ids id_list] [-summary]
```

print_proc_new_vars

Check for new variables created within a Tcl procedure.

```
string print_proc_new_vars
```

print_suppressed_messages

Displays an alphabetical list of message ids that are currently suppressed.

```
string print_suppressed_message
```

printenv

Prints the value of environment variables.

```
string printenv
[variable_name]
```

printvar

Prints the values of one or more variables.

```
string printvar
[pattern] [-user_defined] [-application]
```

proc_args

Displays the formal parameters of a procedure.

```
string proc_args
proc_name
```

proc_body

Displays the body of a procedure.

```
string proc_body
proc_name
```

query_objects

Searches for and displays objects in the database.

```
string query_objects
[-verbose]
[-class class_name]
[-truncate elem_count]
object_spec
```

quit

Exits the shell.

```
string quit
```

read_aocvm

Reads AOCVM derate factor tables.

```
int read_aocvm
aocvm_file
```

read_db

Reads in one or more design or library files in Synopsys database (db) format.

```
string read_db
[-netlist_only] [-library]
file_names
```

read_ddc

Reads in design files in the Synopsys DDC format.

```
string read_ddc
[-netlist_only]
[-scenario scenario_name]
file_names
```

read_file

Reads a netlist or library file. This is a DC Emulation command provided for compatibility with Design Compiler.

```
string read_file
[-format type]
[-single_file ns1]
[-names_file ns2]
[-define ns3]
file_list
```

read_lib

Reads in a Synopsys library (.lib) file.

```
Boolean read_lib
file_name
```

read_milkyway

Reads in one linked design from milkyway database.

```
int read_milkyway
[-version version]
[-netlist_only]
[-library design_library]
[-scenario scenario_name]
CEL_name
```

read_parasitics

Reads net parasitics information from an SPEF, DSPF, RSPF, PARA, or binary parasitics file (SBPF) and uses it to annotate the currently linked design.

```
Boolean read_parasitics
 [-format file_fmt]
 [-complete_with completion_type]
 [-lumped_cap_only]
 [-pin_cap_included] [-increment]
 [-path prefix]
 [-keep_capacitive_coupling]
 [-coupling_reduction_factor factor]
 [-triplet_type ttype]
 [-verbose] [-syntax_only]
 [-eco]
 [-original_file_name file_name]
 [-ilm_context]
 [-keep_variations]
 [-create_default_variations]
 file_names
```

read_saif

Reads a SAIF file and annotates switching activity information on nets, pins, ports, and cells in the current design.

```
int read_saif
file_name
[-strip_path prefix]
[-path prefix]
[-ignore ignore_name]
[-exclude exclude_file_name]
[-derate_glitch value]
[-quiet]
```

read_sdc

Reads in a script in Synopsys Design Constraints (SDC) format.

```
int read_sdc
file_name [-echo]
[-syntax_only]
[-version sdc_version]
```

read_sdf

Reads leaf cell and net timing information from a file in Standard Delay Format (SDF) and uses that information to annotate the current design.

```
string read_sdf
[-load_delay net | cell]
[-analysis_type single | bc_wc |
on_chip_variation]
[-min_file min_fname]
[-max_file max_fname]
[-path path_name]
[-type sdf_min | sdf_typ | sdf_max]
[-min_type sdf_min | sdf_typ | sdf_max]
[-max_type sdf_min | sdf_typ | sdf_max]
[-cond_use min | max | min_max]
[-syntax_only]
[-strip_path strip_path_name]
[-verbose] [-worst ]
file_name
```

read_vcd

Specifies the switching activity information generated by simulation for use in power calculation. Internally, non-VCD format switching activity is converted to VCD.

```
int read_vcd
[-path prefix]
[-strip_path prefix]
[-zero_delay]
[-pipe_exec command]
[-format format]
[-time window_list]
[-rtl]
file_name
```

read_verilog

Reads in one or more Verilog files.

```
string read_verilog
[-hdl_compiler] file_names
```

read_vhdl

Reads in one or more VHDL files.

```
Boolean read_vhdl
[-vhdl_compiler] file_names
```

redirect

Redirects the output of a command to a file.

```
string redirect
[-append] [-tee] [-file | -variable |
-channel] [-compress]
target
{command_string}
```

remote_execute

Builds a buffer of commands and triggers execution of these commands on remote slaves.

```
boolean remote_execute
[-pre_commands pre_command_string] (string
containing pre commands to be executed at
slave)
command_string (string containing commands
to be executed at slave)
[-post_commands post_command_string] (string
containing post commands to be executed at
slave]
[-verbose]
```

remove_annotated_check

Removes annotated timing checks from the design, either on specific cells, between specific pins, or on all cells in the current design.

```
string remove_annotated_check
[-all]
[-from from_pins]
[-to to_pins]
[-rise] [-fall]
[-clock clock_check]
[-setup | -recovery]
[-hold | -removal]
[-nochange_high | -nochange_low]
[object_spec]
```

remove_annotated_clock_network_power

Remove the annotate power on clock networks.

```
string remove_annotated_clock_network_power
[-clock clock_object]
```

remove_annotated_delay

Removes annotated delays from the design, either on specific cells or nets, between specific pins, or all annotated delays in the design.

```
string remove_annotated_delay
[-all]
[-from from_list]
[-to to_list]
[object_spec]
```

remove_annotated_parasitics

Removes all annotated parasitics from nets of the current design.

```
Boolean remove_annotated_parasitics
[ -all | net_list ]
```

remove_annotated_power

Remove previously-annotated power from unresolved black-box cells or leaf cells.

```
int remove_annotated_power
-all | cell_list
```

remove_annotated_transition

Removes previously-annotated transition times from pins or ports in the current design.

```
int remove_annotated_transition
-all | pin_list
```

remove_aocvm

Removes AOCVM information.

```
int remove_aocvm
[-coefficient] [-derate]
[object_list]
```

remove_buffer

Removes specified buffers from the current design.

```
int remove_buffer
cell_list
```

remove_capacitance

Removes capacitance on nets or ports.

```
string remove_capacitance net_or_port_list
```

remove_case_analysis

Removes the case analysis value on input.

```
string remove_case_analysis port_or_pin_list
```

remove_cell

Removes cells from the current design.

```
int remove_cell
cell_list | -all
```

remove_clock

Removes one or more clocks from the current design.

```
string remove_clock
-all | clock_list
```

remove_clock_gating_check

Captures clock-gating checks.

```
string remove_clock_gating_check
[-setup]
[-hold]
[-rise]
[-fall]
[-high | -low]
[object_list]
```

remove_clock_groups

Removes specific exclusive or asynchronous clock groups from the current design.

```
Boolean remove_clock_groups
-physically_exclusive | -exclusive |
-asynchronous
-name name_list | -all
```

remove_clock_latency

Removes clock latency information from specified objects.

```
string remove_clock_latency [-source]
[-clock clock_list]
object_list
```

remove_clock_sense

Removes unateness information defined on pins or cell timing arcs.

```
string remove_clock_sense
[-all]
[-clocks clock_list]
object_list
```

remove_clock_transition

Removes clock transition time information.

```
string remove_clock_transition
clock_list
```

remove_clock_uncertainty

Removes clock uncertainty information previously set by the set_clock_uncertainty command.

```
string remove_clock_uncertainty
[object_list |
 -from from_clock
  | -rise_from rise_from_clock
  | -fall_from fall_from_clock
 -to to_clock
  | -rise_to rise_to_clock
  | -fall_to fall_to_clock]
[-rise]
[-fall]
[-setup]
[-hold]
[object_list]
```

remove_connection_class

Removes connection class value from ports.

```
int remove_connection_class
object_list
```

remove_context

Deletes the timing context information.

```
string remove_context
[-timing][-environment]
[-design_rules]
[-constant_inputs]
cell_list
```

remove_coupling_separation

Removes the constraints set by set_coupling_separation command.

```
int remove_coupling_separation
 [-pairwise pair_nets]
 [-all]
 nets
```

remove_current_session

Removes the previously set session.

```
boolean remove_current_session
```

remove_data_check

Removes specified data-to-data checks previously set by set_data_check.

```
string remove_data_check
{-from from_object
 | -rise_from from_object
 | -fall_from from_object}
{-to to_object
 | -rise_to to_object
 | -fall_to to_object}
[-setup | -hold]
[-clock clock]
```

remove_design

Removes one or more designs from memory.

```
string remove_design
-all -hierarchy designs
```

remove_design_mode

Removes specified design modes and/or cell mode and path mappings to design modes.

```
string remove_design_mode
mode_list
[-from from_pin_list]
[-to to_pin_list]
[-through through_pin_list]
[cell_mode_list]
[instance_list]
```

remove_disable_clock_gating_check

Restores clock gating checks previously disabled by set_disable_clock_gating_check, for specified cells and pins.

```
string remove_disable_clock_gating_check
object_list
```

remove_disable_timing

Enables the previously disabled timing arcs.

```
string remove_disable_timing
[-from from_pin_name]
[-to to_pin_name]
object_list
```

remove_distributed_hosts

Remove all the hosts added to the distributed hosts list.

```
int remove_distributed_hosts
-all
```

remove_drive_resistance

Removes drive resistance for input or inout ports.

```
string remove_drive_resistance
port_list
```

remove_driving_cell

Removes port driving cell information.

```
string remove_driving_cell
[-rise]
[-fall]
[-min]
[-max]
[-clock clock_name]
[-clock_fall]
port_list
```

remove_fanout_load

Removes fanout load information from output ports in the current design.

```
string remove_fanout_load
port_list
```

remove_from_collection

Removes objects from a collection, resulting in a new collection. The base collection remains unchanged.

```
collection remove_from_collection
base_collection
```

remove_generated_clock

Removes generated clock objects from the current design.

```
Boolean remove_generated_clock
-all | clock_list
```

remove_host_options

Removes hosts options set using the set_host_options command.

```
int remove_host_options
[host_option_names]
```

remove_ideal_latency

Removes ideal latency values from the specified objects.

```
int remove_ideal_latency
[-rise] [-fall]
[-min] [-max]
object_list
```

remove_ideal_network

Removes sources of ideal networks in the current design. Cells and nets in the transitive fanout of the specified objects are no longer treated as ideal.

```
int remove_ideal_network
object_list
list object_list
```

remove_ideal_transition

Removes ideal transition values from the specified objects.

```
int remove_ideal_transition
[-rise] [-fall]
[-min] [-max]
object_list
```

remove_input_delay

Removes input delay information from ports or pins.

```
string remove_input_delay
[-clock clock_name]
[-clock_fall]
[-level_sensitive]
[-rise]
[-fall]
[-max]
[-min]
port_pin_list
```

remove_input_noise

Removes input noise for a library pin or port.

```
int remove_input_noise
[-above]
[-below]
[-low]
[-high]
object_list
```

remove_lib

Removes one or more libraries from memory.

```
string remove_lib
-all
libraries
```

remove_license

Removes a licensed feature.

```
int remove_license
feature_list
```

remove_max_area

Removes the max_area attribute from the current design.

```
int remove_max_area
```

remove_max_capacitance

Removes maximum capacitance limits from pins, ports, clocks or designs.

```
string remove_max_capacitance
object_list
```

remove_max_fanout

Removes maximum fanout limits from ports or designs.

```
string remove_max_fanout
object_list
```

remove_max_time_borrow

Removes time borrow limit for latches.

```
string remove_max_time_borrow
object_list
```

remove_max_transition

Removes maximum transition limits from pins, ports, clocks or designs.

```
string remove_max_transition
object_list
```

remove_min_capacitance

Removes minimum capacitance limits from ports or designs.

```
string remove_min_capacitance
object_list
```

remove_min_pulse_width

Removes a previously-specified minimum pulse width constraint from specified design objects.

```
string remove_min_pulse_width
[-low]
[-high]
[object_list]
```

remove_multi_scenario_design

Removes all multi scenario objects from memory and removes from disk all images generated by multi scenario analysis.

```
boolean remove_multi_scenario_design
```

remove_net

Removes nets from the current design.

```
int remove_net
net_list | -all
```

remove_noise_immunity_curve

Removes noise immunity curve for a library pin or port.

```
int remove_noise_immunity_curve
[-above]
[-below]
[-low]
[-high]
object_list
```

remove_noise_lib_pin

Removes an equivalent noise library pin for a driver or load.

```
int remove_noise_lib_pin
pins
```

remove_noise_margin

Removes noise margin for a library pin or port.

```
int remove_noise_margin
[-above]
[-below]
[-low]
[-high]
object_list
```

remove_operating_conditions

Removes operating conditions from current design, cells or ports.

```
string remove_operating_conditions
[-object_list objects]
```

remove_output_delay

Removes output delay from output ports or pins.

```
string remove_output_delay
[-clock clock_name]
[-clock_fall]
[-level_sensitive]
[-rise]
[-fall]
[-max]
[-min]
port_pin_list
```

remove_parasitic_corner

Removes a previously set parasitic corner in the presence of variation-aware parasitics.

```
Boolean remove_parasitic_corner
```

remove_path_group

Removes path_group objects.

```
string remove_path_group
-all | path_group_list
```

remove_port_fanout_number

Removes fanout number information on ports.

```
string remove_port_fanout_number
port_list
```

remove_power_groups

Remove the existing power groups.

```
string remove_power_groups
groups | -all
```

remove_propagated_clock

Removes a propagated clock specification.

```
string remove_propagated_clock
object_list
```

remove_pulse_clock_max_transition

Removes maximum transition limits from pulse clock network and input of pulse generator.

```
string remove_pulse_clock_max_transition
object_list
[-rise][-fall]
[-transitive_fanout]
object_list
```

remove_pulse_clock_max_width

Removes maximum pulse width limits from pulse clock network.

```
string remove_pulse_clock_max_width
[-transitive_fanout]
object_list
```

remove_pulse_clock_min_transition

Removes minimum transition limits from input of pulse generator.

```
string remove_min_transition
object_list
[-rise][-fall]
object_list
```

remove_pulse_clock_min_width

Removes minimum pulse width limits from pulse clock network.

```
string remove_pulse_clock_min_width
[-transitive_fanout]
object_list
```

remove_qtm_attribute

Removes an attribute setting from the QTM object.

```
string remove_qtm_attribute
-class class_name
attr_name
object_names
```

remove_rail_voltage

Removes power rail voltage that was set by the set_rail_voltage command on cells.

```
int remove_rail_voltage
cell_list
```

remove_resistance

Removes resistance on nets.

```
string remove_resistance
net_list
```

remove_scenario

Removes a scenario in multi scenario analysis.

```
remove_scenario
scenario list
```

remove_setup_hold_pessimism_reduction

Removes the optimization constraints for setup-hold pessimism reduction.

```
remove_setup_hold_pessimism_reduction
[-setup_cutoff]
[-hold_cutoff]
```

remove_si_aggressor_exclusion

Removes the exclusive groups set by the set_si_aggressor_exclusion command.

```
int remove_si_aggressor_exclusion
[-rise]
[-fall]
[-all]
[anets]
```

remove_si_delay_analysis

Removes the effect of the set_si_delay_analysis command.

```
int remove_si_delay_analysis
[-reselect rnets]
[-ignore_arrival inets]
[-victims vnets]
[-aggressors anets]
[-rise]
[-fall]
[-min]
[-max]
[-all]
```

remove_si_delay_disable_statistical

Removes the effect of the set_si_delay_disable_statistical command.

```
int remove_si_delay_disable_statistical
dnets
```

remove_si_noise_analysis

Removes the effect of the set_si_noise_analysis command.

```
int remove_si_noise_analysis
[-ignore_arrival inets]
[-victims vnets]
[-aggressors anets]
[-above]
[-below]
[-low]
[-high]
[-all]
```

remove_si_noise_disable_statistical

Removes the effect of set_si_noise_disable_statistical command.

```
int remove_si_noise_disable_statistical
dnets
```

remove_steady_state_resistance

Removes steady state resistance for a library pin or port.

```
int remove_steady_state_resistance
[-above]
[-below]
[-low]
[-high]
object_list
```

remove_user_attribute

Removes a user attribute from an object.

```
string remove_user_attribute
[-quiet]
[-class class_name]
object_spec
attr_name
```

remove_user_sensitization

Report user sensitization of an instance or library arc for write_spice_deck output.

```
int remove_user_sensitization
[-analysis_type [rise | fall | high | low]]
[-arc arcs_list]
[-library library_name]
[-design design_name]
```

remove_variation

Removes one or more variations.

```
int remove_variation
[-all]
[variation_list]
```

remove_wire_load_min_block_size

Removes the minimum block size for automatic wire load selection.

```
int remove_wire_load_min_block_size
```

remove_wire_load_model

Removes wire load model from designs, hierarchical cells, or ports.

```
string remove_wire_load_model
[object_list]
```

remove_wire_load_selection_group

Removes wire load selection_group from current design.

```
string remove_wire_load_selection_group
```

rename

Rename or delete a command.

```
string rename
oldName newName
```

rename_cell

Change the name of a cell.

```
int rename_cell
cell new_name
```

rename_design

Change the name of a design.

```
int rename_design
design new_name
```

rename_net

Change the name of a net.

```
int rename_net
net new_name
```

report_activity_waveforms

reports on activity analysis of VCD

```
int report_activity_waveforms
[-nosplit]
```

report_alternative_lib_cells

Generates a report that contains data to aid in the selection of alternative library cells for a cell in the current design.

```
string report_alternative_lib_cells
[-current_library]
[-libraries lib_spec]
[-delay_type delay_type]
[-all_pins]
[-weighted_design_cost]
[-total_design_cost]
[-significant_digits digits]
[-nosplit]
cell
```

report_analysis_coverage

Generates a report about coverage of timing checks.

```
string report_analysis_coverage
[-status_details status_list]
[-check_type check_type_list]
[-exclude_untested untested_reason_list]
[-sort_by sort_method]
[-significant_digits digits]
[-nosplit]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
```

report_annotated_check

Reports back-annotated timing checks.

```
string report_annotated_check
[-setup] [-hold]
[-recovery] [-removal]
[-nochange]
[-width] [-period]
[-max_skew]
[-clock_separation]
[-max_line num]
[-list_annotated]
[-list_not_annotated]
[-constant_arcs]
```

report_annotated_delay

Reports back-annotated delays.

```
string report_annotated_delay
[-cell]
[-net]
[-from_in_ports]
[-to_out_ports]
[-max_line num]
[-list_annotated]
[-list_not_annotated]
[-constant_arcs]
[-crosstalk_delta]
```

report_annotated_parasitics

Reports net parasitics back-annotated on the *current design*.

```
string report_annotated_parasitics
[-check]
[-internal_nets]
[-boundary_nets]
[-driverless_nets]
[-loadless_nets]
[-pin_to_pin_nets]
[-max_nets num]
[-list_annotated]
[-list_not_annotated]
[-constant_arcs]
[-variation]
[-no_check]
[net_list]
```

report_annotated_power

Report annotated power.

```
int report_annotated_power
[-list_annotated]
```

report_aocvm

Displays information about AOCVM derate tables and coefficients. Also displays details of path-based and graph-based AOCVM calculation.

```
int report_aocvm
[-early] [-late]
[-rise] [-fall]
[-cell_delay] [-net_delay]
[-list_annotated] [-list_not_annotated]
[-nosplit]
[object_list]
```

report_app_var

Shows the application variables.

```
string report_app_var
[-verbose]
[-only_changed_vars]
[pattern]
```

report_attribute

Reports the attributes on one or more objects.

```
string report_attribute
[-class class_name]
[-nosplit]
[-application]
object_spec
```

report_bottleneck

Reports timing bottleneck information.

```
string report_bottleneck
[-cost_type cost_type]
[-delay_type delay_type]
[-slack_lesser_than slack_limit]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-through through_list]
[-rise_through through_list]
[-fall_through through_list]
[-max_cells cell_count]
[-max_paths path_count]
[-nworst_paths paths_per_endpoint]
[-group group_name]
[-significant_digits digits]
[-nosplit]
```

report_bus

Reports the bused ports or nets in the current instance or current design.

```
string report_bus
[-nosplit]
```

report_case_analysis

Reports case analysis entries on ports and pins.

```
string report_case_analysis
[-all]
[-nosplit]
```

report_cell

Reports cell information.

```
string report_cell
[-connections [-verbose]]
[-significant_digits digits]
[-nosplit]
[cell_names]
```

report_clock

Reports clock-related information.

```
string report_clock
[-attributes]
[-skew]
[-groups]
[-nosplit]
[clock_names]
```

report_clock_gate_savings

Reports toggle savings on clock gates

```
int report_clock_gate_savings
[-by_clock_gate]
[-sequential]
[-hierarchical]
[-sort_by]
[clocks clock_list]
[-nosplit]
[object_list]
```

report_clock_gating_check

Displays clock gating check information about specified pins.

```
int report_clock_gating_check
[-significant_digits digits]
[-nosplit]
[object_list]
```

report_clock_timing

Reports timing attributes of clock networks.

```
string report_clock_timing
-type report_type
[-clock clock_list]
[-from_clock from_clock_list]
[-to_clock to_clock_list]
[-from from_list]
[-to to_list]
[-setup] | [-hold]
[-launch] | [-capture]
[-rise] | [-fall]
[-nworst worst_entries]
[-greater_than lower_limit]
[-lesser_than upper_limit]
[-slack_lesser_than slack_upper_limit]
[-include_uncertainty_in_skew]
[-verbose]
[-significant_digits digits]
[-show_clocks]
[-crosstalk_delta]
[-derate]
[-variation]
[-sort_by sort_attr]
[-nosplit]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
```

report_constraint

Displays constraint-related information about a design.

```
int report_constraint
[-all_violators] [-verbose]
[-path_type format] [-max_delay]
[-min_delay]
[-max_capacitance] [-min_capacitance]
[-max_transition] [-min_transition]
[-max_fanout] [-min_fanout]
[-min_pulse_width] [-min_period]
[-pulse_clock_min_width][-pulse_clock_max_wi
dth]
[-pulse_clock_min_transition][-pulse_clock_m
ax_transition]
[-recovery] [-removal] [-max_skew]
[-clock_gating_setup] [-clock_gating_hold]
[-clock_separation]
[-connection_class]
[-ignore_register_feedback
feedback_slack_cutoff]
[-significant_digits digits] [-nosplit]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
```

report_context

Reports the characterized timing context information.

```
string report_context
[-timing] [-environment]
[-design_rules]
[-constant_inputs]
[-nosplit]
cell_list
```

report_crpr

Reports the clock reconvergence pessimism (CRP) calculated between specified register clock pins or ports.

```
int report_crpr
-from from_latch_clock_pin
-to to_latch_clock_pin
[-from_clock from_clock]
[-to_clock to_clock]
[-setup | -hold]
[-significant_digits digits]
```

report_delay_calculation

Displays the actual calculation of a cell or net timing arc delay value.

```
int report_delay_calculation
[-min | -max]
[-from_rise_transition value]
[-from_fall_transition value]
-from from_pin -to to_pin | -of_objects
objects
[-nosplit]
[-thresholds]
[-crosstalk]
```

report_design

Displays attributes on the current_design.

```
int report_design
[-nosplit]
```

report_disable_timing

Reports disabled timing arcs in the current design.

```
string report_disable_timing
[-nosplit]
[cells_or_ports]
```

report_distributed_hosts

Creates a detailed report on user-defined distributed hosts in the farm's pool

```
Boolean report_distributed_hosts
```

report_driver_model

Displays the driver model for a library cell timing arc used to drive annotated parasitics.

```
int report_driver_model
-lib_cell lib_cell
-from_pin from_pin
-to_pin to_pin
-rise_slew rise_slew
-fall_slew fall_slew
-capacitance capacitance
```

report_etm_arc

Reports the data and clock paths traversed while extracting a particular timing arc.

```
string report_etm_arc
[-from from_object]
[-rise_from rise_from_object]
[-fall_from fall_from_object]
[-to to_object]
[-rise_to rise_to_object]
[-fall_to fall_to_object]
[-arc_type arc_type]
[-include path_type_list]
[-context_borrow] | [-latch_level levels]
[-library_cell]
[-etm_report er_file_name]
[-netlist_report nr_file_name]
[-significant_digits digits]
```

report_exceptions

Generates a report of timing exceptions.

```
Boolean report_exceptions
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-ignored]
[-nosplit]
```

report_global_slack

Displays slack of specified pins or ports.

report_hierarchy

Reports the reference hierarchy of the current_instance or current_design.

```
string report_hierarchy
[-full]
[-noleaf]
[-nosplit]
```

report_hosts

Creates a detailed report that describes all host options that you have created.

```
int report_hosts
[-verbose]
[-nosplit]
[host_option_names]
```

report_ideal_network

Displays information about ports, pins, nets, and cells on ideal networks in the current design.

```
int report_ideal_network
[-net]
[-cell]
[-load_pin]
[-timing]
[object_list]
```

report_lib

Reports library information.

```
string report_lib
[-timing_arcs] [-power_arcs]
[-nosplit]
library_name
[lib_cell_list]
```

report_lib_groups

Generates a report of library groups.

```
int report_lib_groups
[-scaling]
[-show]
[-nosplit]
[show_list]
```

report_min_pulse_width

Displays minimum pulse width check information about specified pins or ports.

```
int report_min_pulse_width
[-all_violators]
[-significant_digits digits]
[-nosplit]
[-path_type format]
[-input_pins]
[port_pin_list]
```

report_mode

Displays a report of modes for specified cells or the design

```
string report_mode
[-type cell | design]
[-nosplit]
[instance_list]
```

report_multi_scenario_design

Creates a detailed report on user defined multi-scenario objects and attributes.

```
Boolean report_multi_scenario_design
 [-scenario]
 [-session]
 [-license]
```

report_name_mapping

Report the name mapping rules.

```
string report_name_mapping
 [-nosplit]
```

report_net

Generates a report of net information.

```
string report_net
[-connections [-verbose]]
[-significant_digits digits]
[-segments]
[-nosplit]
[net_names]
```

report_noise

Reports noise analysis information.

```
int report_noise
[-above]
[-below]
[-low]
[-high]
[-nworst_pins pin_count]
[-significant_digits digits]
[-slack_type slack_type]
[-slack_lesser_than slack_limit]
[-all_violators]
[-data_pins]
[-clock_pins]
[-async_pins]
[-verbose]
[-nosplit]
[object_list]
```

report_noise_calculation

Displays the actual calculation of noise information for the specified net arc.

```
int report_noise_calculation
[-above]
[-below]
[-low]
[-high]
[-significant_digits digits]
[-nosplit]
-from from_pin
-to to_pin
```

report_noise_parameters

Reports status of the noise analysis parameters for the current design.

```
int report_noise_parameters
```

report_noise_violation_sources

Reports noise violation sources for failing endpoints.

```
int report_noise_violation_sources
[-above]
[-below]
[-low]
[-high]
[-nworst_endpoints pin_count]
[-max_sources_per_endpoint pin_count]
[-significant_digits digits]
[-slack_type slack_type]
[-verbose]
[-nosplit]
[object_list]
```

report_path_group

Reports path_group information.

```
string report_path_group
[-nosplit]
[path_group_names]
```

report_port

Displays port information within the design.

```
string report_port
[-verbose]
[-design_rule]
[-drive]
[-input_delay]
[-output_delay]
[-wire_load]
[-nosplit]
[port_names]
```

report_power

Generate power reports.

```
int report_power
 [-net_power]
 [-cell_power]
 [-leaf]
 [-include_boundary_nets]
 [-include_estimated_clock_network]
 [-sort_by sort_method]
 [-nworst number]
 [-power_greater_than threshold]
 [-hierarchy]
 [-levels level]
 [-clocks clock_list]
 [-groups group_list]
 [object_list]
 [-verbose]
 [-nosplit]
```

report_power_analysis_options

Report the options for power analysis.

```
int report_power_analysis_options
```

report_power_calculation

Displays the actual calculation of internal power for a pin, leakage power for a cell or switching power for a net.

```
int report_power_calculation
object_list
[-state_condition state]
[-path_sources name_list]
[-rise | -fall]
[-verbose]
```

report_power_domain

Report the specified power domain.

UPF :

```
int report_power_domain
[domain_list]
```

report_power_groups

Report the existing power groups.

```
string report_power_groups
 group_names
 [-nosplit]
```

report_power_net_info

Reports the power net info for the current design.

```
int report_power_net_info
```

report_power_network

Reports connectivity in virtual power network formed by UPF supply nets, ports, and PG pins.

```
string report_power_network
[-nets nets]
```

report_power_pin_info

Reports the power pin info for technology library cells or leaf cells.

```
int report_power_pin_info
object_list
```

report_power_rail_mapping

Report the current power rail mapping.

```
report_power_rail_mapping
[-cells cell_list]
[-verbose]
[-nosplit]
```

report_power_switch

Report all power switches defined in the design.

report_pulse_clock_max_transition

Displays maximum transition computation at the input of pulse generator and pulse clock network.

```
int report_pulse_clock_max_transition
[-rise][-fall]
[-transitive_fanout]
[-all_violators]
[-significant_digits digits]
[-nosplit]
[port_pin_list]
```

report_pulse_clock_max_width

Displays maximum pulse width computation for the pulse clock network.

```
int report_pulse_clock_max_width
[-all_violators]
[-significant_digits digits]
[-nosplit]
[-path_type format]
[-transitive_fanout]
[port_pin_list]
```

report_pulse_clock_min_transition

Displays minimum transition computation at the input of pulse generator.

```
int report_pulse_clock_min_transition
[-rise][-fall]
[-all_violators]
[-significant_digits digits]
[-nosplit]
[port_pin_list]
```

report_pulse_clock_min_width

Displays minimum pulse width computation for the pulse clock network.

```
int report_pulse_clock_min_width
[-all_violators]
[-significant_digits digits]
[-nosplit]
[-path_type format]
[-transitive_fanout]
[port_pin_list]
```

report_qtm_model

Reports Quick Timing Model (QTM) data.

```
string report_qtm_model
[-global_parameters]
[-ports]
[-arcs]
[-nosplit]
```

report_reference

Reports the references in current instance or design.

```
string report_reference
[-nosplit]
```

report_scale_parasitics

Use to report the scaling that was done previously using the scale_parasitics command.

```
int report_scale_parasitics
[net_list]
```

report_scope_data

Reports relavent scope data stored in the specified file.

```
int report_scope_data
[-block_name blk_name]
[-port_names port_names]
[-clock_names clk_names]
[-scope_scenarios names]
[-check_types chk_types]
[-instance inst_name]
[-significant_digits digits]
[-nosplit]
[-verbose]
file_name
```

report_si_aggressor_exclusion

Reports the exclusive groups set by command set_si_aggressor_exclusion.

```
int report_si_aggressor_exclusion
[-rise]
[-fall]
[-nosplit]
[anets]
```

report_si_bottleneck

Identify the crosstalk bottlenecks in the design. This is useful when the major sources of violations come from crosstalk effects.

```
int report_si_bottleneck
-cost_type type
[-slack_lesser_than slack_limit]
[-max_nets count]
[-significant_digits digits]
[-nosplit]
[-include_clock_nets]
[-minimum_active_aggressors
active_aggressor_count]
[-min]
[-max]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
```

report_si_delay_analysis

Generates a report of user coupling information on nets for crosstalk delay analysis.

```
int report_si_delay_analysis
[-reselected]
[-ignored_arrival]
[-excluded]
[-coupling_separated]
[-disabled_statistical]
[-nosplit]
[nets]
```

report_si_double_switching

Reports the double switching violation detected in the design.

```
int report_si_double_switching
[-clock_network]
[-rise]
[-fall]
[-nosplit]
[nets]
```

report_si_noise_analysis

Generates a report of user coupling information on nets for crosstalk noise analysis.

```
int report_si_noise_analysis
[-ignored_arrival]
[-excluded]
[-coupling_separated]
[-disabled_statistical]
[-nosplit]
[nets]
```

report_supply_net

Reports all supply nets associated with the specified power domain.

```
int report_supply_net
[-scope scope]
[-domain domain_name or domain_object]
```

report_switching_activity

Reports statistics on the switching activity and signal probability annotation on the current design or instance.

```
int report_switching_activity
[-cells cell_list]
[-average_activity]
[-base_clock clk]
[-hierarchy]
[-coverage]
[-sort_by [hier | toggle]]
[-toggle_limit limit]
[-list_low_activity]
[-list_by_source source]
[-list_not_annotated]
[-list_annotated]
[-exclude exclusion_group]
[-include_only inclusion_group]
[-only_related_clock clock]
[-show_pin]
```

report_timing

Reports timing paths.

```
string report_timing
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-exclude exclude_list
 | -rise_exclude rise_exclude_list
 | -fall_exclude fall_exclude_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-delay_type delay_type]
[-nworst paths_per_endpoint]
[-max_paths count]
[-path_type format]
[-true]
[-true_threshold path_delay]
[-justify]
[-false]
[-input_pins]
[-unique_pins]
[-start_end_pair]
[-nets]
[-slack_greater_than greater_slack_limit]
[-slack_lesser_than lesser_slack_limit]
[-ignore_register_feedback
feedback_slack_cutoff]
[-report_ignored_register_feedback]
[-group group_name]
[-significant_digits digits]
[-nosplit]
[-transition_time]
[-capacitance]
[-crosstalk_delta]
[-trace_latch_borrow]
[-derate]
[-dont_merge_duplicates]
[-pre_commands pre_command_string]
[-post_commands post_command_string]
[-exceptions exception_type]
[-pba_mode effort]
[path_collection]
```

report_timing_derate

Reports derate factors annotated on the current design.

```
int report_timing_derate
[-include_inherited]
[-variation | -aocvm_guardband]
[-significant_digits digits]
[-nosplit]
list object_list
```

report_transitive_fanin

Reports logic in fanin of specified sink objects.

```
string report_transitive_fanin
[-nosplit]
-to sink_list
[-trace_arcs arc_types]
```

report_transitive_fanout

Reports logic in fanout of specified sources.

```
string report_transitive_fanout
[-nosplit]
-clock_tree
-from source_list
[-trace_arcs arc_types]
```

report_units

Reports the unit information.

```
string report_units
[-nosplit]
```

report_user_sensitization

Report user sensitization of an instance or library arc for write_spice_deck output.

```
int report_user_sensitization
[-analysis_type [rise | fall | high | low]]
[-arc arcs_list]
[-library library_name]
[-design design_name]
```

report_variation

Reports variation for timing paths, cells, nets, library cells, and current design.

```
string report_variation
[-verbose]
[-delay_type delay_type]
[-clock_network]
[-slack_lesser_than slack_limit]
[-nworst num_worst_cells]
[-input_pins]
[-transition]
[-all_cells]
[-all_nets]
[-parametric_sensitivity parameter_list]
[-significant_digits digits]
[-nosplit]
[collection1]
```

report_vcd_hierarchy

Reports the hierarchy in the VCD file.

```
string report_vcd_hierarchy
[-pipe_exec command]
[-full_path]
[-find patten]
[file_name]
```

report_wire_load

Reports wire load information.

```
string report_wire_load
[-nosplit]
[cell_names]
```

reset_design

Removes user specified information from design.

```
string reset_design
[-timing]
```

reset_mode

Resets cell mode groups or design mode groups to the default state.

```
Boolean reset_mode
[-type cell | design]
[-group group_list]
[instance_list]
```

reset_noise_parameters

Resets the noise analysis parameters for the current design.

```
int reset_noise_parameters
```

reset_path

Resets specified paths to single-cycle behavior.

```
Boolean reset_path
[-setup] [-hold]
[-rise] [-fall]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
```

reset_scale_parasitics

Resets the scaling that was done previously using *scale_parasitics* command.

```
int reset_scale_parasitics
[net_list]
```

reset_switching_activity

Resets switching activity annotation on nets, pins, ports, and cells of the current design.

```
int reset_switching_activity
[-static_probability]
[-toggle_rate]
[-state_condition state]
[-path_sources name_list]
[-no_hierarchy]
[object_list]
[-quiet]
```

reset_timing_derate

Resets user specified derate factors set either on a design or on a specified list of instances (cells, nets or library cells).

```
int reset_timing_derate
[-hierarchical_net_delay]
[-scalar] [-variation] [-aocvm_guardband]
object_list
```

reset_variation

Resets the association of one or more variations with one or more timing objects.

```
int reset_variation
[-all]
[variation_list]
object_list
```

restore_session

Restore a PrimeTime session from a directory saved by the save_session command.

```
int restore_session
directory_name
```

save_qtm_model

Saves the current Quick Timing Model (QTM) description.

```
string save_qtm_model
[-format format_list]
[-output file_name] [-library_cell]
```

save_session

Saves data of a PrimeTime session in the named directory so that it can be restored later with restore_session.

```
int save_session
[-replace] [-include <include_list> ]
[-only_used_libraries]
dir_name
```

scale_parasitics

Used to scale the parasitics in memory.

```
int scale_parasitics
[-resistance_factor r_factor]
[-ground_capacitance_factor c_factor]
[-coupling_capacitance_factor cc_factor]
[net_list]
```

set_active_clocks

Sets a group of clocks to be active in the current analysis scope.

```
Boolean set_active_clocks
active_clock_list | [all_clocks]
```

set_annotated_check

Sets the setup, hold, recovery, removal, or nochange timing check value between two pins.

```
string set_annotated_check
-setup | -hold
| -recovery | -removal
| -nochange_high | -nochange_low
[-rise]
[-fall]
[-min]
[-max]
[-from from_pins]
[-to to_pins]
[-clock clock_check]
[-cond sdf_expression]
[-worst]
check_value
```

set_annotated_clock_network_power

Annotate power on clock networks.

```
string set_annotated_clock_network_power
 [-internal_power internal_power]
 [-switching_power switching_power]
 [-leakage_power leakage_power]
 [-total_power total_power]
 [-clock clock_object]
```

set_annotated_delay

Sets the net or cell delay value between two pins.

```
string set_annotated_delay
-cell | -net
[-rise]
[-fall]
[-min]
[-max]
[-load_delay load_delay_type]
[-from from_pins]
[-to to_pins]
[-of_objects objects]
[-cond sdf_expression]
[-increment]
[-delta_only]
[-worst]
-variation variation_object
delay_value
```

set_annotated_power

Annotate power on unresolved black-box cells or leaf cells.

```
int set_annotated_power
 -internal_power internal_power
 -leakage_power leakage_power
 cell_list
```

set_annotated_transition

Sets the transition time to be annotated on specified pins in the current design.

```
int set_annotated_transition
[-rise][-fall][-min][-max]
[-delta_only]
slew_value
pin_list
```

set_aocvm_coefficient

Specifies AOCVM random coefficients on cells and library cells for use during an AOCVM analysis.

```
int set_aocvm_coefficient
[-random]
coefficient
object_list
```

set_app_var

Sets the value of an application variable.

```
string set_app_var
-default
var
value
```

set_capacitance

Sets the capacitance attribute to a specified value on specified ports and nets.

Note: This command is obsolete, and has been replaced by the set_load command. Please use set_load instead.

set_case_analysis

Specifies that a port or pin is at a constant logic value 1 or 0, or is considered with a rising or falling transition.

```
string set_case_analysis
value
port_or_pin_list
```

set_clock_gating_check

Specifies the value of setup and hold time for clock gating checks.

```
string set_clock_gating_check
[-setup setup_value]
[-hold hold_value]
[-rise | -fall]
[-high | -low]
[object_list]
```

set_clock_groups

Specifies clock groups that are mutually exclusive or asynchronous with each other in a design so that the paths between these clocks are not considered during the timing analysis.

```
Boolean set_clock_groups
[-physically_exclusive |
-logically_exclusive | -asynchronous]
[-allow_paths]
[-name name]
[-group clock_list]*
```

set_clock_latency

Specifies latency of clock network.

```
string set_clock_latency
[-clock clock_list]
[-rise][-fall]
[-min][-max]
[-source]
[-late][-early]
[-dynamic dynamic_component_of_delay]
[-pll_shift]
delay
object_list
```

set_clock_sense

Specifies unateness propagating foward for pins with respect to clock source.

```
string set_clock_sense
[-stop_propagation | -positive | -negative |
-pulse pulse_type ]
[-clocks clock_list]
object_list
```

set_clock_transition

Specifies transition time of register clock pins.

```
string set_clock_transition
[-rise]
[-fall]
[-min]
[-max]
transition
clock_list
```

set_clock_uncertainty

Specifies the uncertainty (skew) of specified clock networks.

```
string set_clock_uncertainty
uncertainty
[object_list |
 -from from_clock
  | -rise_from rise_from_clock
  | -fall_from fall_from_clock
 -to to_clock
  | -rise_to rise_to_clock
  | -fall_to fall_to_clock]
[-rise]
[-fall]
[-setup]
[-hold]
```

set_connection_class

Sets the connection class value on ports.

```
int set_connection_connection_class
connection_class_value
object_list
```

set_context_margin

Specifies the margin by which to tighten or relax constraints.

```
string set_context_margin
[-percent]
[-relax]
[-min]
[-max]
value
[object_list]
```

set_coupling_separation

Create a separation constraint on nets.

```
int set_coupling_separation
[-pairwise pair_nets]
nets
```

set_current_command_mode

Sets the current command mode.

```
string set_current_command_mode
-mode command_mode | -command command
```

set_current_power_domain

Sets the specific power domains defined by the UPF create_power_domain command to be included in the power analysis. As default (if not specified), the whole design covered by all the defined power domains are included in the power analysis. The commands can take one single power domain or a combination of power domains in the design.

This command has no effect on power results in non-UPF mode.

```
int set_current_power_domain
list_of_power_domains
list_of_power_domains
```

set_current_power_net

Sets the specific power net(s) defined by UPF create_supply_net command(s) to be included in the power analysis. As default (if not specified), the whole design covered by all the defined supply nets are included in the power analysis. The commands can take one single power net or a combination of power nets in the design.

This command has no effect on power results in non-UPF mode.

```
int set_current_power_net list_of_power_nets
list_of_power_nets
```

set_data_check

Sets data-to-data checks using the specified values of setup and hold time.

```
string set_data_check
{-from from_object
 | -rise_from from_object
 | -fall_from from_object}
{-to to_object
 | -rise_to to_object
 | -fall_to to_object}
[-setup | -hold]
[-clock clock_object]
[check_value]
```

set_design_top

Sets or gets the current design in PrimeTime. It is a synonym for the current_design command.

```
string set_design_top
[design_name]
```

set_disable_clock_gating_check

Disables the clock gating check for specified objects in the current design.

```
string set_disable_clock_gating_check
object_list
```

set_disable_timing

Disables timing arcs in a circuit.

```
string set_disable_timing
[-from from_pin_name -to to_pin_name]
object_list
```

set_distributed_parameters

Configures the distributed environment.

```
Boolean set_distributed_parameters
 [-script script]
 [-shell rsh | remsh | ssh]
 [-collection_levels collection_level]
```

set_distributed_variables

Passes tcl variables from the master to the slaves.

```
Boolean set_distributed_variables
[-pre_commands pre_command_string] (string
containing pre commands to be executed at
slave)
[-post_commands post_command_string] (string
containing post commands to be executed at
slave)
```

set_domain_supply_net

Set the primary power net and primary ground net of an existed power_domain.

```
int set_domain_supply_net
domain_name
-primary_power_net supply_net_name
-primary_ground_net supply_net_name
```

set_dont_touch

Sets the dont_touch attribute on cells, nets, designs, and library cells to prevent synthesis from replacing or modifying them during optimization.

```
string set_dont_touch
object_list [value]
```

set_dont_touch_network

Sets the dont_touch attribute on clock networks for synthesis.

```
string set_dont_touch_network
object_list
```

set_drive

Sets the resistance to a specified value on specified input or inout ports in the current design.

```
string set_drive
[-rise] [-fall]
[-min] [-max]
resistance_value port_list
```

set_drive_resistance

Sets drive resistance for input or inout ports.

Note: This command is obsolete, and has been replaced by the set_drive command. Use set_drive instead.

```
string set_drive_resistance
[-rise]
[-fall]
[-min]
[-max]
resistance
port_list
```

set_driving_cell

Sets the port driving cell.

```
string set_driving_cell
[-lib_cell lib_cell_name]
[-rise]
[-fall]
[-min]
[-max]
[-library lib_name]
[-pin pin_name]
[-from_pin from_pin_name]
[-multiply_by factor]
[-dont_scale]
[-no_design_rule]
[-input_transition_rise rtrans]
[-input_transition_fall ftrans]
[-clock clock_name]
[-clock_fall]
port_list
```

set_equal

Sets two ports to be logically equivalent.

```
string set_equal
port1 port2
```

set_false_path

Identifies paths in a design that are to be marked as false, so that they are not considered during timing analysis.

```
Boolean set_false_path
[-setup] [-hold]
[-rise] [-fall]
[-reset_path]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
```

set_fanout_load

Sets fanout_load for output ports in the current design.

```
string set_fanout_load
value port_list
```

set_host_options

Specifies host options for compute resources.

```
int set_host_options
-name name
[-submit_command command]
[-num_processes number]
[-32bit]
[machine_name]
```

set_ideal_latency

Specifies ideal latency values for the pins in an ideal network.

```
int set_ideal_latency
[-rise] [-fall]
[-min] [-max]
value
object_list
```

set_ideal_network

Marks a set of ports or pins in the design as sources of an ideal network. This disables timing update of cells and nets in the transitive fanout of the specified objects.

```
int set_ideal_network
[-no_propagate]
object_list
```

set_ideal_transition

Specifies ideal transition values for the pins in an ideal network.

```
int set_ideal_transition
[-rise] [-fall]
[-min] [-max]
value
object_list
```

set_input_delay

Defines the arrival time relative to a clock.

```
string set_input_delay
[-clock clock_name]
[-reference_pin pin_port_name]
[-clock_fall]
[-level_sensitive]
[-rise]
[-fall]
[-max]
[-min]
[-add_delay]
[-network_latency_included]
[-source_latency_included]
delay_value
port_pin_list
```

set_input_noise

Sets a noise bump for a pin or port.

```
int set_input_noise
[-add_noise]
[-above]
[-below]
[-low]
[-high]
[-height width_value]
[-width height_value]
object_list
```

set_input_transition

Sets a fixed transition time on input or inout ports.

```
string set_input_transition
[-rise]
[-fall]
[-min]
[-max]
[-clock clock_name]
[-clock_fall]
transition
port_list
```

set_isolation

Defines the UPF isolation strategy for the power domains in the design.

```
int set_isolation
isolation_strategy
-domain power_domain
[-isolation_power_net isolation_power_net]
[-isolation_ground_net isolation_ground_net]
[-clamp_value  0 | 1 | Z | latch]
[-applies_to inputs | outputs | both]
[-elements objects]
[-no_isolation]
```

set_isolation_control

Provides additional options needed for creating isolation cells.

```
status set_isolation_control
isolation_strategy
-domain power_domain
-isolation_signal isolation signal
[-isolation_sense low | high]
[-location self | parent]
```

set_lcd_pulse_width_multipliers

Sets LCD multipliers specific to pulse width check, when using LCD operating conditions.

```
int set_lcd_pulse_width_multipliers
-mult_worst worst_case_multiplier
-mult_nominal nominal_multiplier
-mult_best best_case_multiplier
-library library_name
name
```

set_level_shifter_strategy

Sets the type of strategy to use for reporting the signal level mismatches in the design.

```
int set_level_shifter_strategy
-rule all | low_to_high | high_to_low
```

set_level_shifter_threshold

Sets the minimum threshold beyond which the voltage adjustment is required.

```
int set_level_shifter_threshold
-voltage volt
-percent diff
```

set_lib_rail_connection

Sets a physical power pin on a library cell.

```
int set_lib_rail_connection
-lib_cells lib_cells
-lib_rail_name name of power rail (NOT
SUPPORTED)
-lib_pin name of library pin
```

set_library_driver_waveform

Sets the driver waveform used to characterize the timing library.

```
int set_library_driver_waveform
-type type
[lib_objs]
```

set_load

Sets the capacitance to a specified value on the specified ports and nets in the current design.

```
Boolean set_load
[-min]
[-max]
[-rise]
[-fall]
[-subtract_pin_load]
[-pin_load]
[-wire_load]
capacitance
objects
```

set_max_area

Sets the max_area attribute on the current design to a specified value.

```
int set_max_area area_value
```

set_max_capacitance

Sets maximum capacitance for pins, ports, clocks or designs.

```
string set_max_capacitance
capacitance_value
[-clock_path][-data_path]
[-rise][-fall]
object_list
```

set_max_delay

Specifies a maximum delay for timing paths.

```
Boolean set_max_delay
[-rise] [-fall]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
[-reset_path]
delay_value
```

set_max_fanout

Sets maximum fanout for input ports or designs.

```
string set_max_fanout
fanout_value
object_list
```

set_max_time_borrow

Limits time borrowing for latches.

```
string set_max_time_borrow
value
object_list
```

set_max_transition

Sets maximum transition for pins, ports, clocks or designs with respect to the main library trip-points.

```
string set_max_transition
transition_value
[-clock_path][-data_path]
[-rise][-fall]
object_list
```

set_message_info

Set some information about diagnostic messages.

```
string set_message_info
-id message_id [-limit max_limit|-stop_on]
```

set_min_capacitance

Sets minimum capacitance for ports or designs.

```
string set_min_capacitance
capacitance_value
object_list
```

set_min_delay

Specifies a minimum delay for timing paths.

```
Boolean set_min_delay
[-rise] [-fall]
[-reset_path]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
delay_value
```

set_min_library

Sets the library to be used for minimum delay analysis

The set_min_library command is used to relate a minimum conditions library to a maximum conditions library.

```
string set_min_library
[-min_version min_library]
[-none]
max_library
```

set_min_pulse_width

Sets a minimum pulse width constraint for specified design objects.

```
string set_min_pulse_width
[-low]
[-high]
value
[object_list]
```

set_mode

Selects the active mode of cell mode groups or design mode groups

```
Boolean set_mode
[-type cell | design]
[mode_list]
[instance_list]
```

set_multi_scenario_license_limit

Specifies the upper limit on the number of licenses, of a particular feature, the master in multi-scenario analysis can checkout for dynamic allocation among its slave processes.

```
int set_multi_scenario_license_limit
-feature feature_name
[-force_checkout]
number
```

set_multicycle_path

Defines the multicycle path.

```
Boolean set_multicycle_path
[-setup] [-hold]
[-rise] [-fall]
[-start] [-end]
[-reset_path]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]*
[-rise_through rise_through_list]*
[-fall_through fall_through_list]*
[-to to_list
 | -rise_to rise_to_list
 | -fall_to fall_to_list]
path_multiplier
```

set_noise_derate

Sets noise derate information for the current design.

```
int set_noise_derate
[-above]
[-below]
[-low]
[-high]
[-height_offset hoffset]
[-height_factor hfactor]
[-width_factor wfactor]
[object_list]
```

set_noise_immunity_curve

Sets noise immunity curve for a library pin or port.

```
int set_noise_immunity_curve
[-above]
[-below]
[-low]
[-high]
[-height height_value]
[-width width_value]
[-area area_value]
object_list
```

set_noise_lib_pin

Sets an equivalent noise library pin for a driver or load.

```
int set_noise_lib_pin
pins
lib_pin
```

set_noise_margin

Sets noise margin for a library pin, port, or pin.

```
int set_noise_margin
[-above]
[-below]
[-low]
[-high]
margin_value
object_list
```

set_noise_parameters

Defines the noise analysis parameters for the current design.

```
int set_noise_parameters
[-ignore_arrival]
[-include_beyond_rails]
[-analysis_effort low | high]
[-enable_propagation]
[-analysis_mode report_at_source |
report_at_endpoint]
```

set_operating_conditions

Defines the operating conditions (or environmental characteristics) for the *current design*.

```
int set_operating_conditions
[-analysis_type single | bc_wc |
on_chip_variation]
[-library lib]
[condition]
[-min min_condition]
[-max max_condition]
[-min_library min_lib]
[-max_library max_lib]
[-object_list objects]
```

set_opposite

Sets two ports to be logically opposite.

```
string set_opposite
port1
port2
```

set_output_delay

Sets output path delay values for the current design.

```
string set_output_delay
[-clock clock_name]
[-reference_pin pin_port_name]
[-clock_fall]
[-level_sensitive]
[-rise]
[-fall]
[-max]
[-min]
[-add_delay]
[-network_latency_included]
[-source_latency_included]
[-group_path group_name]
delay_value
port_pin_list
```

set_parasitic_corner

Sets a parasitic corner for the timing analysis in the presence of variation-aware parasitics.

```
Boolean set_parasitic_corner
 -name corner_name
 file_name
```

set_port_fanout_number

Sets number of external fanout points on ports.

```
string set_port_fanout_number
[-min]
[-max]
fanout_number
port_list
```

set_power_analysis_options

Sets the options for power analysis.

```
int set_power_analysis_options
[-static_leakage_only]
[-variation_quantile quantile]
[-waveform_interval sampling_interval]
[-cycle_accurate_cycle_count cycles]
[-cycle_accurate_clock clock]
[-waveform_format fsdb | out | none]
[-waveform_output file_prefix]
[-include top | all_without_leaf |
all_with_leaf]
[-include_groups group_list]
[-cells cell_list]
```

set_program_options

Defines some runtime options for PrimeTime and PrimeTime-SI.

```
int set_program_options
[-enable_high_capacity]
[-disable_high_capacity]
[-enable_eco]
[-disable_eco]
[-enable_fast_analysis]
```

set_propagated_clock

Specifies propagated clock latency.

```
string set_propagated_clock
object_list
```

set_pulse_clock_max_transition

Sets maximum transition for pulse generator input and pulse clock network with respect to the main library trip-points.

```
string set_pulse_clock_max_transition
transition_value
[-rise][-fall]
[-transitive_fanout]
object_list
```

set_pulse_clock_max_width

Sets maximum pulse width constraint for pulse generator network.

```
string set_pulse_clock_max_width
pulse_width_value
[-transitive_fanout]
object_list
```

set_pulse_clock_min_transition

Sets minimum transition at the input of pulse generator with respect to the main library trip-points.

```
string set_pulse_clock_min_transition
transition_value
[-rise][-fall]
object_list
```

set_pulse_clock_min_width

Sets minimum pulse width constraint for pulse generator network.

```
string set_pulse_clock_min_width
pulse_width_value
[-transitive_fanout]
object_list
```

set_qtm_attribute

Sets an attribute to the specified value on QTM object(s).

```
string set_qtm_attribute
-class class_name
attr_name
value
[object_names]
```

set_qtm_global_parameter

Sets a global parameter for QTM.

```
string set_qtm_global_parameter
[-param parameter]
[-lib_cell lib_cell]
[-pin pin_name]
[-clock pin_name]
[-value parameter_value]
```

set_qtm_port_drive

Sets the drive on the QTM port.

```
string set_qtm_port_drive
[-type drive_type]
[-value drive_value]
[-input_transition_rise rtrans]
[-input_transition_fall ftrans]
[-subtract_max_delay_from_total]
port_list
```

set_qtm_port_load

Sets load on Quick Timing Model (QTM) ports.

```
string set_qtm_port_load
[-type load_type]
[-factor multiplication_factor]
[-value load_value]
port_list
```

set_qtm_technology

Sets the QTM technology variables.

```
string set_qtm_technology
[-library name]
[-max_transition trans_value]
[-min_transition trans_value]
[-max_capacitance cap_value]
[-min_capacitance trans_value]
[-wire_load_model wlm_name]
```

set_rail_voltage

Sets power rail voltage on cells.

```
int set_rail_voltage
[-rail_value rvalue | -rail_list
rname_value_list]
[-dynamic_rail_value dynamic_component |
-dynamic_rail_list dynamic_component_list]
[-min]
[-max]
cell_list
```

set_related_supply_net

Associates an external supply net to the port of the design.

```
status set_related_supply_net
[power_net]
[-object_list ports]
[-reset]
[-ground ground_net]
[-power power_net]
```

set_resistance

Sets the ba_net_resistance attribute with a resistance value on specified nets.

```
int set_resistance
[-min] [-max] resistance_value object_list
```

set_retention

Defines the UPF retention strategy for the power domains in the design.

```
int set_retention
retention_strategy
-domain power_domain
[-retention_power_net retention_power_net]
[-retention_ground_net retention_ground_net]
[-elements objects]
```

set_retention_control

Defines the UPF retention control signals for the defined UPF retention strategy.

```
int set_retention_control
retention_strategy
-domain power_domain
-save_signal {save_signal save_sense}
-restore_signal {restore_signal
restore_sense}
```

set_rtl_to_gate_name

Sets the mapping between RTL and gate-level objects. This mapping is used if the user is reading RTL backward SAIF file or RTL VCD file for power estimation.

```
int set_rtl_to_gate_name
-rtl rtl_name
-gate gate_name
-substitute {from_string to_string}
-inverted
```

set_scope

Specify the current UPF scope. Return the current UPF scope prior to the execution of this command as a full path string relative to the current design top if successful and null string if it fails.

```
string set_scope
[instance]
```

set_setup_hold_pessimism_reduction

Set the optimization constraints for setup-hold pessimism reduction.

```
set_setup_hold_pessimism_reduction
-mode SHPR mode
[-setup_cutoff setup_cutoff_slack]
[-hold_cutoff hold_cutoff_slack]
```

set_si_aggressor_exclusion

Sets the given nets to be exclusive while switching in the given direction, when they are aggressors to the same victim net.

```
int set_si_aggressor_exclusion
[-number_of_active_aggressors n]
[-rise]
[-fall]
anets
```

set_si_delay_analysis

Sets coupling information on nets for crosstalk analysis.

```
int set_si_delay_analysis
[-reselect rnets]
[-ignore_arrival inets]
[-exclude]
[-victims vnets]
[-aggressors anets]
[-rise]
[-fall]
[-min]
[-max]
```

set_si_delay_disable_statistical

Disables composite aggressor statistical analysis on nets for crosstalk analysis.

```
int set_si_delay_disable_statistical
dnets
```

set_si_noise_analysis

Sets coupling information on nets for noise analysis.

```
int set_si_noise_analysis
[-ignore_arrival inets]
[-exclude]
[-victims vnets]
[-aggressors anets]
[-above]
[-below]
[-low]
[-high]
```

set_si_noise_disable_statistical

Disables composite aggressor statistical analysis on nets for noise analysis.

```
int set_si_noise_disable_statistical
dnets
```

set_steady_state_resistance

Sets steady-state resistance for a library pin or port.

```
int set_steady_state_resistance
[-above]
[-below]
[-low]
[-high]
res_value
object_list
```

set_supply_net_probability

Sets the static probability annotation on selected supply nets. This probability affects average power analysis.

```
string set_supply_net_probability
supply_nets [static_prob] [-remove]
```

set_switching_activity

Sets switching activity annotation on selected nets, pins, ports, and cells of the current design.

```
int set_switching_activity
[-static_probability value]
[-toggle_count count]
[-clock_derate value]
[-glitch_count count]
[-state_condition state]
[-path_sources name_list]
[-rise_ratio ratio_value]
[-period period_value]
[-base_clock clock]
[-type object_type_list]
[-no_hierarchy]
[object_list]
[-clocks clocks]
[-quiet]
```

set_temperature

Applies an operating temperature on a list of cell objects.

```
int set_temperature
max_case_temperature
[-min min_case_temperature]
-object_list list_of_cells
```

set_timing_derate

Sets delay derating factors for either the current design or a specified list of instances (cells, library cells, or nets).

```
int set_timing_derate
-early | -late
[-rise] [-fall]
[-clock] [-data]
[-cell_delay] [-cell_check] [-net_delay]
[-static] [-dynamic]
[-scalar | -variation | -aocvm_guardband]
derate_value
object_list
```

set_units

Checks the specified units with the main library units. The command fails if the units specified do not match the main library units.

```
int set_units
[-time [optional float][optional
scale_value]s]
[-capacitance [optional float][optional
scale_value]F]
[-resistance [optional float][optional
scale_value]Ohm]
[-voltage [optional float][optional
scale_value]V]
[-current [optional float][optional
scale_value]A]
[-power [optional float][optional
scale_value]W]
```

set_unix_variable

This is a synonym for the setenv command.

set_user_attribute

Sets a user attribute to a specified value on an object.

```
string set_user_attribute
[-class class_name]
[-quiet]
object_spec
attr_name
value
```

set_user_sensitization

Specify user sensitization of an instance or library arc for write_spice_deck output.

```
int set_user_sensitization
-analysis_type [rise | fall | high | low]
arcs_list
-event_pins input_pins_list
-event_states list_of_r_f_1_and_0s
[-event_step
separation_time_in_library_unit]
[-initial_condition { node_name
volt_in_library_unit }]
[-tie_high logic_one_input_pin_list]
[-tie_low logic_zero_input_pin_list]
[-use_pwl_for_clock]
```

set_variation

Sets one or more variations onto one or more timing objects.

```
int set_variation
variation_list
[object_list]
```

set_variation_correlation

Applies a correlation type to a variation(s) or to all instances of that variation(s). May also apply a cross-correlation to a vector of variations.

```
int set_variation_correlation
-name variation_correlation_name
-correlation correlation_object
[object_list]
[-all]
```

set_variation_library

Sets the library that defines a point in the variation space.

```
int set_variation_library
[-parameter_names variation_name_list]
[-values variation_value_list]
[-reference_value]
[library_file_name]
[-link_library link_library_list]
```

set_variation_quantile

Determines quantiles for analysis and reporting.

```
int set_variation_quantile
[-quantile_high high_value]
[-quantile_low low_value]
```

set_voltage

Applies an operating voltage on a list of power nets or pg pins.

```
int set_voltage
max_case_voltage
[-min min_case_value]
[-dynamic dynamic_max_case_value]
[-min_dynamic dynamic_min_case_value]
[-object_list list_of_power_nets]
[-cell cell]
[-pg_pin_name pg_pin]
```

set_wire_load_min_block_size

Sets the minimum block area for automatic wire load selection. Any blocks with an area below the minimum are promoted to the minimum.

```
int set_wire_load_min_block_size
block_size
```

set_wire_load_mode

Sets wire load mode for the current design.

```
string set_wire_load_mode m
ode_name
```

set_wire_load_model

Sets wire load model on designs, ports, or hierarchical cells.

```
int set_wire_load_model
-name model_name
[-library lib_spec]
[-min]
[-max]
[object_list]
```

set_wire_load_selection_group

Sets the wire load selection group for current design.

```
int set_wire_load_selection_group
[-min]
[-max]
[-library lib_spec]
selection_group_name
[object_list]
```

setenv

Sets the value of a system environment variable.

```
string setenv
variable_name new_value
```

sh

Executes a command in a child process.

```
string sh
[args]
```

size_cell

Relinks leaf cells to a new library cell that has the required drive strength (or other properties).

```
int size_cell
[-current_library]
[-libraries lib_spec]
cell_list
lib_cell
```

sizeof_collection

Returns the number of objects in a collection.

```
int sizeof_collection
collection1
```

sort_collection

Sorts a collection based on one or more attributes, resulting in a new, sorted collection. The sort is ascending by default.

```
collection sort_collection
[-descending] collection1
criteria
```

source

Read a file and evaluate it as a Tcl script.

```
string source
[-echo] [-verbose] [-continue_on_error] file
```

start_gui

Starts the Primetime GUI.

```
string start_gui
[-file name_of_script_file]
[-no_windows]
```

start_hosts

Start the hosts specified by the set_host_options command.

```
int start_hosts
[-timeout seconds]
[-min_hosts num_hosts]
```

start_profile

Start profiling PrimeTime commands.

```
Boolean start_profile
```

stop_gui

Stops the Primetime GUI.

```
string stop_gui
```

stop_hosts

Stops all hosts that have been started.

```
int stop_hosts
```

stop_profile

Stop profiling PrimeTime commands.

```
boolean stop_profile
```

sub_variation

Subtracts one variation from another. Returns a collection (that corresponds to this difference variation).

```
collection sub_variation
variation_list
```

suppress_message

Disables printing of one or more informational or warning messages.

```
string suppress_message
[message_list]
```

swap_cell

Swaps one or more cells with a new design or library cell.

```
int swap_cell cell_list swap_in
[-dont_preserve_constraints]
[-file file_name]
[-format file_format]
```

transform_exceptions

Performs transformation on timing exceptions.

```
[-from from_list]
[-rise_from rise_from_list]
[-fall_from fall_from_list]
[-through through_list]
[-rise_through rise_through_list]
[-fall_through fall_through_list]
[-to to_list]
[-rise_to rise_to_list]
[-fall_to  fall_to_list]
[-verbose]
[-dry_run]
[-remove_ignored reason]
[-use_to_for_endpoints]
[-flatten]
```

translate_stamp_model

Translates a STAMP model to a LIB format.

```
string translate_stamp_model
-model_file model_file_name
-data_file data_file_name
-output output_file_name
```

unalias

Removes one or more aliases.

```
string unalias pattern
```

unset_rtl_to_gate_name

Specifies a name without RTL to gate name mapping.

```
int unset_rtl_to_gate_name
name
```

unsuppress_message

Enables printing of one or more suppressed informational or suppressed warning messages.

```
string unsuppress_message
[messages]
```

update_noise

Performs static crosstalk noise analysis for the current design.

```
int update_noise
[-full]
```

update_power

Updates power information on the current design.

```
int update_power
```

update_scope_data

Updates the scope data captured and stored in the scope file.

```
int update_scope_data
[-remove_block blk_names]
[-remove_scenario scenario_names]
[-merge_with other_scope_files]
[-keep_last]
file_name
```

update_timing

Updates timing information on the current design.

```
string update_timing
[-full]
```

upf_version

Specify the version for the UPF file/syntax.

```
string upf_version
[version_id]
```

variation_correlation

Computes the correlation between two variations. These variations must have been obtained through attributes (for example, get_attribute $stat_path variation_slack) or through a statistical operation (for example, add_variation, sub_variation, max_variation, or min_variation) performed on variations obtained from a get_attribute. The function returns a float value (in string format). The value -2.0 is returned if an error is detected.

```
string variation_correlation
variation1
variation2
```

which

Locates a file and displays its pathname.

```
string which filename_list
```

write_activity_waveforms

Create activity waveforms from VCD

```
int write_activity_waveforms
 [-output file_name]
 [-interval sampling_interval]
 [-hierarchical_levels level]
 [-coverage]
 [-exclude_signals list_of_signals]
 [-exclude_cells list_of_modules]
 -vcd file_name
 [-time time_list]
 [-peak_window window_size]
[-peak_type min | max]
 [-strip_path path]
 [-format format]
 [-verbose]
```

write_app_var

Writes a script to set the current variable values.

```
string write_app_var
-output file
[-all | -only_changed_vars]
[pattern]
```

write_arrival_annotations

Writes arrival and slew annotations for ILMs or contexts of the given list of instances or for all top level instances as a script of commands.

```
int write_arrival_annotations
[-instances instance_list]
[-context]
[-design]
```

write_astro_changes

Outputs netlist changes and coupling separations from this session in native Astro formats.

```
int write_astro_changes
-format type
[-dont_merge_changes] file_name
```

write_binary_aocvm

Creates a binary AOCVM file from an AOCVM file.

```
int write_binary_aocvm
[-compress]
aocvm_file
binary_file
```

write_changes

Outputs netlist changes that have been recorded during this session.

```
int write_changes
[-format chg_format]
[-output file_name]
[-reset]
```

write_context

Writes the timing context information, for specified instances, as a pt_shell, dc_shell, or dc_shell-t script.

```
string write_context
[-timing] [-environment]
[-design_rules]
[-constant_inputs]
[-derive_file_name]
[-prefix file_prefix]
[-extension file_extension]
[-script_directory directory]
[-separator name_separator]
[-output file_name]
[-format script_format]
[-nosplit]
cell_list
```

write_ilm_netlist

Writes out a flattened Verilog netlist corresponding to the interface logic for the current design.

```
int write_ilm_netlist
[-include_all_net_pins]
[-verbose]
file_name
```

write_ilm_parasitics

Writes out in SPEF format all annotated parasitics on the interface logic for the current design.

```
int write_ilm_parasitics
[-input_port_nets]
[-constant_nets]
[-compress compression]
[-format format]
file_name
```

write_ilm_script

Writes constraints, assertions and exceptions for interface logic as a script for PrimeTime or Design Compiler.

```
int write_ilm_script
[-instance]
[-format script_format]
[-compress compression]
[-nosplit]
file_name
```

write_ilm_sdf

Writes out a Version 2.1-compliant Standard Delay Format (SDF) back-annotation file for the interface logic of the current design.

```
int write_ilm_sdf
[-input_port_nets]
[-output_port_nets]
[-significant_digits digits]
[-annotated]
[-no_edge]
[-compress compression]
[-version sdf_version]
file_name
```

write_interface_timing

Generates an interface timing ASCII report for a gate-level netlist, an interface logic model (ILM), or an extracted timing model (ETM) design.

```
int write_interface_timing
file_name
[-ignore_ports port_list]
[-significant_digits digits]
[-nosplit]
[-timing_type ttype]
[-verbose]
[-include incl_list]
[-latch_level level]
```

write_parasitics

Writes out annotated parasitics information for the current design.

```
Boolean write_parasitics
 -format file_fmt
 -nets net_list
 -no_name_map
 file_name
```

write_physical_annotations

Writes annotated delays and parasitics for a hierarchical cell.

```
string write_physical_annotations
[-sdf sdf_file]
[-version sdf_version]
[-nets_only]
[-cells_only]
[-boundary_nets]
[-parasitics parasitics_file]
[-append script_file]
[-format script_format]
cell
```

write_pi_parasitics

Writes out cached pi-model parasitics information for the current design.

```
Boolean write_pi_parasitics
-format file_fmt
[-annotated_segments]
file_name
```

write_profile

Writes profiling information for PrimeTime scripts

```
Boolean write_profile
```

write_saif

Writes a backward Switching Activity Interchange Format (SAIF) file.

```
int write_saif
file_name
[-cells cell_list]
[-derate_glitch value]
[-rtl]
[-propagated]
[-exclude_sdpd]
[-no_hierarchy]
```

write_script

Writes design constraints as a script of commands for PrimeTime or Design Compiler.

```
int write_script
[-no_annotated_delay]
[-no_annotated_check]
[-format script_format]
[-output file_name]
[-compress compression]
[-include categories list]
[-nosplit]
```

write_sdc

Writes out a script in Synopsys Design Constraints (SDC) format.

```
int write_sdc
file_name [-version sdc_version]
[-compress compression]
[-include categories list]
[-nosplit]
```

write_sdf

Writes a Standard Delay Format (SDF) back-annotation file.

```
string write_sdf
[-version sdf_version]
[-no_cell_delays]
[-no_timing_checks]
[-no_net_delays]
[-input_port_nets]
[-output_port_nets]
[-significant_digits digits]
[-enabled_arcs_only]
[-no_internal_pins]
[-instance inst_name]
[-context sdf_context]
[-map sdf_map_file_list]
[-annotated]
[-levels level]
[-no_edge]
[-compress compression]
[-include include_list]
[-exclude exclude_list]
[-no_negative_values values_list]
[-no_edge_merging arc_type_list]
[-delay_calculation_only_mode]
file_name
```

write_sdf_constraints

Writes to a disk file the constraints for the place and route layout tools.

```
int write_sdf_constraints
[-version 1.0 | 2.1]
[-max_paths max_path_number]
[-nworst nworst_number]
[-slack_lesser_than slack_value]
[-cover_design]
[-from from_list
 | -rise_from rise_from_list
 | -fall_from fall_from_list]
[-through through_list]
[-rise_through through_list]
[-fall_through through_list]
[-to to_list]
[-significant_digits digits]
[-compress compression]
[-context sdf_context]
file_name
```

write_spice_deck

Writes to a SPICE deck the paths or arcs generated by get_timing_paths or get_timing_arcs.

```
int write_spice_deck
[-align_aggressors]
[-analysis_type type]
[-header header_file_name]
[-initial_delay delay]
[-logic_one_name v1name]
[-logic_one_voltage v1]
[-logic_zero_name v0name]
[-logic_zero_voltage v0]
[-minimum_transition_time trans]
[-output file_name]
[-sub_circuit_file spice_sub_circuit_file]
[-sweep_size number_of_points]
[-sweep_step num]
[-time_precision precision]
[-transient_size tran_size]
[-transient_step tran_step]
[-use_probe]
[-user_measures user_measure_list]
[-sample_size number_of_samples]
paths_arcs_list
```

PrimeTime Variables

PrimeTime defines a set of variables that are used to control its behavior.

For a list of all variables and their current values, enter the following command from within pt_shell:

```
pt_shell> printvar
```

The syntax for setting a variable is

```
pt_shell> set variable_name value
```

arch

This is a synonym for the read-only sh_arch variable.

Default value for this variable is platform-dependent.

auto_link_disable

Disables the auto-link process.

Default value for this variable is false.

auto_wire_load_selection

Default value for this variable is true.

bus_naming_style

Default value for this variable is %s[%d].

case_analysis_log_file

Specifies the name of the file into which the details of case analysis propagation are written.

Default value for this variable is "" (empty).

case_analysis_propagate_through_icg

Determines whether case analysis is propagated through integrated clock gating cells.

Default value for this variable is false.

case_analysis_sequential_propagation

Determines whether case analysis is propagated across sequential cells.

Default value for this variable is never.

collection_deletion_effort

Default value for this variable is low.

collection_result_display_limit

Sets the maximum number of objects that can be displayed by any command that displays a collection.

Default value for this variable is 100.

create_clock_no_input_delay

Default value for this variable is false.

dbr_ignore_external_links

Default value for this variable is false.

default_oc_per_lib

Enables the use of a default operating condition per individual library.

Default value for this variable is true.

disable_case_analysis

Specifies whether case analysis is disabled.

Default value for this variable is false.

disable_case_analysis_ti_hi_lo

Specifies if logic constants should be propagated from pins that are tied to a logic constant value.

Default value for this variable is false.

eco_alternative_area_ratio_threshold

Specifies the maximum allowable area increase of a cell resize operation during the fixing process.

Default value for this variable is 0.

eco_instance_name_prefix

Specifies the prefix used in generating insert_buffer cell instance names.

Default value for this variable is U.

eco_net_name_prefix

Specifies the prefix used in generating insert_buffer net names.

Default value for this variable is net.

eco_write_changes_prepend_libfile_to_libcell

Prepend link library file name information to library cell references in the Bwrite_changes change list.

Default value for this variable is false.

eco_write_changes_prepend_libname_to_libcell

Prepend link library information to library cell references in the write_changes change list.

Default value for this variable is true.

enable_license_auto_reduction

Determines whether or not the master returns licenses to the license server after a slave has finished using them.

Default value for this variable is false.

enable_page_mode

This is a synonym for the sh_enable_page_mode variable.

Default value for this variable is false.

extract_model_capacitance_limit

Defines the maximum bound on the capacitance value for output ports of the netlist.

Default value for this variable is 64.0.

extract_model_clock_transition_limit

Defines the maximum bound on the transition time (slew) for ports that transitively drive the CLK pins of registers.

Default value for this variable is 5.

extract_model_data_transition_limit

Defines the maximum bound on the transition time (slew) for ports that transitively drive the D pins of registers.

Default value for this variable is 5.

extract_model_db_naming_compatibility

Determines whether the library name used in the DB format extracted model (ETM) should maintain the same naming style as before.

Default value for this variable is true.

extract_model_enable_report_delay_calculation

Determines report delay calculation to be performed on the timing arcs contained in models.

Default value for this variable is true.

extract_model_gating_as_nochange
Controls the conversion from clock_gating setup/hold arcs into nochange arcs in the extracted model.

Default value for this variable is false.

extract_model_include_ideal_clock_network_latency
Use this variable to control the behavior of accounting user defined network latencies for ideal clocks in the extracted timing models(ETM). By default, this variable is *false* and ETM does not account for any network latency for ideal clock trees, meaning delays to registers clocked by ideal clocks are always treated as 0.0 in the delay arcs.

Default value for this variable is false.

extract_model_keep_inferred_nochange_arcs
Controls whether to keep PrimeTime inferred nochange relationships as nochange timing arcs in the extracted model.

Default value for this variable is false.

extract_model_lib_format_with_check_pins
Determines if PrimeTime model extraction should write the internal check pins created for DB format models explicitly in the lib format model files.

Default value for this variable is false.

extract_model_merge_clock_gating
Indicates whether to merge clock gating setup and hold constraints with only nonclock gating clock constraints.

Default value for this variable is false.

extract_model_noise_iv_index_lower_factor

Controls the scale factor of the minimum index value used to create a steady-state current table (i.e., I-V curve).

Default value for this variable is -1.0.

extract_model_noise_iv_index_upper_factor

Controls the scale factor of the minimum index value used to create a steady-state current table (i.e., I-V curve).

Default value for this variable is 2.0.

extract_model_noise_width_points

Selects the exact noise width points of extracted noise immunity tables.

Default value for this variable is 5.

extract_model_num_capacitance_points

Controls the size of extracted timing tables by defining the number of capacitance (load) points in these tables.

Default value for this variable is 5.

extract_model_num_clock_transition_points

Controls the size of extracted timing tables by defining the number of clock transition time (slew) points in these tables.

Default value for this variable is 5.

extract_model_num_data_transition_points

Controls the size of extracted timing tables by defining the number of data transition time (slew) points in these tables.

Default value for this variable is 5.

extract_model_num_noise_iv_points

Controls the size of extracted noise steady-state current tables (i.e., I-V curve) by defining the number of index (i.e., voltage) points in these tables.

Default value for this variable is 10.

extract_model_num_noise_width_points

Controls the size of extracted noise immunity tables by defining the number of noise width points in these tables.

Default value for this variable is 5.

extract_model_single_pin_cap

This variable is to provide backward compatability with the introduction of min/max rise/fall specific pin capacitances in accounting for Miller effect. When "true"(the default value), it indicates that the models extracted will keep only a single capacitance value for a pin. The capacitance written is the maximum of all the min/max rise/fall values.

Default value for this variable is true.

extract_model_single_pin_cap_max

This variable is to provide a method to only write minimum capacitance values in a model that is in single capacitance mode. If the *extract_model_single_pin_cap* variable is true, the maximum capacitance is written to the model. If this variable is false, the minimum capacitance is written to the model.

Default value for this variable is true.

extract_model_split_partial_clock_gating_arcs

Controls whether to split the incomplete clock gating check setup/hold arcs in the extracted model.

Default value for this variable is false.

extract_model_status_level

Controls the message displaying for progress of the model extraction process.

Default value for this variable is none.

extract_model_suppress_three_state

Determines report delay calculation to be performed on the timing arcs contained in models.

Default value for this variable is false.

extract_model_use_conservative_current_slew

Enables or disables the adjustment with the current context slew if it is more conservative during the extraction of a timing path. The adjusted models model the netlist behavior better if the netlist is in "worst_slew" propagation mode.

Default value for this variable is false.

extract_model_with_3d_arcs

Enables or disables creating models contain arcs with 3-dimentional delay and transition tables.

Default value for this variable is true.

extract_model_with_clock_latency_arcs

Enables or disables creating clock tree latency, or clock insertion delay arcs in the extracted timing models(ETM).

Default value for this variable is false.

extract_model_write_case_values_to_constraint_file

Controls whether to write logic values due to user set case analysis value propagation seperately into the ETM constraint file.

Default value for this variable is false.

hier_scope_check_defaults

Defines the types of scope checks to be performed by the check_block_scope command, or reported by report_scope_data command. Note that this variable does not impact the scope information to be captured by PrimeTime model creation commands create_ilm and extract_model. The allowed value for this variable is one or more of the following: clock_arrival, clock_transition, data_input_arrival, data_input_transition, clock_uncertainty and clock_skew_with_uncertainty.

Default value for this variable is clock_arrival clock_transition clock_skew_with_uncertainty.

hierarchy_separator

Default value for this variable is / (forward slash).

ilm_ignore_percentage

Specifies a threshold for the percentage of total registers in the transitive fanout of an input port, beyond which the port is to be ignored when identifying interface logic.

Default value for this variable is 25.

ilm_write_verilog_logic_constant_net_names

Specifies that the logic constant net names should be written as 1'b0 or 1'b1 rather than the default way of writing them as nets *Logic0* and *Logic1* and setting a case analysis on corresponding pins.

Default value for this variable is false.

in_gui_session

This read-only variable is *true* when the GUI is active and *false* (the default) when the GUI is inactive.

Default value for this variable is false.

lib_thresholds_per_lib

Enables waveform measurement thresholds and rail-voltages to be taken from each individual library.

Default value for this variable is true.

link_create_black_boxes

Enables the linker to automatically convert each unresolved reference into a black box.

Default value for this variable is true.

link_force_case

Controls the case sensitivity behavior of the link design command.

Default value for this variable is check_reference.

link_library

This is a synonym for the link_path variable.

Default value for this variable is *.

link_path

Specifies a list of libraries, design files, and library files used during linking.

Default value for this variable is *.

link_path_per_instance

Overrides the default link path for selected leaf cell or hierarchical cell instances.

Default value for this variable is (empty).

multi_core_enable_analysis

Enables or disables PrimeTime multicore analysis.

Default value for this variable is false.

multi_core_skip_unsupported

Enables or disables skipping of unsupported commands and variables in the multicore analysis flow.

Default value for this variable is true.

multi_core_working_directory

Defines the root working directory for all multi-core analysis data, including remote process log files.

Default value for this variable is "" (empty).

multi_scenario_fault_handling

Controls how fatals in remote processes are handled.

Default value for this variable is ignore.

multi_scenario_merged_error_limit

Defines the maximum number of errors or warnings of a particular type to be considered for merging in the merged error log on a per task basis.

Default value for this variable is 100.

multi_scenario_merged_error_log

Use to specify a file location where full (compressed) error, warning and informational messages are stored for data produced by the slaves.

multi_scenario_message_verbosity_level

Define the verbosity level of messages printed at the master during slave processing.

Default value for this variable is default.

multi_scenario_working_directory

Defines the root working directory for all multi-scenario analysis data, including log files.

mw_design_library

This variable stores the name of the design library for the read_milkyway command.

Default value for this variable is "" (empty).

mw_logic0_net

This variable controls the name of constant zero net for the read_milkyway command.

Default value for this variable is VSS.

mw_logic1_net

This variable controls the name of the constant one net for the read_milkyway command.

Default value for this variable is VDD.

parasitics_cap_warning_threshold

Specifies a capacitance threshold beyond which a warning message is issued during the reading of a parasitics file.

Default value for this variable is 0.0.

parasitics_rejection_net_size

Defines a threshold number of nodes in an annotated parasitic network beyond which the detailed network is automatically replaced by a lumped capacitance.

Default value for this variable is 20000.

parasitics_res_warning_threshold

Specifies a resistance threshold beyond which a warning message is issued during the reading of a parasitics file.

Default value for this variable is 0.0.

parasitic_variation_default_type

Specifies the type of default distribution used for parasitic variation parameters in PrimeTime VX.

Default value for this variable is normal.

parasitics_warning_net_size

Defines a threshold number of nodes in an annotated parasitic network beyond which a message is issued that warns of a potential extended run time.

Default value for this variable is 10000.

pba_aocvm_only_mode

Specifies that only AOCVM is performed during path-based analysis.

Default value for this variable is false.

pba_derate_list

Specifies path-based derate factors.

Default value for this variable is "" (empty).

pba_disable_path_recalculation_limit

Controls whether regular path-based analysis is limited to 10000 paths (the default) or unlimited.

Default value for this variable is false.

pba_enable_ccs_waveform_propagation

Enables or disables CCS based waveform propagation feature for path-based delay analysis.

Default value for this variable is false.

pba_enable_path_based_physical_exclusivity

This variable controls whether a path-based or stage-based physical exclusivity crosstalk computation is used during path-based analysis of paths involving physically exclusive clocks.

Default value for this variable is false.

pba_enable_xtalk_delay_ocv_pessimism_reduction

During the path based analysis reduces the pessimism due to clock on-chip-variation(OCV) on xtalk delay analysis.

Default value for this variable is false.

pba_exhaustive_endpoint_path_limit

Defines a limit for exhaustive path-based analysis.

Default value for this variable is 25000.

pba_recalculate_full_path

Allow regular path-based analysis to recalculate full clock paths and borrowing path segments.

Default value for this variable is true.

power_analysis_mode

Sets the power analysis mode

Default value for this variable is averaged.

power_calc_use_ceff_for_internal_power

Specifies whether to use effective C for internal power calculation.

Default value for this variable is false.

power_check_defaults

Defines the default checks for the check_power command.

Default value for this variable is out_of_table_range missing_table missing_function.

power_clock_network_include_clock_gating_network

Indicates that clock gating networks are included in the clock network.

Default value for this variable is false.

power_clock_network_include_register_clock_pin_power

Indicates whether the register clock pin power is included when reporting clock_network power.

Default value for this variable is true.

power_default_static_probability

Specifies the default static probability value.

Default value for this variable is 0.5.

power_default_toggle_rate

Specifies the default toggle rate value.

Default value for this variable is 0.1.

power_default_toggle_rate_reference_clock

Specifies how the related clock for default toggle rate is determined.

Default value for this variable is related.

power_domains_compatibility

Indicates whether to revert to power domains mode and disable UPF mode.

Default value for this variable is false.

power_enable_analysis

Enables or disables PrimeTime PX, which provides power analysis.

Default value for this variable is false.

power_enable_leakage_variation_analysis

Enables or disables the leakage variation feature in PrimeTime PX.

Default value for this variable is false.

power_estimate_power_for_unmatched_event

Controls to estimate power when no table is found in the library to match a certain event.

Default value for this variable is true.

power_include_initial_x_transitions

Controls to count x power in the power up initialization stage.

Default value for this variable is false.

power_limit_extrapolation_range

Specifies if extrapolation will be limited to certain range for internal power calculation.

Default value for this variable is false.

power_match_state_for_logic_x

Specifies logic x interpretation.

Default value for this variable is 0.

power_model_preference

Specifies the power model preference if the library contains both NLPM and CCS power data.

Default value for this variable is ccs.

power_rail_output_file

Specifies the output file name for dumping out power information for PrimeRail users.

Default value for this variable is "" (empty).

power_read_activity_ignore_case

Use the *power_read_activity_ignore_case* variable instead of the *power_read_vcd_ignore_case* variable to control ignore case when reading activity files.

Default value for this variable is true.

power_read_vcd_ignore_case

Use the *power_read_activity_ignore_case* variable instead of the *power_read_vcd_ignore_case* variable to control ignore case when reading activity files.

Default value for this variable is true.

power_report_leakage_breakdowns

Controls to report leakage components.

Default value for this variable is false.

power_reset_negative_extrapolation_value

Resets negative extrapolated energy value from library to zero.

Default value for this variable is false.

power_reset_negative_internal_power

Resets the negative internal power to zero.

Default value for this variable is false.

power_scale_dynamic_power_at_power_off

Indicates if the dynamic power will be scaled according to the static probability of the corresponding power supply net. As default, this variable is set to false. Only leakage power is scaled by the power-on probability.

Default value for this variable is false.

power_table_include_switching_power

Indicate whether power tables in technology library include switch power.

Default value for this variable is true.

power_x_transition_derate_factor

Set the scale factor for X-transition power.

Default value for this variable is 0.5.

pt_ilm_dir

Specifies a directory for PrimeTime to create ILM related files.

Default value for this variable is (current directory).

pt_shell_mode

Describes the mode of operation of the current shell.

pt_tmp_dir

Directory that PrimeTime uses for temporary storage.

Default value for this variable is /tmp (the local /tmp partition).

ptxr_root

Specifies an alternative installation root path for PrimeTime to look for the executables required by PrimeTime External Reader (ptxr).

Default value for this variable is By default, this variable is the same as the root path where PrimeTime program is installed.

rc_adjust_rd_when_less_than_rnet

Enables or disables overriding of library-derived drive resistance when it is much less than the dynamic RC network impedance to ground.

Default value for this variable is true.

rc_always_use_max_pin_cap

Specifies whether to override the use of pin-capacitances from the min library during min RC delay-calculation and use the pin-capacitances from the max library instead. This functionality is provided only to obtain backward compatibility with older releases of PrimeTime.

Default value for this variable is false.

rc_cache_min_max_rise_fall_ceff

Specifies whether to cache min/max rise/fall values of effective capacitance computed during RC delay calculation.

Default value for this variable is false.

rc_ceff_delay_min_diff_ps

Specifies a tolerance for determining when the effective-capacitance calculation has converged during RC delay calculation. Please read the description below for important issues regarding the use of this variable.

Default value for this variable is 0.25.

rc_ceff_use_delay_reference_at_cpin

Specifies whether to compute C-effective using a driver delay relative to that for the output pin capacitance. This can improve accuracy for drivers with many internal stages (e.g. extracted timing models), but it requires library data characterized all the way to down to the output pin capacitance.

Default value for this variable is false.

rc_create_and_cache_pi_models

Specifies whether to create and cache pi-model reductions of annotated detailed parasitics during timing updates. The resulting pi-models can be written out to a file using the write_pi_parasitics command.

Default value for this variable is false.

rc_degrade_min_slew_when_rd_less_than_rnet
Enables or disables the use of slew degradation in min analysis mode during the RC-009 condition.

Default value for this variable is false.

rc_driver_count_threshold_for_fast_multidrive_analysis
Specifies how many network drivers beyond which will necessitate fast multi-drive analysis.

Default value for this variable is 9.

rc_driver_model_max_error_pct
Specifies the maximum error tolerated in a driver model used in RC effective-capacitance calculations.

Default value for this variable is 16.0.

rc_driver_model_mode
Specifies which driver model type to use for RC delay calculation.

Default value for this variable is advanced.

rc_filter_rd_less_than_rnet
Enables or disables suppressing the display of RC-009 messages when the network delay is less than the corresponding driver transition time.

Default value for this variable is true.

rc_hide_ceff_warnings_for_enable_arcs
Specifies whether to hide warnings that occur during RC delay-calculation of C-effective for tri-state enable arcs.

Default value for this variable is false.

rc_input_threshold_pct_fall

Specifies the percentage threshold of the startpoint to voltage source for a falling delay calculation.

Default value for this variable is 50.

rc_input_threshold_pct_rise

Specifies the percentage threshold of the startpoint to voltage source for a rising delay calculation.

Default value for this variable is 50.

rc_output_threshold_pct_fall

Specifies the percentage threshold of the endpoint to voltage source for a falling delay calculation.

Default value for this variable is 50.

rc_output_threshold_pct_rise

Specifies the percentage threshold of the endpoint to voltage source for a rising delay calculation.

Default value for this variable is 50.

rc_rd_less_than_rnet_threshold

Specifies the RC-009 threshold, beyond which PrimeTime overrides the library-derived drive resistance with an empirical formula, to improve accuracy.

Default value for this variable is 0.45.

rc_receiver_model_mode

Specifies which receiver model type to use for RC delay calculation.

Default value for this variable is advanced.

rc_slew_derate_from_library
Specifies the derating needed for the transition time in library to match that from the characterization trip points.

Default value for this variable is 1.

rc_slew_lower_threshold_pct_fall
Specifies the percentage threshold of the lower slew endpoint to the voltage source for a falling transition.

Default value for this variable is 20.

rc_slew_lower_threshold_pct_rise
Specifies the percentage threshold of the lower slew startpoint to the voltage source for a rising transition.

Default value for this variable is 20.

rc_slew_upper_threshold_pct_fall
Specifies the percentage threshold of the slew startpoint to the voltage source for a falling transition.

Default value for this variable is 80.

rc_slew_upper_threshold_pct_rise
Specifies the percentage threshold of the upper slew endpoint to the voltage source for a rising transition.

Default value for this variable is 80.

read_parasitics_load_locations
Specifies that read parasitics should load locations information during the reading of a parasitics file.

Default value for this variable is false.

report_default_significant_digits

The default number of significant digits used to display values in reports.

Default value for this variable is 2.

sdc_save_source_file_information

Enables or disables source file name and line number information of a subset of SDC commands related to the current design constraints PrimeTime context.

Default value for this variable is false.

sdc_version

Use in context of reading a Synopsys Design Constraints (SDC) file. Specifies the SDC version that was written.

Default value for this variable is latest version.

sdc_write_unambiguous_names

Determines whether or not ambiguous hierarchical names are made unambiguous when they are written to SDC files.

Default value for this variable is true.

sdf_align_multi_drive_cell_arcs

Boolean variable which specifies whether PrimeTime will unify the small timing differences in driver cell outputs of a parallel network, when writing out sdf delay values.

Default value for this variable is false.

sdf_align_multi_drive_cell_arcs_threshold

Specifies the threshold below which multi drive cell arcs will be aligned during *write_sdf*.

Default value for this variable is 1 ps.

sdf_enable_cond_start_end

Enables or disables support for sdf_cond_start and sdf_cond_end attributes.

Default value for this variable is false.

sdf_enable_port_construct

Enables or disables support for port construct usage during write_sdf.

Default value for this variable is false.

sdf_enable_port_construct_threshold

Sets the threshold value below within which the port construct during write_sdf will be used.

Default value for this variable is 1 ps.

search_path

Shows a list of directory names that contain design and library files that are specified without directory names.

Default value for this variable is "" (empty).

sh_allow_tcl_with_set_app_var

Allow set_app_var and get_app_var commands to work with application variables

Default value for this variable is application specific.

sh_allow_tcl_with_set_app_var_no_message_list

Suppress CMD-104 messages for variables in this list

Default value for this variable is application specific.

sh_arch

Indicates the system architecture of your machine.

Default value for this variable is platform-dependent.

sh_command_abbrev_mode

Sets the command abbreviation mode for interactive convenience.

Default value for this variable is application specific.

sh_command_log_file

Specifies the name of the file to which the application logs the commands you executed during the session.

Default value for this variable is an empty string.

sh_continue_on_error

Allows processing to continue when errors occur during script execution with the source command.

Default value for this variable is Application specific.

sh_dev_null

Indicates the current null device.

Default value for this variable is Platform-dependent.

sh_eco_enabled

Read-only variable that indicates if ECO commands are enabled.

Default value for this variable is false.

sh_enable_line_editing

Enables the command line editing capabilities in PrimeTime.

Default value for this variable is true.

sh_enable_page_mode

Displays long reports one page at a time (similar to the UNIX more command.

Default value for this variable is application specific.

sh_enable_stdout_redirect

Allow the redirect command to capture output to the Tcl stdout channel.

Default value for this variable is application specific.

sh_fast_analysis_mode_enabled

Read-only variable that indicates if fast analysis mode is enabled.

Default value for this variable is false.

sh_high_capacity_effort

Specifies the level of capacity effort for the timing analysis of PrimeTime/PrimeTime-SI. It only provides simple heuristics for tradeoff between capacity and performance of the program. It does not have any impact on the analysis results at all.

Default value for this variable is default.

sh_high_capacity_enabled

A read-only variable for user to query whether high capacity mode is currently enabled or not. The value of this variable will change upon a successful change of the state with command set_program_options.

Default value for this variable is false for small designs, true for large designs.

sh_launch_dir

Defines the launch directory of the current PrimeTime shell.

sh_limited_messages

The set of message types that have a limit by default in each invoking of read_parasitics, report_annotated_parasitics (with -check), read_sdf or update_timing. The limit is defined by sh_message_limit.

Default value for this variable is "DES-002 PARA-004 PARA-006 PARA-007 PARA-040 PARA-041 PARA-043 PARA-044 PARA-045 PARA-046 PARA-047 PARA-050 PARA-051 PARA-053 RC-002 RC-004 RC-005 RC-009 RC-011 RC-104 PTE-014 PTE-060 PTE-070".

sh_line_editing_mode

Enables vi or emacs editing mode in PrimeTime shell.

Default value for this variable is emacs.

sh_message_limit

Default limit of messages defined in sh_limited_messages during read_parasitics, report_annotated_parasitics (with -check), read_sdf and update_timing.

Default value for this variable is 100.

sh_new_variable_message

Controls a debugging feature for tracing the creation of new variables.

Default value for this variable is Application specific.

sh_new_variable_message_in_proc

Controls a debugging feature for tracing the creation of new variables in a Tcl procedure.

Default value for this variable is false.

sh_new_variable_message_in_script

Controls a debugging feature for tracing the creation of new variables within a sourced script.

Default value for this variable is false.

sh_output_log_file

Specifies the name of the file to which all application output is logged.

Default value for this variable is The empty string.

sh_product_version

Indicates the version of the application currently running.

sh_script_stop_severity

Indicates the error message severity level which would cause a script to stop executing before it completes.

Default value for this variable is application specific.

sh_source_emits_line_numbers

Indicates the error message severity level which would cause an informational message to be issued listing the script name and line number where that message occurred.

Default value for this variable is application specific.

sh_source_logging

Indicates if individual commands from a sourced script should be logged to the command log file.

Default value for this variable is application specific.

sh_source_uses_search_path

Indicates if the source command uses the search_path variable to search for files.

Default value for this variable is application specific.

sh_tcllib_app_dirname

Indicates the name of a directory where application-specific Tcl files are found.

sh_user_man_path

Indicates a directory root where the user can store man pages for display with the man command.

Default value for this variable is an empty list.

si_analysis_logical_correlation_mode

Enables or disables logical correlation analysis during PrimeTime-SI delay or noise calculation.

Default value for this variable is true.

si_ccs_aggressor_alignment_mode

Specifies aggressor alignment mode used in the CCS-based gate-level simulation engine.

Default value for this variable is lookahead.

si_ccs_use_gate_level_simulation

Enables or disables the unified CCS timing and CCS noise engine for delay analysis.

Default value for this variable is true.

si_enable_analysis

Enables or disables PrimeTime-SI, which provides crosstalk analysis.

Default value for this variable is false.

si_filter_accum_aggr_noise_peak_ratio

Specifies the threshold for the accumulated voltage bumps introduced by aggressors at a victim node, divided by Vcc, below which aggressor nets can be filtered out during electrical filtering.

Default value for this variable is 0.03.

si_filter_per_aggr_noise_peak_ratio

Specifies the threshold for the voltage bump introduced by an aggressor at a victim node, divided by Vcc, below which the aggressor net can be filtered out during electrical filtering.

Default value for this variable is 0.01.

si_ilm_keep_si_user_excluded_aggressors
Default value for this variable is false.

si_noise_composite_aggr_mode
Specifies the composite aggressor mode for noise analysis.

Default value for this variable is disabled.

si_noise_endpoint_height_threshold_ratio
Specifies a value that defines the threshold where noise propagation stops. The ratio is between 0.0 and 1.0 of VDD.

Default value for this variable is 0.75.

si_noise_limit_propagation_ratio
This variable limits the amount of propagated noise if the noise height passes noise immunity.

Default value for this variable is 0.75.

si_noise_slack_skip_disabled_arcs
Controls whether to skip disabled timing arcs for noise slack calculation.

Default value for this variable is false.

si_noise_update_status_level
Controls the number of progress messages displayed during the update of noise analysis.

Default value for this variable is none.

si_use_driving_cell_derate_for_delta_delay
Allows crosstalk delta delay for one net to be derated using the relevant derate factor for the cell driving that net.

Default value for this variable is false.

si_xtalk_composite_aggr_mode
Specifies the composite aggressor mode for crosstalk delay.

Default value for this variable is disabled.

si_xtalk_composite_aggr_noise_peak_ratio
Used to control the composite aggressor selection for xtalk analysis.

Default value for this variable is 0.01.

si_xtalk_composite_aggr_quantile_high_pct
Used to control the composite aggressor creation for statistical analysis.

Default value for this variable is 99.73.

si_xtalk_delay_analysis_mode
Specifies the arrival window alignment mode for crosstalk delay.

Default value for this variable is all_paths.

si_xtalk_double_switching_mode
Controls the double switching detection during the PrimeTime-SI timing analysis.

Default value for this variable is "disabled".

si_xtalk_exit_on_max_iteration_count
Specifies a maximum number of incremental timing iterations, after which PrimeTime-SI exits the analysis loop.

Default value for this variable is 2.

si_xtalk_exit_on_max_iteration_count_incr
Specifies a maximum number of timing iterations following what-if change (such as size_cell) to the design, after which PrimeTime-SI exits the analysis loop.

Default value for this variable is 2.

si_xtalk_reselect_clock_network
Determines whether or not PrimeTime SI reselects clock network nets for subsequent delay calculations.

Default value for this variable is true.

si_xtalk_reselect_delta_delay
Specifies the threshold of net delay change caused by crosstalk analysis, above which PrimeTime-SI reselects the net for subsequent delay calculations.

Default value for this variable is 5.

si_xtalk_reselect_delta_delay_ratio
Specifies the threshold of the ratio of net delay change caused by crosstalk analysis to the total stage delay, above which PrimeTime SI reselects a net for subsequent delay calculations.

Default value for this variable is 0.95.

si_xtalk_reselect_max_mode_slack
Specifies the max mode pin slack threshold, below which PrimeTime-SI reselects a net for subsequent delay calculations.

Default value for this variable is 0.

si_xtalk_reselect_min_mode_slack

Specifies the min mode pin slack threshold, below which PrimeTime-SI reselects a net for subsequent delay calculations.

Default value for this variable is 0.

si_xtalk_reselect_time_borrowing_path

Determines whether or not PrimeTime-SI reselects time borrowing path nets for subsequent delay calculations.

Default value for this variable is true.

svr_enable_vpp

Enables or disables preprocessing of Verilog files by the Verilog preprocessor.

Default value for this variable is false.

svr_keep_unconnected_nets

This variable is used only by the native Verilog reader to preserve or discard unconnected nets.

Default value for this variable is true.

synopsys_program_name

Indicates the name of the program currently running.

synopsys_root

Indicates the root directory from which the application was run.

timing_all_clocks_propagated

Determines whether or not all clocks are created as propagated clocks.

Default value for this variable is false.

timing_allow_short_path_borrowing

Enable time borrowing through level sensitive latches for hold time checks.

Default value for this variable is false.

timing_aocvm_analysis_mode

Configure an AOCVM analysis.

Default value for this variable is "".

timing_aocvm_enable_analysis

Enable PrimeTime's graph-based AOCVM analysis.

Default value for this variable is false.

timing_bidirectional_pin_max_transition_checks

Determines the extent of max transition design rule checks on bidirectional pins.

Default value for this variable is both.

timing_check_defaults

Defines the default checks for the check_timing command.

Default value for this variable is generated_clocks generic latch_fanout loops no_clock no_input_delay unconstrained_endpoints pulse_clock_non_pulse_clock_merge.

timing_clock_gating_propagate_enable

Allows the gating enable signal delay to propagate through the gating cell.

Default value for this variable is true.

timing_clock_reconvergence_pessimism
Select signal transition sense matching for computing clock reconvergence pessimism removal.

Default value for this variable is normal.

timing_clock_source_driver_pin_use_driver_arc_compatibility
Select between backward compatible behavior of forcing an ideal ramp at driver pin primary clock sources or using the backward cell arc to compute a realistic driver model.

Default value for this variable is true.

timing_crpr_enable_adaptive_engine
Enables or disables the adaptive CRPR engine.

Default value for this variable is false.

timing_crpr_minimize_grouping
Enables or disables the aggressive grouping during CRPR calculations..

Default value for this variable is false.

timing_crpr_remove_clock_to_data_crp
Allows the removal of Clock Reconvergence Pessimism (CRP) from paths that fan out directly from clock source to the data pins of sequential devices.

Default value for this variable is false.

timing_crpr_remove_muxed_clock_crp
Allow CRPR to consider common path reconvergence between related clocks.

Default value for this variable is true.

timing_crpr_threshold_ps
Specifies amount of pessimism that clock reconvergence pessimism removal (CRPR) is allowed to leave in the report.

Default value for this variable is 20.

timing_disable_bus_contention_check
Disable checking for timing violations resulting from transient contention on design busses.

Default value for this variable is false.

timing_disable_clock_gating_checks
Disable checking for setup and hold clock gating violations.

Default value for this variable is false.

timing_disable_cond_default_arcs
Disable the default, non-conditional timing arc between pins that do have conditional arcs.

Default value for this variable is false.

timing_disable_floating_bus_check
Disable checking for timing violations resulting from transient floating design buses.

Default value for this variable is false.

timing_disable_internal_inout_cell_paths
Enable bidirectional feedback paths within a cell.

Default value for this variable is true.

timing_disable_internal_inout_net_arcs
Controls whether bidirectional feedback paths across nets are disabled or not.

Default value for this variable is true.

timing_disable_recovery_removal_checks

Disable or enable the timing analysis of recovery and removal checks in the design.

Default value for this variable is false.

timing_dynamic_loop_breaking

Enable or disable the dynamic breaking of combinational feedback loops.

Default value for this variable is false.

timing_early_launch_at_borrowing_latches

Removes clock latency pessimism from the launch times for paths which begin at the data pins of transparent latches.

Default value for this variable is true.

timing_edge_specific_source_latency

Controls whether the generated clock source latency computation will consider edge relationship or not.

Default value for this variable is true.

timing_enable_clock_propagation_through_preset_clear

Enables propagation of clock signals through preset and clear pins

Default value for this variable is false.

timing_enable_clock_propagation_through_three_state_enable_pins

Allow the clocks to propagate through the enable pin of a three-state cell.

Default value for this variable is false.

timing_enable_constraint_delay_calculation_compatibility

Indicates whether to revert to constraint arc delay calculation behavior to that or an earlier release of PrimeTime.

Default value for this variable is false.

timing_enable_invalid_slew_propagation_compatibility

Enable or disable propagation of slew values driven by disabled arcs or non-existent transitions of half-unate arcs.

Default value for this variable is false.

timing_enable_max_capacitance_set_case_analysis

Specifies max capacitance constraint will be checked on constant pins.

Default value for this variable is false.

timing_enable_multiple_clocks_per_reg

Enables or disables analysis of multiple clocks that reach a single register.

Default value for this variable is true.

timing_enable_preset_clear_arcs

Controls whether PrimeTime enables or disables preset and clear arcs.

Default value for this variable is false.

timing_enable_pulse_clock_constraints

Enables checking of pulse clock constraints.

Default value for this variable is true.

timing_gclock_source_network_num_master_registers

The maximum number of register clock pins clocked by the master clock allowed in generated clock source latency paths.

Default value for this variable is 1.

timing_ideal_clock_zero_default_transition

Specifies whether or not a zero transition value is assumed for sequential devices clocked by ideal clocks.

Default value for this variable is true.

timing_include_available_borrow_in_slack

Determines whether or not PrimeTime includes available borrow time in slack.

Default value for this variable is false.

timing_input_port_clock_shift_one_cycle

Determines whether or not paths originating at input ports are given an extra cycle to meet their timing constraints.

Default value for this variable is false.

timing_input_port_default_clock

Determines whether a default clock is assumed at input ports for which the user has not defined a clock with set_input_delay.

Default value for this variable is true.

timing_keep_loop_breaking_disabled_arcs

Determines whether to keep .db inherited disabled timing arcs for static loop breaking.

Default value for this variable is false.

timing_non_unate_clock_compatibility
Controls whether only non-inverting clock sense is used in the non-unate case.

Default value for this variable is false.

timing_port_clock_and_data_compatibility
Disable or enable the simultaneours behavior of input port as clock and data port,

Default value for this variable is false.

timing_prelayout_scaling
Enables scaling of delay and transition times in pre-layout flow to approximate effects of mismatching driver and load signal levels.

Default value for this variable is true.

timing_propagate_interclock_uncertainty
Enables or disables the propagation of interclock uncertainty through transparent latches in PrimeTime.

Default value for this variable is false.

timing_propagate_through_non_latch_d_pin_arcs
Always propagate cell arcs from data pins for edge-triggered devices.

Default value for this variable is false.

timing_propagate_through_unclocked_registers
Enables or disables propagation of the timing path through unclocked registers.

Default value for this variable is false.

timing_reduce_multi_drive_net_arcs
Enables or disables the collapsing of parallel timing arcs to improve PrimeTime performance and memory utilization.

Default value for this variable is false.

timing_reduce_multi_drive_net_arcs_threshold
Provides a threshold for the product of some net's fanin and fanout beyond which a parallel timing arc in the net's fanin might be reduced.

Default value for this variable is 10000.

timing_remove_clock_reconvergence_pessimism
Enables or disables clock reconvergence pessimism removal

Default value for this variable is false.

timing_report_always_use_valid_start_end_points
Requires the -from/-rise_from/-fall_from options *from_list* objects to be valid timing startpoints and the -to/-rise_to/-fall_to options *to_list* objects to be valid timing endpoints.

Default value for this variable is false.

timing_report_maxpaths_nworst_reached
Controls maxpaths and nworst reached messages displayed during the timing report process.

Default value for this variable is false.

timing_report_recalculation_status
Display progress messages during an exhaustive path-based analysis.

Default value for this variable is low.

timing_report_status_level

Controls the number of progress messages displayed during the timing report process.

Default value for this variable is none.

timing_report_unconstrained_paths

Specifies if PrimeTime searches for unconstrained paths or not when you use the report_timing or get_timing_paths command.

Default value for this variable is false.

timing_report_use_worst_parallel_cell_arc

Enable uniquification of paths through parallel cell arcs.

Default value for this variable is false.

timing_save_pin_arrival_and_required

Specifies whether the arrival and required times of all pins are kept in memory.

Default value for this variable is false.

timing_save_pin_arrival_and_slack

Specifies whether the slacks of all pins are kept in memory.

Default value for this variable is false.

timing_si_exclude_delta_slew_for_transition_constraint

Specifies delta slew to be excluded from maximum and minimum transition constraint checks.

Default value for this variable is false.

timing_slew_propagation_mode

Specifies how slew is to be propagated through the circuit.

Default value for this variable is worst_slew.

timing_slew_threshold_scaling_for_max_transition_compatibility

Specifies the compatibility mode for timing slew threshold scaling.

Default value for this variable is false.

timing_update_default_mode

Determines whether update_timing performs incremental or complete timing analysis.

Default value for this variable is incremental.

timing_update_effort

Controls the computational effort (in CPU time) and memory usage for the fast timing update algorithm in PrimeTime.

Default value for this variable is medium.

timing_update_status_level

Controls the number of progress messages displayed during the timing update process.

Default value for this variable is none.

timing_use_zero_slew_for_annotated_arcs

Allows disabling of the slew calculation to enhance performance in a pure SDF flow.

Default value for this variable is auto.

true_delay_prove_false_backtrack_limit

Specifies the number of backtracks to be used by report_timing -true in searching for false paths.

Default value for this variable is 1000.

true_delay_prove_true_backtrack_limit

Specifies the number of backtracks to be used by report_timing -true in searching for true paths.

Default value for this variable is 1000.

variation_analysis_mode

Specifies the scope of variations analysis performed during a subsequent timing update.

Default value for this variable is default.

variation_derived_scalar_attribute_mode

Enables get_attribute command to return statistical timing attributes of timing_path and timing_point collections in VASTA.

Default value for this variable is quantile.

variation_enable_analysis

Enables statistical variation analysis for PrimeTime.

Default value for this variable is false.

variation_pba_use_worst_parasitics

Enables use of worst parasitic corner for statistical path based analysis (PBA).

Default value for this variable is false.

variation_report_timing_increment_format

Controls the display of report_timing increments for variation-aware timing paths.

Default value for this variable is effective_delay.

write_script_include_library_constraints

This variable is used to control whether constraints set on library objects are written to script output by write_script and write_sdc.

Default value for this variable is true.

write_script_output_lumped_net_annotation

Determines whether or not the write_script command outputs lumped network annotations.

Default value for this variable is false.