PrimeTime
Error Messages

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SYNOPSYS®

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AOCVM-001 (error) The field '%s' has already been specified for the current '%s'

DESCRIPTION

This error occurs when a field is specified more than once for a given table. The error can also occur if the user does not include all fields during a table specification.

WHAT NEXT

Correct the AOCVM syntax by ensuring that each field is only specified once for a given table.

AOCVM-002 (error) The current table is missing one or more fields

DESCRIPTION

This error occurs when a table is found at the end of the aocvm file without the required number of fields.

WHAT NEXT

Correct the AOCVM syntax by adding the missing fields to the file.

AOCVM-003 (error) Expected to find a valid field name but found '%s'.

DESCRIPTION

This error occurs when the parser cannot find a valid field name.

WHAT NEXT

Correct the AOCVM syntax by ensuring that each field is specified in the format name: data

where name is one of
version,table,distance,depth,object_spec,derate_type,delay_type,rf_type,object_type.

AOCVM-004 (error) Cannot specify '%s' for field '%s'.

DESCRIPTION

The data found in the AOCVM file is not valid for the given field.

WHAT NEXT

Check the AOCVM spec to see allowed values for the field and update the AOCVM file appropriately.

AOCVM-005 (warning) Cannot associate table with leaf cell '%s'.

DESCRIPTION

AOCVM does not support the association of AOCVM data with leaf cells.

WHAT NEXT

Associate AOCVM tables with hierarchical cells, library cells and designs only.

AOCVM-006 (warning) Cannot find any objects of type '%s' for specification '%s'.

DESCRIPTION

Could not find any objects for the given specification. The table is not annotated on any objects but parsing and annotation will not stop due to this warning.

WHAT NEXT

Check that the specification is correct.

AOCVM-007 (error) Expected table of size %d but found table

of size %d.

DESCRIPTION

```
The size of the 2D AOCVM table must equal the number of depth indices by the number
of distance indices
```

WHAT NEXT

```
Correct the size of the table
```

AOCVM-008 (error) Cannot finish AOCVM file on a line continuation

DESCRIPTION

```
The AOCVM file ends with a line continuation. The parser expects more data but there
is none.
```

WHAT NEXT

```
Remove the line continuation character
```

AOCVM-009 (error) Could not find the specified AOCVM file

DESCRIPTION

```
The AOCVM file could not be found
```

WHAT NEXT

```
Correct the name and path of the AOCVM file
```

AOCVM-010 (error) The field '%s' must be specified before '%s'

DESCRIPTION

```
While parsing an AOCVM 2D table a field cannot be set because another field has not
been specified
```

Change the order of the field specifications.

AOCVM-011 (error) The version '%s' is not valid. Allowable versions are '%s'

DESCRIPTION

An invalid version number has been specified

WHAT NEXT

AOCVM-012 (error) An aocvm file version must be specified.

DESCRIPTION

The version number is used for backward compatibility purposes if the AOCVM file format changes in the future. It does affect the results of the analysis.

The version of the aocvm file must be specified on the first line of the AOCVM file. e.g version:1.0

WHAT NEXT

Add the version information to the start of the AOCVM file.

AOCVM-013 (error) The %s array does not increase or decrease sequentially

DESCRIPTION

Sequential elements in the specified array must sequentially increase or decrease.

WHAT NEXT

Fix the array so that it sequentially increases or decreases.

AOCVM-014 (error) Negative values are not allowed

DESCRIPTION

Negative values are not allowed for the distance,depth arrays or in the 2D tables.

WHAT NEXT

Remove negative values from the AOCVM file.

AOCVM-015 (error) Cannot specify delay type %s with object type %s

DESCRIPTION

This combination of delay type and object types is not allowed as it makes no sense.

WHAT NEXT

Correct the AOCVM file to remove the invalid combination of delay type and object type.

AOCVM-016 (error) Cannot specify a non-monotonic derate table.

DESCRIPTION

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

The timing derates specified in each row and each column of the derate table must increase or decrease monotonically.

WHAT NEXT

Fix the specified table so that sequential elements in each row and each column of the table sequentially increase or decrease.

AOCVM-017 (error) Derate table variability is not decreasing

with increasing depth.

DESCRIPTION

This message is issued because the derate table specified in the message is
incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each row of the derate
table must decrease monotonically as depth increases. For an early derate table, the
timing derates specified in each row of the derate table must increase monotonically
as depth increases.

No further restriction is placed on the table contents; however, typically, derate
variability should be proportional to 1/sqrt(depth).

WHAT NEXT

Fix the specified table so that sequential elements in each row of the early (or
late) table sequentially increase (or decrease) as depth increases.

AOCVM-018 (error) Derate table variability is not increasing with increasing distance.

DESCRIPTION

This message is issued because the derate table specified in the message is
incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each column of the derate
table must increase monotonically as distance increases. For an early derate table,
the timing derates specified in each row of the derate table must decrease
monotonically as distance increases.

No further restriction is placed on the table contents; however, typically, derate
variability should be proportional to distance.

WHAT NEXT

Fix the specified table so that sequential elements in each column of the early (or
late) table sequentially decrease (or increase) as distance increases.

ATTR

ATTR-1 (warning) Attribute '%s' has not been defined for %s

DESCRIPTION

The attribute you are referencing is not defined for the class of object(s) you are using. It is possible that the attribute is not defined at all.

Application attributes are all defined at runtime by the application. You can create user-defined attributes at any time.

WHAT NEXT

Verify that the attribute name is spelled correctly. If this is a documented application attribute, contact support. If this is a user-defined attribute, ensure that you have defined the attribute for all appropriate classes.

ATTR-2 (warning) Attribute '%s' is not user-defined for %ss; can't %s it

DESCRIPTION

The attribute you are referencing is an application attribute. These cannot be set or removed by the user using set_user_attribute or remove_user_attribute, respectively. There might be other commands which allows you to set or remove the attribute.

WHAT NEXT

Consult the documentation to determine if it is possible to set or remove this attribute.

ATTR-3 (warning) Attribute '%s' does not exist on %s '%s'

DESCRIPTION

The attribute you are trying to get is not found on the object. This is definitely a sparse attribute, and most likely user-defined. There is a way to suppress this message if you desire. For example, if this is in a loop or in a procedure (-quiet?)

ATTR-4 (warning) Value '%s' is not valid for '%s' on %ss

DESCRIPTION

```
The value you are trying to set on the attribute cannot be converted to the data
type defined for the attribute. For example, if the attribute is defined as "float",
setting the attribute to "true" is not valid.
```

WHAT NEXT

```
Enter an appropriate value for the attribute.
```

ATTR-5 (warning) Value '%s' for '%s' is not in range (%s)

DESCRIPTION

```
The numeric value you are trying to set on the attribute is not in the range
specified for the attribute. Ranges are either within a minimum and maximum value,
greater than or equal to a minimum value, or less or equal to a maximum value. The
message text indicates the violated constraint.
```

WHAT NEXT

```
Enter an appropriate value for the attribute.
```

ATTR-6 (warning) Value '%s' for '%s' is not valid. Specify one of: %s

DESCRIPTION

```
The string value you are trying to set on the attribute is not one of the valid
strings defined for the attribute. The message text indicates the allowable values.
```

WHAT NEXT

```
Enter an appropriate value for the attribute.
```

ATTR-7 (information) Inferred definition of attribute '%s' for class '%s'
 because it is imported for class '%s'

DESCRIPTION

You used the **define_user_attribute** command to define a design or port attribute, and asked for it to be imported from DB files. Since design attributes are inherited onto cells (an instance of a design) and port attributes are inherited onto pins (an instance of a port), the attribute you defined for a design/port must also be defined for a cell/pin, respectively. PrimeTime defines the attribute for you if you have not already done so, and issues this message.

WHAT NEXT

If you want to remove this message, add the appropriate class to the list of classes in your **define_user_attribute** command, or add a dedicated **define_user_attribute** command earlier in the script to define the attribute for the cell or pin class.

SEE ALSO

define_user_attribute (2).

CLE

CLE-01 (information) Command line editor mode is set to %s successfully.

DESCRIPTION

This information message confirms that the command line editor mode is set to the mode you specified. Use the **sh_line_editing_mode** variable to set the line editing mode to either vi or emacs.

WHAT NEXT

This is an information message only. No action is required.

SEE ALSO

sh_line_editing_mode (3)

CLE-02 (warning) Command line editor mode cannot be set to %s. Proceeding with %s mode.

DESCRIPTION

This warning message occurs when you attempt to set the line editor mode to an invalid value. The **sh_line_editing_mode** variable can be set to either vi or emacs. If you attempt to set the variable to an invalid value, then the tool uses either the existing edit mode, if the mode is set, or the default emacs mode.

WHAT NEXT

This is only a warning message. No action is required.

However, if the mode indicated in the warning message is not the mode you intended, set the **sh_line_editing_mode** variable to a valid value, either vi or emacs.

SEE ALSO

sh_line_editing_mode (3).

CLE-03 (warning) Command line editor is already in %s mode.

DESCRIPTION

This warning message occurs when you specify the same value for the command line
editor mode that is currently in use by the editor.

WHAT NEXT

This is a warning message only. No action is required.

However, if the result is not what you intended, use the **sh_line_editing_mode**
variable to set the line editing mode to either vi or emacs.

SEE ALSO

sh_line_editing_mode (3)

CLE-04 (warning) Variable sh_enable_line_editing can be set only in the .synopsys_pt.setup file.

DESCRIPTION

This warning message occurs when you attempt to enable command line editing by
setting the **sh_enable_line_editing** variable in the shell rather than in the
.synopsys_pt.setup file.

WHAT NEXT

This is a warning message only. No action is required.

However, you can enable command line editing by setting the **sh_enable_line_editing**
variable to true in the .synopsys_pt.setup file.

SEE ALSO

sh_enable_line_editing (3)

CLE-05 (Warning) Command line editing is not active.

DESCRIPTION

Command line editing is not currently active, so setting **sh_line_editing_mode** has no effect.

WHAT NEXT

Enable line editing mode by setting **sh_enable_line_editing** to true in the .synopsys_pt.setup file.

SEE ALSO

sh_line_editing_mode (3) **sh_enable_line_editing** (3)

CLE-06 (information) %s is currently in %s editing mode.

DESCRIPTION

This information message displays the current editing mode.

WHAT NEXT

This is only an informational message. No action is required.

However, you can use the **sh_line_editing_mode** variable to set the line editing mode to either vi or emacs.

SEE ALSO

sh_line_editing_mode (3)

CLE-07 (information) Terminal beep is %s.

DESCRIPTION

This information message displays the current terminal beep mode.

WHAT NEXT

This is only an informational message. No action is required.

However, you can use the **set_cle_options** command to set the terminal beep to either on or off.

SEE ALSO

set_cle_options(2)

CLE-08 (error) Terminal beep mode value can be either on or off.

DESCRIPTION

This message occurs when you attempt to set the line editor beep mode to an invalid value. The value can be either **on** or **off**. If you attempt to set the beep mode to an invalid value, then the tool uses the existing beep mode.

WHAT NEXT

Use the **set_cle_options** command to specify a valid beep mode.

SEE ALSO

set_cle_options(2)

CLE-09 (warning) -defaults option will override other options.

DESCRIPTION

-defaults option will override the other options of **set_cle_options** command.

WHAT NEXT

This is only a warning message. No action is required.

SEE ALSO

set_cle_options(2)

CLE-100 (Warning) Cannot use command line editor for

terminal type '%s'.

DESCRIPTION

The command line editor has failed to initialize for terminal type '%s'. This can occur when the terminfo database could not be found or the database does not have an entry for the terminal type '%s'. If this message is printed then advanced shell editing capabilities can not be used.

WHAT NEXT

Use a terminal window that has the required capabilities, such as a linux dtterm.

CMCR-001 (error) Cannot specify option '%s' with local host.

DESCRIPTION

The command **set_host_options** was used with an option that is not compatible with the local host setting. The options which cannot be used in conjunction with the '-local' option are: '-submit_script', '-submit_options', '-num_processes' and '-32bit'.

WHAT NEXT

See the man page for the **set_host_options** command.

CMCR-002 (error) Cannot specify machine name '%s' with local host.

DESCRIPTION

The command **set_host_options** was used with a specified machine name while using the local host setting. The machine name cannot be specified when using the '-local' option.

WHAT NEXT

See the man page for the **set_host_options** command.

CMCR-003 (warning) replacing host options '%s'.

DESCRIPTION

The command is defining host options with the name specified. However, host options of the same name already exist. The original host options will be removed and all associated host instances will be shutdown. The new host options will replace the original host options.

WHAT NEXT

The **start_hosts** command must be called in order to launch the processes specified by the new host options.

CMCR-004 (warning) no submit command specified to access remote host '%s'. The 'rsh' command will be used.

DESCRIPTION

Calling the **set_host_options** command without specifying the '-submit_command' option implies the process should be setup locally on the host on which the command is called. However, the hostname provided to the command is not the name of the host on which the command was called. In order to launch the process on the remote host the 'rsh' command will be used.

WHAT NEXT

If the process should be run locally, call the **set_host_options** command specifying the name of the host on which the command is called or localhost.

If the process should be run remotely, call the **set_host_options** command specifying the name of the host as before and provide suitable '-submit_command' options to remotely run the process on that host.

See the **set_host_options** command for further details.

CMCR-005 (warning) not all processes could be added for starting.

DESCRIPTION

While adding the processes to be launched, some of the processes could not be added due to internal limits.

WHAT NEXT

Use the **report_hosts** command to determine which host options did not have some processes started.

CMCR-006 (error) Timeout has been set to '%d' seconds.

Timeout must be set to a non-negative value.

DESCRIPTION

The command **start_hosts** was used with the '-timeout' parameter set to a negative
value. This parameter specifies the maximun duration the command will block for
remote processes to come online before returing and must be set to a value greater
than or equal to 0.

WHAT NEXT

See the man page for the **start_hosts** command.

CMCR-007 (error) The '-min_hosts' parameter has been set to '%d'. This parameter must be set to a non-negative value.

DESCRIPTION

The command **start_hosts** was used with the '-min_hosts' parameter set to a negative
value. This parameter specifies the minimun number of hosts that must come online
before returning and must be set to a value greater than or equal to 0.

WHAT NEXT

See the man page for the **start_hosts** command.

CMCR-008 (error) the host options named '%s' does not exist.

DESCRIPTION

The named host options referred to does not exist.

WHAT NEXT

Use the **set_host_options** command to create the named host options.

CMCR-009 (warning) process '%d' could not be stopped for host

options '%s'

DESCRIPTION

The process indicated could not be stopped. Since the process could not be stopped the associated host options could not be removed.

WHAT NEXT

Examine the logged information when the processes were started. If there was a error in the options used to laucnh the processes then these process will never come online or be able to shutdown and hence cannot be controlled. If there was no error during the launch of the processes then wait for the processes to come online and then remove the host options.

CNTXT-001 (error) Cannot characterize context in min and max mode.

DESCRIPTION

The design has a minimum and a maximum operating condition defined on it. Context characterization requires only one operating condition be set on the design.

WHAT NEXT

Set the operating condition for which you want to characterize the context on the design.

CNTXT-002 (information) Characterizing the context for cell '%s'

DESCRIPTION

You receive this message to inform you that the **characterize_context** command is characterizing the context for the specified cell.

WHAT NEXT

This is an informational message only. No action is required on your part.

CNTXT-003 (information) Deleting the context for cell '%s'

DESCRIPTION

The internal data structures associated with the context of the cell were deleted. Therefore the context cannot be written out (*write_context*) or reported (*report_context*). This occurs when the context is deleted by *remove_context*.

WHAT NEXT

This is an information message. No action is required unless you want to use *write_context* or *report_context* on the cell for which **CNTXT-003** was issued. Otherwise context must be created by *characterize_context*.

CNTXT-004 (error) This command applies to hierarchical cells only

  Cell '%s' is a leaf cell.

DESCRIPTION

You receive this message because the specified cell is a leaf cell, and the command
you executed applies only to hierarchical cells.

WHAT NEXT

Re-execute the command and ensure that you do not specify a leaf cell.

CNTXT-005 (information) The design has rise/fall qualified exceptions which will not be written out.

DESCRIPTION

You receive this message to inform you that **write_context** will not write out the
rise/fall qualified exceptions in your design. Rise/Fall qualified exceptions are
supported only by Primetime; neither **write_context** nor **write_sdc** will write them out
for either dcsh or dctcl mode.

WHAT NEXT

This is an informational message only. No action is required on your part.

DB

DB-1 (error) File is not a DB file.

DESCRIPTION

The identified file was not in the DB file format.

WHAT NEXT

Check to see what format the file is in, and read it with the appropriate command. For example, edif files can be read into **dc_shell** with the **read -format edif <filename>** command.

DB-3 (warning) Can't locate file '%s'.

DESCRIPTION

This warning message will be printed out the first time if we can not resolve a link to a given file. In the absense of the given file, there will be some unresolved references.

WHAT NEXT

Check the link_library and the search_path variables and set their value accordingly.

DB-4 (error) Open gen_state (0x%x) -- %s object '%s' (0x%x) attach '%s' id = %d

DESCRIPTION

WHAT NEXT

DB-5 (error) Limit exceeded: Cannot create attribute %s for

class %s, so program cannot continue.

DESCRIPTION

This message appears when the internal limit of 32k attributes per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

WHAT NEXT

Check the scripts to see if an excessive number of **create_attribute** commands are run with unique attribute names. Try to reuse names where possible. If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DB-6 (error) Limit exceeded: Cannot create attach %s for class %s, so program cannot continue.

DESCRIPTION

This message appears when the internal limit of 32k types of attaches per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

WHAT NEXT

If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DBR-001 (error) Cannot read file '%s'.

DESCRIPTION

```
The file you specified either does not exist or you do not have read access to the
file.
```

WHAT NEXT

```
Check the search_path or use the file command to verify the existence and other
attributes of the file.
```

DBR-002 (information) Errors reading file '%s'.

DESCRIPTION

```
Errors occurred while reading the specified file.
```

WHAT NEXT

```
Check previous messages, which indicate what went wrong and what action you can take
to correct the problem. If there are no messages preceeding DBR-002, then the file
is most likely corrupt.
```

DBR-003 (warning) Design '%s' (file '%s') is already registered. Remove the design before rereading.

DESCRIPTION

```
While reading a design from a file, that design/file combination was found in
memory. This means that the file was read previously.
```

WHAT NEXT

```
If the file has changed and you want to reread it, remove the design using the
remove_design command, then reread the file.
```

DBR-004 (warning) Library '%s' (file '%s') is already registered.

DESCRIPTION

While reading a DB file, a library/file combination that is already in memory was found. This means that the file was read previously.

WHAT NEXT

If the file has changed and you want to reread it, you can remove the library using the **remove_lib** command, then reread the file. However, in the process, if a linked design references this library, that design will need to be unlinked and will need to be completely rebuilt.

DBR-005 (information) Design '%s' not loaded.

DESCRIPTION

While reading in a design, some inconsistencies were found, so the design was not loaded. It's likely that the db file has errors, such as multiple nets with the same name on a single design.

WHAT NEXT

Check previous messages which will indicate what went wrong, and what action you can take to correct the problem. Usually, the application which created the db is the cause.

DBR-006 (error) Unknown pin '%s' makes instance '%s' of '%s' in design '%s' inconsistent with previous instances.

DESCRIPTION

While reading in a design, an instance of a design is inconsistent with previous instances because a pin is not found.

WHAT NEXT

Make sure that the DB is valid.

DBR-007 (warning) Found unsupported LSI reference '%s' to '%s' in design '%s'.
 The linker will not be able to resolve this reference.

DESCRIPTION

```
While reading in a design, an instance of a design was found to be derived from an
LSI netlist. This tool only supports fully name-based references from LSI netlists.
Order-based or mixed order and name based references are not supported.
```

WHAT NEXT

```
Use another Synopsys tool to read the DB, link it, and write it out to a new DB
file. This will resolve the naming issue.
```

DBR-008 (error) Cannot remove library '%s':

DESCRIPTION

```
The library contains objects which are being referenced. For example, some cells may
used in the current design, or a wire load model may be in use. If a QTM model is
being created, and it is referencing the library, then it must be saved before the
library can be removed.
```

```
Each reason why the library cannot be removed is listed.
```

WHAT NEXT

```
Remove the designs with the remove_design command before using remove_lib, since a
design is the source of most library references. Other causes, like QTM model
creation, may require other actions.
```

DBR-009 (warning) Found name-based LSI reference '%s' to '%s' in design '%s'.
 The linker might not be able to resolve this reference.

DESCRIPTION

```
While reading in a design, an instance of a design was found to be derived from an
```

LSI netlist. The reference is fully name-based. However, even in the case of name-based references, the linker might not be able to resolve references. The LSI netlist allows unconnected pins to be omitted from the reference, so, for example, an FD1 with D, CP, and Q pins connected, would be represented with the QN pin missing. The linker will indicate that the reference has too few ports.

WHAT NEXT

Use another Synopsys tool (like Design Compiler) to read the DB, link it, and write it out to a new DB file. This will resolve the missing pins issue.

DBR-010 (error) Cannot access temp directory '%s'%s.

DESCRIPTION

The read process utilizes a temporary directory to create transient files. These files are deleted when the read process completes. The name of the directory is found in the variable 'pt_tmp_dir'. In this case, the program was unable to create files in that directory.

WHAT NEXT

Verify that the specified directory exists, is writeable, and that the disk has some space available. If no space is available, try setting pt_tmp_dir to an alternate directory.

DBR-011 (error) Problem in read_%s: %s.

DESCRIPTION

The read process detected an error, which is detailed in the message. Some are intermediate file problems (see DBR-010); others are process related. For example, if the message indicates "invalid access", it means that the command is not being used correctly.

WHAT NEXT

Action based on the message text.

DBR-012 (error) Cannot read design db files. A db file must be

a library.

DESCRIPTION

```
Reading designs in the db format is not supported. Reading of db files is supported
for libraries only.
```

WHAT NEXT

```
Do not read files containing designs in db format. Use other supported formats for
reading design files.
```

DBR-013 (error) read_min_max_lib can only merge libraries.

DESCRIPTION

```
The read_min_max_lib can only be used to read and merge two library DBs - one min
library, and one max library.
```

WHAT NEXT

```
Check the arguments provided to command read_min_max_lib.
```

DBR-014 (error) multiple libraries in a single DB not supported.

DESCRIPTION

```
Command read_min_max_lib can only be used on a DB file which contains multiples
libraries.
```

WHAT NEXT

```
Check the arguments provided to command read_min_max_lib.
```

DBR-015 (warning) Ignoring degenerated cell '%s' from library

'%s'.

DESCRIPTION

```
This message warns you that PrimeTime has found a degenerated cell in the library
and is ignoring it.
```

WHAT NEXT

```
This is a warning message only. No action is required on your part.
```

DBR-016 (error) Cannot find port '%s' for cell '%s' in all libraries.

DESCRIPTION

```
You receive this message because PrimeTime has found the specified port in either
the min or max condition library db file but not the other. The ports of the library
cells in the min and max condition libraries must be identical.
```

WHAT NEXT

```
Examine the min and max condition libraries and ensure that they contain the same
set of library cells with the same ports.
```

DBR-017 (error) Cannot find %s '%s' in all libraries.

DESCRIPTION

```
You receive this message because PrimeTime has found the specified cell in either
the min or max condition library db file but not the other. The library cells in the
min and max condition libraries must be identical.
```

WHAT NEXT

```
Examine the min and max condition libraries and ensure that they contain the same
set of library cells.
```

DBR-018 (error) %s value '%g' of operating condition '%s' is

different from the nominal %s value '%g'.

DESCRIPTION

You receive this message if PrimeTime finds the specified operating condition value
in either the min or max condition library db file and that value is different from
the nominal value.

WHAT NEXT

Ensure that all operating conditions in the min and max library db files are
nominal.

DBR-019 (error) Cannot find operating condition '%s' in library '%s'.

DESCRIPTION

You receive this message because the operating condition you specified cannot be
found in the specified library.

WHAT NEXT

Use the **report_lib** command to list the operating conditions in the specified
library. Then re-execute the command, using only the available operating conditions.

DBR-020 (information) Renamed scalar %s '%s' to '%s' in design '%s'.

DESCRIPTION

While reading a Verilog file with PrimeTime's native Verilog reader, two net or port
names were found to be in conflict, requiring one of the objects to be renamed. This
can occur for one of two reasons: an ambiguous bus naming style or escaped names.

Given a bus_naming_style of "%s%d" and the following verilog port declarations:

output z1;
output [1:0] z;

the bus reference z[1] infers a port named z1. This conflicts with the scalar port

z1, declared with the first output statement.

The second case can be shown with the following verilog wire declarations:

```
wire \z[1];
wire [1:0] z;
```

Assuming the default bus_naming_style of "%s[%d]", the problem here is that bus reference z[1] infers a net named z[1], and so does the scalar declaration.

WHAT NEXT

No action is required. This is an informational message.

DBR-021 (warning) Library file '%s' is already registered.

DESCRIPTION

You tried to read a library DB file which has already been loaded into memory.

WHAT NEXT

If the file has changed and you want to reread it, you can remove the library using the **remove_lib** command, then reread the file. However, in the process, if a linked design references this library, that design will need to be unlinked and will need to be completely rebuilt. If you were using **read_min_max_lib**, then using the -force option will do all of this for you.

DBR-022 (error) Template %s is not the same in min and max libraries.

DESCRIPTION

The two libraries given to command read_min_max_lib contain a template of the same name but different content. Two templates must be the same to allow use of the cell lookup tables from two libraries as one min-max table. This is both an implementation limitation and a feature to improve performance of delay calculation. Two templates are considered same if the variables and indices have same name and same order, same size of the array for each index, and each index value is the same.

WHAT NEXT

Check the libraries provided to command read_min_max_lib. They should contain same templates. The easiest way to achieve this is to do textual difference on the two .lib files and make sure that the sections describing templates are absolutely the same (excluding blanks and formating). In case when the templates differ you will have to choose one of the sets of templates, put it into the other .lib file, and manually or using a script recalculate all cell delay tables in that library to conform to the new templates. Another way is to set options in the characterization tool that generates .lib files to use a fixed template for both libraries if such option is available.

DBR-023 (error) Duplicate reference port '%s/%s' in module %s ending at line %d in %s

DESCRIPTION

While reading a Verilog file with PrimeTime's native Verilog reader, an instance was found where a scalar port and a bus port in the terminal list are in conflict because of the bus_naming_style. For example:
BOX i0 (.DATA1(a), .D({c ,d}), .\D[1] (b), .Z(z));
Here, the scalar port D[1] and the bus port D[1] are in conflict if the bus_naming_style is %s[%d]. If the bus_naming_style is %d(%d), there is no conflict. This is an error because renaming reference ports is unpredictable, and therefore, not supported.

WHAT NEXT

Either change the bus_naming_style or investigate how such a conflict was introduced into your netlist.

DBR-024 (warning) Can't connect pin '%s' to net '%s' in design '%s':
already connected to net '%s'

DESCRIPTION

An attempt was made to connect a pin to a net and the pin is already connected to a net. This is typically an error in the netlist, such as a duplicated connection. For example, this message would be generated when reading an EDIF file which has a construct similar to this:

```
(net d
  (joined
```

```
      (portRef d)
      (portRef D (instanceRef n1))
      (portRef D (instanceRef n1))
    )
  )
```

WHAT NEXT

This is a warning indicating that the connection was ignored, so no specific action
is necessary.

DBR-026 (error) Unable to create %s '%s' in design '%s'

DESCRIPTION

While reading in a design, an object (such as a port, cell, or net) could not be
created. It's likely that the db file has errors, such as multiple nets with the
same name on a single design. The object name and design name are given in the
message. Such an error will cause the loading of the design to fail, although other
designs in the file which do not exhibit problems will be loaded.

WHAT NEXT

Usually, the application which created the db is the cause.

DBR-030 (error) Invalid global reference '%s' -
%s
in module ending at line %d in %s

DESCRIPTION

You receive this message if PrimeTime finds an invalid global reference while
reading a Verilog file with PrimeTime's native Verilog reader. A global reference is
a connection to a wire in another module. PrimeTime's native Verilog reader puts
several restrictions on the use of global references. For a reference of the form
module.wire, all of the following must be true:

• The module must exist in the file being read.

• The module must precede the module that is making the reference.

• The wire must exist in the module.

• The wire must be a logic constant.

Any deviation from these rules generates this error message.

WHAT NEXT

There is no other support for global signals. You must remove them from your netlist.

DBR-031 (error) Attribute '%s' cannot be imported:
 You defined it as %s; db defines it as '%s'.

DESCRIPTION

You receive this error message because while reading an attribute from db, there was a mismatch between the type (integer, string, etc.) that db defines for the attribute and the type that PrimeTime defines for the attribute. Usually, this is a user-defined attribute, defined with the **-import** option on **define_user_attribute**, and the types do not match.

WHAT NEXT

Rerun PrimeTime and define the attribute correctly. You might need to use other Synopsys applications to determine the actual type of the attribute.

DBR-032 (information) Ignoring library cell '%s' which does not have
 any pins defined on it.

DESCRIPTION

This message indicates that while reading the library, PrimeTime detects that the named library cell does not have any pins defined on it. Library cells without pins are ignored and not loaded because they do not have any effect in the timing analysis.

WHAT NEXT

There is no user actions required unless you think the indicated cell should have pins. If so, you need to go back to the original source of the library in order to fix it.

DBR-033 (warning) Found bad bus definition for '%s' - %s.

DESCRIPTION

This message indicates that while reading the DB file, PrimeTime detected that the named bus definition is wrong or not consistent. PrimeTime may not be able to properly link the design due to this problem.

WHAT NEXT

Normally, this indicates errors in the DB file. Please fix the bus definition in the DB file by going back to the source of the DB file and regenerate it from the tools originally created this DB file.

DBR-040 (error) Design '%s' was not found in '%s'

DESCRIPTION

You receive this message because **swap_cell** loaded the file you specified using the **-file** option, but did not find the specified design in the file. This error could be caused by a misspelling or typo in the design name or filename, or both; or by inadvertently specifying a file that does not contain the intended design.

WHAT NEXT

Examine the file, verify that the intended design name is contained in the file, and note the spelling of the design name. Then re-execute **swap_cell** using the correct design and file names.

DBR-050 (warning) Number of state table inputs for %s/%s/%s (%d) exceeds %d.

DESCRIPTION

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 16 inputs. This message warns you that the presence of this cell with its large state table will degrade read performance, because processing is exponential.

WHAT NEXT

This is a warning message only. No action is required on your part.

DBR-051 (error) Too many table inputs for %s/%s/%s (%d). State table information ignored in this case.

DESCRIPTION

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 30 inputs. PrimeTime cannot load state table information for more than 30 inputs, and is ignoring this information.

WHAT NEXT

Consult the Library Compiler documentation for alternatives to storing state tables.

DBR-060 (error) Can't set min library to %s.

DESCRIPTION

You receive this message if the min library you passed to **set_min_library** is invalid. For example, the min library you specified might have been the same as the max library, or it might have already been used as the max library in a **set_min_library** command. The max and min libraries must be different. The message text will indicate the condition.

WHAT NEXT

Re-execute **set_min_library** and specify a valid min library.

DBR-061 (information) '%s' already has '%s' as its min library.

DESCRIPTION

The min library you passed to **set_min_library** has already been related to the max library using **set_min_library**.

WHAT NEXT

This is an informational message only; no action is required on your part. However,

if you intended to change the relationship of the max library to a different min
library, check the spelling of the min library argument and re-execute the command
if necessary.

DBR-062 (warning) Cannot create max/min library cell relationship for '%s':
 %s.

DESCRIPTION

The **set_min_library** command found a library cell in the min library that matches the
library cell in the max library. However, some aspect of the two library cells is
different. For example, one might have more pins than the other; the pins might be
in a different order; or the timing arcs might be different. The text of the message
states the most serious difference. To create a max/min library cell relationship,
both cells must have the same timing arcs and the same pins, with the same order and
direction.

For cells where the max/min relationship fails, as in the current situation, the
command uses a minimum condition delay calculation based on the max library. If even
one of the library cell pairs matches and compares correctly, the **set_min_library**
command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should
read the message text to determine why the cells are different, and ensure that the
max and min libraries are compatible.

DBR-063 (warning) No match for %s/%s in library '%s'.

DESCRIPTION

The **set_min_library** command could not find a library cell in the min library that
matches the specified library cell in the max library. Therefore, a max/min library
cell relationship cannot be created for that cell.

For cells where the max/min relationship fails, as in the current situation, the
command uses a minimum condition delay calculation based on the max library. If even
one of the library cell pairs matches and compares correctly, the **set_min_library**
command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should

determine why there is not a match for the specified cell, and ensure that the max and min libraries are compatible.

DBR-100 (information) Ignoring external links found in design '%s'
 (file '%s')
 because dbr_ignore_external_links is set to true.

DESCRIPTION

You receive this message if your design contains external links but the **dbr_ignore_external_links** variable is set to *true*. In this case, the application ignores the external links and instead searches for an object by name only in the libraries in the **link_path**.

External links are created by Design Compiler in certain situations when writing a DB file; for example, when there is a link from a design to a wire load model in a library. The external link records information about the library to which the wire load was linked. Operating conditions can also have external links created for them.

You would set the **dbr_ignore_external_links** variable to *true* if you wanted to use a different library in PrimeTime than was used in Design Compiler.

WHAT NEXT

If you intended for the external links to be ignored, no action is required on your part. Otherwise, set the **dbr_ignore_external_links** variable to *false* and reexecute the application.

DBR-101 (warning) Pin '%s' is not found on library cell '%s'. Generated clock defined on this pin will not be created.

DESCRIPTION

While reading in a design, a generated clock definition has been found for a library cell, but the source pin of the generated clock does not exist on that library cell. Thus, the generated clock will not be created if this was the only source pin of the generated clock.

WHAT NEXT

The Synopsys database format (.db) appears to be incorrect. Please recreate the database with the correct source pin name for the generated clock.

DBR-200 (warning) Cannot read DDC attribute %s for design %s.

DESCRIPTION

```
The specified attribute could not be read for the given design. The attribute is
ignored.
```

WHAT NEXT

```
Modify the design in the tool that generated the DDC file so that it does not
generate this attribute.
```

DBR-201 (warning) Unknown pin direction in DDC for pin %s

DESCRIPTION

```
The DDC file has a pin direction that PrimeTime does not recognize. It uses the
internal direction for such pins.
```

WHAT NEXT

```
Change the design so that the tool that generates the DDC file does not generate the
bad pin direction.
```

DBR-202 (error) Scenario name %s supplied when no scenarios stored

DESCRIPTION

```
A read_ddc command was issued with a scenario name argument, but there were no
scenarios stored in the DDC file.
```

WHAT NEXT

```
Either re-generate the DDC rile with the scenario, re-issue the read_ddc command as
-netlist_only to ignore all constraints, or re-issue the read_ddc command without
the scenario to pick up the non-scenario constraints.
```

DBR-203 (error) Scenario name %s did not match an available

scenario %s.

DESCRIPTION

A `read_ddc` command was issued with a scenario name that did not match any of the scenarios in the DDC file. A list of available scenarios is listed.

WHAT NEXT

Choose one of the available scenarios and re-issue the `read_ddc` command with the chosen scenario.

DBR-204 (error) File %s is not in DDC format.

DESCRIPTION

The `read_ddc` command was issued for the given file, but the file is not in DDC format.

WHAT NEXT

Either remove the file from the `read_ddc` command, or generate the file as a DDC file.

DBR-205 (error) File %s has too old a version for PrimeTime to read.

DESCRIPTION

PrimeTime cannot read the given file because the DDC version number is too old.

WHAT NEXT

Convert the DDC file to a new version. Simply read the file into a tool that can write DDC (such as DC), then write the file out again. The tool will write it out as a new version.

DBR-206 (Warning) The library has non-continuous base curves and can have a negative impact on PrimeTime's

performance and memory.

DESCRIPTION

The base-curve ids for the CCS library that is used is not numbered continuously. For eg, the curve_y ids for the base curves in the library are (1, 2, 5, 6, 7 ..) instead of the recommended sequential ordering (1, 2, 3, 4, 5, ...). Such libraries can cause a negative impact on performance and memory of PrimeTime.

WHAT NEXT

Use the latest version of Library Compiler to get a compatible version of the library.

DCM-100 (warning) Unable to load DCM library for '%s'. Using the default delay model as specified in the .db library.

DESCRIPTION

The program is unable to load the DCM library corresponding to the .db library as specified in the error message. This happens because of one of the following reasons:

* One or more of the following shell environment variables
  are not set or are incorrectly set:
DCMRULEPATH (or CDCRULEPATH)
DCMRULESPATH (or CDCRULESPATH)
DCMTABLEPATH (or CDCTABLEPATH)
* The DCM library does not exist in the location specified or
  it does not have the proper file permissions.
* Your installation is not authorized for the DCM-Delay-Calculation
        feature.

When this error is encountered, the program treats the library as a non-DCM library and derives the delay model as though it were a .db library.

WHAT NEXT

The error messages preceding this one should make the exact cause of the problem clear. Make sure that the aforementioned shell environment variables are set correctly and the DCM library exists as specified with the correct file permissions. Make sure your Synopsys key file includes the DCM-Delay-Calculation license.

DCM-101 (error) Errors found during rule_init() - library '%s' will be unloaded.

DESCRIPTION

The PI function rule_init() of the Delay Calculation System (DCS) standard returned an error code. Typically, the DCS itself issues the diagnostic messages that display before this message. When this message is issued, the program cannot load the remaining DCM subrules and link the EXPOSE and EXTERNAL functions correctly.

Please contact the library provider or Synopsys if you encounter this message.

DCM-102 (warning) No DCM model for cell '%s' of library '%s'.

DESCRIPTION

This error message is issued when the DCM library returns a nonzero error status

WHAT NEXT

Check the error messages issued by the DCM prior to this error message and correct
any problems. Verify that you have matching versions of the DCM timing and auxilary
cell libraries. Contact your library provider for more information.

DCM-103 (error) Unable to load DCM EXPOSE function '%s' from the DCM library. This
library cannot be used by this program without the specified EXPOSE function.

DESCRIPTION

This message is issued when the program tries to load the specified DCM EXPOSE
function from the specified DCM library and cannot locate a matching function.
Because this EXPOSE function is considered critical for the proper calculation of
delay values, this library cannot be used by this program for timing calculations.

WHAT NEXT

Please contact your library provider for more information.

DCM-104 (error) The following feature of the DCL language is not (yet)
supported by this program: %s.

DESCRIPTION

The current implementation of the program does not fully support the specified

feature of the Delay Calculation System (DCS) standard specification. This can
result in this particular DCM library being unsuitable for use for delay
calculations by this program.

WHAT NEXT

You cannot use this DCM library for timing calculations until this restriction is
removed. Please contact your library provider to see if a version of the library
without the specific feature is available.

DCM-105 (error) Error while processing DCL external function '%s' - passed pin '%s' is
 not part of the current timing arc.

DESCRIPTION

The DCL-PI standard defines a number of functions that request the netlist
information from the timer application using the pin name rather than the pin
pointer. The current implementation of the program supports this feature only as
long as the referenced pin name is part of the timing arc currently under
consideration. That is, you can substitute the external call with the equivalent
byPin() call.

by the equivalent byPin() call.

WHAT NEXT

If you have access to the DCM library source, modify it such that the equivalent
byPin() function is used instead of the named external function. Otherwise, please
contact your library vendor. equivalent byPin() function is used instead of the
named external function. Otherwise, please contact your library vendor.

DCM-106 (warning) The DCL-PI function '%s' returned a nonzero error code %d while
 processing the timing segment '%s'.

DESCRIPTION

This message appears when the program calls one of the CALCULATION functions as
defined in the DCS standard specification and that function returns a bad error
code. This typically indicates a problem in the DCM library itself.

If you have access to the DCL source code of the library, modify please contact your
library provider.

DCM-107 (warning) Unsupported test type or edge propagation pair '%s' specified for
 the arc '%s'. This arc will be ignored.

DESCRIPTION

This message is displayed when the program loads the timing arc and detects that
test type or the edge propagation characteristics specified for this arc types and
edge propagation pairs, please consult your documentation.

WHAT NEXT

If you have access to the DCL source code of the library, change program. Otherwise,
please contact your DCM library provider.

DCM-108 (warning) Internal timing pin '%s' of cell '%s' in library '%s' is
 not defined in the corresponding .db library. Any timing arcs connecting to or from
 this pin will be ignored.

DESCRIPTION

This message is displayed when the program loads the timing arcs and detects that
the DCM has requested the creation of a new timing point, but no of the library
cell's pins, including the internal timing points, must be defined in the technology
library .db file before they can be referenced in the DCM.

WHAT NEXT

If you have access to the source code of the Synopsys technology library (.lib)
corresponding with the DCM being loaded, you can add a new internal timing pin for
the corresponding cell in the library. Note that current limitations of the Library
Compiler product dictate that a "timing()" group must be present for each internal
timing pin. However, when using the DCM library, all the each internal timing pin.
However, when the DCM library is used, all the timing information comes from the DCM

library and any timing data specified in the .db library is ignored.

DCM-109 (warning) %s '%s' is invalid. The valid values are '%s' and '%s'

DESCRIPTION

This message is displayed when an invalid version is set.

WHAT NEXT

Change the version to one of the valid values and re-run the design.

DCM-110 (warning) DPCM expose dpcmAddWireLoadModel not supported in DPCL library. Therefore DB/custom wireload models are not supported.

DESCRIPTION

This message is displayed when the expose dpcmAddWireloadModel is not supported in the DPCM Procedural Interface.

WHAT NEXT

Use DPCM wireloads. If db wireload has to be used support the expose in DPCM.

DCM-111 (warning) The design %s read in has wireload %s, which is not present in the current DPCM. Changing to default DPCM wireload %s.

DESCRIPTION

You receive this warning message when the current wireload attached to the design is not present in one of the DPCM libraries.

WHAT NEXT

Use a wireload that is in one of the DPCM libraries. To see a list of wireloads in

the DPCM libraries, use the **report_lib** command.

DCM-112 (warning) The design %s read in has a DCPM wireload %s. Deleting the dpcm wireload.

DESCRIPTION

This message is displayed when the current wireload attached to the design is from a DPCM library and not db.

WHAT NEXT

Use DB wireloads. List DB wireloads by doing report lib.

DCM-113 (information) Propagating clocks through cell '%s' instantiated from design '%s'.

DESCRIPTION

Generate ouput clocks for special cells such as DLL/DCM.

DCM-114 (information) The clock '%s' with period '%s' generated on pin '%s'.

DESCRIPTION

Generate a clock for ouput pin of special cells such as DLL/DCM.

DCM-115 (information) Please check CLKFX_DIVIDE value: '%s'.

DESCRIPTION

CLKFX_DIVIDE value is not valid.

DCM-116 (information) Please check CLKFX_MULTIPLY value: '%s'.

DESCRIPTION

```
CLKFX_MULTIPLY value is not valid.
```

DCM-117 (information) Please check CLKDV_DIVIDE value: '%s'.

DESCRIPTION

```
CLKDV_DIVIDE value is not valid.
```

DCM-118 (warning) During the polynomial reduction procedure, the '%s' variable is saturated from %f to %f.

DESCRIPTION

```
This warning message occurs when a boundary value instead of the original variable
value is used for polynomial reduction.
```

WHAT NEXT

```
A polynomial is reduced before final calculation if its parameters contain one of
the following variables defined in the operating conditions: temperature,
parameter1, parameter2, parameter3, parameter4, parameter5, voltage, voltage1, ...,
voltage99.

If the variable value defined in the operating conditions is out of the boundary
defined in the polynomial, then the closest boundary value for the variable will be
used for polynomial reduction.

For example, if the temperature variable defined in the current operating condition
is 20, while the range of the temperature in the polynomial is [25, 40], then 25
instead of 20 is used to reduce this polynomial.
```

DDB

DDB-1 (warning) Cell %s not added to design %s because a cell with that name already exists.

DESCRIPTION

WHAT NEXT

DDB-2 (warning) Net %s not added to design %s because a net with that name already exists.

DESCRIPTION

A net with the specified name already exists.

WHAT NEXT

Reissue the command with a new net name. Use the **report_net** command to find a list of all the nets currently present in the design.

DDB-3 (warning) Consistency problem: port %s is not owned by any design or reference.

DESCRIPTION

The specified port is not owned by any design.

WHAT NEXT

Check the consistency of your design database.

DDB-4 (warning) Consistency problem: a pin is not owned by

any cell.

DESCRIPTION

```
The specified pin is not owned by any design.
```

WHAT NEXT

```
Check the consistency of your design database.
```

DDB-5 (warning) Consistency problem: cell %s is not owned by any design.

DESCRIPTION

WHAT NEXT

DDB-7 (warning) Consistency problem: net %s is not owned by any design.

DESCRIPTION

WHAT NEXT

DDB-8 (warning) Consistency problem: a pin was found without a corresponding port.

DESCRIPTION

WHAT NEXT

DDB-9 (warning) Consistency problem: cell %s was found

without a corresponding reference.

DESCRIPTION

WHAT NEXT

DDB-10 (warning) Consistency problem detected in design %s %s

DESCRIPTION

WHAT NEXT

DDB-11 (warning) Internal error %s

DESCRIPTION

WHAT NEXT

DDB-12 (warning) Removed duplicate cell '%s'.

DESCRIPTION

WHAT NEXT

DDB-13 (warning) The name of net '%s' in design '%s' can't be changed

to the name of both ports '%s' and '%s' to which it's connected.

DESCRIPTION

WHAT NEXT

DDB-14 (warning) The net '%s' in design '%s' is connected to both
 ports '%s' and '%s'.

DESCRIPTION

Two ports can only be connected to a net if they are inout ports or if they drive
wired logic. Connecting two input ports to a net can limit the optimization that can
be performed by Design Compiler on the net.

WHAT NEXT

Disconnect one of the ports from the net using the **disconnect_net** command.

DDB-21 (error) Conflict between logic 0 and 1. Can't %s.

DESCRIPTION

The two specified ports were set previously as logic 0 and 1. They might not have
been directly set, but could have been implicitly set by a sequence of **set_equal** and
set_opposite commands.

WHAT NEXT

If the ports were directly set as logic 0 and 1, the next steps are as follows:

Use **report_attributes** commands on the two ports. They will have the
driven_by_logic_zero and driven_by_logic_one attributes set.

Remove one of these two attributes, one of which is incorrect,
using the **remove_attribute** command

Reissue the original command.

If the ports were implicitly set as logic 0 and 1 through a sequesce of **set_equal**
and **set_opposite** commands, the next step is as follows:

Use the **reset_design** command to remove the setting of 0 and 1 on the ports. this command removes all other constraints on the design and should be used with caution.

DDB-22 (error) Can't set equal ports opposite in design '%s': '%s' '%s'.

DESCRIPTION

The two ports were set as equal ports previously. They might not have been directly set, but could have been implicitly set by a sequence of **set_equal** and **set_opposite** commands.

WHAT NEXT

The two specified ports were set previously as equal ports. The only way to revert back this setting is to reset the design using the **reset_design** command. This command removes all other constraints on the design and should be used with caution.

DDB-23 (error) Can't set opposite ports equal in design '%s': '%s' '%s'.

DESCRIPTION

The two ports were set as opposite ports previously. They might not have been directly set, but could have been implicitly set by a sequence of **set_equal** and **set_opposite** commands.

WHAT NEXT

The two specified ports were previously set as opposite ports. The only way to revert back this setting is to reset the design using the **reset_design** command. This command removes all other constraints on the design and should be used with caution.

DDB-24 (warning) Overwriting design file '%s/%s'.

DESCRIPTION

Overwriting the specified version of the design with more recent version.

Warning only. No action is required.

DDB-27 (error) '%s' value must be positive.

DESCRIPTION

A negative value was entered. Constraint values must be positive (or 0).

WHAT NEXT

Please enter a non-negative value.

DDB-28 (error) '%s' cannot be set on %s pin '%s'.

DESCRIPTION

The specified constraint cannot be set on a pin of the specified direction. The constraint command will be ignored.

WHAT NEXT

Please enter a correct constraint command.

DDB-29 (error) '%s' cannot be set on %s port '%s'.

DESCRIPTION

The specified constraint cannot be set on a port of the specified direction. The constraint command will be ignored.

WHAT NEXT

Please enter a correct constraint command.

DDB-30 (error) Can't specify output port '%s' as a path

startpoint.

DESCRIPTION

Output ports are not valid as path startpoints. There are no timing paths from such
ports.

WHAT NEXT

Examine the design to determine the correct startpoint for the path.

DDB-31 (error) Can't specify input port '%s' as a path endpoint.

DESCRIPTION

Input ports are not valid as path endpoints. There are no timing paths to such
ports.

WHAT NEXT

Examine the design to determine the correct endpoint for the path.

DDB-32 (error) Can't specify hierarchical cell '%s' as a path '%s'.

DESCRIPTION

Hierarchical cell names are not valid as path startpoints or endpoints.

WHAT NEXT

Use a clock, port, pin (leaf or hierarchical), or cell (leaf only) as the path
startpoint or endpoint.

DDB-33 (error) Pin '%s' does not have a library hold time.

DESCRIPTION

None.

WHAT NEXT

```
Check the target library.
```

DDB-34 (error) %s '%s' is in design '%s', but %s '%s' is in design '%s'.

DESCRIPTION

```
None.
```

WHAT NEXT

```
None.
```

DDB-35 (error) '%s' does not exist in library '%s'.

DESCRIPTION

```
The listed key in the error message does not exist in the library.
```

WHAT NEXT

```
Check the key file.
```

DDB-38 (error) Can't open security file '%s' for protected library '%s'.

DESCRIPTION

```
Cannot open security file.
```

WHAT NEXT

```
Check the security file.
```

DDB-39 (error) Bad security key in file '%s' for library '%s'.

DESCRIPTION

You are trying to invoked **read_lib** on a protected library.

WHAT NEXT

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed. Then reinvode the **read_lib** command.

DDB-40 (error) Can't read protected library '%s'.

DESCRIPTION

You are trying to invoked **read_lib** on a protected library.

WHAT NEXT

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed.

DDB-41 (error) Incomplete library protection attributes.

DESCRIPTION

WHAT NEXT

DDB-43 (warning) Could not create attribute '%s' for %s objects.

DESCRIPTION

WHAT NEXT

DDB-44 (error) Can't read unprotected library '%s'.

DESCRIPTION

WHAT NEXT

DDB-45 (error) A design with name '%s' already exists in the same
 design file as design '%s'.

DESCRIPTION

WHAT NEXT

DDB-46 (error) A reference with name '%s' already exists in

design '%s'.

DESCRIPTION

WHAT NEXT

DDB-47 (error) A cell with name '%s' already exists in design '%s'.

DESCRIPTION

WHAT NEXT

DDB-48 (warning) Creating port '%s' on design '%s' with direction unknown.

DESCRIPTION

WHAT NEXT

DDB-51 (warning) In the value of %s, the characters separating the "%%s" and "%%d those separating each "%%d

DESCRIPTION

WHAT NEXT

DDB-52 (error) The value of %s

must include one "%%s" and two "%%d

DESCRIPTION

WHAT NEXT

DDB-53 (error) The value of %s
 must include one "%%s" and one "%%d

DESCRIPTION

The message is printed out when the current command found invalid value in the
indicated variable.

WHAT NEXT

Check the value of the given variable and provide the valid value.

DDB-54 (error) The value of %s
 must include only one "%%s" and only two "%%d

DESCRIPTION

The error message is printed out when the current command found invalid value in the
indicated variable.

WHAT NEXT

Provide the valid value for this variable.

DDB-55 (error) The value of %s
 must include only one "%%s" and only one "%%d

DESCRIPTION

The error message is printed out when the current command found invalid value for
the indicated variable name included in the message.

Provide the valid value for this variable.

DDB-56 (error) In the value of %s, there are no characters separating %s.

DESCRIPTION

This error message is printed out when the current command found that there are no character separators.

WHAT NEXT

Provide the valid value for the command.

DDB-57 (error) In the value of %s, the %s of the characters separating %s must not be%s a digit.

DESCRIPTION

This error message is printed out when the current command found digit in the character separators.

WHAT NEXT

Provide the valid value for the command.

DDB-58 (warning) In the value of %s, there are no characters separating the "%%s" and "%%d be ambiguous).

DESCRIPTION

If no characters separate the array name from the member number, the bus names will be ambiguous for arrays whose names end in a digit. For example, with **bus_naming_style** set to "%s%d", the name of the third member of array "A1" and the thirteenth element of array "A" would both have the name "A13".

Most likely you should change the value of the bus naming style to contain some
characters between the "%s" and "%d". See the help page for **bus_naming_style** for
details.

DDB-60 (error) Could not find library pin for pin '%s'.

DESCRIPTION

The back-annotation failed because the pin does not have a corresponding pin in the
link library.

WHAT NEXT

Verify that the design is fully linked with the 'link' command. Verify that all link
and target library search paths are valid.

DDB-66 (warning) Removing group '%s'.

DESCRIPTION

The path group is being removed because the operation being performed has removed
the last path from the group.

WHAT NEXT

Be aware that any subsequent attempts to use this path group will fail because the
group has been deleted. If you think the group should not have been deleted,
identify at least one path you think should still be in the group and trace back to
find which action deleted that path.

DDB-67 (warning) Removing %s from group '%s'.

DESCRIPTION

WHAT NEXT

DDB-68 (warning) Removing external delay related to clock %s.

DESCRIPTION

When a clock source is deleted from the design using the 'remove_clock' command, all
input and output delay values that were specified relative to that clock are also
deleted from the design. For example, consider the following script:

```
create_clock -name CLK -period 10 set_input_delay 2 -clock CLK all_inputs()
set_output_delay 2 -clock CLK all_outputs()

remove_clock CLK
```

The 'remove_clock' command will also have the effect of removing the input and
output delay values that were specified relative to CLK.

WHAT NEXT

No action is required, this is merely an informational warning.

DDB-70 (error) None of the selected cells were grouped.

DESCRIPTION

When using the 'group' command on an hdl design that has not been compiled yet, it
is possible that the cells you specified to be grouped cannot be grouped because
they need to stay with thier neighboors until the design has gone through resource
sharing in compile.

WHAT NEXT

Use the 'group' command after the design has been compiled.

DDB-71 (error) Design '%s' requires one of the following

licenses: '%s'.

DESCRIPTION

The specified design is licensed and requires one of the listed licenses to be available. An error has occurred because none of the licenses could be obtained.

WHAT NEXT

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If your site does have one of the licenses, try again when the license is available.

DDB-72 (information) Added key list '%s' to design '%s'.

DESCRIPTION

Indicates that the listed set of licenses have been associated with the specified design. Accessing the design will require that one of the listed licenses can be successfully checked out.

WHAT NEXT

No action is required since this is just an information message.

DDB-73 (warning) License '%s' contains the illegal character '%c'.
It was ignored.

DESCRIPTION

One of the licenses associated with a design contains an invalid character. That license will be dropped from the list of licenses which can be used to access the design.

WHAT NEXT

If a design is associated with multiple licenses, it may be possible to access the design via a different, valid license. In any case the license name should be updated so that it does not contain any invalid characters. Invalid characters include: ',', '}', '{', '*', ''.

DDB-74 (warning) Design '%s' inherited license information from design '%s'.

DESCRIPTION

All of the licenses associated with one design have now been associated with another design. This typically happens when a design is ungrouped. In that situation, the parent design will inherit all licensing information from the ungrouped design.

WHAT NEXT

Although this is classified as a warning, it is essentially just an information message. No action is required.

DDB-75 (warning) Design '%s' is being converted to a limited design.

DESCRIPTION

This message indicates that the indicated design has been converted into a limited design. A limited design is a design which can be compiled and analyzed, but whose contents may not be examined or written out.

A design gets converted into a limited design in two situations. In the first case you have only an evaluation license for the design (obtained by manually setting synlib_disable_limited_licenses = "FALSE"), and the design will remain limited because the intent of an evaluation license is for the design data to be restricted. In the second case the design was derived from a DesignWare part and has not yet been run through the **compile** command. In this latter case the design remains limited only until after it has been compiled, at which point the limitation is removed. The intent of this latter limitation is to protect the technology- independent structure of the design.

WHAT NEXT

If you have only an evaluation license for the limited design, then the only way to gain access to the internals of that design is through the use of a full license for that part; if a full license is subsequently obtained then the first **compile** command will remove the 'limited design' restrictions. If the design has already been compiled, it is sufficient to run the **get_license** command to convert the limited design back to a regular, unrestricted format.

If you already have a full license for the limited design, then after the first **compile** command you can expect the design to be converted back to a regular, unrestricted format.

DDB-76 (error) Cannot load design '%s'.

DESCRIPTION

The named design cannot be loaded into Design Compiler's internal data structures.
This can happen if certain synthetic parts cannot be found.

WHAT NEXT

Attempt to link the design with the command *link -all*. If this fails, check that the
software is correctly installed.

DDB-77 (error) License '%s' is a Synopsys internal key and should
 not have a seed associated with it.

DESCRIPTION

When license names are set on a design, third party keys must have a seed associated
with them. It is an error, however, for Synopsys internal keys to have seeds.

WHAT NEXT

When creating your own license names, make sure that they do not clash with the
Synopsys internal license names.

DDB-78 (error) No seed provided for the third-party license '%s'.

DESCRIPTION

When adding a third-party license, you must specify both a license name and a non-
zero seed. This prevents third party vendors from creating keys for each other's
licenses.

WHAT NEXT

Specify the license name as *name/seed*. For example: "MY_LIC/1234"

DDB-79 (error) The license '%s' has an invalid seed associated

with it.

DESCRIPTION

This error occurs when the *set_design_license command* is used to store a third party
license and a seed, and the seed that is specified is not consistent with the seed
that was used to create the key.

WHAT NEXT

Either generate a new key with the correct seed, or change the *set_design_license*
command line so that the seeds are consistent.

DDB-80 (error) The seed '%s' specified for license '%s' is not a valid 32-bit integer.

DESCRIPTION

Licenses can be specified in the from '<license>/<seed>' where <seed> is supposed to
be a valid integer which can be represented in 32 bits. In this case the <seed>
specified was either not an integer, or was too large to be represented in 32 bits.

WHAT NEXT

The <seed> associated with the license needs to be corrected such that it is a valid
integer which can be stored in at most 32 bits.

DDB-81 (warning) Unable to find specified driving_cell for port '%s'.

DESCRIPTION

The driving_cell attributes indicate that a port should inherit its drive capability
from a certain library cell. This error means that the tool was unable to locate a
matching library cell or pin on that library cell. This may happen if the
link_library does not contain the library for that cell, or if the cell name or pin
name was incorrect. The driving cell information can be seen using **report_port -
drive**. It may have been set by either **set_driving_cell** or **characterize**.

WHAT NEXT

If the driving cell requires a library that has not been identified in the

link_library, the **link_library** should be changed to include that library. Otherwise, check the information for errors in cell_name, library name, or pin names using **report_port -drive -only** *port_name*.

DDB-84 (error) Only ports of the same direction can be grouped.

DESCRIPTION

WHAT NEXT

DDB-85 (error) Objects must be either all ports or all nets.

DESCRIPTION

This error message is issued if a mixture of objects of different types is given as input to a command that requires a homogenous set of ports or nets as input.

WHAT NEXT

Re-issue the command specifying only ports or only nets as input.

DDB-86 (error) Bus name '%s' conflicts with existing names.

DESCRIPTION

This error message is issued when an attempt is made to create a bus with a name that conflicts with the name of an existing bus.

WHAT NEXT

Re-issue the command with a non-conflicting name for the bus.

DDB-87 (error) All objects must be from the same design.

DESCRIPTION

This error message is issued if a command that requires a set of objects belonging to the same design is invoked with objects that belong to different designs.

Re-issue the command with a set of objects that belong to the same design.

DDB-88 (error) At least one of the port objects specified is already a member of a bus.

DESCRIPTION

This error message is displayed if an attempt is made to insert a port that belongs to a bus into a new bus.

WHAT NEXT

Re-issue the command with ports that do not belong to an existing bus.

DDB-89 (error) Type name '%s' conflicts with existing type.

DESCRIPTION

This error message is issued if an attempt to create a type for a new bus object is made with a type name that is already used for another bus object with a different width.

WHAT NEXT

Change the name of the new bus type.

DDB-90 (error) specified range is different from number of objects to be bussed.

DESCRIPTION

WHAT NEXT

DDB-91 (error) only designs or references can have busses

created in them.

WHAT NEXT

DDB-92 (error) Cannot load design '%s' for an HDL embedded command.

DESCRIPTION

```
The named design cannot be loaded for the current command embedded in an HDL file.
The current embedded command is not legal within an embedded script. See the HDL
Compiler Manual for details.
```

WHAT NEXT

```
Change the embedded script so that it does not use the offending command.
```

DDB-95 (warning) Unable to find net instance '%s' in design '%s'.

DESCRIPTION

```
Back-annotation, such as a set_load or set_resistance value, was stored on a net
instance within the design, but that instance can no longer be found. This can occur
if a lower-level design containing the net instance was modified but the top-level
design was unaware of this change. Commands which could modify lower level designs
include ungroup, change_names, and compile.
```

WHAT NEXT

```
Perform ungroup and change_names at the top level so that the top level design will
have a chance to update its back-annotation records. Use characterize to move
annotation to a subdesign before running compile or reoptimize_design on that
subdesign.
```

DDB-100 (warning) Unable to find minimum version of library

cell '%s/%s' in library '%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum
analysis must use a particular library, but this library cell cannot be found in
that minimum library. Design Compiler will use the maximum version of the cell for
both maximum and minimum analysis in this case.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum
analysis. See if the indicated library cell was accidentally left out of the minimum
analysis library.

DDB-101 (warning) Unable to find minimum version of library pin '%s/%s' in library '%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum
analysis must use a particular library, but the indicated library cell has
conflicting pin descriptions between the maximum and minimum libraries. In this
case, a pin exists on the library cell in the maximum library, but that pin does not
exist in the minimum library. Design Compiler will use the maximum version of the
library pin for both maximum and minimum analysis in this case.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum
analysis. See if the indicated library pin was accidentally left out of the minimum
analysis library.

DDB-102 (warning) Conflicting timing arc descriptions between maximum library '%s' and minimum library '%s' to pin '%s/%s'.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum
analysis must use a particular library, but the indicated library cell has
conflicting timing arc descriptions between the maximum and minimum libraries. In
this case, a timing arc exists on the library cell in the maximum library, but a
corresponding timing arc does not exist in the minimum library. Design Compiler will

use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to consider timing arcs as compatible between minimum and maximum libraries, they must have the same sense (for example, positive unate, or clear), they must have the same SDF condition, and there must be the same number of arcs of each type between a pair of pins.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if timing arcs to the indicated library pin were accidentally left out of the minimum analysis library.

DDB-103 (warning) Pin %s of lib cell %s exists in maximum library %s but not in minimum library %s. Assuming min delay for pin to be same as max delay.

DESCRIPTION

The **set_min_library** command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has some pins in the max library which don't exist in the minimum libraries. Design Compiler will use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to be compatible between minimum and maximum libraries, the library cells must have the same pins and same timing arcs (same sense (for example, positive unate, or clear), they must have the same SDF condition), and there must be the same number of arcs of each type between a pair of pins.

WHAT NEXT

Check that the **set_min_library** command specified the correct library for minimum analysis. See if the specified pins of the specified library cell were accidentally left out of the minimum analysis library.

DDB-105 (warning) Design '%s' requires one of the following licenses: '%s'.
Waiting for license to become available, press <ctrl>-C to

terminate.

DESCRIPTION

The specified design is licensed and requires one of the listed licenses to be available. None of the licenses could be obtained. Design Compiler will wait for one of the licenses to become available and then continue.

WHAT NEXT

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If you wish to terminate the command instead of waiting for the license to become available, set synlib_wait_for_design_license = {}

DDB-107 (warning) Deleted or recreated %d internal pin(s) on cell '%s'. All attributes and attaches on it(them) are lost.

DESCRIPTION

The **access_internal_pins** variable controls creation and deletion of internal pins and user access to them. Because of the source of internal pins, they are created or deleted during link time, depending on the setting of this variable. You can use the **find** and **get_pins** commands to show internal pins, if such pins exist. Certain timing commands can also set constraints on internal pins.

WHAT NEXT

If this is what you intended to do, no action is necessary.

SEE ALSO

find (2), **get_pins** (2), **link** (2); **access_internal_pins** (3).

DDC-1 (error) Unable to open DDC file '%s' for writing.

DESCRIPTION

`dc_shell` encountered an I/O error when it attempted to open the specified DDC file for writing.

WHAT NEXT

Check that the file name is correct, that the directory exists and is writable, and that the filesystem is not full. If the target file already exists it must be writable in order for dc_shell to overwrite it.

DDC-2 (error) Unable to open file '%s' for reading.

DESCRIPTION

The tool encountered an error when it attempted to open the specified DDC file for reading.

WHAT NEXT

Check that the path to the file is correct and that the file is readable by the current user. Also verify that the file was written in DDC format.

SEE ALSO

write_file(2)

DDC-3 (error) DDC internal write error in design '%s'.

DESCRIPTION

`dc_shell` encountered an internal error while attempting to write the specified design. No DDC file was produced.

WHAT NEXT

Please contact the Synopsys Support Center for assistance.

DDC-4 (error) DDC internal read error in file '%s'.

DESCRIPTION

dc_shell encountered an internal error while attempting to read the specified file.
No designs were read.

WHAT NEXT

Please contact the Synopsys Support Center for assistance.

DDC-5 (error) Design data is corrupt in DDC file.

DESCRIPTION

The file being read has been modified or corrupted since it was originally written
by **dc_shell**.

WHAT NEXT

The DDC file must be re-created from the original design source. Note that DDC files
cannot be edited by the user.

DDC-6 (error) DDC file version is not compatible. The DDC file was written with
 dc_shell version %s dated %s.

DESCRIPTION

The file being read is an incompatible version of DDC that cannot be read with this
release of **dc_shell**.

WHAT NEXT

If the DDC file was written with an older release of **dc_shell**, you can run that
version of **dc_shell** to read the file and write it out in DB format. The current
version of **dc_shell** should be able to read the DB file and convert it to the current
DDC format.

If a newer release of **dc_shell** was used to write the DDC file, you must use that
version to read it back in.

DDC-7 (error) File is not in DDC format.

DESCRIPTION

`dc_shell` has determined that the file being read is not a DDC format file.

WHAT NEXT

Verify that the correct format option has been provided to the read_file command, and that the file path is correct.

DDC-8 (error) Attempt to write duplicate design name '%s' to DDC file.

DESCRIPTION

`dc_shell` detected an attempt to write multiple designs with the same name to a DDC file, which is not allowed by the DDC format.

WHAT NEXT

Check the list of designs provided to the write command. It is possible, although unusual, for duplicate design names to have been read from different files, such as multiple .db files. If the duplicate design names must be preserved, they must be written to separate DDC files.

DDC-9 (warning) The DDC format cannot be used to store physical data. Any physical
 information that is present will not be written to the DDC file.

DESCRIPTION

You receive this warning message when you write out a DDC file that contains physical data. The DDC file format is not capable of representing physical data. Only the logical representation will be written to the DDC file.

WHAT NEXT

It is considered best practice to use the Milkyway storage format for designs that contain physical information. You can use the **write_milkyway** command to write the design to a Milkyway database.

write_milkyway(2)

DDC-10 (error) Scenario '%s' does not exist.

DESCRIPTION

The specified scenario, which was provided with the -scenarios option to the **write** command, does not exist.

WHAT NEXT

Check that the scenario name is correct, and that any scenarios which are to be written to the DDC file have been created.

SEE ALSO

write(2)
create_scenario(2)

DDC-11 (error) DDC file contains packed command syntax that cannot be processed by
this version of dc_shell. Please use a current version of dc_shell to read this file.

DESCRIPTION

The current DDC file contains embedded commands (constraints) which were written by a newer version of **dc_shell** and utilize a syntax which cannot be parsed by the current executable.

WHAT NEXT

Use the same (or newer) version of **dc_shell** to read the file as was used to write it.

SEE ALSO

ddc_allow_unknown_packed_commands(3)
read_file(2)

DDC-12 (warning) DDC file was written with a newer version of dc_shell.
Some embedded commands may be ignored.

DESCRIPTION

You are trying to read a DDC file which was written by a newer version of **dc_shell**, and the DDC file contains some packed commands (constraints) which are not recognized by the older version of **dc_shell**. Normally this would result in a DDC-6 error; however, if the variable ddc_allow_unknown_packed_commands is set to "true" then **dc_shell** will attempt to read the file, but any unrecognized packed commands will be ignored. (A DDC-13 warning message will be printed when each such command is first encountered.)

WHAT NEXT

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of **dc_shell** as was used to write it.

SEE ALSO

DDC-13(n)
ddc_allow_unknown_packed_commands(3)
read_file(2)

DDC-13 (warning) Ignoring unknown packed command #%d: %s

DESCRIPTION

dc_shell attempted to unpack an embedded command which it does not recognize. This can happen when a DDC (or Milkyway) file which was written with a newer version of **dc_shell** is read with an older version of the product, while the variable ddc_allow_unknown_packed_commands is set to "true". The unrecognized command is simply discarded.

WHAT NEXT

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of **dc_shell** as was used to write it.

SEE ALSO

ddc_allow_unknown_packed_commands(3)

DDC-14 (information) This file contains data for the following %d scenarios:
 %s

DESCRIPTION

The DDC or Milkyway reader prints this message if the file being read contains any scenario-specific constraint data. The message will report the name of each scenario for which the file contains data. If the scenario was inactive when the file was written, an asterisk (*) appears after the scenario name.

WHAT NEXT

This is an informational message. No action is required.

SEE ALSO

read_file(2)
read_milkyway(2)
create_scenario(2)
current_scenario(2)
all_scenarios(2)
all_active_scenarios(2)

DDC-15 (warning) Ignoring %s attribute %s on %s object(s):
 Attribute type conflicts with existing attributes.

DESCRIPTION

An attribute contained in the DDC file conflicts in type with with an attribute that is already registered with the tool. The conflicting attribute is ignored by the DDC reader.

An attribute saved in a DDC file must have the same type as an existing attribute of the same name on the same netlist object class (e.g., string attribute on design objects).

This message is most likely seen when reading in DDC files written by the X-2005.09 release or earlier. Attribute conflicts from more-recent files are silently discarded.

WHAT NEXT

This message could appear if there happens to be a user-defined attribute that has the same name (but different type) as a built-in attribute that was added in a later

version of the tool. It is good practice to use a prefix for user-defined attributes, such as your company's name, that is unlikely to be used by Synopsys in the future.

SEE ALSO

```
set_attribute(2)
report_attribute(2)
```

DDC-16 (error) ddc file contains no scenario-specific data. Cannot specify
 -scenarios option for this file.

DESCRIPTION

The *-scenarios* option to the **read_file** command can only be used to read files that contain scenario-specific constraint data.

WHAT NEXT

See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

```
read_file(2)
read_ddc(2)
```

DDC-17 (error) ddc file contains no data for any of the requested scenarios

DESCRIPTION

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-scenarios* option to the **read_file** command.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

DDC-18 (error) DDC file contains no data for any of the requested active scenarios

DESCRIPTION

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-active_scenarios* option to the **read_file** command.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-active_scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

read_file(2)
read_ddc(2)

DDC-19 (warning) ddc file contains no data for the following requested scenarios:
 %s

DESCRIPTION

The specified ddc file does not contain any constraint data for one or more of the scenarios specified to the *-scenarios* option to the **read_file** command. The file will be read and the list of scenarios to be read in will be restricted according to the remaining scenarios specified to the *-scenarios* option.

WHAT NEXT

Check the list of scenario names supplied to the **read_file** *-scenarios* option. See **read_file**(2) for more information on controlling which scenarios' constraints are read from the ddc file.

SEE ALSO

```
read_file(2)
read_ddc(2)
```

DEL-001 (error) You cannot mix an LCD operating conditon with a non LCD operating condition.

DESCRIPTION

A operating condition is detected to be an LCD operating condition, while another specified operating condition is not an LCD operating condition. The ability to specify two different types of operating conditions is not supported.

WHAT NEXT

Supply a consistent min and max operating conditions. Either two non-LCD operating conditions or two LCD operating conditions.

DEL-002 (error) You cannot specify a single LCD operating conditon.

DESCRIPTION

LCD operating conditions can be specified in min-max mode only.

WHAT NEXT

You need to use the min-max mode with LCD operating conditions.

DEL-003 (warning) Library '%s' has time unit of %gns but the main library unit is %gns

DESCRIPTION

If multiple libraries are used in analysis, they must have the same units. This restriction will be removed in a future version of PrimeTime.

WHAT NEXT

Convert the units in the .lib and regenerate a library .db file using Library Compiler if possible.

DEL-004 (warning) Library '%s' has capacitive_load unit of %gpF
but the main library unit is %gpF

DESCRIPTION

```
If multiple libraries are used in analysis, they must have the same units. This
restriction will be removed in a future version of PrimeTime.
```

WHAT NEXT

```
Convert the units in the .lib and regenerate a library .db file using Library
Compiler if possible.
```

DEL-005 (error) Cannot remove operating_condition from cell '%s': Power rails inherited from '%s' would not match rails of cell '%s'.

DESCRIPTION

```
Removing rail voltages or an operating condition from a hierarchical cell, may cause
a lower level leaf cell to inherit a new set of power rails from a higher level
hierarchical cell. Such a removal is disallowed unless the power rails in the
library of the leaf cell are a subset of the newly inherited rails.
```

WHAT NEXT

```
Ensure that appropriate rail voltages/ operating conditions have been previously set
on such leaf cells.
```

DEL-006 (warning) The operating condition does not define all rails
of cell '%s'.

DESCRIPTION

```
The operating condition or rail voltage does not contain all power rails therefore
default voltages will be used on the remaining power rails. The default voltages are
defined in power_supply section of the .lib.
```

WHAT NEXT

Ensure that the power rails specified in the library of the cell are same as (or a subset of) the rails in the operating condition.

DEL-007 (warning) Setting of multi-rail operating condition or rail voltage on hierarchical cell '%s' may result in incomplete assignment of power rails.

DESCRIPTION

Assignment of voltages to power rails on multi-rail cells is based on matching rail names in the operating conditions and power_supply definition in library description of the cell.

When setting operating condition or rail voltages on hierarchical cell this information is inherited by all cells in the hierarchy unless they have their explicit operating condition or rail voltage. Since rails in two different libraries can have same name then the effect of setting operating condition or rail voltage with multiple rails on hierarchical cell may result in unintended or incomplete voltage assignment.

WHAT NEXT

Set an operating condition or rail voltages on any lower level cells that require different power rail voltages.

DEL-008 (warning) Default %s operating conditions per library resulted in
 cells having different temperature, e.g.,
 %s has %g but
 %s has %g.

DESCRIPTION

This warning message tells you that default operating conditions assigned to cells may not represent actual operating environment because temperature is not same for all cells in the design.

This message is displayed during update_timing.

WHAT NEXT

If the temperature difference is intentional and you are trying to model temperature variation on the chip then no action is required. If not intentional then use set_operating_conditions to explicitly set operating conditions on the design or individual blocks.

SEE ALSO

set_operating_conditions (2). **report_cell** (2). **default_oc_per_lib** (3).

DEL-009 (error) Cannot set single rail voltage on multirail cell '%s'.

DESCRIPTION

You may not set a single rail voltage on a cell using set_rail_voltage -rail_rvalue if that cell has multiple power rails defined in the library.

WHAT NEXT

Use set_rail_voltage -rail_list.

DEL-010 (Error) Unable to parse input/output_voltage in lib '%s': ('%s' = '%s').

DESCRIPTION

When parsing the input_voltage or output_voltage attribute of a library, PrimeTime has encountered a string that it cannot parse. Note that PrimeTime can only parst binary expressions for input/output_voltage.

WHAT NEXT

Ensure that the input/output_voltage attributes of you library contain only binary expressions.

DEL-011 (information) The most constraining rise and fall values of the '%s'

constraint arc occur for different input conditions.

DESCRIPTION

Due to non-monotonicity in arc data, the most constraining rise and fall delay
values arise from different computation input parameters. In most libraries,
constraint arcs are characterized with respect to the transition time at the clock
or reference pin as well as the transition time at the data or related pin. In min-
max analysis modes, the arc delay can be computed in two libraries, with min and max
values on the input transitions. Specifically, in on-chip-variation (OCV) mode, up
to eight calculations may be necessary to identify the most constraining value of
the arc delay.

Given that the delay is a potential permutation of various input parameters, it is
possible that the most constraining, or maximum, rise and fall delays arise from
different permutations of the input parameters. This scenario has occurred for the
specific constraint arc delay being reported.

WHAT NEXT

This is an advisory message as no further action is necessary.

DEL-012 (error) The desired operating-condition or rail-voltage or temperature for cell '%s' is outside the domain covered by the applicable scaling library group.

DESCRIPTION

You may not set an operating-condition or rail-voltage or temperature that goes
outside the domain covered by an applicable scaling library group. If the
define_scaling_lib_group command was used to setup a group of libraries that
includes the specified cell, any operating-condition or rail-voltage set on the cell
must be within the process, voltage, and temperature domain covered by the group.

WHAT NEXT

Correct either the operating condition or the scaling library group.

SEE ALSO

define_scaling_lib_group (2), **create_operating_conditions** (2),
set_operating_conditions (2), **set_rail_voltage** (2). **set_temperature** (2).

DEL-013 (information) Assuming the default level shifter strategy '%s'

DESCRIPTION

The commands without any arguments resets the level shifter strategy to the default 'all'. Default strategy is to reports all driver and load signal signal level mismatches.

WHAT NEXT

To set a specific startegy use **set_level_shifter_strategy -rule <strategy>**.

SEE ALSO

set_level_shifter_strategy (2), **check_timing** (2), **set_level_shifter_threshold** (2).

DEL-014 (information) The operating conditions set are outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation is being done.

DESCRIPTION

If you set an operating-condition that goes outside the domain covered by an applicable scaling library group, extrapolation will be done for the given operating condition it the scaling libraries are defined for atleast two different operating conditions. If the define_scaling_lib_group command was used to setup a group of libraries that includes the specified cell, any operating-condition or rail-voltage set on the cell must be within the process, voltage, and temperature domain covered by the group to avoid any extrapolation.

WHAT NEXT

Correct either the operating condition or the scaling library group if extrapolation is not desirable.

SEE ALSO

define_scaling_lib_group (2), **create_operating_conditions** (2), **set_operating_conditions** (2),

DEL-015 (warning) The operating conditions set are far outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation far beyond the safe range is being done.

DESCRIPTION

```
If you set an operating-condition that is outside the domain covered by an
applicable scaling library group, extrapolation will be done for the given operating
condition if the scaling libraries are defined for atleast two different operating
conditions. If the define_scaling_lib_group command was used to setup a group of
libraries that includes the specified cell, any operating-condition set on the cell
must be within the process, voltage, and temperature domain covered by the group to
avoid any extrapolation. The accuracy of results may not be good if the operating
conditions are set far outside the domain of the scaling group.
```

WHAT NEXT

```
Correct either the operating condition or the scaling library group if extrapolation
is not desirable.
```

SEE ALSO

```
define_scaling_lib_group (2), create_operating_conditions (2),
set_operating_conditions (2),
```

DEL-016 (information) PrimeTime did not compute a valid '%s' transition at input;
  report_delay_calculation will use zero instead.

DESCRIPTION

```
Transition times at the output of disabled arcs or non-driven transitions of half
unate arcs are considered invalid and are propagated as such in PrimeTime so as not
to merge with valid signal transitions downstream. For the purposes of delay
calculation, a zero slew is used to perform the cell arc calculation. Even though
using a zero input slew could result in a corresponding non-zero output slew, this
output slew is in turn marked invalid.
```

WHAT NEXT

```
This is an advisory message as no further action is necessary.
```

DEL-017 (information) The minimum values of the '%s' constraint arc
are not used by timing analysis.

DESCRIPTION

For the evaluating the worst possible conditions for a timing violation and given
that timing constraint senses implicitly encode minimum versus maximum conditions
such as hold and setup, PrimeTime strictly uses the maximum computed constraint arc
delay values for computing endpoint slack.

PrimeTime computes and preserves the minimum delay values for constraint arcs for
two reasons. First, these minimum values are exported through attributes off the
timing_arc object for general use. Second, other applications dependent on PrimeTime
delay calculation through SDF generation do require minimum values to be present.

WHAT NEXT

This is an advisory message as no further action is necessary.

DES-001 (error) Current design is not defined.

DESCRIPTION

```
The current design is not defined. Many commands require that the current design is
set.
```

WHAT NEXT

```
You must read a design database file and link a design.
```

DES-002 (error) Cannot find %s '%s' in design '%s'

DESCRIPTION

```
The specified object cannot be found in the given design. This is sometimes seen
while reading SDF and parasitics files. In those cases, it could indicate a file
which is out of sync with the design.
```

WHAT NEXT

```
If reading SDF or parasitics, verify that the file matches the design.
```

DES-003 (error) '%s' cannot be used on %s %s '%s'.

DESCRIPTION

```
Certain commands are valid only for input or output objects.
```

WHAT NEXT

```
Enter the command with a valid list of objects.
```

DES-004 (error) Cannot find design '%s'.

DESCRIPTION

There is no design with that name is in memory.

WHAT NEXT

Read in the design or reenter the command with a different name.

DES-005 (error) Cannot set current instance to leaf cell '%s'.

DESCRIPTION

The current instance must be a hierarchical cell.

WHAT NEXT

DES-006 (error) Cannot find pin '%s' on cell '%s'.

DESCRIPTION

The pin does not exist on the specified cell.

WHAT NEXT

Use **query_objects [select_pin -of_object [select_cell *cell_name*]]** to list pin names on the cell.

DES-007 (warning) '%s' is not a valid object type.

DESCRIPTION

When -from or -to option is used with set_disable_timing or remove_disable_timing , the object list can only be a cell or a lib cell. This warning is generated for objects of type port and pin.

Don't use -from or -to option to disable pins or ports.

DES-008 (error) Cannot find %s '%s' in library '%s'.

DESCRIPTION

The specified object cannot be found in the given library.

WHAT NEXT

Enter the command again with a valid object name.

DES-009 (error) Cannot find pin '%s' on library cell '%s'.

DESCRIPTION

The pin does not exist on the specified library cell.

WHAT NEXT

Enter the command again with a valid object name.

DES-010 (error) Cannot find %s '%s'.

DESCRIPTION

The specified object cannot be found.

WHAT NEXT

Enter the command again with a valid object name.

DES-011 (error) Cell '%s' is not hierarchical.

DESCRIPTION

```
The command only works on hierarchical cells.
```

WHAT NEXT

```
Enter the command again with a hierarchical cell.
```

DES-012 (error) Cannot use '%s' command on %s '%s'.

DESCRIPTION

```
The command works only on ports of a specific direction.
```

WHAT NEXT

DES-013 (error) Current design is not in min-max mode.

DESCRIPTION

```
Most of the -min and -max options of commands work only when the design is in min-
max mode. The design is considered in min-max mode when 2 operating conditions are
specified, such as "set_operating_condition -min OCbest -max OCworst". The design
can also be in min-max mode after reading an SDF file with the -min_max option (for
example, read_sdf -min_max mydesign.sdf).
```

WHAT NEXT

DES-014 (error) Object '%s' is not in the current design.

DESCRIPTION

```
You attempted an operation on an object that is outside of the scope of current
design. For example, if you select a cell from one design, and attempt to set the
current instance to that cell in a different (current) design, this error is
generated.
```

DES-015 (error) Cannot use '%s' command on %s '%s' because it is a limited design.

DESCRIPTION

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but some cannot.

WHAT NEXT

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-016 (error) Cannot use '%s' command on %s '%s' because it contains instances of limited designs%s.

DESCRIPTION

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but others cannot.

WHAT NEXT

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-017 (information) Could not auto-link design '%s'.

DESCRIPTION

You executed a command that tried to link the current design. The design could not be linked or it already failed to link. The design now has unresolved references.

WHAT NEXT

Determine the reason for the unresolved references. This might require changing the value of the search_path or link_path variables. If these references are not yet defined, you can make the linker create black-boxes for them by setting the variable link_create_black_boxes to true. Finally, relink the design using the **link_design** command.

DES-018 (error) There is already an operating condition named '%s' in library '%s'.

DESCRIPTION

The **create_operating_condition** command cannot overwrite an existing operating condition.

WHAT NEXT

Choose a new name for the operating condition. To list the existing operating conditions in the specified library, use **report_lib**.

DES-019 (warning) Library '%s' has been generated with an old version
 of the Library Compiler. It needs to be rebuilt to support case analysis on sequential cells.

DESCRIPTION

You receive this message if the current library DB is out of date. The library DBs have detailed functional information generated by Library Compiler from the library .lib file. Information generated by Library Compiler prior to version 2000.11 is not supported.

WHAT NEXT

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

        dc_shell> **read_lib mylibrary.lib**

2. Write out the .db file.

```
dc_shell> write mylibrary.db
```

DES-020 (warning) No operating condition is specified, assuming a voltage value of %s volts for RC delay calculation.

DESCRIPTION

```
No operating condition is specified for the current library, so PrimeTime does not
know what is the voltage value when performing RC delay calculation
```

WHAT NEXT

```
Specify the operating condition of the current library with set_operating_condition.
To get a list of the operating conditions of your library, use report_library.
```

```
pt_shell> report_library my_lib.db
```

```
   Name                Process   Temp       Voltage    Tree Type
   -------------------------------------------------------------------------
   WCCOM               3.00      115.00     3.00       balanced_case
```

```
pt_shell> set_operating_condition WCCOM
```

DES-021 (warning) These environment variables need to be set for accurate RC delay calculation:
 Variable name Default
 ----
 rc_slew_lower_threshold_pct_rise 20
 rc_slew_lower_threshold_pct_fall 20
 rc_slew_upper_threshold_pct_rise 80
 rc_slew_upper_threshold_pct_fall 80
 rc_input_threshold_pct_rise 50
 rc_input_threshold_pct_fall 50
 rc_output_threshold_pct_rise 50
 rc_output_threshold_pct_fall 50
 rc_slew_derate_from_library 1

DESCRIPTION

When parasitics are annotated on a design, timing calculations use these variables
to compute delays and transition times. The values can be set by either a cell
library or equivalent shell variables. If one of these approaches does not set all
of the values, this warning message is issued to alert the user. If both approaches
set the values, the shell variables take precidence.

WHAT NEXT

Either set all of the above values in a cell library or set them all with shell
variables. See the man page for each variable for more info.

DES-022 (warning) Some of the following settings have an incorrect value less than or equal to 1, or they are equal to 100. The proper range for these values is exclusively between 1 and 100. Here are the fallback values that will be used:

Setting Fallback

----

rc_slew_lower_threshold_pct_rise %d
rc_slew_lower_threshold_pct_fall %d
rc_slew_upper_threshold_pct_rise %d
rc_slew_upper_threshold_pct_fall %d
rc_input_threshold_pct_rise %d
rc_input_threshold_pct_fall %d
rc_output_threshold_pct_rise %d
rc_output_threshold_pct_fall %d

DESCRIPTION

These values are used by delay-calculation with annotated parasitics. They should be
set by libraries, but if not, shell variables with the same names can be set to
provide the values. In either case, the values represent percentages, not decimal
fractions. If a value less than or equal to 1 is encountered, it will be interpreted

as a decimal fraction and this warning will be issued.

If a zero value is encountered, it will be changed to 5%; if 1 or 100 value is encountered, it will be changed to 95%. We suggest the user to set the delay and slew trip point thresholds in the library directly, and suggest the user to keep them in the range of 10 to 90.

Please note that this warning message is only shown for either the main library (i.e. first in link_path) or the shell variables.

WHAT NEXT

Set a percentage value between 1 and 100 (exclusive) to specify the characterization thresholds of the Synopsys library.

SEE ALSO

lib_thresholds_per_lib (3), **rc_input_threshold_pct_fall** (3),
rc_input_threshold_pct_rise (3), **rc_output_threshold_pct_fall** (3),
rc_output_threshold_pct_rise (3), **rc_slew_lower_threshold_pct_fall** (3),
rc_slew_lower_threshold_pct_rise (3), **rc_slew_upper_threshold_pct_fall** (3),
rc_slew_upper_threshold_pct_rise (3).

DES-023 (warning) Net '%s' is multi-driven.

DESCRIPTION

The specified net is multi-driven by non-three-state cells. PrimeTime will try to peform multi-driven delay calculation for all switching scenarios defined by the networks attached to the drivers' from-pins. In order for such scenarios to be valid, a given from-net must uniquely cover all of the strong drivers attached to the multi-driven to-net.

If a from-net does not cover all of the strong drivers, or if a from-net is attached to more than one pin on a specific driver, detailed RC delay calculation cannot be performed. Instead, fractional lumped analysis will be used; the load will be assumed to be the total capacitance of the multi-driven net divided by the number of drivers.

WHAT NEXT

Verify that you indeed want the indicated net to be multi-driven. This capability is commonly used to wire cells in parallel to achieve greater drive strength.

SEE ALSO

RC-002 (n), **RC-003** (n).

DES-024 (warning) Net '%s' has an incomplete RC network.

DESCRIPTION

The specified net has an imcomplete RC network. This means that some RC elements are
dangling, or that all drivers and loads of the nets are not connected by all the RC
elements.

WHAT NEXT

The RC network annotation is ignored for the specified net.

DES-025 (error) Pin '%s' is not connected to
net '%s'.
Ignoring annotation on net '%s'.

DESCRIPTION

You receive this message if the **read_parasitics** command has found the specified pin
in the parasitics file but not in the design file; therefore, **read_parasitics** cannot
annotate the associated net. Possible causes for this error could include spelling
errors or typos, or writing the parasitics file and the design file from different
versions of the design.

WHAT NEXT

Verify that the specified pin is connected to the specified net in both the
parasitics file and the design file, and that both are spelled correctly. Regenerate
the files if necessary, then reexecute **read_parasitics**.

SEE ALSO

read_parasitics (2).

DES-026 (error) %s pin '%s' is not connected to the RC network
of

net '%s'. Ignoring the incomplete RC network of the net.

DESCRIPTION

You receive this message if **report_annotated_parasitics** detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network on the specified net is being ignored, because it is incomplete; the specified pin is not physically connected to the RC network.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

WHAT NEXT

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature **read_parasitics -complete_with** or **complete_net_parasitics**. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute **read_parasitics**.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

SEE ALSO

complete_net_parasitics (2), **read_parasitics** (2), **report_annotated_parasitics** (2).

DES-027 (warning) net '%s' has too many (%d) RC elements. Lumped capacitance is used.

DESCRIPTION

The specified net has too many RC elements (more than 10,000). RC delay calculation using AWE technique cannot handle such large RC networks.

WHAT NEXT

The very large RC network of the net needs to be reduced to a smaller number of RC elements to be handled by PrimeTime.

DES-028 (info) Derived library resistance unit is %f Kohm (Time unit is %.f ns, and Capacitance unit is %f pF).

DESCRIPTION

```
The library resistance unit is implicit in the synopsys library, it is derived from
the library time and capacitance units which are explicit.
```

WHAT NEXT

DES-029 (error) Library '%s' has no voltage rails defined.

DESCRIPTION

```
An attempt was made to define rail voltages to a library which does not have defined
rail voltages. It is usually because the library is not a DPCM library, or that the
DPCM library does not have pre-defined rail voltages.
```

WHAT NEXT

DES-030 (error) cannot find rail voltage '%s' in library '%s'.

DESCRIPTION

```
The specified rail voltage is not declared in the DPCM library. It may be because of
a typo.
```

WHAT NEXT

```
Report the specified rail voltage names specified in the DPCM library by executing
command report_lib for the specified library. report_lib reports all specified rail
voltage names declared in DPCM.
```

DES-031 (error) Upper threshold must be greater than lower threshold for variables rc_slew_lower_threshold_pct_* and

rc_slew_upper_threshold_pct_*.

DESCRIPTION

The variable rc_slew_upper_threshold_pct_rise must be strictly greater than rc_slew_lower_threshold_pct_rise. Similarly, variables rc_slew_upper_threshold_pct_fall must be strictly greater than rc_slew_lower_threshold_pct_fall.

WHAT NEXT

Set variables rc_slew_lower_threshold_pct_rise, rc_slew_upper_threshold_pct_rise, rc_slew_lower_threshold_pct_fall, rc_slew_upper_threshold_pct_fall.

DES-032 (warning) Failed to compute %s RC net delay from '%s' to '%s'.

DESCRIPTION

The delay calculation failed to compute the delay for the given detailed RC network, hence the lump model will be used for delay calculation.

WHAT NEXT

Simplify the RC network and check if the RC enviorment vairables are set correctly.

DES-033 (warning) Failed to compute C-effective for the following timing arc:
 (%s) %s/%s-->%s (%s %s)

DESCRIPTION

The cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so the total capacitance will be used.

The two most common reasons for this failure are (1) an unrealistically large input transition time or output capacitance has occurred, and/or (2) the RC threshold environment variables are set incorrectly.

Another frequent reason is that library data for the specific sense of timing arc in question is missing or invalid. The timing arc is displayed by the warning message

in the following manner:

```
(<reference-name>) <instance-name>/<from-pin>--><to-pin> (<sense-name>)
```

The sense name has two parts: a rising/falling direction on the to-pin and a sense description.

WHAT NEXT

You may have to annotate transition times with **set_annotated_transition** to circumvent unrealistic loading conditions (e.g. like those which you might later solve with buffer trees). Also, be sure the RC threshold environment variables are set correctly, and that valid library data exists for the desired sense of timing arc through the cell of interest.

SEE ALSO

set_annotated_transition (2), **rc_slew_lower_threshold_pct_rise** (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3).

DES-034 (warning) subckt '%s' defined multiple times.

DESCRIPTION

The SPICE deck and all its include files that define the pin order for the SPICE output of the critical has define a sub-circuit multiple times.

DES-035 (error) out of memory at file %s line %d.

DESCRIPTION

Run out of memory during SPICE pin order deck parsing.

DES-036 (warning) pin '%s defined multiple times in subckt '%s'.

DESCRIPTION

A pin is defined multiple time on the SPICE subckt header. Only the first one is used.

DES-037 (warning) No SPICE pin order info for cell '%s' (%s).

DESCRIPTION

You receive this message if **write_spice_deck** cannot find the specified cell type in the file you specified using the **-sub_circuit_file** option.

WHAT NEXT

Examine the subcircuit file and verify that it contains the subcircuit description of the specified library cell. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-038 (error) Library pin '%s' for cell '%s' is not in the SPICE sub-circuit definition.

DESCRIPTION

You receive this message if **write_spice_deck** finds the specified cell in the file you specified using the **-sub_circuit_file** option, but does not find the specified pin.

WHAT NEXT

Examine the subcircuit file and verify that it contains the specified pin and is consistent with the PrimeTime library. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-039 (warning) SPICE pin '%s' for cell '%s' is not in the library.

DESCRIPTION

You receive this message if **write_spice_deck** finds the specified pin in the subcircuit file but cannot find it in the library. If the pin is a power or ground pin, PrimeTime might still be able to do the analysis.

WHAT NEXT

If the pin is not a power or ground pin, examine the subcircuit file and verify that it is consistent with the PrimeTime library. Make any corrections necessary, then re-execute **write_spice_deck**.

DES-040 (warning) The driver waveform %s is bad and will be ignored.

DESCRIPTION

While reading the driver waveform, the application found that waveform is bad. For example, the number of voltage points in the waveform are less than two.

WHAT NEXT

Examine your waveform is according to the liberty syntax for driver waveforms. Correct the waveform and re-execute it.

DES-050 (error) Too many %ss matched '%s' in design '%s'

DESCRIPTION

While searching for an object by name, the application found multiple objects that match the name. This usually occurs after some flattening of the design, when the hierarchy character becomes embedded in the names. For backannotation, this is an ambiguous situation, because the application cannot determine which object to annotate.

This situation occurs rarely, during the reading of parasitics files, and could be caused by a design error. Multiple objects in the flat space should not have the same name.

WHAT NEXT

Examine your design to determine why multiple objects in the flattened file have the same name. Correct the design, then re-execute the application.

DES-051 (Error) Command requires a linked design but linking is blocked
 because auto_link_disable is TRUE.

DESCRIPTION

You receive this message if you execute a command that requires a linked design, your design is not linked, and the **auto_link_disable** variable is set to true. By default, many PrimeTime commands automatically attempt to link the current design for you (for example, **set_load** invokes the linker if the current design is not

linked). Setting **auto_link_disable** to true disables the default auto-link process.

WHAT NEXT

If you intend for auto linking to be disabled, you must link the design manually before executing any commands that require a linked design. Setting **auto_link_disable** to true is intended to be used in conjunction with a manual link step. For more information, see the manual page for the **auto_link_disable** variable.

Alternatively, if you want to enable auto linking, set the **auto_link_disable** variable to false.

DES-060 (warning) Ignoring retain library timing arc from '%s' to '%s'.

DESCRIPTION

You receive this message if the current library DB is out of date. Retain arcs generated by Library Compiler prior to version 2000.11 are not supported.

WHAT NEXT

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

    dc_shell> **read_lib mylibrary.lib**

2. Write out the .db file.

    dc_shell> **write mylibrary.db**

DES-061 (warning) Found duplicate instantiation of cell '%s' when flattening the hierarchical netlist.

DESCRIPTION

You receive this message while outputting a hierarchical netlist in a flattened manner. When flattening the netlist, two instances are being mapped to same name. For example, you may have a cell by name "a/b" at top level and a cell named "b" inside a hierachy named "a". The name of the cell under conflict is given in this message.

You should uniquify the names of the cells under conflict before doing the current operation.

DES-062 (warning) '%s' unit specified as '%s' does not match with the main library unit '%s%s'.

DESCRIPTION

set_units command can only check the consistency of the specified units with the main library units. Actual setting of units are not allowed.

WHAT NEXT

If the units of sdc scripts are different, change the sdc scripts so that the units are same as the main library units. It is also possible to select a different library as the main library, which has consistent units as that of sdc scripts.

DES-063 (warning) '%s' unit should be specified in '%s'.

DESCRIPTION

.

WHAT NEXT

.

DES-064 (warning) Power unit cannot be checked.

DESCRIPTION

Power unit cannot be checked since no power unit available.

WHAT NEXT

Enable power analysis mode by setting power_enable_analysis to true, and running power related commands, such as update_power, read_vcd, read_saif, set_switching_activity, etc.

DES-065 (warning) '%c' is an unsupported scale.

DESCRIPTION

```
Valid scales are f|p|n|u|m|k|M.
```

WHAT NEXT

```
Scale the value to the supported scale.
```

DES-066 (error) Command requires a linked design but linking is blocked
 because of existing collections.

DESCRIPTION

```
You receive this message if you execute a command that requires a linked design,
your design is not linked, and there are some collections with this design.
```

WHAT NEXT

```
Perform a link first and re-issue the command.
```

DES-067 (error) Design is already linked.

DESCRIPTION

```
You are attempting to link a design that is already fully linked. If you want PT to
relink, please use -force option.
```

WHAT NEXT

```
No need of any action.
```

DES-068 (error) Could not find library cell '%s'.

DESCRIPTION

```
You are attempting to use a library cell in a command and the library cell could not
```

be located in any of the loaded libraries.

WHAT NEXT

Re-issue the command with the correct library cell.

ENV-001 (error) Value for %s cannot be larger than the %s value.

DESCRIPTION

Some commands work in pairs, specifying a max and min value. The min value must be less than the max value. For example, never specify a **min_capacitance** which is larger than the **max_capacitance** for the same design or port.

WHAT NEXT

Remove the old value or use a different value.

ENV-002 (warning) Invalid value '%s' for variable '%s'. %s

DESCRIPTION

You received this message because you specified an invalid value for the specified variable. The message should provide valid values for the variable.

WHAT NEXT

If the message did not provide valid values for the variable, refer to the manual page for the variable. Reset the variable with a valid value, then reexecute the command.

ENV-003 (Information) Using automatic %s wire load selection group '%s'%s.

DESCRIPTION

Automatic wire load selection by area is being performed on the design or on a hierarchical cell. The specified selection group is used to determine which wire load model to apply to hierarchical cells at and below this cell or design, based on their cell area. There might be a different selection group for max and min conditions.

WHAT NEXT

To see which wire load models are set, you can use the **report_wire_load** command.

FLT-002 (information) Errors preprocessing compiled filter.

DESCRIPTION

This is a summary message generated after a filter expression has successfully parsed, but unsuccessfully processed because of an unknown identifier, type mismatch in a relation, or invalid operator in a relation.

WHAT NEXT

Look at previous error messages to determine the problem with the filter expression. Correct the problems, and retry the operation.

FLT-003 (error) while parsing filter expression: %s at '%s'

DESCRIPTION

A filter expression could not be successfully parsed, typically because of a syntax error. The point in the expression that caused the failure is shown along with the remainder of the expression.

WHAT NEXT

Look at the man pages for filter expression syntax, and verify that your expression conforms to the syntax. Ensure that supported relation and logical operators are in use, that the expression is constructed of a series of relations separated by logical operations, etc.

FLT-005 (error) Unknown attribute '%s'.

DESCRIPTION

Filters are evaluated within a context. Given the current context, an attribute which you entered is unknown.

A relation in a filter expression is very simple. For example, "area <= 2.4". In this case, the attribute is "area". If you were applying the filter to a pin collection, since "area" is not a valid pin attribute, this error would occur.

WHAT NEXT

Look at the man pages for the given command, and ascertain the valid values for attributes.

FLT-006 (error) Type mismatch between '%s' and '%s'.

DESCRIPTION

A relation in a your filter expression has an identifier and value with inconsistent types. The following simple rules apply:

Identifier Type mismatch generates:when value is: -------------------------------
------------------ stringn/a - never an error numeric literalstring, true, false
boolean   numeric literal, string

Note some important distictions: the boolean words TRUE and FALSE are interpretted as strings in a string relation, or as boolean in a boolean relation. Simlilarly, the numeric literal 2.4E-9 is interpretted as a string in a string relation, or as a number in a numeric relation.

WHAT NEXT

Re-enter the filter with valid identifier/value relations.

FLT-007 (error) Invalid operator '%s' for '%s' and '%s'.

DESCRIPTION

A relation in a your filter expression has an identifier and value with consistent types but an invalid operator. The following simple rules apply:

Type: Invalid operators: --
----- string   None. All operators ok. numeric literal=~, !~ boolean=~, !~,
<, >, >=, <=

WHAT NEXT

Re-enter the filter with a valid operator for the failed relation.

GEN

GEN-1 (error) Cell '%s' instance '%s' pin '%s' has same Y coordinate as cell '%s' instance '%s' pin '%s'.

DESCRIPTION

Two pins of the same cell, or different cells in the same column, are found to
overlap. This was probably caused by a problem in either the symbol library being
used or in schematic generation. Check the identified pins in your symbol library
source to see if they are pins of the same cell and if the same Y coordinate has
been defined for them. If so, correct the Y coordinates, recompile the symbol
library, and rerun the test. If this is not the case, report this as a bug in
schematic generation.

WHAT NEXT

GEN-2 (error) Pin '%s' on Cell '%s' does not lie on a grid.

DESCRIPTION

WHAT NEXT

GEN-3 (warning) Creating a symbol for cell '%s' of type '%s'.

DESCRIPTION

This warning is issued when the *gen_show_created_symbols* dc_shell variable is set to
"true" and *create_schematic* can not locate the symbol template for a cell in the
database or in any of the symbol libraries. In such a case, *create_schematic*
automatically generates a rectangular symbol template to use in the schematic. In
general, this is done by putting all the input pins on the left side of the symbol
and all other pins on the right side. The size of the generated symbol can be
controlled by setting the *gen_max_ports_on_symbol_side* variable to an appropriate
value.

WHAT NEXT

If this warning is issued for primitive gates, that may indicate that the
symbol_library or *search_path* variables have not been set properly. This can be
resolved by (1) finding the symbol library (a file with a .sdb suffix) to be used

and appending it to the *symbol_library* variable, and (2) appending its directory path to the *search_path* variable.

Libraries usually don't have symbol templates for hierarchical cells, so this warning should be ignored for such cells.

GEN-4 (error) Could not find pin: '%s', in cell: '%s' in schematic library '%s'.

DESCRIPTION

WHAT NEXT

GEN-5 (error) Symbol library doesn't have off-sheet connectors.

DESCRIPTION

WHAT NEXT

GEN-6 (warning) Symbol exceeds sheet size.

DESCRIPTION

This warning is issued when one of the symbol templates *create_schematic* creates exceeds the size of the sheet being used. This may be caused by either the sheet being too small or there being too many pins on the symbol.

This message is only issued for symbols that have so many pins that *create_schematic* creates a smaller square symbol with all the pins equally distributed along the four sides, and even then this symbol exceeds the sheet size.

WHAT NEXT

If this is of concern, use a larger sheet size. Since *create_schematic* will automatically create the smallest symbol possible for the given number of ports when this message is issued, the only way to make the symbol fit the sheet is to use a larger sheet.

GEN-7 (warning) Maximum ports on symbol side limit of '%d'

exceeded.

DESCRIPTION

WHAT NEXT

GEN-8 (warning) Can't rename off-sheet connector of net '%s' to the name of its port '%s' because net '%s' already exists.

DESCRIPTION

WHAT NEXT

GEN-10 (warning) Couldn't find all the port symbols in the generic symbol library.

DESCRIPTION

WHAT NEXT

GEN-11 (error) Couldn't find pin name '%s' in ripper symbol '%s'.

DESCRIPTION

WHAT NEXT

GEN-12 (error) Couldn't find a ripper symbol for creating a

bussed schematic.

DESCRIPTION

WHAT NEXT

GEN-13 (error) Annotator '%s' has an invalid format specification '%s'.

DESCRIPTION

WHAT NEXT

GEN-14 (error) An unnamed annotator has an invalid format specification '%s'.

DESCRIPTION

WHAT NEXT

GEN-15 (error) Annotator '%s' has more than %d '%%s' specifications
 in the format string.

DESCRIPTION

WHAT NEXT

GEN-16 (error) An unnamed annotator has more than %d '%%s'

specifications in the format string.

DESCRIPTION

WHAT NEXT

GEN-17 (error) Annotator '%s' has an invalid expression '%s'.

DESCRIPTION

WHAT NEXT

GEN-18 (error) An unnamed annotator has an invalid expression '%s'.

DESCRIPTION

WHAT NEXT

GEN-19 (warning) The symbol for cell '%s' has a pin off the route grid.
 You may be mixing symbol libraries with different route grids.

DESCRIPTION

```
This warning is issued when one of the schematic symbols is found to have a pin that
is located outside the route grid being used by create_schematic, i.e., the pin is
somewhere in the middle of the square region defined by the four points around it
that represent the intersection of vertical and horizontal grids instead of being on
one of the edges or corners. This indicates that the schematic may contain symbols
from more than one symbol library and that these libraries specify different route
grids. In such a case, create_schematic picks up the route grid specified in the
first symbol library it runs into, and uses that route grid in the schematic. Any
symbols coming from libraries whose route grids do not match the one being used by
create_schematic are not guaranteed to have their pins aligned with the route grid.
```

WHAT NEXT

If this is a problem in transferring the schematic to some external environment, try using symbol libraries with the same route grid. If this is not possible, try modifying the route grids in your symbol libraries to match each other. This is done by editing the .slib file and changing the argument to the *set_route_grid()* specification and then recompiling that library with the *read_lib* command.

GEN-20 (error) One of the pins or port busses is corrupted.

DESCRIPTION

This error is issued when one of the design ports or pins is found to have a corrupt bus structure. This can happen sometimes because of inconsistent bus creation by different tools in the design. In such a case, the port or pin that is found to have a corrupt bus structure will be drawn unbussed in the schematic, i.e. its bus will be ignored by *create_schematic*.

WHAT NEXT

If there are no other problems with the tool run, this message should be ignored as *create_schematic* automatically ignores the bus objects responsible for corruption.

GEN-21 (error) Cell %s's pin %s is on wrong side.

DESCRIPTION

WHAT NEXT

GEN-22 (error) Net %s connects pins of different widths.

DESCRIPTION

WHAT NEXT

GEN-23 (warning) The netlist contains bus-to-bus connections. Any
 nets involved in inter-bus connections will be

displayed as disconnected in the no-ripper schematic.

DESCRIPTION

WHAT NEXT

GEN-24 (error) Could not find the type mapper symbol in the generic symbol library. The generic symbol library is probably old - Please use a new library and recreate the schematic.

DESCRIPTION

GEN-25 (warning) All cells are power/ground or have no connection.

DESCRIPTION

```
Cells in the current design are all power cells or all ground cells. Or the cells
have no pins.
```

WHAT NEXT

GEN-26 (error) member '%d not found in bus '%s' . Only following members present : '%s'. The design is corrupted.

DESCRIPTION

WHAT NEXT

GEN-27 (warning) Creating a very large schematic. It is approximately %d wide and %d tall.

Must skip the 'improve' algorithm due to insufficient memory.

DESCRIPTION

You receive this warning when you are trying to create a schematic for a very large
design, but there is not sufficient memory available to perform the "improve"
algorithm.

WHAT NEXT

You have available three courses of action:

• You can let the schematic creation continue, with the possibility that it will
succeed, if there is enough memory.

• You can monitor the performance, using a UNIX utility such as **top**, to see if you
are close to running out of address space.

• You can send an interrupt to the application, which terminates the schematic
creation at the next check point in the algorithm.

Because large schematics are difficult to work with graphically, consider whether
you really want your schematic to be so large. If you have flattened your design,
going back to an unflattened design might be more workable and require less address
space.

If it is imperative that you produce the schematic, rerun your application using the
64-bit version (if it is available to you), which has a memory address space limit
exceeding 4 gigabytes. The process should eventually succeed, providing you have
enough swap space on your machine.

SEE ALSO

create_schematic (2).

GEN-28 (warning) Creating a schematic with an extreme number of sheets.
 The schematic being created has %d sheets.
 Aborting attempt to create schematic.

DESCRIPTION

You receive this warning because you are trying to create a schematic that has too

many sheets, making it impractical to use. The process is terminated.

WHAT NEXT

You can avoid the issue by choosing a larger sheet size, which will result in fewer sheets: -size A is the smallest sheet size, -size B is larger, and so on, up to -size infinite, which is always just one sheet. For more information about sheet sizes, see the man page for the **create_schematic** command.

SEE ALSO

create_schematic (2).

ILM-001 (error) The interface logic on the current design '%s' has not been identified.

DESCRIPTION

You receive this error message because you have not performed the step to identify interface logic on the current design.

WHAT NEXT

Execute the **identify_interface_logic** command on the current design to set the attribute **is_interface_logic_pin** on pins that are part of the interface logic of the current design.

SEE ALSO

identify_interface_logic (2).

ILM-002 (warning) No object has been identified as belonging to the interface logic on the current design '%s'.

DESCRIPTION

You receive this warning message because you have attempted to identify interface logic on the current design. However, no pin has the attribute **is_interface_logic_pin** set to true.

WHAT NEXT

Verify that the value given to the **-ignore_ports** option when calling the **identify_interface_logic** command does not include all the input and output ports on the design.

SEE ALSO

identify_interface_logic (2).

ILM-003 (warning) Update_timing has already been performed

on the current design
'%s'. The interface logic identified will be a function of the
assertions applied on the design.

DESCRIPTION

You receive this message if you issue the **identify_interface_logic** command after
either executing **update_timing** on the specified design, or issuing commands that
caused **update_timing** to be executed. The recommended procedure is to execute
identify_interface_logic before **update_timing**, so that the interface logic is
independent of the assertions (**set_disable_timing**, **set_case_analysis**) defined on the
design. Thus, you can change **set_disable_timing** and **set_case_analysis** statements
without having to regenerate the interface model for the design.

This message warns you that, because update timing has already been performed, the
interface logic identified is a function of the assertions applied on the design. In
this case, timing arcs on the design could be disabled by the **set_disable_timing** and
set_case_analysis commands, so that logic in the fanout/fanin of the disabled timing
arcs would not be part of the interface logic on the current design.

WHAT NEXT

If it is acceptable to you that the interface logic of the current design is a
function of the assertions applied on the design, no action is required on your
part. Otherwise, execute the **identify_interface_logic** command before executing
update_timing on the current design.

ILM-004 (warning) No clocks have been defined on the current design
'%s'. All clocks must be defined prior to identifying
interface logic or extracting model.

DESCRIPTION

You receive this message if you issue the **identify_interface_logic** or **extract_model**
command and have not defined any clocks for the current design. You must define all
clocks in a design before executing the **identify_interface_logic** command. This
message warns you that errors could result in identifying the interface logic on the
current design.

WHAT NEXT

Use the **create_clock** and **create_generated_clock** commands to define all clocks on the
current design. Then reissue the **identify_interface_logic** command.

ILM-005 (warning) A wire-load mode other than "top" is set on the
 current design '%s'. The wire-load mode needs to be set to "top" for
 timing of the ILM to match the timing of the design.

DESCRIPTION

You have not defined a wire-load mode of "top" on the current design. This needs to
be set for the ILM timing to match design timing in a pre-layout design flow. The
reason for this is that ILM's are flattened representations of the original design
and do not preserve design hierarchy.

WHAT NEXT

To not encounter verify errors in a pre-layout design flow when comparing the ILM
against the original design you need to ensure that a wire-load mode of "top" is set
on the original design.

ILM-006 (Information) Port '%s' belongs to the ignore list because it fans
 out to %d%% of the registers on the design.

DESCRIPTION

You receive this message if you execute the **identify_interface_logic** command with
the **-auto_ignore** option, and the fanout of the specified input port has a larger
percentage of the total number of registers than the percentage specified by the
current value of the **ilm_ignore_percentage** variable (default 25). (For example, for
the default value of 25, a port's fanout is ignored if the port fans out to 25% or
more of the total number of registers in the design.) This message informs you that
the specified port's fanout will be ignored.

WHAT NEXT

This is an informational message only; if it is acceptable to you that the specified
port is on the ignore list, no action is required on your part. Otherwise, you can
query the current value of the **ilm_ignore_percentage** variable by executing the
following:

pt_shell **printvar ilm_ignore_percentage**

If you want to set the variable to a higher or lower threshold percentage, execute the following:

pt_shell **set ilm_ignore_percentage** *new_value*

SEE ALSO

identify_interface_logic (2); **ilm_ignore_percentage** (3).

ILM-007 (Warning) -auto_ignore, -context_borrow, -latch_level options do not have any affect while generating a critical pins interface logic model.

DESCRIPTION

You receive this message if you execute the **identify_interface_logic** command with the **-critical_pins** option along with one of **-auto_ignore, -context_borrow or -latch_level** options. These options do not make sense while generating a critical pins interface logic, and will be ignored.

WHAT NEXT

This is a warning message only, no action is required on your part. To get rid of the warning, re-run **identify_interface_logic** without specifying the above options.

SEE ALSO

identify_interface_logic (2);

ILM-008 (Information) The use of -include_all_net_pins option to identify_interface_logic is recommended when you extract a critical pins ILM .

DESCRIPTION

You receive this message if you execute the **identify_interface_logic** command with the **-critical_pins** option (that means you are extracting a critical pins ILM), and did not issue the **-include_all_net_pins** option. This message informs you that the usage of **-include_all_net_pins** option is recommended when extracting a critical pins ILM. There can be certain constraints in the design that do not work properly if you do not give the **-include_all_net_pins** option.

WHAT NEXT

This is an informational message only; if you know that this option does not affect your design, you can ignore this message. Otherwise, redo the **identify_interface_logic** command by giving the **-include_all_net_pins** option.

SEE ALSO

identify_interface_logic (2);

ILM-009 (Warning) There are some input/output delays defined with respect to an internal clock '%s'.

DESCRIPTION

You receive this message if the **write_ilm_script** command encounters input/output delays defined with respect to an internal (non-ilm) clock. The clock is deleted because none of the sources of the clock are ILOGIC pins.

WHAT NEXT

Try to fix the input/output delays generated in the script to take care of this problem. Alternatively, rewrite your original delays with respect to ILM clocks.

SEE ALSO

write_ilm_script (2);

ILM-010 (Error) -ignore_boundary_pins can only be used with -instances option.

DESCRIPTION

You receive this message if the create_ilm command is invoked with -ignore_boundary_pins option without using the -instances option. The -ignore_boundary_pins can be used to ignore the input boundary pins of an instance when an instance ILM is being extracted.

WHAT NEXT

If you want to extract instance ILM, use the -instances option. Otherwise, drop the -ignore_boundary_pins option.

ILM-011 (Information) Context for block '%s' has been created in directory %s.

DESCRIPTION

You receive this message to inform you that the create_si_context command has
created a context for the block in the specified directory.

WHAT NEXT

No action required.

SEE ALSO

`create_si_context` (2);

ILM-012 (Information) ILM for block/design '%s' has been created in directory %s.

DESCRIPTION

You receive this message to inform you that the create_ilm command has created an
ILM for the block/design in the specified directory.

WHAT NEXT

No action required.

SEE ALSO

`create_si_context` (2);

ILM-013 (Error) Option -instances must be used along with -

top_inst.

DESCRIPTION

You receive this message if you call create_si_context command with -top_inst
argument without specifying the -instances option.

WHAT NEXT

Provide the -instances option

SEE ALSO

create_si_context (2);

ILM-014 (Error) No valid instance is found with name '%s'.

DESCRIPTION

You receive this message if the -instances or -top_inst option is used with wrong
instance name argument. Either there is no instance with the given name or it refers
to a black-box.

WHAT NEXT

Check the instance name and reissue the command with correct instance names.

SEE ALSO

create_ilm (2); **create_si_context** (2);

ILM-015 (Error) The parent hierarchy of instance '%s' is not '%s'.

DESCRIPTION

You receive this message if the create_ilm command is issued with inconsitent values
to the -top_inst and -instances option. The top instance specified must be the
parent hierarchy for all the instances specified via -instances option.

WHAT NEXT

Check the instance names and reissue the command with correct instance names.

ILM-016 (Error) The xtalk_pins option cannot be used for criical pins ILM.

DESCRIPTION

You receive this message if the create_ilm command is issued with -critical_pins and
-include {xtalk_pins} options. The xtalk_pins option is not currently supported for
critical pins ILM.

WHAT NEXT

Remove the xtalk_pins option and re-run.

SEE ALSO

`create_ilm` (2);

ILM-017 (error) value '%s' for option '-include' is not valid. Specify one of:
 si_delay_pins, si_noise_pins, net_pins, boundary_cells

DESCRIPTION

You receive this message if the create_ilm command is issued with -include option
and the value provided to -include is not valid.

WHAT NEXT

Rerun the command with one of the specified values for -include option.

SEE ALSO

`create_ilm` (2);

ILM-018 (warning) For the values of '-include' option,

'xtalk_pins' is
 renamed as 'si_delay_pins' and 'noise_pins' is renamed as 'si_noise_pins'.
 The old names will work for now but will be obsoleted in future.

DESCRIPTION

You receive this message if the create_ilm command is issued with -include option
and the value provided to -include is either xtalk_pins or noise_pins.

WHAT NEXT

Update your script to replace 'xtalk_pins' with 'si_delay_pins' and 'noise_pins'
with 'si_noise_pins'.

SEE ALSO

create_ilm (2);

ILM-019 (Information) Could not find pin '%s' to write annotation.

DESCRIPTION

You receive this message to inform you that the write_arrival_annotations command
could not find the specified pin in the design. No annotations are written out for
this pin.

WHAT NEXT

No action required.

SEE ALSO

write_arrival_annotations (2);

ILM-020 (warning) Parasitics on port net %s can not be

maintained.

DESCRIPTION

```
You receive this message to inform you that the create_si_context command cannot
create port parasitics for the given net in the block wrapper being generated.
```

WHAT NEXT

```
No action required.
```

SEE ALSO

create_si_context (2)

ILM-021 (warning) Net connected to port %s is eliminated as aggressor in block wrapper.

DESCRIPTION

```
You receive this message to inform you that the create_si_context command removed
the given port net as an aggressor to nets inside the block for which the wrapper is
being generated.
```

WHAT NEXT

```
No action required.
```

SEE ALSO

create_si_context (2)

INT-1 (fatal) Unknown interrupt signal '%d' encountered.

DESCRIPTION

WHAT NEXT

INT-2 (information) Interrupting current command.

DESCRIPTION

WHAT NEXT

INT-3 (information) One more interrupt will exit process.

DESCRIPTION

WHAT NEXT

INT-4 (information) Process terminated by interrupt.

DESCRIPTION

WHAT NEXT

INT-5 (information) Preparing to interrupt optimization...

DESCRIPTION

This message indicates that a Control-c (SIGINT) was received by the process during the trials phase of compile, and compile is preparing to either print out a menu (interactive mode) or to write a checkpoint file (background mode). Compile must finish the current transform before the menu or checkpoint file can be written. It

may take a few minutes to finish the current transform, so please wait until you see that the checkpoint file has been written before hitting Ctrl-C again.

WHAT NEXT

No action is required on your part. If you want to abort the current compile, hit Control-c twice.

INT-6 (information) Aborting optimization...

DESCRIPTION

This message indicates that two Control-c signals (SIGINT) were received by the process after the Delay Optimization phase of compile, so compile will abort. **compile** will end optimization and return the design in its current state.

WHAT NEXT

No action is required on your part. If you want to abort the process, press Control-c three times.

INT-7 (information) Ignoring interrupt signal since the design is being mapped. One more interrupt will abort optimization without transferring the design...

DESCRIPTION

This message indicates that one Ctrl-C signal (SIGINT) was received by the process before the Delay Optimization phase of compile. Since the design is being mapped, compile will ignore the first interrupt signal. The second Ctrl-C will abort compile and not write out the design.

If you want to abort the process, then hit Ctrl-C three times in a row.

WHAT NEXT

INT-8 (information) Aborting optimization without transferring

the design...

DESCRIPTION

This message indicates that two Ctrl-C signals (SIGINT) were received by the process
before the Delay Optimization phase of compile, so compile is going to abort.
Compile will end optimization but not return the design in its current state because
the design has not been fully mapped.

If you want to abort the process, then hit Ctrl-C three times in a row.

WHAT NEXT

LICSVR

LICSVR-1 (error) Variable '%s' has invalid value '%s'. Allowed values are: 'package', 'individual', 'package individual' and 'individual package'.

DESCRIPTION

WHAT NEXT

LICSVR-2 (error) Could not obtain a license.

DESCRIPTION

```
The license for the feature being run could not be obtained.
```

WHAT NEXT

```
Check the key file to see if the feature exists. Check the location of the keyfile,
either the default location or at $SYNOPSYS_KEY_FILE. It could also be that all the
licenses are in use.
```

LICSVR-3 (error) SYNOPSYS_DS is not set. You must set this environment
variable to the root of the installed Synopsys software.

DESCRIPTION

```
SYNOPSYS_DS variable should be set inorder for the application to find the default
location.
```

WHAT NEXT

```
Set the SYNOPSYS_DS environment variable to SYNOPSYS root.
```

LICSVR-4 (error) DISPLAY is not set. You must set this

environment
variable before running the Synopsys software.

DESCRIPTION

```
The DISPLAY environment variable displays the application on the terminal on which
it was brought up.
```

WHAT NEXT

```
Check to see if this environment variable is set to the correct value.
```

LICSVR-5 (error) Can't initialize the license server.

DESCRIPTION

```
The vendor daemon will be brought up by the Flexlm license manager lmgrd on the
SERVER mentioned in the keyfile. The machine must be accessible.
```

WHAT NEXT

```
Check to see if the machne is up and running. If you are starting the license server
from a machine other than the server, then you must be able to ping and rsh to the
SERVER.
```

LICSVR-6 (error) The Synopsys License Server has crashed.

DESCRIPTION

```
The license server went down due to some reason. This may cause the lmgrd and
synopsysd processes to hang.
```

WHAT NEXT

```
If the machine is down, the machine needs to be up and running. If the license
server is being brought up from the startup script, check to make sure that the
lmgrd and synopsysd processes have icome up cleanly. Use lmstat to check. If you
have to bring up the license server daemons manually, make sure that you do not have
any zombie processes for lmgrd and synopsysd. Start the license manager using lmgrd.
```

LINK

LINK-1 (error) Can't find %s port '%s' on reference to '%s' in '%s'.

DESCRIPTION

This message indicates that the specified port has no corresponding port on the design to which the reference is to be linked. Therefore, the reference cannot be linked to the design.

This situation could arise if extra pin names were specified in the name-based instantiation of the cell in the source file. Alternatively, the name of the design port might be misspelled or incorrectly specified in the cell instantiation.

Another, less likely possibility is that there are design name conflicts that caused the linker to attempt to link the reference to the wrong design.

WHAT NEXT

Check the original source file for one or both of the above problems in the cell instantiation, and edit the file to correct the pin names. Check also for incorrect design names and correct them. Then re-execute **link**.

LINK-2 (error) Too many ports on reference to '%s' in '%s'.

DESCRIPTION

WHAT NEXT

LINK-3 (error) Width mismatch on port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The reference above could not be resolved due to a port size mismatch. The linker found a design that matches the requested reference name, but the port sizes do not match.

WHAT NEXT

Check that the ports of the target design or library cell are compatible with the reference.

LINK-4 (error) Too few ports on reference to '%s' in '%s'.

DESCRIPTION

WHAT NEXT

LINK-5 (warning) Unable to resolve reference '%s' in '%s'.

DESCRIPTION

This warning is issued when a suitable design can not be found to link a cell reference to. This will result in any cells using that reference being left as "black boxes". Generally this will happen because of one of two reasons: (1) either a design with the same name as the reference does not exist in the database, link libraries and the directories specified by the search_path, or, (2) the design exists but there are port mismatches between the reference and the design. In the second case an additional error message indicating the exact nature of the mismatch would be given.

If this error occurs while building a synthetic library part, you probably need to use "set_local_link_library" within your implementation description. Please refer to the section "Adding Hierarchy-Control Directives" in the DesignWare Developer Guide.

WHAT NEXT

If there are additional error messages indicating the name and nature of the port mismatches, modify the original souce to make the port specifications match in the instantiation and the design. If there are no such messages, find the library or the directory on which the required design resides. If it is a library, then add that library to the *link_library* variable, and the location of the library to the *search_path* variable. If it is in a design file, add its directory to the *search_path* variable. After doing this, run the **link** command again.

LINK-6 (error) Could not find pin '%s' on design '%s' for cell '%s'.

DESCRIPTION

WHAT NEXT

LINK-7 (error) Recursive hierarchy detected in design '%s'.

DESCRIPTION

WHAT NEXT

LINK-8 (error) Cannot resolve enumeration for cell '%s' on design '%s'.

DESCRIPTION

WHAT NEXT

LINK-9 (warning) Unable to resolve reference to synthetic module '%s' in '%s'.

DESCRIPTION

WHAT NEXT

LINK-10 (error) '%s' was not identified as a synthetic library module
and could not be successfully elaborated from design library

'%s'.

DESCRIPTION

```
The reference above could not be resolved to a synthetic library module in your
current link_library variable. The design also could not be elaborated from a design
that had been analyzed into the given design library. This causes linking to fail
for parameterized instances.
```

WHAT NEXT

```
If the reference should resolve to a synthetic library module, you should double
check that the appropriate synthetic library is in your link_library and that the
library contains the given module. If other libraries precede your synthetic library
in the link_library list, be sure that the two libraries do not contain a cell of
the same name. Note that VHDL references are case-insensitive; for example, you
could erroneously link to a cell named ADD from a technology library when you
intended to link to a module add from a synthetic library.
```

```
If the reference should resolve to a parameterized part, you must analyze that part
into an appropriate design library before linking. There may have been an error in
the actual elaboration. Check the error messages that preceded this one.
```

LINK-11 (error) Unconstrained port '%s' in design referenced by '%s' in '%s'.
 This version does not support unconstrained ports.

DESCRIPTION

WHAT NEXT

LINK-12 (warning) Unable to find library '%s'. This was probably caused by bad Synopsys installation.

DESCRIPTION

WHAT NEXT

LINK-13 (warning) design library '%s' was used in design '%s'

but it was never defined. Ignoring.

DESCRIPTION

Your VHDL source code contains a library clause for the given design. This library
has not been defined in Design Compiler.

WHAT NEXT

Define the library using **define_design_lib**.

LINK-14 (warning) Instance of '%s' is defined in both libraries '%s' and '%s', which are both visible in design '%s'. The first library will be used.

DESCRIPTION

Your VHDL source code for the given design contains a library clause for both
libraries listed above. Both libraries define an entity for the instance given.
Technically, this is an error in VHDL. We are using the entity from the first
library listed.

WHAT NEXT

There is nothing to do for now. In the future, it will be important to choose an
entity explicitly in a VHDL configuration.

LINK-15 (error) Cannot continue with auto_link disabled. Set 'auto_link_disable = false'.

DESCRIPTION

The **auto_link_disable** variable is only to be used for speeding up long sequences of
set_load, **set_resistance**, and **set_annotated_delay** commands. The current command
cannot be executed while auto_link is disabled.

WHAT NEXT

Set **auto_link_disable** = false, and re-execute the command.

LINK-16 (warning) Parameter mismatch in linking reference '%s' by name.
 Linked to '%s', which has the correct parameters.

DESCRIPTION

```
An attempt was made to link a parameterized reference by name, but the name of the
reference pointed to a design with incorrect parameters. The link process resolved
the reference to the design above, which had the correct parameters.
```

WHAT NEXT

```
To avoid this message, you should attempt to keep your design names unique. This is
done by keeping your parameter values below the hdl_naming_threshold, and by
including special naming parameters in your HDL designs. For details, refer to the
VHDL Compiler Reference Manual.
```

LINK-17 (warning) Design '%s' was renamed to '%s' to avoid a conflict with another design that has the same name but different parameters.

DESCRIPTION

```
A design was automatically elaborated by HDL Compiler, but the name generated for
the new design was already in use by another design. The new design was renamed to
avoid overwriting the existing design.
```

WHAT NEXT

```
To avoid this message, ensure that your design names are unique by keeping your
parameter values below the hdl_naming_threshold, and by including special naming
parameters in your HDL designs. For details, refer to the VHDL Compiler Reference
Manual.
```

LINK-18 (warning) Parameter mismatch in linking reference '%s' by name.

Can't find design.

DESCRIPTION

An attempt was made to link a parameterized reference by name, but the name of the
reference pointed to a design with incorrect parameters. The processing that follows
this message will attempt to elaborate a new design with the correct parameters. If
it fails, this reference will remain unresolved.

WHAT NEXT

To avoid this message, you should attempt to keep your design names unique. This is
done by keeping your parameter values below the **hdl_naming_threshold**, and by
including special naming parameters in your HDL designs. For details, refer to the
VHDL Compiler Reference Manual.

LINK-19 (warning) "Port '%s' was unresolved on reference to '%s' in '%s'.

DESCRIPTION

This warning is issued when a port can not be resolved on a reference. Ports in the
given reference may be duplicate by ignoring cases. If it fails, this reference will
remain unresolved.

WHAT NEXT

To avoid this message, you should attempt to keep your ports in a reference unique.
Check for attribute value dblink_case_insensitive in the warning reference.

LINK-20 (warning) "Attempting to resolve reference '%s' from non-synthetic design library '%s'.

DESCRIPTION

This warning is issued when a reference suspected to be a DesignWare part fails to
link from a DesignWare library such as dw02.sldb. However, the reference may still
successfully link from a non-DesignWare library.

WHAT NEXT

Often this warning results from neglecting to specify the required synthetic

libraries using the `link_library` variable. This can be quickly fixed using the
following shell script line:

```
link_library = link_library + synthetic_library
```

This ensures that the `link_library` variable specifies the necessary DesignWare
libraries for your design. Also check that the variable, `synlib_library_list`,
specifies the correct design library names for DesignWare parts. Note that if you
are using an external implementation of a DesignWare part, you may receive this
warning during normal use.

LINK-21 (warning) Design '%s' has %d extra %s port(s) than reference '%s' in '%s'.

DESCRIPTION

You receive this message if the external netlist used by the preserved function has
extra ports that are not defined in the preserved function. These ports are unused.

WHAT NEXT

To avoid this message, use a netlist with I/O ports exactly matching the I/O ports
specified in the preserved function.

LINK-22 (error) Reference '%s' in '%s' is a preserved function and
 cannot have inout ports.

DESCRIPTION

This error is issued when a port can not be resolved on a reference because the
direction of the port is inout. Bidirectional ports are not allowed with preserved
functions and external netlists.

WHAT NEXT

To avoid this error, change the direction of the port to make it either an input or
output port.

LINK-23 (error) Design '%s' used to resolve reference '%s' in

'%s' is a external netlist and cannot have inout ports.

DESCRIPTION

You receive this message if a port cannot be resolved on a reference. In the
external netlist used to resolve the reference, the direction of the corresponding
port is inout. Bidirectional ports are not allowed with preserved functions and
external netlists.

WHAT NEXT

To avoid this error, use a netlist that has only input or output ports that match
the ports of the preserved function.

LINK-24 (error) Port '%s' of reference '%s' in '%s' is connected to port '%s' of the external netlist '%s'. The directions of these two ports are not compatible.

DESCRIPTION

This error is issued when a port can not be resolved on a reference because the
direction of the corresponding port of the netlist is different. Note that 'inout'
ports are not allowed in preserved functions and external netlists.

WHAT NEXT

To avoid this error, input ports in the preserved function must be same as the input
ports in the external netlist. Similarly, output ports in the preserved function
must be same as the output ports in the external netlist.

LINK-25 (error) Unable to match ports of cell %s ('%s') to '%s'.

DESCRIPTION

The tool issues this error message because it encountered problems when attempting
to match the ports of the cell's existing reference to the new reference.

WHAT NEXT

Check that the ports of the target design or library cell are compatible with the
cell's current reference. You may need to modify the original source to make the
port specifications match in the instantiation and the design.

`change_link` (2), `link` (2).

LINK-26 (warning) Design '%s' was renamed to '%s' to resolve a long name which is not supported by some down stream tools.

DESCRIPTION

```
Down stream tools have limitation for the length of design name. The design name
generated by HDL compiler is shortened, then the design can be accepted by down
stream tools.
```

WHAT NEXT

```
To avoid this message, ensure that your design names do not exceed the limit.
```

LINT

LINT-0 (warning) In design '%s', input pin '%s' of leaf cell '%s' is not connected to any net. %s assumed.

DESCRIPTION

This message appears when a leaf cell has an unconnected input pin. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-1 (warning) In design '%s', cell '%s' does not drive any nets.

DESCRIPTION

This warning alerts you that the output(s) of a component is not connected to any load nets. This usually indicates that a design has not been correctly specified. The Design Compiler may remove such components from your design unless they are protected by a *dont_touch* attribute.

WHAT_NEXT

Make sure that you really want the named component to exist in the given design, even though it has no output pins connected. If so, add a *dont_touch* attribute with the *dont_touch* command to keep the component from being removed.

LINT-2 (warning) In design '%s', net '%s' driven by pin '%s' has

no loads.

DESCRIPTION

This warning message occurs when a net is driven by an output pin (or pins) but has no load pins connected to it. This usually indicates that a design is not correctly specified. The Design Compiler may remove such nets and their driving components from your design unless they are protected by a don't touch attribute.

WHAT_NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Make sure that you want the named net to exist in the given design, even though it has no load pins connected. If so, add a don't touch attribute with the **dont_touch** command to keep the net from being removed.

Check the value of the **hdlin_keep_signal_name** variable. For some settings, signals without drivers or loads are preserved in the elaborated design. Check the **hdlin_keep_signal_name** man page for more information.

SEE ALSO

hdlin_keep_signal_name(3)

LINT-3 (warning) In design '%s', net '%s' has no drivers. %s assumed.

DESCRIPTION

This warning message occurs when there is a net that is not driven by any source pins. Synopsys tools will assume a logical value, such as logic zero or logic one) for these unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

This is only a warning. You can eliminate this warning message by the following the instructions below.

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating net to the correct logical value in your design.

Check the value of the **hdlin_keep_signal_name** variable. For some settings, signals

without drivers or loads are preserved in the elaborated design. Check the
hdlin_keep_signal_name man page for more information.

SEE ALSO

hdlin_keep_signal_name(3)

LINT-4 (information) In design '%s', net '%s' has multiple drivers. Wired AND assumed.

DESCRIPTION

This warning indicates that *check_design* has found a net with multiple source pins.
Synopsys tools must make an assumption regarding the functionality of such wired-
logic nets. This message indicates which wired-logic net (for example, wired-AND,
wired-OR) will be used for this particular net. The assumption is made based on a
description of wired-logic functionality in the technology library that you are
using.

WHAT_NEXT

Make sure that you intended to have multiple drivers on the given net. Errors in
specifying a design could lead to this message in a situation where wired logic is
not intended.

You could also use *set_attribute* and *remove_attribute* commands to specify or remove
the wired logic type for a given net.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'. While

remove_attribute [get_nets z] wired_and

would remove the 'wired_and' attribute on net 'z'.

LINT-5 (warning) In design '%s', output port '%s' is not driven.

DESCRIPTION

This error message occurs when the **check_design** command finds the specified output
port for the design is not driven by any signal.

WHAT_NEXT

Check your design to be sure that it is connected correctly, and then run the command again.

SEE ALSO

`check_design` (2).

LINT-6 (warning) In design '%s', input port '%s' drives wired logic.
(port-direction may have been specified incorrectly.)

DESCRIPTION

This warning is issued when the *check_design* command encounters an input port connected to a net which has multiple drivers. In other words, the input port (which acts as a driver on the net) is part of a wired-logic gate.

WHAT_NEXT

Make sure that you intend to have multiple drivers on the net driven by the indicated port. Errors in specifying a design could lead to this message in a situation where wired logic is not intended. For example, if the direction of an output port is accidentally specified as "input," then this message could occur. Otherwise, you've encountered a situation where the optimizer has created wired logic on a design boundary. Check the components created by the optimizer to ensure that this is the functionality that you originally intended. Use the *verify* command to compare the design you currently have with the original design, in addition to simulating the synthesized design to ensure correctness.

LINT-7 (error) Recursive hierarchy detected in design '%s'.

DESCRIPTION

The *check_design* command traces the hierarchy of your design to ensure that "recursive hierarchy" does not occur. The term "recursive hierarchy" means that a module in a design instantiated a sub-module that, in turn, instantiated the original module. Hierarchically recursive designs cannot be handled by the Design Compiler. This is an error message, not a warning.

WHAT_NEXT

This error usually occurs when a design has been incorrectly described. Modify your

```
design description to remove the recursive hierarchy.
```

LINT-8 (warning) In design '%s', input port '%s' is unloaded.

DESCRIPTION

```
The check_design command issues this warning when it finds an unconnected (for
example, "unloaded") input port on a design. This means that the given input port
does not connect to any logic inside the design.
```

WHAT_NEXT

```
Make sure that you intended that the specified port be unused in your design.
```

LINT-10 (warning) In design '%s', cell '%s' has no output pins.

DESCRIPTION

```
This warning message indicates that check_design has found a cell with no output
pins. Unless such cells are protected through the use of the dont_touch command, the
compile command will remove them from the design, since they have no functionality.
```

WHAT_NEXT

```
This warning probably appeared because of an error in specifying a component in your
design, or a component in your technology library. Check the design/library to find
the problem, and correct the description of the given cell/design.
```

LINT-11 (fatal) In design '%s', db_object '%s' does not have a '%s' attribute.

DESCRIPTION

```
This is a fatal error in the check_design command. An object in the Synopsys
internal database for your design has become corrupt or does not have information
regarding signal direction (for example, input, output or bidirectional).
```

WHAT_NEXT

```
Recreate or re-read your design. If you specified a component pin without a
direction attribute, you can fix the problem by making sure that a direction exists
```

for the given pin. Otherwise this error could indicate that there is an internal
problem in the Synopsys software that needs to be reported to the Synopsys Hotline
or to your Synopsys application engineer.

LINT-12 (fatal) Unable to db_gen_init '%s' from db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. An object in the Synopsys
internal database for your design has become corrupt, or that an object in your
design does not have ports attached to it.

WHAT_NEXT

Recreate or re-read your design. If you specified a component without ports, you can
fix the problem by making sure that ports exist for the given pin. Otherwise this
error could indicate that there is an internal problem in the Synopsys software that
needs to be reported to the Synopsys Hotline or to your Synopsys application
engineer.

LINT-20 (error) In design '%s', cell '%s' does not have a reference.

DESCRIPTION

This error describes a problem in the database representation for your design. The
error means that a particular instantiation of a component (or "cell" in Synopsys
terms) does not indicate which type of component it actually is. In Synopsys
terminology "reference" describes the part of a design representation that points to
the actual component for a given instantiation or cell. If you have an inverter
(INV) in your technology library, and you've instantiated that inverter in your
design as cell13 and cell23, then each of the instantiations (cells) should own a
pointer (reference) to the actual component (in this case INV). This error indicates
that, for some reason, the reference does not exist on the cell.

WHAT_NEXT

Make sure that your design specifies the type of the given cell. If you specified a
cell without a type, fix the problem by changing your design description. Otherwise
this error could indicate that there is an internal problem in the Synopsys software
that needs to be reported to Synopsys Hotline or to your Synopsys application
engineer.

LINT-21 (fatal) Unable to db_new_attribute to db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to allocate memory to create an object in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These small markers are removed after *check_design* is finished. This error indicates that an attempt to create a marker failed for some reason. This is probably due to a lack of memory, in which case the fatal error was accompanied by an "out of memory" error message. It is.also possible that this message could occur in a badly mangled design which has recursive hierarchy.

WHAT_NEXT

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-22 (warning) In design '%s', ref '%s' was not used.

DESCRIPTION

This warning indicates that there is a dangling "reference" with the given name on your design. In Synopsys terminology "reference" describes the part of a design representation that points to the actual component for a given instantiation or cell. If you have an inverter (INV) in your technology library, and you've instantiated that inverter in your design as cell13 and cell23, then each of the instantiations (cells) should own a pointer (reference) to the actual component (in this case INV). Sometimes, during the process of building or modifying a design, a reference will remain, even though all cells that refer to it have been removed or changed. Although this is a waste of memory, it should not impair the functionality of the design or the operation of Synopsys tools.

WHAT_NEXT

A large number of dangling references in your design can increase the memory size of the design. Sometimes these can be removed by writing the entire design out (in Synopsys database "db" format) and then reading it to Synopsys tools again. Otherwise, make a note of when the message occurs and pass the problem and an example to the Synopsys support Hotline or to your application engineer. Dangling references indicate that the tool is not managing memory efficiently.

LINT-23 (fatal) Unable to remove attribute '%s' from db_object

'%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to
deallocate memory to free an object in the Synopsys internal database description
for your design. The *check_design* command creates small markers on your design as it
traverses the design checking for errors. These markers are removed after
check_design is finished. This error indicates that an attempt to remove a marker
failed for some reason. This is probably due to an internal memory error in Synopsys
tools.

WHAT_NEXT

The problem is either a faulty design or an internal Synopsys error. The
check_design command may have destroyed your design. Report the problem to the
Synopsys Hotline or to your Synopsys application engineer.

LINT-25 (warning) Design '%s' does not have any output ports.

DESCRIPTION

This warning message indicates that *check_design* has found a design with no output
pins. Unless such designs are protected through the use of the *dont_touch* command,
the *compile* command will remove instances of such designs, since they have no
functionality.

WHAT_NEXT

This warning probably appeared because of an error in specifying a component in your
design, or a component in your technology library. Check the design/library to find
the problem, and correct the description of the given cell/design.

LINT-26 (fatal) Unable to db_set_attribute to db_object '%s'.

DESCRIPTION

This is a fatal error in the *check_design* command. Synopsys tools were unable to
allocate memory to create an attribute in the Synopsys internal database description
for your design. The *check_design* command creates small markers on your design as it
traverses the design checking for errors. These markers are removed after
check_design is finished. This error appears when an attempt to create a marker
failed for some reason. This is probably due to a lack of memory, in which case the
fatal error was accompanied by an "out of memory" error message. It is also possible
that this message could occur in a badly mangled design which has recursive

hierarchy.

WHAT_NEXT

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-27 (error) Object '%s' is not of class dd_design, and should not be seen by db_lint.

DESCRIPTION

This message indicates that the *check_design* command has been called on a database object that is not a design. It indicates an internal problem in the user-interface for the *check_design* command, or a corrupted design database.

WHAT_NEXT

Recreate or re-read your design, and then runn *check_design*. If this does not work, then there is probably an internal problem in the Synopsys software that should be reported to the Synopsys Hotline or to your Synopsys application engineer.

LINT-28 (warning) In design '%s', port '%s' is not connected to any nets.

DESCRIPTION

This warning alerts you that a port in a design is not connected to any nets. This usually indicates that a design has not been correctly specified. However, there are some situations where, as a designer, you choose to specify a port on a design for compatibility reasons, even though the port is not internal to design use. The Synopsys tools leave unconnected ports alone, with one exception; that is, you specified that a given input port is opposite or equal to another input port in a design.

WHAT_NEXT

Make sure that you want the named port to exist in the given design, even though it has no nets connected. Remove the port from your design if you choose.

LINT-29 (warning) In design '%s', input port '%s' is connected directly to output port '%s'.

DESCRIPTION

This warning alerts you to a situation where an input port in a design is directly connected to an output port. This warning is issued because some technologies do not allow such a connection. Many ASIC vendors stipulate that a buffer must be used to connect an input to an output. This restriction might or might not apply to your technology.

WHAT_NEXT

If directed to do so, *compile* inserts the necessary buffering to prevent a direct connection of an input port and an output port. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design. This variable also instructs *compile* to make sure that multiple output ports are not connected to the same electrical net. See the manual page on *compile_variables* for more information.

LINT-30 (warning) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* warning message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of warnings.

WHAT_NEXT

Use *check_design* to obtain more information about the warning.

LINT-31 (warning) In design '%s', output port '%s' is connected directly to output port '%s'.

DESCRIPTION

This warning alerts you to a situation where an output port in a design is connected directly to another output port. This warning is issued because some technologies do not allow such a connection. This restriction might or might not apply to your technology.

If directed to do so, *compile* inserts the necessary buffering to make sure that multiple output ports are not connected to the same electrical net. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design.

This variable also instructs *compile* to prevent a direct connection of an input port and an output port. See the manual page on *compile_variables* for more information.

LINT-32 (warning) In design '%s', a pin on submodule '%s' is connected to logic 1 or logic 0.

DESCRIPTION

check_design issues this warning when it finds an instance of a hierarchical design (for example, a sub-module) that has an input connected to a logic constant. This warning is issued to verify that this is a desired connection on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it has optimized and eliminated the logic driving a submodule.

WHAT_NEXT

Verify that you want the given submodule input connected to logic one or zero. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile*, whenever feasible.

LINT-33 (warning) In design '%s', the same net is connected to more than one pin on submodule '%s'.

DESCRIPTION

check_design issues this warning when it finds an instance of a hierarchical design (for example, a sub-module) that has more than one input connected to the same net. This warning is issued to verify that these are desired connections on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it determines that multiple inputs on a submodule are driven by the same logical signal.

WHAT_NEXT

Verify that you want the given submodule inputs connected to the same logical signal. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile* whenever

```
feasible.
```

LINT-34 (warning) In design '%s', three-state bus '%s' has non three-state driver '%s'.

DESCRIPTION

```
Synopsys libraries contain descriptions of three-state driving pins on components.
Synopsys tools classify a net as a three-state net if it is driven by at least one
pin that has this three-state attribute. Normally, if there are multiple drivers on
such nets, it is assumed that all driving pins should be three-state drivers, for
correct operation of the three-state bus. This warning message indicates a situation
where at least one non-three-state driver appears on a three-state net.
```

WHAT_NEXT

```
Verify that this is what you have intended for the given net. If the non-three-state
driver pin specified in the message is really on a three-state driver in your ASIC
technology, verify that the technology library description is correct.
```

LINT-35 (information) In design '%s', net '%s' has multiple drivers. Wired OR assumed.

DESCRIPTION

```
This warning message indicates that check_design has found a net with multiple
source pins. Synopsys tools make an assumption regarding the functionality of such
wired logic nets. This message gives the interpretation (for example, Wired-And,
Wired-Or) that will be used for this particular net. This assumption is made based
on a description of wired logic functionality in the technology library used.
```

WHAT_NEXT

```
Make sure that you intend to have multiple drivers on the given net. Errors in
specifying a design could lead to this message in a situation where wired logic is
not intended.

You could also use set_attribute and remove_attribute commands to specify or remove
the wired logic type for a given net.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'. While
```

```
remove_attribute [get_nets z] wired_and
```

would remove the 'wired_and' attribute on net 'z'.

LINT-38 (warning) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

DESCRIPTION

This warning message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

WHAT_NEXT

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

```
set_attribute [get_nets z] wired_and true -type boolean
```

would set 'wired_and' attribute on net 'z'.

LINT-39 (warning) In design '%s', net '%s' has %s emitters, exceeding the maximum of %s.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have a limit on the number of emitters that can legally be connected together. This limit is given by the *max_wired_emitters* attribute in the technology library.

WHAT_NEXT

Make sure that you intend to have this many emitters on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net of this size is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the specification for the maximum number of wired emitters is correct.

LINT-40 (warning) In design '%s', net '%s' has drivers with conflicting wired connection classes.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have to meet *connection class* requirements that ensure that all drivers on the net may be legally connected together. All drivers on a wired logic net must share the same wired connection class. Each driver's class is defined in the technology library description for the driver by the *wired_connection_class* attribute.

WHAT_NEXT

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library, to be sure that the connection classes for the given components are correct.

LINT-41 (warning) In design '%s', pin '%s' is not allowed to drive wired logic.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. All driving pins on a wired logic net must be capable of driving wired logic. The technology library description for driving pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level and gives a default value for components in the library.

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-42 (warning) In design '%s', pin '%s' is not allowed to be driven by wired logic.

DESCRIPTION

This warning message indicates that *check_design* has found a wired logic net that is illegal. All load pins on a wired logic net must be capable of being driven by wired logic. The technology library description for pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level to give a default value for components in the library.

WHAT_NEXT

Make sure that you intend to have these loads on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these loads is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-44 (information) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* informational message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of some important information.

WHAT_NEXT

Use *check_design* to obtain more information about the informational message.

LINT-45 (information) Design '%s' is instantiated %d times.

DESCRIPTION

This information message indicates that a single design is instantiated more than once in the design hierarchy below the current design. This message is issued when "check_design -multiple_designs" is used in XG mode.

WHAT_NEXT

Right now all DC commands handle designs with multiple instances. Each command may invoke *uniquify* under the hood to uniquify user designs if necessary.

LINT-46 (warning) Design '%s', cell '%s', pin '%s' is illegally connected,
 since primary output '%s' is unconnected.

DESCRIPTION

This warning message occurs for ECL designs in ECL technologies that use the *primary output* designator for paired ECL outputs. By designating an output as a *primary output* your ASIC vendor has indicated that the given output must be connected before any other outputs of the same polarity are used. As an example, suppose that a component NOR2 has two positive phase outputs, X1 and X2. Suppose that the technology library description for the gate shows X1 as a primary output. Designating X1 as a primary output means that it is illegal to connect output X2 to a net unless X1 is already connected to a different net. This warning indicates a case where (to use this example) output X2 is connected but output X1 is not connected. This is a violation of the design rule described in the technology library.

WHAT_NEXT

Be sure that your design was created correctly. If the Design Compiler or DFT Compiler have created an illegal design, check the technology library to be sure that the *primary_output* attribute is used properly for the given technology. If everything is alright in the technology library and *compile* has created an illegal design, contact your Synopsys application engineer or the Synopsys Hotline with a test case.

LINT-47 (warning) In design '%s' net '%s' has a connection

class violation:

DESCRIPTION

This warning message indicates that *check_design* has found a net that does not meet the connection class requirements described in the technology library. These connection class requirements ensure that all pins on a net can legally be connected. All pins connected together on a net must share at least one connection class in common. Each pin's class is defined in the technology library description for the pin, through the *connection_class* attribute.

WHAT_NEXT

Determine whether the design you are checking was (1) created manually as a netlist, or (2) created by Design Compiler (possibly from a high-level description) or DFT Compiler. If (1) is true, investigate the violation to be sure that you have specified the net correctly in your design. If (2) is true, examine the illegal net(s) created by the tool. It might not always be possible for the given net to be legalized. For example, a net might connect though hierarchy to pins whose connection classes cannot be matched. Or, other design rules, such as fanout restrictions or transition time restrictions might have made legalization for connection rules impossible. Also, check your technology library to determine whether there are level shifting components available to convert between the given connect classes.

LINT-48 (error) Not a valid part and speed grade

DESCRIPTION

This error message indicates that *check_design* has found that the part specified on the design does not exist in the technology library.

WHAT_NEXT

Do a *report_library* on the technology library to get the list of parts supported. Select the one you want and attribute on the design.

LINT-49 (warning) The part %s has fewer I/O ports %d than that required by the design %d.

DESCRIPTION

This warning message indicates that *check_design* has found that the part specified on the design does not have enough number of input/output ports to hold the design.

Do a *report_library* on the technology library to get the list of parts supported. Select the bigger part and attribute it on the design.

LINT-50 (warning) The part %s has fewer flip-flops %d than that required by the design %d.

DESCRIPTION

This warning message indicates that *check_design* has found that the part specified on the design is unable to accomodate the number of flip-flops present in your design.

WHAT_NEXT

Do a *report_library* on the technology library to get the list of parts supported. Select the part which has more number of flip-flops than the previous part and attribute it on the design.

LINT-51 (warning) Part related checkings is not supported for the technology library.

DESCRIPTION

This warning message indicates that *check_design* has found that the technology library doesn't have any parts information specified in it.

WHAT_NEXT

Part specific checking is supported only for FPGA technology library. Make sure that you are using FPGA technology library and they have part information specified in them. If there is no part information, ask your vendor to supply a technology library with part information.

LINT-52 (warning) In design '%s', output port '%s' is connected

directly to '%s'.

DESCRIPTION

```
This warning alerts you to a situation where an output port in a design is connected
directly to Logic 1 or Logic 0. This warning is issued because some technologies do
not allow such a connection. This restriction might or might not apply to your
technology. Most case it is a design error.
```

WHAT_NEXT

```
Please check the net list carefully to make sure this case is desired, and discuss
with your technology team to make sure it is allowed.
```

LINT-53 (error) In design '%s', net '%s' is driven by both logic 0 and logic 1.

DESCRIPTION

WHAT_NEXT

LINT-54 (warning) In design '%s', net '%s' is driven by %s.

DESCRIPTION

```
This message alert you the net is driven by const net.
```

WHAT_NEXT

```
Please visit your design and make sure it is desired.
```

LINT-55 (information) Design '%s' does not contain any cells or

nets.

LINT-56 (error) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

DESCRIPTION

This error message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

WHAT_NEXT

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_unknown_wired_logic_type* to *true*.

LINT-57 (error) In design '%s', %s.

DESCRIPTION

This is the terse version of a *check_design* error message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of errors.

WHAT_NEXT

Use *check_design* to obtain more information about the error.

LINT-58 (warning) In design '%s', input pin '%s' of leaf cell '%s' is connected to undriven net '%s'.

DESCRIPTION

This message appears when leaf cell input pin has a connected net, but the net has no driver.

WHAT_NEXT

LINT-59 (warning) In design '%s', input pin '%s' of hierarchical cell '%s' has one or more internal loads, but is not connected to any nets. '%s' is assumed.

DESCRIPTION

This message appears when hierachical cell input pin has internal load, but no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-60 (warning) In design '%s', input pin '%s' of hierarchical cell '%s' has no internal loads and is not connected to any nets.

DESCRIPTION

This message appears when hierarchical cell input pin has no internal load and no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

WHAT_NEXT

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-62 (error) In design '%s', three-state bus '%s' has non three-state driver '%s'.

DESCRIPTION

Synopsys libraries contain descriptions of three-state driving pins on components. Synopsys tools classify a net as a three-state net if it is driven by at least one pin that has this three-state attribute. Normally, if there are multiple drivers on such nets, it is assumed that all driving pins should be three-state drivers, for correct operation of the three-state bus. This Error message appears when at least one non-three-state driver appears on a three-state net.

WHAT_NEXT

Verify that this is what you have intended for the given net. If the *non-three-state* driver pin specified in the message is really on a three-state driver in your ASIC technology, verify that the technology library description is correct.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_non_tristate_drivers_on_tristate_bus* to *true*.

LINT-63 (warning) Net '%s' has a single tri-state driver.

DESCRIPTION

You receive this warning message when the **check_design** command detects that a net is

```
driven by a single tri-state driver.
```

WHAT NEXT

LINT-78 (information) Design '%s' has multiply instantiated designs. Use the '-multiple_designs' switch for more information.

DESCRIPTION

```
This message indicates that the current_design has one or more multiply instantiated
designs. To get a list of all the multiply instantiated designs with the instance
names, use -multiple_designs switch.
```

WHAT_NEXT

```
Use -multiple_designs to obtain more information about the multiply instantiated
designs.
```

LINT-98 (information) Use the 'check_design' command for more information about warnings.

DESCRIPTION

```
This message indicates that a terse version of informational messages or warnings on
a design has just been displayed. To obtain more complete information, use
check_design. This message is displayed when user used check_design -summary to get
a summary of the potential design problems.
```

WHAT_NEXT

```
Use check_design to obtain more information about the design.
```

LINT-99 (information) There are %d potential problems in your design. Please run 'check_design' for more information.

DESCRIPTION

```
This message indicates that there are %d potential design problems in the user
```

design. To obtain detailed information, use *check_design*. This message is displayed
when Synopsys commands like *compile* perform a design check as part of their
operation. If *compile* issued the message but completed its operation, the design
might have to be read again for *check_design* to report what was wrong initially.

WHAT_NEXT

Use *check_design* to obtain more information about the design.

LINT-100 (warning) The design does not have back-annotated delays.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does
not have back-annotated delays.

WHAT_NEXT

To back-annotate delays onto the design, use the *read_timing* command or a series of
set_annotated_delay command.

LINT-101 (warning) Missing %s delay annotation between pins '%s' and '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a timing arc on a cell
that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate
the delay directly with the *set_annotated_delay* command.

LINT-102 (warning) The design does not have back-annotated

cluster assignments.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have back-annotated cluster assignments (The clusters corresponds to the physical hierarchy of the design).

WHAT_NEXT

To back-annotate cluster assignments onto the design, use the *read_clusters* command to read in the *PDEF* file.

LINT-103 (warning) Missing cluster annotation on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a cell which is not assigned to a cluster.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that cells with missing cluster assignment are correctly assigned to a cluster.

LINT-104 (warning) The design does not have back-annotated cell locations.

DESCRIPTION

check_design -post_layout issues this warning when it finds that the design does not have cell locations back-annotated.

WHAT_NEXT

To back-annotate cell locations onto the design, use the *read_clusters* command to read in the *PDEF* file with cell location (i.e., *PDEF* version 2.0 or later)..

LINT-105 (warning) Missing cell location for cell '%s'.

DESCRIPTION

`check_design -post_layout` issues this warning when it finds a cell which does not have cell location back-annotated.

WHAT_NEXT

Modify the `PDEF` file before applying `read_clusters` command such that cells with missing cell locations are correctly assigned a cell location.

LINT-106 (warning) Missing %s delay annotation from pin '%s/%s' to pin '%s/%s' on net '%s'.

DESCRIPTION

`check_design -post_layout` issues this warning when it finds a net timing arc that does not have back-annotated delay.

WHAT_NEXT

Modify the `SDF` file such that the missing delay is correctly described or annotate the delay directly with the `set_annotated_delay` command.

LINT-107 (warning) The design does not have back-annotated net capacitances.

DESCRIPTION

`check_design -post_layout` issues this warning when it finds that the design does not have back-annotated net capacitances.

WHAT_NEXT

To back-annotate net capacitances on the design, use a series of `set_load` command.

LINT-108 (warning) Missing capacitance annotation on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net that does not have back-annotated capacitance.

WHAT_NEXT

To back-annotate capacitances on nets with missing capacitance annotation, use a series of *set_load* command.

LINT-109 (warning) Missing orientation annotation on cluster '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated row-orientation.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing orientations are correctly assigned an orientation.

LINT-110 (warning) Missing bounding box for cluster '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated bounding box.

WHAT_NEXT

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing bounding box are correctly assigned a bounding box.

LINT-111 (warning) Missing %s delay annotation for *setup* arc

from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *setup* timing arc on a cell that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-112 (warning) Missing %s delay annotation for *hold* arc from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *hold* timing arc on a cell that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-113 (warning) Missing %s delay annotation for 'preset' or 'clear' timing arc from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a *preset* or *hold* timing arc on a cell that does not have back-annotated delay. If the warning message indicates a missing *rise* delay annotation, the timing arc with missing annotation is a *preset* timing arc; otherwise, it is a *clear* timing arc.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-114 (warning) Missing %s delay annotation from port '%s%s' to pin '%s/%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a pin that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-115 (warning) Missing %s delay annotation from pin '%s/%s' to port '%s%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a pin to a *port* that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-116 (warning) Missing %s delay annotation from port '%s%s' to port '%s%s' on net '%s'.

DESCRIPTION

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a *port* that does not have back-annotated delay.

WHAT_NEXT

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-117 (warning) The design does not have any back-annotation information.

DESCRIPTION

You receive this warning message when the **check_design -post_layout** command is executed and it detects that the design does not have any back-annotation information.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command or a series of **set_annotated_delay** commands. To back-annotate cluster assignments onto the design, use the **read_clusters** command to read in the PDEF file. To back-annotate net capacitances on the design, use a series of **set_load** commands.

LINT-118 (warning) The design has '%d' cells which do not have cluster annotation on them. The cells with missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that do not have cluster information back-annotated on them. The message reports the total number of all such cells, and prints the percentage of cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds cells with missing cluster annotations.

WHAT NEXT

To back-annotate cluster assignments onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-119 (warning) The design has '%d' cells which do not have locations annotation on them. The cells with missing annotations

represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that do not have location information back-annotated on them. The message reports the total number of all such cells and gives the percentage of the cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds cells with missing location annotations.

WHAT NEXT

To back-annotate location assignments onto the design, correct the PDEF file, and use the **read_clusters** command to read in the PDEF file.

LINT-120 (warning) The design has '%d' cells annotated with clusters which have no orientation. The cells with this type of missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that are annotated with clusters that have no orientation. The warning message reports the total number of all such cells and prints the percentage of the cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds cells annotated with clusters that have no orientation.

WHAT NEXT

To back-annotate cluster assignments with orientation onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-121 (warning) The design has '%d' cells annotated with clusters which have no bounding box. The cells with this type of

missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that are annotated with clusters that have no bounding box. The command reports the total number of all such cells and prints the percentage of cells with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it detects cells annotated with clusters that a have missing bounding box.

WHAT NEXT

To back-annotate cluster assignments with a bounding box onto the design, correct the PDEF file and use the **read_clusters** command to read in the PDEF file.

LINT-122 (warning) The design has '%d' cells which have missing delay arc annotations. The cells with missing annotations represent '%f' of all cells.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has cells that have missing delay arc annotations. The command reports the total number of all such cells and prints the percentage of cells with the missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds cells with missing delay arc annotations.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command, or a series of **set_annotated_delay** commands.

LINT-123 (warning) The design has '%d' nets which have missing delay arc annotations. The nets with missing

annotations represent '%f' of all nets.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has nets that have missing delay arc annotations. The command reports the total number of all such nets and prints the percentage of nets with the missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning when it finds nets with missing delay arc annotations.

WHAT NEXT

To back-annotate delays onto the design, use the **read_sdf** command or a series of **set_annotated_delay** commands.

LINT-124 (warning) The design has '%d' nets which do not have capacitance annotation on them. The nets with missing annotations represent '%f' of all nets.

DESCRIPTION

You receive this warning message when the **check_design -post_layout -summary** command detects that the design has nets that do not have capacitance information back-annotated on them. The command reports the total number of all such nets and prints the percentage of nets with missing annotations.

The **check_design -only_post_layout -summary** command also issues this warning message when it finds nets with missing capacitance annotations.

WHAT NEXT

To back-annotate net capacitances on the design, use a series of **set_load** commands.

LNK-001 (error) Cannot read link_path file '%s'.

DESCRIPTION

The file, specified in the link_path variable, cannot be read. Either the file does not exist or it is not a DB file.

WHAT NEXT

Check the existence of the file in the search_path using the **which** command.

LNK-002 (information) Design '%s' is already linked.

DESCRIPTION

The specified design has already been linked.

WHAT NEXT

Verify that this is the design that you wanted to link.

LNK-003 (information) Design '%s' was not successfully linked: %d unresolved references.

DESCRIPTION

A summary message indicating that the link process failed for your design.

WHAT NEXT

See previous error messages for more details.

LNK-004 (error) Unsupported LSI reference '%s' to '%s'

cannot be resolved

DESCRIPTION

The linker tried to resolve a reference which was derived from an LSI netlist, and the reference a form that the tool does not support. This tool only supports fully name-based references from LSI netlists. Order-based or mixed order and name based references are not supported.

WHAT NEXT

Use another Synopsys tool to read the DB, link it, and write it out to a new DB file. This will resolve the naming issue.

LNK-005 (warning) Unable to resolve reference to '%s' in '%s'.

DESCRIPTION

During the link process, a reference in the design could not be resolved. This means that no match was found for the reference using the semantics of the link_path variable.

This message is generated only for the first instance of the reference. In order to see all of the instances that are unresolved, use "link_design -verbose".

WHAT NEXT

Examine the link_path variable, log messages, and use the **which** command to find out which files were loaded.

LNK-006 (warning) Cannot resolve instance %s/%s (%s).

DESCRIPTION

During the link process, a reference in the design could not be resolved. This message is for the instance that was trying to link to the reference.

This message is only displayed in verbose mode.

WHAT NEXT

Examine the link_path variable, log messages, and use the **which** command to find out which files were loaded.

LNK-007 (error) Cannot instantiate design '%s' in '%s'.

DESCRIPTION

During the link process, a reference was resolved, but the design to which it resolved cannot be instantiated due to errors in the read process.

This message is generated only for the first instance of the reference. Use "link_design -verbose" in order to see all of the instances of this design which could not be instantiated.

WHAT NEXT

Examine the output of the tool when design files were loaded to see what caused the design to be in a state that cannot instantiate.

LNK-008 (error) Cannot find port '%s' on design '%s', referenced by instance '%s'.

DESCRIPTION

During the link process, an instance in the design could not be resolved because a port on the instance was not found in the design. This indicates a mismatch between the pinout of the instance and the design to which it should have resolved.

For example, if you have only these three instances of an FD1 in a design:

```
  FD1 u1 ( .Q(n1), .CP(clock1), .D(data1));
  FD1 u2 ( .Q(n2), .CP(clock2), .D(data2));
  FD1 u3 ( .Q(n3), .CK(clock3), .D(data3));
```

There is a typo in the third instance, listing "CK" instead of "CP". By default, you will get the LNK-008 message for the first instance only.

```
Error: Cannot find port 'CK' on design 'FD1',
       referenced by instance 'u1'. (LNK-008)
```

This might seem confusing, since that instance does not have a CK port. But for a name-based reference, each instance expects at least the total of all listed ports. To see all instances which cannot be resolved, use the -verbose option to **link_design**:

```
Warning: Cannot resolve instance top/u1 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u2 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u3 (FD1). (LNK-006)
```

The LNK-006 messages are generated in addition to LNK-008.

Examine the `link_path` variable, log messages, and use the **which** command to find out which files were loaded. This could also be due to a typo in the netlist source.

SEE ALSO

link_design (2). **LNK-006** (n).

LNK-009 (error) Reference '%s' to '%s' is missing the following ports:
 %s.

DESCRIPTION

The linker tried to resolve a reference which had the correct number of ports, but was unable to match the ports on the reference to those on the target design or library cell. This is an indication of a mismatch between the library and the netlist.

WHAT NEXT

Verify that the library and netlist are in sync.

LNK-010 (error) Too few ports on instance '%s' of '%s' in '%s'.

DESCRIPTION

The specified reference to a design or library cell does not have enough ports. This indicates a mismatch between the library and the netlist.

WHAT NEXT

Make sure the library is correct. Then, verify that the netlist is referencing the correct cell.

LNK-011 (error) Too many ports on instance '%s' of '%s' in '%s'.

DESCRIPTION

The specified reference to a design or library cell has too many ports. This usually
indicates a mismatch between the library and the netlist. It can also indicate that
there are multiple conflicting references to the same library cell or black box. One
such conflict is two references with different pin counts.

WHAT NEXT

This error will cause the link to fail. Make sure the library is correct. Then,
verify that the netlist is referencing the correct cell.
If this occurs during black box creation, you would see additional messages, for
example:

Error: Too many ports on instance 'u1' of '*SELECT_OP' in 'd1'. (LNK-011)

The first instance of *SELECT_OP for which a black box was created had fewer pins
than this reference. This often happens with generic logic. Other than GTECH,
PrimeTime does not support generic logic. In this case, the solution is to remove
the design containing the generic logic from the link path, or add a wrapper design
which creates a black box at a higher level.

LNK-012 (error) Width mismatch on port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker matched a bused port on an instance with a bused port on a library cell,
but bus width is different between the two. This could indicate an incorrect library
or a netlist which is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-013 (error) Could not resolve %s port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker could not find a port (bused or not) on an instance while resolving a

reference with a target library cell. This could indicate an incorrect library or a
netlist which is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-014 (error) Could not resolve direction of port '%s' of reference to '%s' in '%s'.

DESCRIPTION

The linker matched a port on an instance with a port on a library cell, but the
directions do not match. This might indicate an incorrect library or a netlist which
is out of date with the library.

WHAT NEXT

Verify that your source is in sync with the library.

LNK-015 (Warning) Could not swap '%s' ('%s') with '%s'%s.

DESCRIPTION

You tried to swap a cell with a new design or lib cell, and this action failed.
Additional information might be included with this message and previous messages.

WHAT NEXT

Action based on reasons given in message text.

LNK-016 (Information) %s failed due to previous errors.

DESCRIPTION

This is a summary message indicating that the given action was not accomplished.

WHAT NEXT

Action based on reasons given in text of previous messages.

LNK-018 (Error) Cannot swap cells; design is not linked.

DESCRIPTION

The current design is either unlinked or partially linked. Swapping a cell for a new library cell or design can only be done in the context of a linked design.

WHAT NEXT

Link the current design, then retry your swap operation.

LNK-019 (Error) Can only swap in a single target object.

DESCRIPTION

The specification for the design or library cell to **swap_cell** resulted in more than one object. Either you specified a list or used a collection that matched multiple objects.

WHAT NEXT

Narrow the search parameters so only a single object is selected.

LNK-020 (Error) Cannot swap in '%s': it is the current design.

DESCRIPTION

The design you specified is the current design and you cannot instantiate a design within itself.

WHAT NEXT

Select a different design.

LNK-021 (Information) Previous messages occurred while trying to do:

’%s’.

DESCRIPTION

While linking the design, an attempt was made to transfer some information from the
source design files which you read to the final linked design and some diagnostics
occurred. This message shows you what was attempted which caused the diagnostics.

WHAT NEXT

Action based on the messages referenced.

LNK-023 (error) Recursive hierarchy detected in design ’%s’: %s.

DESCRIPTION

The linker detected recursive hierarchy in the design that is being linked. This is
a design error. The message will list the designs that create the recursion.

For example, if design A has an instance of B and design B has an instance of A,
that is a recursive loop.

WHAT NEXT

Remove the recursion, reread the designs, and relink.

LNK-024 (Warning) All timing information (backannotation, exceptions, etc.) is being removed from design ’%s’. User-created annotations must be restored after relinking this design.

DESCRIPTION

When a design is linked and there is another design currently linked, the current
design is unlinked before the new design is linked. When this occurs, all
annotations on the currently linked design are removed. This includes any timing
information loaded from DB or added by user commands.

The next time the design is linked, information originally loaded from DB will be
automatically restored. For example, clocks stored in the DB which was read in to

PrimeTime will be recreated on the design. However, any information which was added to the design after the link can only be restored if it was saved with **write_script**. For example, if you used the create_clock command to create a new clock, this clock will not be automatically restored.

WHAT NEXT

To save the state of the design before linking a new design, use the write_script command. Then, after relinking the design, source the script which was written to restore all annotations.

, , ,

LNK-025 (information) Link interrupted. Unlinking design: please wait...

DESCRIPTION

You entered a control-C to interrupt the link before it completed. The design which was being linked will be unlinked.

WHAT NEXT

No action.

LNK-026 (warning) min library '%s' found in link_path.

DESCRIPTION

During the link process, a library has been found in the link path that is in use as a min library. Only the max library is used in the link path for min/max analysis with the **set_min_library** command.

WHAT NEXT

Remove the min library from the value of the **link_path** variable, and ensure that the max library is in the link path.

SEE ALSO

set_min_library (2), **link_path** (3).

LNK-028 (Warning) unable to apply some DB constraints because they were
cached in file '%s'
and that file no longer exists.

DESCRIPTION

While linking the design, an attempt was made to transfer some information from the source design DB files which you read to the final linked design. When that information (constraints, exceptions, and so on) is large, it is cached to disk after an initial link. On a subsequent link, that data will be reloaded and reapplied. If the file has been deleted between the first link and the subsequent link, this message is issued.

WHAT NEXT

Examine why the file may have been deleted. Equally, examine why you are linking a second time. Usually this is a bug in a script, for example, executing a command which does an implicit link, followed by an explicit link. It is usually best to pick one style: implicit or explicit. Synopsys recommends that you build the design explicitly, that is, read the files that you want, then issue a link_design command.

SEE ALSO

`link_design(2).`

LNK-030 (information) Using '%s' as link path for instance '%s'

DESCRIPTION

This informational message tells you that the **link_path_per_instance** variable has been used, and an a match has been found for an instance. The link path and the instance name are shown in the message. The link path should match your setting in **link_path_per_instance** for the instance.

This message is displayed only if the *-verbose* option is used with **link_design**.

WHAT NEXT

No action required. This is strictly for your information.

SEE ALSO

link_design (2). **link_path_per_instance** (3).

LNK-031 (warning) Replacing link path for '%s' with '%s'

DESCRIPTION

This message warns you that you have the same instance listed multiple times in the setting for the **link_path_per_instance** variable. For example, here the instance *i2* is listed twice.

```
set link_path_per_instance [list
    [list i2 "* lib1.db"]
    [list i2 "* lib2.db"]
    [list i2/u1/u1 "* lib1.db"]]
```

WHAT NEXT

Examine the setting for the **link_path_per_instance** variable, and ensure that only one valid link path exists per instance.

SEE ALSO

link_path_per_instance (3).

LNK-033 (error) Incorrect format for link_path_per_instance: %s

DESCRIPTION

This message tells you that the format for the **link_path_per_instance** variable is incorrect. Various things can be wrong. The variable must be a list. Each element is itself a list of exactly two elements, where the first sub-element is a list of instances, and the second is a valid link path. The content of the message will isolate where the problem exists.

WHAT NEXT

Correct the setting for the **link_path_per_instance** variable.

SEE ALSO

link_path_per_instance (3).

LNK-034 (information) Removing %d unneeded designs.....

DESCRIPTION

This message tells you that a number of designs are being deleted following a successful link. This message is issued when you issue **link_design** command without using the **-keep_sub_designs** option or issued a command that performed an implicit link.

WHAT NEXT

No action is required. This is just information only.

SEE ALSO

link_design (2).

MC-001 (warning) Changing the multi_core_enable_analysis variable from
TRUE to FALSE triggers the update to be completed at the master.

DESCRIPTION

When the **multi_core_enable_analysis** variable is changed from TRUE to FALSE and the design has been initially timed, a full timing update is completed at the master. This ensures that all subsequent analysis is completed in the single-core analysis mode.

WHAT NEXT

If you want to perform multicore analysis, set the **multi_core_enable_analysis** variable to TRUE. However, this requires a full timing update.

MC-002 (warning) Changing the multi_core_enable_analysis variable from
FALSE to TRUE triggers a full update.

DESCRIPTION

When the **multi_core_enable_analysis** variable is changed from FALSE to TRUE and the design has been initially timed, a full timing update is triggered. This ensures that all subsequent analysis is performed in the multicore analysis mode.

WHAT NEXT

If you want to perform a single-core analysis, set the **multi_core_enable_analysis** variable to FALSE. However, this requires a full timing update.

MC-004 (information) Changing variable '%s' from '%s' to '%s'.

DESCRIPTION

```
Certain variables are not compatible with multicore analysis. These unsupported
variables must be changed before the analysis can begin.
```

MC-007 (Warning) The multi_core_enable_analysis variable has been
automatically set to FALSE as the following is not supported - '%s'.
The update will now complete in single-core analysis mode and no partitions
will be launched.

DESCRIPTION

```
You have attempted to perform a distributed timing update, but PrimeTime has
detected a command or flow that is not supported in distributed mode. All partition
processes will be terminated and your update will now complete as a single-core
update.
```

WHAT NEXT

```
You can continue with your timing analysis. All commands will execute in single-core
analysis mode. If you want to return to multicore analysis mode, set the
multi_core_enable_analysis variable to TRUE. (This triggers a full update).
```

MC-008 (information) Collecting timing information from
partitions to support single-core analysis functional capabilities.

DESCRIPTION

```
Data calculated during the distributed update_timing is being sent to the master to
enable execution of commands in a single-core analysis context.
```

MC-009 (warning) restore_session failed: The number of hosts

online
 is '%d' but the number of hosts required is '%d'.

DESCRIPTION

```
While in multicore analysis mode, the restore_session command failed because the
number of hosts online was less than the number of hosts required.
```

WHAT NEXT

```
You need to add the same number of hosts that were in use when the session was
saved. Alternatively, edit the 'multicore_compute_resources.tcl' file in the saved
session directory to add more hosts.
```

MC-010 (information) Number of hosts added = '%d'.

DESCRIPTION

```
This information message displays the number of hosts that were added while
restoring the session in multicore analysis mode.
```

MC-011 (warning) restore_session failed: The number of required hosts
 is '%d' but the number of licensed hosts is '%d'.

DESCRIPTION

```
While in multicore analysis mode, the restore_session command failed because the
number of required hosts is greater than the number of licensed hosts.
```

WHAT NEXT

```
Add more licensed hosts to anable the restore_session command to succesfully
complete.
```

MC-012 (warning) In the multicore analysis flow, '%s' for the command
 '%s' is not supported in distributed mode. The command will

now
 execute in the single-core analysis context.

DESCRIPTION

In multicore analysis mode, several reporting commands can be performed in
distributed mode. This implies that the analysis is done at the partitions and the
results are collated and saved at the master. Some options of these commands are not
supported in distributed mode. When this situation arises, the partition
communicates its timing data back to the master, if this has not already occurred,
and then the reporting commands are executed at the master.

WHAT NEXT

Expect the reporting command to take longer, particularly if timing data must be
collected and communicated back to the master.

MC-013 (information) The multi_core_enable_analysis variable has been
 changed from %s to %s.

DESCRIPTION

This informational message is displayed if **restore_session** is issued and the
multi_core_enable_analysis variable switches in value as a result of the restored
session having a different value for the **multi_core_enable_analysis** variable
compared to the session from which the **restore_session** command was issued.

WHAT NEXT

No action necessary.

MC-014 (warning) The number of required hosts is '%d' but the number of licensed hosts is '%d'.

DESCRIPTION

The number of licensed hosts is less than the number of specified hosts online.

WHAT NEXT

You can continue with your timing analysis. In future runs, ensure that sufficient
licensing resources are available for the specified compute resources.

MC-015 (error) The PrimeTime master process detected PrimeTime
 slave instances that encountered fatal errors. The master
 and all slave processes will now terminate.

DESCRIPTION

While executing commands one or more PrimeTime slave processes encountered fatal
errors requiring them to exit. In this situation, the master cannot proceed and
terminates the entire session.

WHAT NEXT

MC-016 (fatal) Internal system error in partition '%s'

DESCRIPTION

While executing commands in multi_core analysis the partition indicated experienced
a critical internal error causing it to terminate.

WHAT NEXT

Re-run the analysis.

MC-017 (Warning) Execution of '%s' is being skipped. Reason: %s.

DESCRIPTION

While executing commands in multicore analysis, an unsupported command was
encountered. This command has not been executed, instead it was skipped.

WHAT NEXT

To enable the command to execute in PrimeTime, set the **multi_core_skip_unsupported** variable to *false*. This causes PrimeTime to revert from the multicore analysis flow to the single-core analysis flow when it encounters an unsupported command. You can then execute the command in the single-core analysis flow.

MC-018 (Warning) Commands and/or variables were skipped as they are unsupported in multicore analysis.

DESCRIPTION

While performing a multicore analysis, PrimeTime encountered unsupported commands and/or variables. By default, PrimeTime skips unsupported commands and resets unsupported variables to their default values.

WHAT NEXT

To prevent PrimeTime from skipping unsupported commands or resetting unsupported variables, set the **multi_core_skip_unsupported** variable to *false*. This causes PrimeTime to revert from the multicore analysis flow to the single-core analysis flow when it encounters an unsupported command and/or variable. You can then execute the command/use the variable in the single-core analysis flow.

MC-019 (Warning) The variable '%s' is being changed from '%s' to '%s'.

DESCRIPTION

PrimeTime has encountered a variable that is unsupported in multicore analysis. The value of this variable has been changed so the multicore analysis may proceed.

WHAT NEXT

To prevent PrimeTime from changing the value of the variable, set the **multi_core_skip_unsupported** variable to *false*. This causes PrimeTime to revert from the multicore analysis flow to the single-core analysis flow when it encounters an unsupported variable.

MDBG-2 (error) Did not specify either the -from or -to option.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and did not specify a **-from** option *from_object* value or a **-to** option *to_object* value. For the **-from** option, you must specify one of the following valid values: **-fall_from**, **-from**, or **-rise_from**. For the **-to** option, you must specify one of the following valid values: **-fall_to**, **-rise_to**, or **-to**.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying the missing option.

SEE ALSO

report_etm_arc (2).

MDBG-3 (error)Specified invalid 'from' object. No port/clock matched.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and did not specify a valid port/clock as the value for the **-from**, **-rise_from**, or **-fall_from** option.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying a valid startpoint (port/clock).

SEE ALSO

report_etm_arc (2).

MDBG-4 (error) Specified invalid 'to' object. No port/clock

matched.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and did not specify a valid port/clock as the value for the **-to**, **-rise_to**, or **-fall_to** option.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying a valid endpoint (port/clock).

SEE ALSO

report_etm_arc (2).

MDBG-5 (error) Specified invalid value for -arc_type option.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified an invalid *arc_type* value for the **-arc_type** option. Valid values are: **clock_gating_hold**, **clock_gating_setup**, **hold**, **max_combo_delay**, **max_seq_delay**, **min_seq_delay**, **min_combo_delay**, **recovery**, **removal**, and **setup**.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying a valid *arc_type* value for the **-arc_type** option.

SEE ALSO

report_etm_arc (2).

MDBG-6 (warning) Cannot open the file '%s' for the ETM report.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified an invalid file name for the *er_file_name* value of the **-etm_report** option.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying a valid file name for the *er_file_name* value of the **-etm_report** option.

SEE ALSO

report_etm_arc (2).

MDBG-7 (warning) Cannot open the file '%s' for the netlist report.

DESCRIPTION

You received this message because you executed the **report_etm_arc** command and specified an invalid file name for the *nr_file_name* value of the **-netlist_report** option.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying a valid file name for the *nr_file_name* value of the **-netlist_report** option.

SEE ALSO

report_etm_arc (2).

MDBG-8 (error) Cannot specify more than one object to -from and -to options.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified more than one value for either the *from_object* value of the **-from** option or the *to_object* value of the**-to** option.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying one object for both the **-from** and the**-to** options. You can issue this command more than once to get multiple arcs.

MDBG-9 (error) Specified invalid path_name '%s' for the -include option.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified an invalid *path_type_list* value for the **-include** option. The only valid values are **clock_path** and **netlist_path**.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying one (or both) of the valid *path_type_list* values for the **-include** option.

SEE ALSO

`report_etm_arc` (2).

MDBG-10 (error) Specified invalid options for a constraint arc.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified a value for the **-arc_type** option that does not agree with the **-from** option *from_object* value or the **-to** option *to_object* value. Specify a port for the **-from** option and a clock for the **-to** option to obtain the constraint arc.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying valid values for the **-from** and **-to** options.

SEE ALSO

`report_etm_arc` (2).

MDBG-11 (error) Specified invalid options for a sequential arc.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified an argument for the **-arc_type** option that does not agree with the **-from** option *from_object* value or the **-to** option *to_object* value. Specify a clock for the **-from** option and a port for the **-to** option to obtain the sequential arc.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying valid values for the **-from** and **-to** options.

SEE ALSO

report_etm_arc (2).

MDBG-12 (error) Specified invalid options for a combinational arc.

DESCRIPTION

You receive this message because you executed the **report_etm_arc** command and specified an argument for the **-arc_type** option that does not agree with the **-from** option *from_object* value or the **-to** option *to_object* value. Specify a port for the **-from** option and a port for the **-to** option to obtain the combinational arc.

WHAT NEXT

Reexecute the **report_etm_arc** command, specifying valid options for the **-from** and **-to** options.

SEE ALSO

report_etm_arc (2).

MEXT

MEXT-1 (error) Design '%s' does not have any connections between
 cells. Model extraction is not allowed on such designs.

DESCRIPTION

You received this message because you executed the **extract_model** command but the
extractor detects that the netlist to be extracted does not have any effective net
connectivities among the cells that are instantiated from the library.

WHAT NEXT

Please inspect the netlist and make sure there are effective connectivities among
cell instances. This is to avoid improperly exposing timing related information in
the libraries you are using.

MEXT-2 (warning) Variable 'extract_model_use_conservative_current_slew'
 is set to 'true' while design is in 'worst_arrival' slew propagation mode.
The variable is not effective in this mode and therefore ignored in extraction.

DESCRIPTION

You received this message because you executed the **extract_model** command with
variable 'extract_model_use_conservative_current_slew' set to 'true' while the
design is in 'worst_arrival' slew propagation mode. The 'worst_arrival' slew
propagation mode makes this model extraction variable not effective and therefore
its value is ignored and it will have no impact on model extraction.

WHAT NEXT

Please decide what model you want. If you want the model to propagate the worst
conservative slew calculated from the context slews set on input ports, put the
design in 'worst_slew' mode and set the model extraction variable to 'true'. If you
want the model to propagate real path specific slew regardless of any context slews
propagated from other paths, set the model extraction variable to 'false'. This

makes the model match the netlist better if the timing report of the netlist is
performed in 'worst_arrival' slew propagation mode.

MEXT-03 (error) The value '%s' set for the modeling environment variable '%s' is illegal.

DESCRIPTION

You receive this message because the value you set for the specified variable is
illegal. If it is for number of table index points, it has to be a positive integer;
if it is for the maximum limit of the table index, it has to be a non-negative
floating point number.

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model
extraction.

MEXT-3 (warning) The %s '%s' timing arc extracted from pin '%s' to
  pin '%s' has only '%s' tables.
  They are copied to make the missing '%s' tables.

DESCRIPTION

You received this message because the sequential paths contribute to the specified
timing arc only have the specified transition applicable. The resulting timing arc
is half-unate. It could be caused by disable timing, false paths or cells with half-
unate timing arcs in the path. Because there are tools, such as LibraryCompiler,
etc. which do not accept half unate sequential arcs. The extracted model has copied
the existing half to create the missing half.

WHAT NEXT

Please verify the path setup and confirm that the arcs are what you expected.

MEXT-4 (warning) Detected max_transition violation in the

circuit to be extracted.

DESCRIPTION

You receive this message if the circuit you are currently extracting has max_transition violations. The resulting model can do max_transition checking only at its boundaries; therefore, the model will be inaccurate because it does not reproduce the errant behavior.

The current problem might be caused by an unrealistically low value of the maximum transition time. Many ASIC libraries supply a **default_max_transition** or a **max_transition** attribute on the gate outputs. If a gate in the design does not have a **max_transition** attribute in its library definition, the **extract_model** command uses the value of the **extract_model_transition_limit** variable; the default is 5.0.

WHAT NEXT

Correct the violations using timing analysis and synthesis on the original circuit, or reset the maximum transition time to a higher value. Then reexecute **extract_model**.

MEXT-5 (warning) Some pins do not have clock defined. One example is pin '%s'. Paths to and from such pins are ignored. Run check_timing for details.

DESCRIPTION

You receive this message because the **extract_model** command did not find a clock for some pins. Transparent latches and flip-flops in a design you want to extract must have a clock defined for them. This message warns you that **extract_model** is ignoring all paths to and from such pins that have no clock.

WHAT NEXT

If it is acceptable to you for **extract_model** to ignore paths to and from such pins, no action is required on your part. Otherwise, use the **create_clock** command to define all design clocks on the pins or clock networks. Then reexecute **extract_model**.

In the future, to prevent receiving this message, first execute the **check_timing** command to detect any clock pins that are missing clocks. Create the missing clocks, then execute **extract_model**.

MEXT-6 (warning) Environment variable '%s' has not been set during this
session. Using default value '%s'.

DESCRIPTION

```
You receive this message if the specified environment variable is not set. This
message informs you that the default value is being used.
```

WHAT NEXT

```
If it is acceptable to you for the specified default value to be used for this
environment variable, no action is required on your part. Otherwise, set this
variable to one of its allowed values using the command set variable value. If you
want to set the value only for the current session, you can enter this command at
the pt_shell prompt or place it in a script file, which you then execute. If you
want the variable value to persist, you can enter it in your .synopsys_pt.setup
file.
```

MEXT-7 (warning) Environment variable 'extract_model_tolerance' has a value
that is too low. Using minimum value '%s'.

DESCRIPTION

```
You receive this message if the extract_model_tolerance variable is set with a value
less than 0.02. The behavior of the extractor degrades sharply when tolerances are
below these values. This message informs you that the specified minimum value is
being used instead.
```

WHAT NEXT

```
If it is acceptable to you for the extract_model command to use the specified
minimum value, no action is required on your part. Otherwise, set the
extract_model_tolerance variable to a value greater than 0.02. Then reexecute
extract_model.
```

MEXT-8 (warning) Environment variable 'extract_model_tolerance' has a value that is unreasonably high.

Using maximum value '%s'.

DESCRIPTION

You receive this message if the **extract_model_tolerance** variable is set with a value greater than .50. There is little benefit in extractor speed or output file size beyond 50% tolerance. This message informs you that the specified maximum value is being used instead.

WHAT NEXT

If it is acceptable to you for the **extract_model** command to use the specified maximum value, no action is required on your part. Otherwise, set the **extract_model_tolerance** variable to a value less than 0.50. Then reexecute **extract_model**.

MEXT-10 (error) Unknown format '%s' for the -format option.

DESCRIPTION

You received this message because you executed the **extract_model** command and specified an argument for the **-format** option that was neither *db* or *lib*. These are the only valid arguments for the **-format** option; you can use one or both.

WHAT NEXT

Reexecute **extract_model** and specify one or both of **-format db** or **-format lib**.

MEXT-11 (error) Invalid operating condition '%s' specified.

DESCRIPTION

You receive this message if the operating condition you specified using **extract_model -operating_conditions** cannot be found in any library. The operating condition must exist in some library that is in the **link_path**.

This error could be caused by a spelling error or typo, or by the appropriate library not being in the **link_path**.

WHAT NEXT

First, examine the libraries, design files, and library files listed in the **link_path** variable, to ensure that the intended operating condition appears in one of them. (Use the **report_lib** command to list operating conditions defined in a

single library.) If so, note the correct spelling. If not, add the appropriate library to the **link_path**. Next, reexecute **extract_model -operating_conditions** using the correct operating condition name.

MEXT-12 (warning) Pin '%s' is an internal start or end point. Ignoring paths to and from this pin.

DESCRIPTION

You receive this message if the **extract_model** command finds a pin that is an external start or end point, indicating that the pin is participating in a timing exception or has an input delay specified on it. Because of an extracted model (ETM) limitation, **extract_model** does not support such qualifiers.

WHAT NEXT

Remove all **max_delay**, **min_delay**, and external delays from the pin. Then reexecute **extract_model**.

MEXT-16 (warning) No master clock exists for generated clock '%s'.

DESCRIPTION

You receive this message because the **extract_model** command found a generated clock without a master clock defined.

WHAT NEXT

If it is acceptable to you for **extract_model** to ignore paths to and from the named generated clock, no action is required on your part. Otherwise, use the **report_clock** command to see the source pin that needs a clock defined on it.

MEXT-17 (warning) Zero (or negative) max capacitance on library pin.
  Assuming %f for library cell %s output %s.

DESCRIPTION

You receive this message if the **extract_model** command finds a 0.0 or negative

maximum capacitance specified on a library cell pin. You cannot have a zero or
negative maximum capacitive loading for a library output pin. This message warns you
that **extract_model** is assuming the specified value for max capacitance instead.

Many ASIC libraries supply a maximum allowable capacitance on gate outputs. If a
gate in the design does not have a **max_capacitance** attribute in its library
definition, the **extract_model** command uses the value of the PrimeTime
extract_model_capacitance_limit variable. The default is 64.

WHAT NEXT

Correct the library to specify a maximum capacitance for all arcs. Or, use the
PrimeTime variable **extract_model_capacitance_limit** to set a maximum allowable
capacitance for all gate outputs in the design. Then reexecute **extract_model**.

MEXT-19 (information) Clock '%s' has multiple sources.

DESCRIPTION

You receive this message to inform you that the specified clock has multiple
sources, potentially causing longer runtime and higher memory use than a clock with
a single source. Timing arcs are extracted from all clock sources, so a larger model
will result because of an increase in the number of timing arcs.

WHAT NEXT

Consider redeclaring your clocks with a single source pin per clock. For information
about the implications of delaring clocks with multiple sources, see the *PrimeTime
Modeling User Guide*.

MEXT-20 (warning) Clock '%s'
has source on hierachical pin '%s'.
Consider moving to: %s

DESCRIPTION

The specified clock has a source on the specified hierarchical pin. This message
warns you that PrimeTime might not be able to extract a propagated delay for this
clock.

WHAT NEXT

If it is acceptable to you for PrimeTime not to extract a propagated delay for the
clock, no action is required on your part. Otherwise, to avoid ambiguity of design

intent, move the clock source back to an output pin of the physical driver circuit, then reexecute **extract_model**. The list of possible driver pins to use are those that drive the net containing the hierarchical pin.

MEXT-21 (error) Cannot compute generated clock propagated delay.
 Cannot compute delay from pin '%s'
 to hierarchical pin '%s'.

DESCRIPTION

You receive this message if a clock pin has a source specified on a hierarchical pin of a net containing RC data. The model extractor cannot compute the propagated delay to this logical node on the net. This message is related to the MEXT-20 warning message.

WHAT NEXT

Move clock sources back to output pins of the physical clock divider circuit to avoid delays to non-physical pins, then reexecute **extract_model**. Warning MEXT-20 might have been issued previously with a list of driver pins on the net with the hierarchical pin.

MEXT-22 (warning) A path from generated clock '%s' back to its master clock is ignored because its length exceeded %d arcs.

DESCRIPTION

A path from the specified generated clock back to the master clock was found to exceed the specified number of arcs. This message warns you that the path(s) is being ignored. The propagated delay to the generated clock will include only the paths shorter than this length. Thus, the propagated delay might not represent the correct min or max path value.

WHAT NEXT

If it is acceptable to you for the path(s) to be ignored, no action is required on your part. Otherwise, check the design topology for excessively long (false) paths from a master clock to a generated clock, and make changes if necessary. Then reexecute **extract_model**.

MEXT-23 (warning) No net is connected to generated clock '%s' %s pin '%s'.

DESCRIPTION

The specified generated clock has no net connected to either the master clock pin or a clock source pin, as the message indicates. Generated clocks must have net connections even if the clocks are not set to be propagated.

WHAT NEXT

Review the circuit to ensure that all clock specification points are properly connected within the design. Make necessary corrections, then reexecute **extract_model**.

MEXT-24 (error) Internal error found while creating a generated clock.

DESCRIPTION

You receive this message if an internal error is detected during the creation of a generated clock.

WHAT NEXT

Execute the **report_clocks** command on both the original netlist and the extracted model. Verify that the period and edges of the generated clocks in the model match those in the original netlist.

MEXT-28 (warning) More than %d boundary nets have detailed parasitics and multiple drivers or load pins.

DESCRIPTION

This message is issued to limit the number of MEXT-27 messages you receive, and warns you of the total number of boundary nets that have detailed parasitics and multiple drivers or load pins.

Model extraction sometimes combines the RC characteristics of one fanout or fanin with the constraint characteristics of another. This can lead to an inaccurate model.

If possible, buffer the net, then reexecute **extract_model**. Always verify the model
if you receive this warning.

MEXT-29 (error) ETM Limitation - Arcs between operating conditions do not match.
No model will be written. The first mismatch is from '%s' to '%s'.

DESCRIPTION

You receive this message if **extract_model** cannot write a model because the arcs
between the various operating conditions do not match. For correct DB format, arcs
between the different operating conditions of the same model must match exactly.

This error could be caused by a difference in naming of internal nodes, or by the
merging of arcs being different between operating conditions.

WHAT NEXT

Write the models for each condition to separate files, or use an interface logic
model (ILM) instead of an extracted model (ETM).

MEXT-30 (warning) ETM Limitation - Option '-operating_conditions' is not recommended.
The extracted models may not be able to be combined into one db file.

DESCRIPTION

You receive this message if you issue the **extract_model** command with the **-operating_conditions** option. Using this option is not recommended, because there
might be a mismatch between extracted arcs for various operating conditions of the
same model. DB format requires that the arcs match exactly between the different
operating conditions of the same model. If the arcs do not match, an error message
is generated and the model is not written.

Mismatch errors could be caused by a difference in naming of internal nodes, or by
the merging of arcs differing between operating conditions.

WHAT NEXT

Write the models for each condition to separate files or use an interface logic model (ILM) instead of an extracted model (ETM).

MEXT-35 (warning) ETM Limitation - -remove_internal_arcs option
is not recommended.

DESCRIPTION

You receive this message if you issued the **extract_model** command with the **-remove_internal_arcs** option. This option removes all internal pins from the extracted model without moving the constraints or generated clocks to external pins, and its use is not currently recommended.

WHAT NEXT

Reexecute **extract_model** without the **-remove_internal_arcs** option.

MEXT-36 (warning) A core-cell stamp model will be written.
The stamp model must be used with a wrapper design.

DESCRIPTION

The stamp model written without using the **-library_cell** option models only the core of the design being extracted. Boundary nets are modeled in a separate wrapper model. This default behavior was different in previous releases.

WHAT NEXT

If you want a stamp model that includes the boundary nets, rerun the **extract_model** with the **-library_cell** option.

SEE ALSO

extract_model (2).

MEXT-37 (error) extract_model -parasitic_format option has

unknown format '%s'.

DESCRIPTION

The valid formats for the `-parasitic_format` option of the `extract_model` command are `spef`, `dspf`, and `binary`. Any other option is invalid.

WHAT NEXT

Use only the `spef`, `dspf`, and `binary` formats.

SEE ALSO

`extract_model` (2).

MEXT-38 (error) -parasitic_format cannot be used with the -library_cell option.

DESCRIPTION

The `-parasitic_format` option controls the format for boundary net parasitics. When you use the `-library-cell` option, the boundary nets are included in the model and no parasitics can be written for them.

WHAT NEXT

Remove either the `-parasitic_format` option or the `-library-cell` option, and execute the `extract_model` command again.

SEE ALSO

`extract_model` (2).

MEXT-40 (warning) ETM Limitation - the -latch_level option is recommended only
 when you know the latch-borrowing behavior at the interface. Use -context_borrow

instead.

DESCRIPTION

You receive this message if you execute **extract_model** and use the **-latch_level**
option. This option is provided for backward compatibility and is not recommended
for general use.

WHAT NEXT

Reexecute the **extract_model** command and use the **-context_borrow** option instead of **-
latch_level**.

MEXT-43 (information) When tracing paths from %s '%s', borrowing level-sensitive
  latches ('%s') were traversed through.

DESCRIPTION

You receive this message to inform you that the tracing for model extraction started
from the indicated port/clock has gone through some borrowing level-sensitive
latches.

WHAT NEXT

If you observe timing discrepancies, this message might be helpful in debugging.

MEXT-44 (information) Sequential arc '%s' is added only as an '%s' transition.
  Transition ('%s') is being copied from the existing transition.

DESCRIPTION

You receive this message to inform you that in the process of extracting the named
sequential arc, either the rising output or falling output is not a valid path.
PrimeTime does not support this type of arc. The invalid transition is being added
to the model by giving it the same values as the valid transition.

You can set false paths when using this model to avoid using the invalid transition.

MEXT-45 (warning) ETM Limitation - hold value for -arc_types specified without specifying setup value.
Clock gating hold arcs will not be extracted.

DESCRIPTION

You receive this message because you specified **hold**, but not **setup**, among your values for the **-arc_types** option of the **extract_model** command. Clock gating hold arcs will not be extracted without relevant setup arcs. As a result, your model will not include clock gating hold arcs. All other hold arcs will be extracted.

WHAT NEXT

If you want clock gating hold arcs, reissue the **extract_model** command with the **-arc_types** option specifying both setup and hold values.

SEE ALSO

extract_model (2).

MEXT-46 (error) The requested number of delay table points %d does
not fit into the %3.4f to %3.4f index range that is set on, or derived
for, %s %s.

DESCRIPTION

You receive this message because the requested number of delay table points is so big or the min/max bounds for the table index are so tight that the delay table points cannot be reasonably divided into the requested number of pieces. For SI analysis, the transition set on block input ports is used as the maximum transition table point; if the input transition is zero, then this message will result.

Adjust the settings of the PrimeTime environment variables before executing model extraction. For SI analysis, check the transition value on input ports and increase it to the expected maximum value.

MEXT-47 (error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The range is too tight to fit in the requested number of table points.

DESCRIPTION

You receive this message because the requested number of delay table points is so big or the max bound for the table index is so small that it cannot be reasonably divided into the requested number of pieces.

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-48 (error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The product of these two variables %d indicates that the requested size
 of delay tables is bigger than 100.

DESCRIPTION

You receive this message because the requested number of delay table points is too big. The size of delay tables in the extracted model is limited to less than 100 (for example, less than a 10 by 10 table).

WHAT NEXT

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-49 (warning) The model extraction environment variable

%s

is obsolete and has no effect on model extraction.

DESCRIPTION

You received this message because you have set the indicated model extraction
environment variable to some value before you execute the model extraction.

If the vairable warned is 'extract_model_transition_limit', start from the PrimeTime
2002.03 release, this variable is obsolete and replaced by two new variables
"extract_model_data_transition_limit" and "extract_model_clock_transition_limit".

If the variable warned is 'extract_model_core_cell_stamp', start from PrimeTime
2001.08 release, the behavior has changed and the models will always be the same
regardless of output format. The model is totally controlled by the "-library_cell"
option of command **extract_model**.

If the variable warned is 'extract_model_min_delay_threshold', start from PrimeTime
2001.08 release, the variable has been obsolete and all minimum delay and hold
timing arcs are extracted.

WHAT NEXT

Please remove the settings of the old variable and use the new variables to set up
the environment for model extraction if applicable.

MEXT-50 (error) ETM Limitation - The design has multiple clocks on the
same source. Clock '%s' defines multiple clocks on source %s.

DESCRIPTION

You receive this message because you defined multiple clocks on the same source, so
extraction cannot be performed on that design.

WHAT NEXT

Eliminate the definition of multiple clocks on a single source. Do this by removing
all but one clock on the clock source.

SEE ALSO

remove_clock (2).

MEXT-51 (error) ETM Limitation - Path borrowing is not supported for short paths during extraction.

DESCRIPTION

```
You received this message because you set "timing_allow_short_path_borrowing"
variable to TRUE. Path borrowing is not supported for min paths during extraction.
```

WHAT NEXT

```
Set the variable "timing_allow_short_path_borrowing" to FALSE.
```

MEXT-52 (error) ETM Limitation - Timing paths cannot be propagated through unclocked registers during extraction.

DESCRIPTION

```
You received this message because you set
"timing_propagate_through_unclocked_registers" variable to TRUE. Unclocked registers
are not supported during extraction.
```

WHAT NEXT

```
Set the variable "timing_propagate_through_unclocked_registers" to FALSE.
```

MEXT-53 (warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because certain constraints had to be moved to the closing edge of latch. Example: %s.

DESCRIPTION

```
You receive this message because the model extraction process found that the design
has a specific set of non-borrowing latch arrangements where it was necessary to
move the constraint from the opening to the closing edge. Hence, the model arc
embodies a half-a-clock-cycle and, so, is not a context-independent w.r.t clock
frequency.
```

WHAT NEXT

If you observe timing discrepancies at a different clock frequency, this message might be helpful in debugging.

MEXT-54 (warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because some of the MCP exceptions could not be moved to the boundary. Example: %s.

DESCRIPTION

You receive this message because the model extraction process found that the design has a specific set of multi-cycle path exceptions where it was not possible to move the MCP out to boundary. Hence, the model arc embodies the MCP shift and, so, is not a context-independent w.r.t clock frequency.

This means that the ETM arc has had the current clock period subtracted from the arcs effected by this MCP. When validating the module, use the default slack mode. The option -timing_type arc should not be used for write_interface_timing.

WHAT NEXT

Use write_interface_timing -timing_type slack to validate the model. Do not use write_interface_timing -timing_type arc, or the model arc will differ from the netlist arc, my the MCP adjustment value.

If you observe timing discrepancies at a different clock frequency, create a new ETM for the new clock frequency.

MEXT-55 (warning) The -ignore_ports is obsolete.

DESCRIPTION

You receive this message because you have used the -ignore_ports option. This option will reduce the amount of the design that arcs are extracted for, but may in some cases extract some arcs for the ignored ports.

WHAT NEXT

Use the report_etm_arc command to debug the model.

MEXT-56 (warning) Model cannot create a valid noise table for pin %s.

DESCRIPTION

You received this message because the noise immunity table for one or more noise regions of this pin cannot be created. This can occur either because there's no noise immunity table defined for the given region or because the effective capacitance loading of the first level cell(s) or the noise width points is far outside the bounds of its library cell characterization. Only one message is output per extract_model command, so other pins may also be missing one or more noise immunity tables in the model.

WHAT NEXT

If there's no noise immunity table defined for the given noise region, then use set_noise_immunity_curve or set_noise_margin for that region.

If there is a noise immunity table for the given noise region, there are several options: 1. If possible, re-characterize the library to expand the width and capacitance range of the pertinent library cell to include the width/capacitance value used in this design. 2. Use set_load to override the load capacitance of the library cell(s) affecting the pin of interest. 3. Set the variable extract_model_noise_width_points to the same set of widths used for the noise_immunity_table of interest. 4. Use set_noise_immunity_curve or set_noise_margin for the given pin for the problematic region(s).

MEXT-57 (error) The -operating_conditions option can not be used with min_library.

DESCRIPTION

You receive this message because you have used the -operating_conditions option while the -min_library option was used for the set_operating_condition command. The -operating_conditions option to extract_model is obsolete and does not work correctly when the -min_library option to set_operating_condition is used.

WHAT NEXT

Either produce one ETM for bc_wc or on_chip_variation mode, or create one ETM for each desired operating condition by using the set_operating_condition command followed by extract_model.

MEXT-58 (warning) The -operating_conditions option is

obsolete.

DESCRIPTION

You receive this message because you have used the -operating_conditions option. This option is being phased out because it can not support all the functionality of set_operating_condition. Today, it will produce a model for each of the operating conditions listed in single analysis mode. It can not support min_library or multi-voltage options.

WHAT NEXT

Convert your script to call extract_model once for each desired operating condition. Use set_operating_condition and related commands to set the operating conditions between each call to extract_model.

MEXT-59 (warning) The -update option is obsolete.

DESCRIPTION

You receive this message because you have used the -update option. This option is being phased out because support for the scaled cell model it produces is being phased out.

WHAT NEXT

Create separate models for each operating condition.

MEXT-60 (warning) Noise features are not supported for the format '%s'

DESCRIPTION

You received this message because you executed the **extract_model** command and specified an option **-noise** with the **-format** option that included an argument other than *lib*. Noise features are not supported in any format other than *lib*, so only the timing model will be written in those formats.

WHAT NEXT

If the *lib* format was not used, re-execute **extract_model** including the *lib* argument with the **-format** option.

MEXT-61 (warning) Model does not support noise steady state current tables.

DESCRIPTION

You received this message because some cell(s) in the design that reach an output port contain steady state current tables for noise analysis. This feature is not supported yet. Steady-state resistance will be used if it's available either in the cell library or added via user-defined commands.

WHAT NEXT

Either re-characterize the affected cell libraries with steady state resistance or set steady-state resistance via noise commands on the output pins of interest.

MEXT-62 (warning) Model cannot create a valid noise I-V curve for pin %s.

DESCRIPTION

You received this message because the steady-state current table (i.e., I-V curve) for one or more noise regions of this pin cannot be created. This may occur because the voltage bounds or number of points need to be adjusted. Only one message is output per extract_model command, so other pins may also be missing one or more noise steady-state current tables in the model.

WHAT NEXT

Use the extract_model variables for noise I-V tables to adjust the number of points or the range of voltages.

MEXT-63 (warning) No input noise defined on port %s.

DESCRIPTION

You received this message because there was no positive input noise defined on the specified input port. It is assumed that all input ports are set to their worst-case input noise level in order to ensure a conservative noise model. Only one message is output per extract_model command, so other input ports may also have no input noise defined.

Use set_input_noise to define an input noise for the specified port.

MEXT-64 (warning) Conflicting clock sense at model pin: %s

DESCRIPTION

You received this message because a pulse clock sense propagates the model pin in the message, but there is a conflicting clock sense that also propagates to this pin. No pulse_clock attribute was added to the model at this pin.

WHAT NEXT

In using the model add generated clocks to model the different pulse clock generators internal to this model.

MEXT-65 (information) Found logic constant value '%s' at output boundary pin/port '%s' due to propagation of case analysis value.

DESCRIPTION

You receive this message to inform you that model extractor detected the specified logic constant has propagated to the output boundary of the block due to certain case analysis settings for the block.

WHAT NEXT

Some tools treat logic constant values differently depending on the values are caused by user set case analysis or intrinsic functional constant of the circuit. By default, ETM writes out .lib and .db files the resulting logic constants from both cases as 'function' attributes for relevant pins. If this behavior is not desired, you can optionally use variable **extract_model_write_case_values_to_constraint_file** to write the user case analysis caused constant values to the ETM constraint files. Note logic value due to functional constant propagation is always written in the .lib and .db ETM files as "function" attribute for pin.

MKW

MKW-001 (error) Could not open Milkyway library %s.

DESCRIPTION

```
The specified Milkyway library could not be opened.
```

WHAT NEXT

```
Check the location of Milkyway library and reissue the command.
```

MKW-002 (error) Could not open Milkyway CEL view file %s.

DESCRIPTION

```
The specified Milkyway library could be opened but the given CEL view file could not
be opened.
```

WHAT NEXT

```
Check the name of the file name and reissue the command.
```

MKW-003 (error) Could not get the top level cell instance from the Milkyway CEL.

DESCRIPTION

```
Something is wrong in the Milkyway CEL database. The command will be aborted.
```

WHAT NEXT

```
Check the name of the Milkyway library and the name of CEL file and reissue the
command.
```

MKW-004 (warning) Could not resolve library cell '%s'. Any non-

physical instances will be black boxes.

DESCRIPTION

A library cell exists in the Milkyway database that could not be located in the logical technology libraries. All the non-physical instances of this library cell will be created as black boxes.

WHAT NEXT

Check link_path, search_path variables and the name of Milkyway library and the name of CEL file and reissue the command.

MKW-005 (warning) Resolved library cell '%s' has greater number of pins in logical library.

DESCRIPTION

A library cell exists in the Milkyway database that was resolved successfully to a library cell in logical library. Usually, it happens that the number of pins in Milkyway database are greater than the number of pins in logical library due to the presence of physical pins. However in this particular case, the library cell in the logical library has more number of pins than the library cell in Milkyway database.

WHAT NEXT

No action required but please check the link_path and search_path variables.

MKW-006 (information) Creating black box for cell '%s'.

DESCRIPTION

The library cell corresponding to the given cell could not be resolved and hence a black box is being created.

WHAT NEXT

No action required but please check the link_path and search_path variables.

MKW-007 (warning) Found a hierarchical library cell pin %s with

invalid direction for library cell %s.

DESCRIPTION

```
The MW database has an invalid direction for the given library cell pin.
```

WHAT NEXT

```
No action required but please check the validity of MW CEL view.
```

MKW-008 (warning) Found a design port %s with invalid direction.

DESCRIPTION

```
The MW database has an invalid direction for the given port.
```

WHAT NEXT

```
No action required but please check the validity of MW CEL view.
```

MKW-009 (warning) link_create_black_boxes is not supported in the Milkyway flow.

DESCRIPTION

```
You are getting this message since you disabled the creation of black boxes and are
using "read_milkyway" command. The Milkyway database is a physically linked
database. When it is read into PT/PTSI, a linked database is read in. For this
reason, a linking step does not occur in the "read_milkyway" flow. Any unresolved
library cells will be created as black boxes.
```

WHAT NEXT

```
No action required.
```

MKW-010 (error) Scenario name %s supplied when no

scenarios stored

DESCRIPTION

A **read_milkyway** command was issued with a scenario name argument, but there were no scenarios stored in the milkyway database.

WHAT NEXT

Either re-generate the milkyway database with the scenario, re-issue the **read_milkyway** command as *-netlist_only* to ignore all constraints, or re-issue the **read_milkyway** command without the scenario to pick up the non-scenario constraints.

MKW-011 (error) Scenario name %s did not match an available scenario %s.

DESCRIPTION

A **read_milkyway** command was issued with a scenario name that did not match any of the scenarios in the milkyway database. A list of available scenarios is listed.

WHAT NEXT

Choose one of the available scenarios and re-issue the **read_milkyway** command with the chosen scenario.

MKW-012 (error) Cannot read all constraints from Milkyway%s.

DESCRIPTION

The **read_milkyway** command could not read all of the constraints from the given Milkyway design.

WHAT NEXT

Ensure that the constraints were written to the Milkyway database correctly and with the correct scenario name(s) if scenarios are being used.

The most likely cause of this is an incompatible version of IC Compiler or the CEL was generated from Astro. PrimeTime does not support reading constraints written by Astro into a CEL.

If the CEL was generated from Astro, you can write out the SDC for the CEL in Astro

and then read the SDC into PrimeTime.

MKW-013 (error) Cannot find bussed port %s.

DESCRIPTION

The Milkyway Database defines a port in the bus section but not in the regular ports section. The bus will not include the given port.

WHAT NEXT

Check the creation of Milkyway database and re-run.

MKW-014 (error) net %s is declared twice

DESCRIPTION

The net was declared twice in the design. This can happen if two net names are the same except for escape characters.

WHAT NEXT

Regenerate the design using net names that are unique.

MODEL

MODEL-1 (error) Cannot write the updated model to the db file. The scaled cell model has different ports from the original model saved
 in the db file %s.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-update** option, and the ports or timing arcs of the updated model are different from those of the original model. Two models written to the same db file must have exactly the same ports and number and order of arcs; the only difference allowed is in the timing values. This message informs you that **extract_model** did not update the db file with the new information.

Some possible reasons why the two models are different could include these:

• You might have used a slightly different version of the design when performing the update.

• The design might have different false path definitions, which could result in different timing arcs.

• You might have inadvertently used a different design when performing the update.

• You might have used different options (for example, **-library_cell** or **-ignore_ports**) for the original and for the updated model.

WHAT NEXT

Ensure that the original and the updated model have the same timing arcs and ports. Then reexecute **extract_model** with the **-update** option.

SEE ALSO

extract_model (2).

MODEL-2 (error) Port name %s found in %s design is not

found in %s design (operating_condition - %s).

DESCRIPTION

You receive this message if **extract_model** detects a port in the nominal model (that is, at nominal operating condition) that is not in the scaled cell (at a different operating condition). The scaled cell must contain the same ports and arcs as the nominal model.

WHAT NEXT

Ensure that the scaled cell model contains the same ports as the nominal model, then reexecute the command.

SEE ALSO

extract_model (2).

MODEL-3 (warning) A scaled cell for operating condition %s already
exists. Replacing it with the new cell.

DESCRIPTION

You receive this message if **extract_model** finds that a scaled cell is already present for the specified operating condition. This message warns you that the existing scaled cell is being replaced by the new one.

WHAT NEXT

This is a warning message only; no action is required on your part. In the future, before executing this command, save a copy of the *_lib.db file so that you can restore any cells that are unintentionally overwritten.

SEE ALSO

extract_model (2).

MODEL-4 (error) Cannot generate a report; cell %s is not an

interface timing specification (ITS) cell.

DESCRIPTION

You receive this message if **report_model** finds in the design an instantiated cell that is not an interface timing specification (ITS) cell. **report_model** generates reports only for designs that are composed entirely of ITS cells. You create such designs using **extract_model**.

WHAT NEXT

Ensure that your design contains only ITS cells. Then reexecute **report_model**.

SEE ALSO

extract_model (2), **report_model** (2).

MODEL-5 (error) Cannot generate a report; the design %s does not instantiate a PrimeTime model.

DESCRIPTION

You receive this message if **report_model** finds that the design does not instantiate a PrimeTime model. The design might contain more than one cell; a PrimeTime model contains one cell per library. **report_model** generates reports only for PrimeTime designs.

WHAT NEXT

You cannot use **report_model** on this design.

SEE ALSO

report_model (2).

MODEL-6 (Information) Min delay arc from '%s' to '%s' missing for

operating_condition '%s'; substituting with a max_delay arc.

DESCRIPTION

The extractor did not extract the min delay arc between the two points for the operating condition. This min delay arc is present in other operating conditions.

WHAT NEXT

No further action is needed.

MODEL-7 (Error) Cannot open file %s for writing.

DESCRIPTION

You receive this message if the command could not write to the specified file. You might be in a directory where you do not have write permission, or perhaps the file exists and is write-protected.

WHAT NEXT

Either change the permissions on the file or directory so that you can write to it, or use another file and directory for which you have write permission. Then reexecute the command.

SEE ALSO

extract_model (2), **save_qtm_model** (2), **write_interface_timing** (2).

MODEL-8 (information) STAMP %s file %s was successfully compiled.

DESCRIPTION

This is an informational message indicating the STAMP file has been compiled succussfully.

WHAT NEXT

No action is needed.

compile_stamp_model (2).

MODEL-9 (Error) You must use the -library_cell option with the -remove_internal_arcs option.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option and did not also use the **-library_cell** option. You cannot use **-remove_internal_arcs** without also using **-library_cell**.

WHAT NEXT

Reexecute **extract_model** and use the **-library_cell** option along with the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-10 (warning) The -test_design option is valid only with the -library_cell option. Ignoring the -test_design option.

DESCRIPTION

You receive this message if you execute **extract_model** and use the **-test_design** option without the **-library_cell** option. The **-test_design** option specifies that a test design instantiating the model lib_cell is to be generated; therefore, **-test_design** is invalid without the **-library_cell** option. This message warns you that the **-test_design** option is being ignored.

WHAT NEXT

If it is acceptable to you that the **-test_design** option is ignored, no action is required on your part. However, if you still want to use the **-test_design** option, reexecute the **extract_model** command and use both the **library_cell** and **-test_design** options.

SEE ALSO

extract_model (2).

MODEL-11 (warning) Cannot update library %s; that library does not exist.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-update** option, but the specified library does not exist. **extract_model** therefore cannot update the library.

WHAT NEXT

If it is acceptable to you that the specified library was not updated, no action is required on your part. Otherwise, do one of the following:

1. Reexecute **extract_model -update** and specify the name of an existing library that is consistent with the current design; or

2. Reexecute **extract_model** without the **-update** option and write a new library.

SEE ALSO

extract_model (2).

MODEL-12 (information) %s.

DESCRIPTION

This is a general purpose modeling related informational message usually issued to indicate the progress or status of the program.

WHAT NEXT

No action is needed.

MODEL-13 (warning) Cannot write generated clock %s to the model because all of the clock's derived sources are on internal pins and the **-remove_internal_arcs** option was

specified.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option, but one or more generated clocks have their derived sources on internal pins. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

WHAT NEXT

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute **extract_model** and do not use the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-14 (warning) Cannot write generated clock %s to the model
 because the clock's master pin is on an internal pin, and the
 -remove_internal_arcs option was specified.

DESCRIPTION

You receive this message if you execute **extract_model** with the **-remove_internal_arcs** option, but the specified generated clock has its master pin on an internal pin. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

WHAT NEXT

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute **extract_model** and do not use the **-remove_internal_arcs** option.

SEE ALSO

extract_model (2).

MODEL-16 (warning) The models to be merged have different design names
%s and %s, respectively, use %s."

DESCRIPTION

```
This is to warn that the design names defined in the models to be merged are not the
same.
```

WHAT NEXT

```
Please check if the names are actually correct. This is a warning message, the
models will still be merged.
```

MODEL-17 (information) extract_model: %-40s

DESCRIPTION

```
This message shows the progress of the extract_model command. The body of each
message reflects a specific aspect of the process.
```

WHAT NEXT

```
This is an informational message only; no action is required on your part. However,
if you want to suppress the display of these messages, or change the level of
messages that are displayed, set the extract_model_status_level variable to a
different value. Allowed values are none, low, medium, or high.
```

SEE ALSO

```
extract_model (2); extract_model_status_level (3).
```

MODEL-18 (error) Found different values defined for attribute
'%s', %s and %s in the models, cannot merge them.

DESCRIPTION

```
This is an error indicating that the named attribute defined for the models to be
merged are not the same. Model merging cannot proceed with this difference.
```

Please make sure that the named attribute is defined to have the same values across all the models to be merged.

MODEL-19 (error) The %s defined in the models are different.

DESCRIPTION

This is a general error indicating that the named object(s) defined in the models to be merged are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-20 (error) Found %s '%s' in the models defined with different %s, cannot merge them.

DESCRIPTION

This is a general error indicating that the named object(s) defined in the models are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-21 (error) %s '%s' is not defined in all models, cannot merge.

DESCRIPTION

This is a general error indicating that the named object is not defined in all the models. Model merging cannot proceed with the difference.

Please make sure that the named object is defined across all the models to be merged.

MODEL-22 (error) The port/pin number %d is different in the models. They
 are defined as %s and %s, respectively.

DESCRIPTION

This is an error message indicating that the port/pin defined at the specified position in the models are not the same. Model merging cannot proceed with the difference.

WHAT NEXT

Please make sure that the order of pins of direction INPUT/OUTPUT/INOUT/TRIOUT are are defined the same across all the models to be merged. INTERNAL pin order is not important.

MODEL-23 (error) Cannot merge %s '%s' with different '%s'
  %s and %s in the models.

DESCRIPTION

This is an error indicating that the named attribute defined for the named object are not the same. Model merging cannot proceed with this difference.

WHAT NEXT

Please make sure that the named attribute is defined to have the same values across all the models for the named object.

MODEL-24 (warning) Found %s '%s' with different '%s'

%s and %s in the models, use %s.

DESCRIPTION

```
This is a warning indicating that the named attribute defined for the named object
are not the same. Model merging will use the value specified.
```

WHAT NEXT

```
Please check if the named attribute should have the same values for the named
object.
```

MODEL-25 (error) The bit number %d in bus %s is different in the models.
They are defined as %s and %s, respectively.

DESCRIPTION

```
This is an error message indicating that the specified bit of the bus in the models
are not the same. Model merging cannot proceed with the difference.
```

WHAT NEXT

```
Please make sure that the bits and the order of bits are the same in the bus across
all models to be merged.
```

MODEL-26 (information) Found unique internal pin '%' in one of the models,
copied into the merged model.

DESCRIPTION

```
This is an informational message.
```

WHAT NEXT

```
No action required.
```

MODEL-27 (error) %s.

DESCRIPTION

This is a general purpose modeling related error message usually issued to indicate the reason why model merging cannot proceed.

WHAT NEXT

Please invetigate the models to be merged and fix the identified problems and try merge them again.

MODEL-28 (warning) Found %s '%s' with conflict '%s' '%s' and '%s' set in the models, no constant is set for it in the merged model.

DESCRIPTION

This is a warning indicating that the named attribute defined for the named object are not the same. Model merging will use the value specified.

WHAT NEXT

Please check if the named attribute should have the same values for the named object.

MODEL-29 (warning) The %s command will be discontinued in future releases. Changes to model validation has made this command unecessary

DESCRIPTION

A command has been rendered unnecessary by changes to model validation commands. The old command is being supported temporarily but will cause syntax errors in future releases

WHAT NEXT

Use the new functionality instead of the discontinued command.

MODEL-30 (error) Cannot merge models because no model files were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying model files through either the -model_files or -lib_files option.

WHAT NEXT

Add model files to the command using either the **-model_files** or **-lib_files** option.

SEE ALSO

merge_models (2).

MODEL-31 (error) Cannot merge models because no data files were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying any data files in conjunction with the **-model_files** optoin. The **merge_models** command requires data files when **-model_files** is present.

WHAT NEXT

Add data files to the command using the **-data_files** option.

SEE ALSO

merge_models (2).

MODEL-32 (error) Cannot merge models because no mode

names were specified

DESCRIPTION

You receive this message if you execute **merge_models** without specifying any mode names. The **merge_models** command requires one mode name for each input file.

WHAT NEXT

Add mode names to the command using the **-mode_names** option.

SEE ALSO

merge_models (2).

MODEL-33 (error) Cannot merge models because the number of model files does not match the number of data files.

DESCRIPTION

The **merge_models** command requires the number of model and data files match. One model and data file combine to define a model in STAMP format, so **merge_models** requires a one for one correspondance.

WHAT NEXT

Adjust the **-data_files** or **-model_files** as needed so the list lengths match.

SEE ALSO

merge_models (2).

MODEL-34 (error) Cannot merge models because the number of mode names does not match the number of model files.

DESCRIPTION

The **merge_models** command requires the number of mode names to match the number of model files. The model files are specified with either the **-model_files** or **-lib_files** option. A combination of model file and mode name defines a model to merge, so the number in each list must match.

WHAT NEXT

Adjust the mode names or the number of models so that the list lengths match.

SEE ALSO

merge_models (2).

MODEL-35 (error) Cannot merge models because there are duplicate mode names

DESCRIPTION

The **merge_models** command requires that the mode names be unique. There cannot be any duplicates.

WHAT NEXT

Change the duplicate mode names to be unique.

SEE ALSO

merge_models (2).

MODEL-36 (error) Cannot merge models because of an empty %s list

DESCRIPTION

A list for **merge_models** is empty. All lists must have at least one element in them.

WHAT NEXT

Add elements to the list, or remove the option for the list from the command line.

SEE ALSO

merge_models (2).

MODEL-37 (error) Cannot use %s in conjunction with %s

DESCRIPTION

You cannot specify both of these options for **merge_models** at the same time.

WHAT NEXT

Remove one or both of these options from the command.

SEE ALSO

merge_models (2).

MODEL-38 (error) Cannot merge models because there are data files with no model files.

DESCRIPTION

The **merge_models** command cannot have **-data_files** without corresponding **-model_files**.

WHAT NEXT

Either add **-model_files** to merge STAMP files, or remove the **-data_files** to merge LIB files.

SEE ALSO

merge_models (2).

MODEL-39 (error) Library file was not extracted.

DESCRIPTION

When the **merge_models** command read in one of the files in the **-lib_files** list of library files, it did not see at least one required attribute. Each of the library files must be the result of the **extract_models** command.

WHAT NEXT

Ensure that all of the library files are the output of the **extract_model** command.

MODEL-40 (error) Library file is invalid for merging.

DESCRIPTION

When the **merge_models** command read in one of the files in the **-lib_files** list of library files, it found that one of the libraries was missing some expected attributes, had inconsistant attributes, or had unexpected attributes. Each of the library files must be the result of the **extract_models** command.

WHAT NEXT

Ensure that all of the library files are the output of the **extract_model** command.

SEE ALSO

merge_models (2). **extract_model** (2).

MODEL-41 (error) The %s and %s arguments are mutually exclusive

DESCRIPTION

The **merge_models** command cannot be invoked with both of the arguments at the same time, only one is allowed.

WHAT NEXT

Remove one of the arguments and invoke the command again.

MS

MS-001 (warning) Requested '%d' '%s' licenses, '%d' checked out.

DESCRIPTION

The requested increase in the number of licenses checked out for the feature
indicated was not successful. This occurs when the license server cannot fulfill the
requests for the number of licenses due to a lack of licenses or because some of its
licenses are already in use. The number of license indicated as checked out are all
the license that can be acquired at this time.

By default the PrimeTime shell can only check out licenses for a single feature from
a single license server at a time. If the licenses for a feature are split across
multiple license servers, the maximum number of licenses of that feature that the
shell can check out is determined by the license server with the largest number of
licenses. By default the PrimeTime shell cannot span its license check outs for a
single feature across multiple license servers. However, it can check out licenses
for different features from different license servers.

WHAT NEXT

Increase the number of licenses available on the license server so that subsequent
attempts to checkout licenses succeed.

To be able to checkout licenses for a single feature across multiple license
servers, incremental license handling must be enabled. Incremental license handling
is enabled by setting the UNIX environmental
SNPSLMD_ENABLE_INCREMENTAL_LICENSE_HANDLING to 1. This can be done by issuing the
following command in the UNIX environment before the PrimeTime shell is launched.

setenv SNPSLMD_ENABLE_INCREMENTAL_LICENSE_HANDLING 1

If the variable SNPSLMD_ENABLE_INCREMENTAL_LICENSE_HANDLING is not defined in the
UNIX environment or has a value other than 1, incremental license handling is
disabled.

MS-002 (warning) Requested '%d' '%s' licenses, '%d' checked out.

DESCRIPTION

The requested reduction in the number of licenses checked out for the feature
indicated, was not successful. This occurs when incremental license handling is not

enabled or when there is a problem with the license server.

WHAT NEXT

Before launching PrimeTime, activate the incremental handling of license by setting
the ENABLE_INCREMENTAL_LICENSE_HANDLING UNIX environmental variable to 1.

For example, setenv ENABLE_INCREMENTAL_LICENSE_HANDLING 1

MS-003 (Information) Multi-scenario distributed processing has checked
 out the following licenses for the duration of this session.

 Slave Usage: %4d %s license(s)

DESCRIPTION

This message identifies the number of licenses, of the feature in question,
 that have been checked out for the duration of the multi-scenario session.
 The number of licenses indicated are for usage by the slave processes.

MS-004 (Warning) The current session has been terminated.

DESCRIPTION

The last scenario in the current session has been removed, therefore the current
session has been terminated.

MS-005 (Warning) The search_path entry %s could not be resolved.

DESCRIPTION

The master was unable to find the directory location of an entry in the search_path.
The erroneous entry will not be sent to the slave

Remove or correct the erroneous search_path entry.

MS-006 (error) The slave was unable to resolve the working directory %s.

DESCRIPTION

The working directory is specified during the setup phase of the master. At that stage a check is done to verify that the working directory is understood by the master. This error occurred because the slave could not understand the location of the working directory.

WHAT NEXT

Change the multi_scenario_working_directory variable to point to a location which can be resolved by the slave.

MS-007 (error) The PrimeTime multi-scenario master process detected
 PrimeTime slave instances that encountered fatal errors. The master
 and all slave processes will now terminate.

DESCRIPTION

While executing commands in multi-scenario analysis one or more PrimeTime slave instances encountered fatal errors requiring them to exit. In this situation the master cannot proceed accepting user commands. The master will complete the last command issued and issue the reporting information that has been processed.

WHAT NEXT

Re-run the current session excluding the scenario in which the problem occurred.

MS-008 (error) The number of licenses made available for

slaves in multi-scenario analysis cannot be decreased.

DESCRIPTION

This error has occurred because the user has attempted to reduce the license limit
for multi_scenario analysis below a previously set limit for a feature type.

WHAT NEXT

Only issue the set_multi_scenario_license_limit with the number of licenses for each
feature type greater than the existing limit for that feature type.

MS-009 (warning) Failed to exchange timing path data with the master.

DESCRIPTION

This warning refers to the timing path printed directly after this warning. While
exchanging timing path information with the master process, a pin was found in the
path that was not explicitly mentioned in the netlist and hence is unknown to the
master. As a result the timing information in the path will not be included in the
merged timing report produced at the master. Typically these pins are unconnected
pins.

WHAT NEXT

Identify the unconnected pin from the timing report and explicitly mention it in the
netlist.

MS-010 (error) The PrimeTime multi-scenario master exceeded the
 task processing limit.

DESCRIPTION

This errors occurred because the master submitted tasks outside
 the range of tasks that can be processed in a single PrimeTime instance.
 Currently, the master process can manage up to 4900 tasks; PrimeTime
 cannot process tasks beyond this range.

This is a limitation of the current multi-scenario capability.

MS-011 (error) %s image generation failed.

DESCRIPTION

The multi-scenario image generated failed validation.

WHAT NEXT

Examine the slave log files for the cause of the failure and correct the problem.

MS-012 (error) Cannot set multi_scenario_working_directory variable after a distributed farm has been launched.

DESCRIPTION

It is forbidden to change the working directory, once the create_distributed_farm command has been successfully issued.

WHAT NEXT

Change the multi_scenario_working_directory before issuing the create_distributed_farm command

MS-013 (warning) Setting all scenarios in the current session into
 command focus for the '%s' command.

DESCRIPTION

One or more scenarios in the current session was not in command focus. The command requires that all scenarios in the current session be in command focus before the command can be executed. All scenarios in the current session have been put in command focus to allow the command to execute.

WHAT NEXT

```
No further action is required.
```

MS-014 (information) Implicitly specifying the '-base_names' option with the get_alternative_lib_cells command, because the command has been called in a master context.

DESCRIPTION

```
This message is issued if you have called the get_alternative_lib_cells command in a
master context and have not specified the '-base_names' option. This option must be
used in a master context and thus has been implicitly specified.
```

WHAT NEXT

```
To obtain a collection of valid alternative library cells for a cell in one
scenario, call the command in a slave context on that scenario.

To obtain a list of valid alternative library cell base names for a cell in one
scenario, call the command in a slave context with the '-base_names' option on that
scenario.

To obtain a list of valid alternative library cell base names for a cell common to
all scenarios, call the command in a master context with the '-base_names' option.
```

SEE ALSO

```
get_alternative_lib_cells(2)
```

MS-015 (warning) The upper limit on the number of licenses of the
 '%s' feature has not been specified.

DESCRIPTION

```
The upper limit on the number of licenses of the specific feature has not been set
at the master and a slave has requested a license for that feature. Since no license
limit has been set for the feature, the master is unable to fulfill any requests for
licenses of that feature.

The slave requesting the license will issue an error message that the site is not
licensed for that feature and proceed just as standard PrimeTime would without the
```

```
feature enabled.
```

WHAT NEXT

```
Use the set_multi_scenario_license_limit command to specify an upper limit on the
license usage for the feature in question.
```

MS-016 (error) Errors detected during master/slave task processing.

DESCRIPTION

```
One or more slave processes encountered an error in processing a task that can give
rise to incomplete results.
```

WHAT NEXT

```
Examine the errors reported during the master/slave task processing and correct any
problem found. Further information about the error encountered can be found in the
multi-scenario merged error log as specified by the multi_scenario_merged_error_log
variable if it was set.
```

MS-017 (error) failed to create current session with '%d' scenarios.
 Maximum allowable scenarios in a session using common data '%d'.
 Maximum allowable scenarios in a session not using common data '%d'.

DESCRIPTION

```
When setting the current session, the number of scenarios being used to create the
session is beyond the number supported. When any scenario has common data, the
number of scenarios supported is less than when no scenario has any common data. The
limits are as specified above.
```

WHAT NEXT

```
Reduce the number of scenarios being used to form a session within the limits
specified above.
```

MS-018 (warning) Removing the following terminate scenarios from the session.

DESCRIPTION

When scenarios abnormally terminate, they are removed from any further subsequent analysis in the current session.

WHAT NEXT

If the terminated scenarios are to be re-analyzed, create a new session, including the terminated scenarios, and analyze them as normal.

MS-019 (warning) Removing the current session.

DESCRIPTION

The resource requirements for the existence of a session have been invalidated so the current session was removed.

WHAT NEXT

See the **current_session** command for the resource requirements needed to create the current session and how to check the availability of those resources.

MS-020 (warning) Removing the following scenarios from the session.

DESCRIPTION

The scenarios indicated were removed from the current session because the scenarios providing baseline images for them to use abnormally terminated while producing the images. These scenarios cannot start-up without the baseline images and must be excluded from further analysis.

WHAT NEXT

If the scenarios are to be re-analyzed, create a new session including the scenarios

and analyze them as normal. If the issue continues to arise, remove the scenario
that is failing to produce the baseline image from the session and re-analyze as
normal.

MS-021 (fatal) Internal system error in scenario '%s'

DESCRIPTION

While executing commands in multi-scenario analysis the scenario indicated
experienced a critical internal error causing it to terminate.

WHAT NEXT

Re-run the current session excluding the scenario in which the problem occurred.

MV-001 (warning) Port '%s' is unconstrained.

DESCRIPTION

You receive this message because a port has been found to be unconstrained while running the **write_interface_timing** command. Unconstrained ports leave the paths connected to that port unevaluated, so any modeling issues associated with these paths would be hidden.

WHAT NEXT

Use the **check_timing** command on the current design or **report_port** on a specific port to verify the port constraints before running **write_interface_timing**.

SEE ALSO

check_timing (2), **report_port** (2), **write_interface_timing** (2).

MV-002 (error) Path group list is empty for design '%s'.

DESCRIPTION

You receive this message because no path groups were defined when running the **write_interface_timing** command. This should occur only if all path groups were removed (for example, by running the **remove_path_group** command with the **-all** option).

WHAT NEXT

Use the **report_path_group** command to verify that path groups are defined before using **write_interface_timing**. Path groups should be left in their default state during model creation and validation.

SEE ALSO

remove_path_group (2), **report_path_group** (2), **write_interface_timing** (2).

MV-003 (warning) Unknown -ignore option '%s'.

DESCRIPTION

You receive this message because an entry in the **-ignore** option *ign_list* in the **compare_interface_timing** command line was invalid.

WHAT NEXT

Check the spelling of the option used and compare it against the names listed in the **compare_interface_timing** command man page or **-help** list.

SEE ALSO

compare_interface_timing (2).

MV-004 (warning) Unknown -include option '%s'.

DESCRIPTION

You receive this message because an entry in the -include option *cmp_list* in the **compare_interface_timing** command line was invalid.

WHAT NEXT

Check the spelling of the option used and compare it against the names listed in the **compare_interface_timing** command man page or **-help** list.

SEE ALSO

compare_interface_timing (2).

MV-005 (warning) The format of the timing file '%s' is nonstandard.

DESCRIPTION

You receive this message because one of the timing files specified in the **compare_interface_timing** command line does not exactly follow the **write_interface_timing** output format.

WHAT NEXT

This should occur only if the timing file has been modified or if it was created by some means other than by using the **write_interface_timing** command. Compare the nonstandard timing file with one generated by **write_interface_timing** to determine what condition might be causing the warning.

SEE ALSO

compare_interface_timing (2), **write_interface_timing** (2).

MV-006 (warning) The design name was missing from the timing file '%s'.

DESCRIPTION

You receive this message because one of the timing files specified in the **compare_interface_timing** command line is missing the Design field.

WHAT NEXT

This should occur only if the timing file has been modified or if it was created by some means other than by using the **write_interface_timing** command. Compare the nonstandard timing file with one generated by **write_interface_timing** to determine what condition might be causing the warning.

SEE ALSO

compare_interface_timing (2), **write_interface_timing** (2).

MV-007 (warning) An unknown attribute '%s' was found in a timing file.

DESCRIPTION

You receive this message because one of the timing files specified in the **compare_interface_timing** command line contains an unknown path attribute.

WHAT NEXT

This should occur only if the timing file has been modified or if it was created by some means other than by using the **write_interface_timing** command. Refer to the **write_interface_timing** command man page for a list of acceptable attributes.

compare_interface_timing (2), **write_interface_timing** (2).

MV-008 (error) No data is found in section '%s' of timing file '%s'.

DESCRIPTION

You receive this message because one of the timing files specified in the **compare_interface_timing** command line is missing one of the following four sections: slack, transition_time, capacitance, or design_rules.

WHAT NEXT

This should occur only if the timing file has been modified or if it was created by some means other than by using the **write_interface_timing** command.

SEE ALSO

compare_interface_timing (2), **write_interface_timing** (2).

MV-009 (warning) The -include option '%s' should not be used with '%s' data.

DESCRIPTION

You receive this message because one of the timing files specified in the **compare_interface_timing** command line contains a different type of timing data than is specified in the **-include** option.

WHAT NEXT

Match the timing data name with a keyword in the *cmp_list* specified in the **-include** option.

SEE ALSO

compare_interface_timing (2).

MV-010 (error) Arc data '%s' cannot be compared with slack

data '%s'.

DESCRIPTION

You receive this message because the two timing files specified in the **compare_interface_timing** command line contain different timing data types: arc data in the first and slack data in the second.

WHAT NEXT

Determine that the **-timing_type** option of **write_interface_timing** was set correctly when the command was used to create these two files. To compare the other data sections, use the **compare_interface_timing** command with the **-include** option to list the sections you want.

SEE ALSO

compare_interface_timing (2), **write_interface_timing** (2).

MV-011 (warning) No data was written for section '%s'.

DESCRIPTION

You receive this message because the particular data section of **write_interface_timing** will be empty.

WHAT NEXT

This warning indicates that the design is not properly setup to do model validation. To identify the problem, run **check_timing** or look for errors/warnings that preceded this command.

SEE ALSO

write_interface_timing (2). **check_timing** (2).

MV-012 (warning) Pin '%s' is an internal start or end point. Ignoring paths to and from this pin.

DESCRIPTION

You receive this message if the **write_interface_timing** command finds a pin that is

an internal start or end point, which indicates that the pin is participating in a timing exception such as by **set_max_delay** or **set_min_delay** specified on it. Because of **extract_model** does not support such qualifiers, **write_interface_timing** does not check it.

WHAT NEXT

Use **report_exceptions** to identify all **max_delay**, **min_delay**, remove them, and re-execute **write_interface_timing**.

SEE ALSO

write_interface_timing (2). **extract_model** (2). **set_max_delay** (2). **set_min_delay** (2). **report_exceptions** (2).

MVOLT-001 (error) Set_voltage failed on %s.

DESCRIPTION

```
Could not find the power net or pg pin to set voltage on.
```

WHAT NEXT

```
Make sure that teh object exists. Power net: Create power net by
create_power_net_info. PG pin: Use PG-aware Liberty libraries.
```

MVOLT-052 (error) Power net %s does not exist.

DESCRIPTION

```
Could not find the power net.
```

WHAT NEXT

```
Create power net by create_power_net_info.
```

MVOLT-065 (error) Cell %s already belongs to power domain %s.

DESCRIPTION

```
A cell can not belong to more than one power domain.
```

WHAT NEXT

```
Review all create_power_domain -object_list commands and make sure that they define
non-overlapping sets of objects.
```

NED-001 (error) Cannot size '%s' - it is not a leaf cell.

DESCRIPTION

The **size_cell** command will only work with leaf cells. The specified cell is hierarchical.

WHAT NEXT

You can swap a hierarchical cell using the **swap_cell** command.

NED-002 (warning) Could not find alternative library cells for %s.

DESCRIPTION

Alternative library cells could not be found for the cell or library cell specified. Perhaps there were no equivalent library cells in the libraries searched. The criteria used to determine that a library cell is an alternative for another library cell is the same which is used by the size_cell command.

WHAT NEXT

Perhaps specify other libraries using the -libraries option.

SEE ALSO

size_cell(2).

NED-003 (warning) Both the -estimate and -exact option cannot be specified.

DESCRIPTION

Both the -estimate and -exact options cannot be specified at the same time for the report_alternative_lib_cells command.

Specify either -estimate or -exact.

NED-004 (warning) The -weighted_design_cost or -total_design_cost options cannot be be used when -estimate is specified.

DESCRIPTION

The -weighted_design_cost and -total_design_cost options are only applicable when -exact is specified.

WHAT NEXT

Either use -exact, or do not use the -weighted_design_cost or -total_design_cost options.

NED-005 (Error) Could not size '%s' ('%s') with '%s'%s.

DESCRIPTION

You tried to size a cell, and this action failed. Additional information might be included with this message and previous messages. A typical reason is that the target library cell is not compatible with the existing cell because it has a different pin count, or different pin directions, and so on.

WHAT NEXT

Action based on reasons given in message text. Use the **get_alternative_lib_cells** command to determine what library cells can be used to size your cell.

NED-006 (Error) Can only have a single target object.

DESCRIPTION

The specification for the target library cell to commands like **size_cell**, **insert_buffer**, and **create_cell** resulted in more than one object. Either you specified a list or used a collection that matched multiple objects.

Narrow the search parameters so only a single library cell is selected.

NED-007 (error) Cannot specify the '%s' option and explicitly specify the library in which the library cell exists.

DESCRIPTION

This message is produced if either the '-current_library' option or the '-libraries' option is specified while explicitly specifying the library in which the library cell exists.

WHAT NEXT

Either explicitly specify the library in which the library cell exists using the syntax 'lib_name/lib_cell_name'; or specify the library cell name only with the option needed to resolve the library name.

SEE ALSO

insert_buffer(2), **create_cell**(2), **size_cell**(2).

NED-008 (information) Renamed cell '%s' to '%s' in %s.

DESCRIPTION

The **rename_cell** command was issued to rename a cell.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-009 (information) Renamed net '%s' to '%s' in %s.

DESCRIPTION

The **rename_net** command was issued to rename a net.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-010 (error) Could not insert '%s' - %s.

DESCRIPTION

You tried to insert a buffer, and the action failed for the reason given. A typical reason is that the library cell chosen is not classified as a buffer. A buffer must have one input, and each output must be functionally input or !input.

WHAT NEXT

Action based on the reason.

NED-011 (error) Cannot insert buffer '%s' with%s %s

DESCRIPTION

You tried to insert a buffer, and the command options are inconsistent. Either you specified the -inverter_pair option and the library cell does not have an inverting output, or you did not specify the -inverter_pair option, and the library cell has only inverting outputs.

WHAT NEXT

Check the library cell to see what output pins are available.

NED-012 (error) Could not insert a buffer on %s '%s': %s

DESCRIPTION

You tried to insert a buffer, and the action failed for the given reason. An example reason would be trying to insert a buffer on a port when current instance is not at the top of the hierarchy. Another example would be trying to insert a buffer on a pin which is out of scope (that is, the pin is not in or below the current instance).

WHAT NEXT

```
Check the arguments to the command.
```

NED-013 (warning) Duplicate argument (%s '%s') to %s ignored

DESCRIPTION

```
You tried to use a netlist editing command, and you specified the same argument more
than once. This is just a warning.
```

WHAT NEXT

```
Verify that the argument was specified correctly.
```

NED-014 (information) Created cell '%s' in %s with '%s'.

DESCRIPTION

```
The create_cell command was issued to create a new cell using the specified library
cell.
```

WHAT NEXT

```
For more information please refer to PrimeTime User Guide.
```

NED-015 (information) Removed cell '%s'.

DESCRIPTION

```
The remove_cell command was issued to remove the specified cell.
```

WHAT NEXT

```
For more information please refer to PrimeTime User Guide.
```

NED-016 (information) Created net '%s' in %s.

DESCRIPTION

The **create_net** command was issued to create a new net.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-017 (information) Removed net '%s'.

DESCRIPTION

The **remove_net** command was issued to remove a net.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-018 (information) Connected '%s' to '%s'.

DESCRIPTION

The **connect_net** command was issued to connect a net to a pin.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-019 (information) Disconnected '%s' from '%s'.

DESCRIPTION

The **disconnect_net** command was issued to disconnect a net from a pin.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-020 (error) Could not rename design '%s' to '%s': %s

DESCRIPTION

An attempt to rename a design failed. The reason is given in the message text. Given that you tried to rename *a* to *b*, one reason the rename would fail would be that there is already a design named *b* associated with the file of *a*. Another reason would be that there are instances of *a* in a linked design.

WHAT NEXT

Choose a name which does not conflict with existing design names. Also, renaming designs in PrimeTime should be done prior to any linking to avoid the case of instantiation conflicts.

NED-021 (error) Could not rename %s to '%s': %s%s.

DESCRIPTION

You tried to rename a cell or net, and it could not be renamed for the reason given. A typical reason is that a cell or net by that name already exists at that point in the hierarchy.

WHAT NEXT

Action based on the reason.

NED-040 (error) No changes made.

DESCRIPTION

This is a summary message for netlist editing. It indicates that no changes were made by the command. For example, no cells were created, or no pins were disconnected from a net.

The netlist editing commands succeed if at least one change is made. This message is only issued if no changes were made.

None.

NED-041 (error) Could not create %s '%s': %s%s.

DESCRIPTION

You tried to create a cell or net, and it could not be created for the reason given. A typical reason is that a cell or net by that name already exists at that point in the hierarchy.

WHAT NEXT

Action based on the reason.

NED-042 (error) Could not connect '%s' to '%s' %s

DESCRIPTION

This message is issued by the **connect_net** command if the net could not be connected to the given object. The reason is given in the message. Reasons include: the object is already be connected to a net; the connection would cross a hierarchical boundary; attempted to connect a port to a net which is not in the top level of the hierarchy.

WHAT NEXT

Action based on the reason.

NED-043 (error) Object '%s' is not connected to net '%s'

DESCRIPTION

This message is issued by the **disconnect_net** command if the target object is not connected to the net.

Verify that the target object was specified correctly.

NED-044 (error) Argument to %s (%s'%s') is invalid: %s

DESCRIPTION

This message is issued by the netlist editing commands if the object is not valid for the command. The reason is given in the message. Many netlist editing commands use this message when the object is not in scope - the object must be in or below the current instance.
The **remove_buffer** command uses this extensively to indicate many problems, for example:

- The cell is not a buffer.
- The cell has too many or too few pins connected.
- The cell needs to be an inverter, but isn't.
- The cell is an inverter, paired with another argument. But, they are not connected, or the intermediate net has too many connections.
- The output net has too many drivers.

WHAT NEXT

Action based on the reason.

SEE ALSO

remove_buffer(2).

NED-045 (information) Sized '%s' with '%s'.

DESCRIPTION

The **size_cell** command was issue to size the specified cell with a target library cell.

For more information please refer to PrimeTime User Guide.

NED-046 (information) Inserted %s at %s with %s.

DESCRIPTION

The **insert_buffer** command was issued to buffer specific pins with a target library cell. In the case of an inverter pair two cells will have been inserted.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-047 (information) Removed buffer %s.

DESCRIPTION

The **remove_buffer** command was issued to remove a specific buffer or inverter pair.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-048 (error) The variable %s cannot be set to '%s'

DESCRIPTION

You received this message because you have tried to set the variable to a value that violates the rules set down for its value.

WHAT NEXT

See the man page for the variable and set its value appropriately.

NED-049 (warning) disconnecting port-connected net from

output pin/port '%s'.

DESCRIPTION

```
You received this message because you have performed a buffer insertion that has
disconnected a port from its connected-net.
```

WHAT NEXT

NED-050 (error) Cannot disconnect a port-connected net from pin/port '%s', because the net has the same name as the pin/port.

DESCRIPTION

```
You received this message because you have performed a disconnect_net command at a
hierarchical pin or port. The command attempted to disconnect a port-connected net
from a hierarchical pin or port of the same name.
```

```
This operation is not allowed because third-party verilog readers will infer that
the net and pin/port are still connected as they share the same name. This would
results in a shorting out of any object that is subsequently reconnected to the net.
```

WHAT NEXT

```
To continue with the disconnection of the port-connected net, you must firstly
rename the port-connected net (using the rename_net command) to some name that is
not the pin/port name.
```

NED-051 (error) This netlist editing command ('%s') is not supported in IC Compiler.

DESCRIPTION

```
You received this message because you are writing netlist eco changes for IC
Compiler, but the command is not supported in IC Compiler. The requested changes is
commented out, to show you what PrimeTime did. Because the command will not be
executed in IC Compiler, you may get different results from your run in PrimeTime.
```

Please do not use this netlist editing command in PrimeTime, if you intend to write
the changes for IC Compiler.

NED-052 (error) This netlist editing command ('%s') is not fully supported in IC Compiler.

DESCRIPTION

You received this message because you are writing netlist eco changes for IC
Compiler, but the command is not fully supported in IC Compiler: the "-exact" option
cannot be used. The write_changes output file contains the command, but not the "-
exact" option. Because the command will not be executed in IC Compiler exactly as in
PrimeTime, you may get different results from your run in PrimeTime.

WHAT NEXT

Please do not use this netlist editing command with the "-exact" in PrimeTime, if
you intend to write the changes for IC Compiler.

NED-053 (error) This netlist editing command ('%s') is not fully supported in IC Compiler.

DESCRIPTION

You received this message because you are writing netlist eco changes for IC
Compiler, but the command is not supported in IC Compiler: the net name cannot
contain wildcard character, or the hiearch separator. Because the command will not
be executed in IC Compiler, you may get different results from your run in
PrimeTime.

WHAT NEXT

Please do not use this netlist editing command with the restricter characters in the
net name, if you intend to write the changes for IC Compiler.

NED-054 (information) write_changes: change_list redundancy removal results: ('

%s')

DESCRIPTION

This information message gives the details of how many change commands were redundant.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

NED-055 (warning) Buffer cell %s is dont_touched.

DESCRIPTION

A *dont_touch* has been detected on the indicated buffer cell. Although this buffer type can still be sized and inserted into the design, it becomes *dont_touched* for further optimization once it has been inserted into the design. This might place restrictions on the optimization process.

WHAT NEXT

It might be desirable to use the **set_dont_touch** command to set a *dont_touch* value of *false* on the affected buffer library cells.

NOISE-001 (information) Activating steady state resistance estimation mode for library %s.

DESCRIPTION

You received this informational message because during the noise analysis the steady state resistance estimation was activated for one of the library cells in this library.

This estimation mode is activated during the noise analysis update, when no steady state resistance or I-V curve could be determined from the library or specified by the command **set_steady_state_resistance**. Steady state resistance estimation uses the existing delay and slew tables in the library and also relies on CMOS threshold voltage values for the design, specified by the variables / fBsi_noise_nmos_threshold_ratio/fP and /fBsi_noise_pmos_threshold_ratio/fP.

WHAT NEXT

This message indicates that for one of the drivers in the design, there was no steady state I-V curve or steady state resistance. Therefore, it is recommended that this information be characterized for all the library cells which are used in the design, and the library DB be regenerated. If this is not possible, the characterized steady state resistance can be directly set using the **set_steady_state_resistance** command.

SEE ALSO

set_steady_state_resistance (3), **si_noise_nmos_threshold_ratio** (3).
si_noise_pmos_threshold_ratio (3).

NOISE-002 (warning) Steady state resistance estimation failed for %s %s.

DESCRIPTION

You received this informational message because during the noise analysis the steady state resistance estimation was activated and failed for the library pin or port shown above. A fixed steady state resistance value is being used.

This estimation mode is activated during the noise analysis update, when no steady state resistance or I-V curve could be determined from the library or specified by the command **set_steady_state_resistance**. Steady state resistance estimation uses the

existing delay and slew tables in the library and also relies on CMOS threshold
voltage values for the design, specified by the variables /
fBsi_noise_nmos_threshold_ratio/fP and /fBsi_noise_pmos_threshold_ratio/fP.

WHAT NEXT

This message indicates that for the library pin or port mentioned above, there was
no steady state I-V curve or steady state resistance, and our steady state
resistance estimation mode has failed and a fixed value has been used. Therefore, it
is recommended that this information be characterized for this library pin or port,
and the library DB be regenerated. If this is not possible, the characterized steady
state resistance can be directly set using the **set_steady_state_resistance** command.

SEE ALSO

set_steady_state_resistance (3), **si_noise_nmos_threshold_ratio** (3).
si_noise_pmos_threshold_ratio (3).

NOISE-003 (warning) Noise height constraint value of %.2f for pin %s is out of valid range.

DESCRIPTION

You received this informational message because during noise analysis the height
constraint value for the library pin or port shown above is negative. This condition
can occur when a noise bump width is outside the characterization range of the noise
immunity table. In this situation, the immunity curve specified by the table is
extrapolated to obtain the noise height constraint. If the curve is monotonically
decreasing in the extrapolated area, a negative value may result. PrimeTime will
replace this negative height constraint with zero so that any such condition will be
flagged as a noise violation. The area slack in these cases will be the negative of
the bump height area.

WHAT NEXT

This warning indicates a characterization problem for the noise immunity tables in
the library. Noise immunity height is expected to remain constraint when
extrapolation is required. Please contact your library vendor.

You may also override the library-specified noise immunity table by using the
set_noise_immunity_curve command.

SEE ALSO

set_noise_immunity_curve (2).

NOISE-004 (information) Starting incremental noise update.

DESCRIPTION

Update of noise data is done incrementally (faster than full default update). The incremental updates are faster because only the affected parts of the design are updated. That includes the nets directly affected by design changes (such as size_cell), their aggressors, and nets where timing windows changed.

Due to iterative nature of signal integrity updates the incremental update may not perfectly match the full update. The difference should be marginal in most cases but if significant then please perform full update.

WHAT NEXT

This is an informational message. No action is required on your part. However, you can trade off accuracy for performance by forcing full update by e.g., **update_noise -full**

SEE ALSO

update_timing (2), **update_noise** (2), **XTALK-016** (n).

NOISE-005 (error) The command is available only in report_at_endpoint noise analysis mode.

DESCRIPTION

You received this error message because this command works only in report_at_endpoint noise analysis mode.

WHAT NEXT

Please use **set_noise_parameters** command to set noise analysis mode to report_at_endpoint. You also may need to run **noise_update** to see correct results.

SEE ALSO

set_noise_parameters (2), **report_noise** (2). **report_noise_violation_sources** (2).

NOISE-006 (information) Setting report_at_endpoint analysis

mode enables noise propagation.

DESCRIPTION

You received this informational message because you have specified
report_at_endpoint noise analysis mode.

The report_at_endpoint mode requires noise propagation because violations are
reported at endpoints after injected noise bumps propagate from violation sources to
endpoints.

WHAT NEXT

If noise propagation is not desired, switch to report_at_source mode by using
set_noise_parameters command.

SEE ALSO

set_noise_parameters (2), **report_noise** (3), **report_noise_violation_sources** (3).

NOISE-007 (warning) Cannot calculate noise immunity for library pin %s
  due to invalid CCS-noise information.

DESCRIPTION

You received this warning message because the indicated pin does not have valid CCS-
noise information to calculate noise immunity.

You may have to set noise immunity on the pin manually by yourself. Otherwise, you
may miss a violation if no slack value is available from the pin.

WHAT NEXT

Check if the characterization on this pin has been done properly.

SEE ALSO

report_noise_calculation (2), **report_noise** (2).

NOISE-008 (warning) %s is not an endpoint. Only an endpoint can be reported in report_at_endpoint mode.

DESCRIPTION

You received this error message because the indicated pin is not an endpoint, but you tried to run **report_noise command** on the pin.

The report_noise command reports only endpoints in the report_at_endpoint mode.

WHAT NEXT

Use **report_noise_calculation** command to report noise infomration on the pins that are not endpoints.

SEE ALSO

set_noise_parameters (2), **report_noise_calculation** (2), **report_noise** (2).

NOISE-009 (warning) %d percent of the rail voltage is assumed for the
 noise height constraint value of library pin %s because no noise
 immunity information is available for the pin.

DESCRIPTION

You received this warning message because during noise analysis any height constraint value for the library pin or port shown above is not available.

PrimeTime SI will assume 40% of the rail voltage as noise immunity value, which might be more pessimistic than the real value.

WHAT NEXT

This warning indicates a characterization problem for the pin. Please check your library, or contact your library vendor.

If you know the noise immunity value for the pin, you may use **set_noise_margin** command to specify the right value.

You may also override the value by using the **set_noise_immunity_curve** command.

set_noise_margin (2), set_noise_immunity_curve (2).

NOISE-010 (Information) Updating %-35s

DESCRIPTION

Shows the progress of update noise. The update of noise can happen explicitly by calling update_noise or implicitly by calling one of the commands that need update noise such as report_noise.

NOISE-011 (warning) %d percent of the rail voltage is assumed for the
  noise height constraint value of pin %s because no noise
  immunity information is available for the pin.

DESCRIPTION

You received this warning message because during noise analysis any height constraint value for the library pin or port shown above is not available.

PrimeTime SI will assume 40% of the rail voltage as noise immunity value, which might be more pessimistic than the real value.

WHAT NEXT

This warning indicates a characterization problem for the pin. Please check your library, or contact your library vendor.

If you know the noise immunity value for the pin, you may use **set_noise_margin** command to specify the right value.

You may also override the value by using the **set_noise_immunity_curve** command.

SEE ALSO

set_noise_margin (2), set_noise_immunity_curve (2).

NOISE-012 (error) Signal integrity analysis is disabled.

DESCRIPTION

You received this error message because the **si_enable_analysis** variable has been set to **false** while the command requires signal intgegrity analysis.

WHAT NEXT

First, determine whether you want to perform signal integrity analysis. If you do, then set **si_enable_analysis** to **true**.

SEE ALSO

update_noise (2), **si_enable_analysis** (3). ~

NOISE-013 (information) In HiCap mode, please use report_noise_calculation for individual noise bumps.

DESCRIPTION

You received this error message because the **report_noise -verbose** won't report individual noise bumps under HiCap mode. Please use **report_noise_calculation** for individual noise bumps.

WHAT NEXT

First, determine whether you need individual noise bumps. If you do, then use **report_noise_calculation**.

SEE ALSO

report_noise (2), **report_noise_calculation** (2). ~

PA-001 (error) The PrimeTime master process detected PrimeTime
slave instances that encountered fatal errors. The master and all slave processes will now terminate. The fatal errors detected are listed below.

DESCRIPTION

While executing commands one or more PrimeTime slave processes encountered fatal errors requiring them to exit. In this situation, the master cannot proceed and terminates the entire session.

WHAT NEXT

PA-002 (error) Insufficient hosts added for command '%s' ('%d' added, '%d' required)

DESCRIPTION

The PrimeTime master encounterd a command requiring a minimum number of hosts to be added before allowing it to proceed. Since the number of hosts added was below the minimum, the command could not execute successfully.

WHAT NEXT

Use the add_distributed_hosts command to add a sufficient number of hosts to fulfil at least the minimum number of hosts required by the command. See the man page for the specific command to determine its host requirements.

PA-003 (error) Insufficient hosts online for command '%s' ('%d' online, '%d' required)

DESCRIPTION

The PrimeTime master encountered a command requiring a minimum number of hosts to be

online before allowing it to proceed. Since the number of hosts online was below the minimum, the command could not execute successfully.

WHAT NEXT

If the create_distributed_farm command has not been called to launch the remote hosts then no remote processes will have been launched. Call the create_distributed_farm command to launch the hosts.

If the create_distribued_farm command has been called use the report_distributed_hosts command to examine how many hosts have come online. Once the create_distributed_farm command has returned the user to the pt_shell prompt then hosts will come online in the background. Until sufficient hosts have come online the command specified cannot proceed.

PA-004 (warning) Slave report logging enabled.

DESCRIPTION

For several merged reporting commands, the output of the command issued to the individual partitions or scenarios is not written out to the slave output logs by default. This helps limit the size of the logs, as the information is only useful for debugging purposes.

WHAT NEXT

PA-005 (error) Distributed report message size must be greater than 0.

DESCRIPTION

WHAT NEXT

PA-006 (error) '%s' cannot be changed after slave processes have been launched.

DESCRIPTION

The working directory in which remote processes are working cannot be changed after they have been launched.

WHAT NEXT

PARA-001 (error) Cannot open file '%s'.

DESCRIPTION

The file name provided to **read_parasitics** cannot be opened.

WHAT NEXT

Validate that the file name is correct.

PARA-003 (information) The net '%s' has many (%d) nodes, which might result in long runtime.

DESCRIPTION

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the **parasitics_warning_net_size** variable (default 10000). This message warns you that extended runtime could occur.

If the number of nodes exceeds the value of **parasitics_rejection_net_size** (default 20000), the network is rejected and automatically replaced by a lumped capacitance to avoid extended runtime. You receive a message (PARA-004) warning you of that action.

The value of **parasitics_warning_net_size** is ignored if it is greater than or equal to the value of **parasitics_rejection_net_size**.

The values of these variables are checked every time **read_parasitics** is issued.

WHAT NEXT

This is an informational message only. No action is required on your part. To avoid receiving this message, you can increase the value of the **parasitics_warning_net_size** variable, or modify your parasitic network so that it contains fewer nodes.

SEE ALSO

PARA-004 (n).

PARA-004 (warning) The net '%s' has too many (%d) nodes, so a lumped capacitance will be used instead.

DESCRIPTION

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the **parasitics_rejection_net_size** variable. This message warns you that the detailed network is being replaced by a lumped total capacitance to avoid extended runtime.

If the number of nodes exceeds the value of the **parasitics_warning_net_size** variable (default 10000), you receive a message (PARA-003) warning you that extended runtime could occur.

The value of **parasitics_warning_net_size** is ignored if it is greater than or equal to the value of **parasitics_rejection_net_size**.

The values of these variables are checked every time **read_parasitics** is issued.

WHAT NEXT

If it is acceptable to you for your detailed network to be replaced by a lumped total capacitance, no action is required on your part. Otherwise, you can increase the value of the **parasitics_rejection_net_size** variable, or modify the annotated parasitic network so that it contains fewer nodes.

SEE ALSO

PARA-003 (n).

PARA-005 (error) Cannot use -keep_capacitive_coupling with %s format.

DESCRIPTION

You specified the **read_parasitics** command with the **-keep_capacitive_coupling** option, and the file format does not support it. Detailed Standard Parasitic Format (DSPF) and Reduced Standard Parasitic Format (RSPF) do not support **-keep_capacitive_coupling**.

To read this file, reenter the **read_parasitics** command without using the **-keep_capacitive_coupling** option.

PARA-006 (error) %s pin '%s' is missing in the RC annotation for net '%s'. Ignoring the incomplete RC annotation.

DESCRIPTION

You receive this message if **report_annotated_parasitics** detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network annotation on the specified net is being ignored because it is incomplete; the specified pin is not physically connected to the RC network annotation.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

This message is not issued for unconnected hierarchy pins; when these are missing in RC annotations, warning message PARA-007 is issued and the annotation is not ignored during delay calculation.

WHAT NEXT

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature **read_parasitics -complete_with** or **complete_net_parasitics**. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute **read_parasitics**.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

SEE ALSO

PARA-007 (n), **read_parasitics** (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-007 (warning) Unconnected hierarchy pin '%s' is missing

in the RC annotation for net '%s'.

DESCRIPTION

You receive this message if **read_parasitics** or **report_annotated_parasitics -check** detects an incompletely back-annotated RC network in the current design. PrimeTime can tolerate missing unconnected hierarchy pins in RC annotations, so the annotation is not ignored during delay calculation. This message is only a warning; it can be suppressed with the **suppress_message** command.

If a missing pin is not an unconnected hierarchy pin, error message PARA-006 is issued instead and the RC annotation is ignored during delay calculation.

WHAT NEXT

If you have not intentionally disconnected hierarchy pins from networks with exisiting RC annotations, investigate the source of the disconnection. Some tools temporarily add routing ports and fail to remove those unused after routing, and others disconnect test ports during scan-chain reordering.

SEE ALSO

PARA-006 (n), **read_parasitics** (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-008 (error) The RC annotation for net '%s' has too many near-zero elements.

DESCRIPTION

This message is shown if **report_annotated_parasitics** detects that the RC annotation has too many near-zero elements. Too many near-zero elements can lead to numeric instability in calculations.

A resistor with value less than or equal to 0.01 ohm is considered near-zero.

A capacitor with value less than or equal to 0.001 femtofarad is considered near-zero.

PrimeTime allows up to ten-thousand near-zero resistors and up to ten-thousand near-zero capacitors before rejecting the annotation.

Please note that near-zero capacitor elements can occur in an annotation due to specifying resistors without specifying the capacitors at resistors' nodes. In such cases PrimeTime will automatically create such capacitors with values of 0.001 femtofarad.

WHAT NEXT

The only known instance of this problem is trying to annotate a gigantic clock-tree
as a single net (i.e. with tens of thousands of fanouts) with near-zero placeholder
data. The annotation must make physical sense in order to be used in RC delay
calculations. Either the near-zero data must be changed or the net must be broken-up
into smaller segments.

SEE ALSO

read_parasitics (2), **report_annotated_parasitics** (2), **complete_net_parasitics** (2).

PARA-010 (error) multiple occurrences of net '%s' in this file. Removed parasitics from this net.

DESCRIPTION

You read a binary parasitics (SBPF) file and there were multiple occurrences of some
nets in that file, which is illegal. This is a very serious error. Either the
netlist does not match the parasitics file, or there is a problem with the writer of
the file. Each of these nets with corrupt parasitics has had its parasitics removed,
generating this message. Further, all coupling for the entire file is ignored.

The binary parasitics file is expected to be an image of parasitics. That is, it is
meant to be restored to the same netlist from which it was generated. Attempting to
restore a binary parasitics file to a different netlist is an unsupported flow.

WHAT NEXT

This condition has put the parasitics annotated on the design into an incomplete
state. This may lead to inaccurate or incorrect results. You should discontinue the
current session and determine if this is a mismatch between the file and the
netlist, or if there is a problem with the provider of the binary parasitics file.

SEE ALSO

read_parasitics (2). **PARA-011** (n).

PARA-011 (error) Due to previous errors, all effects of coupling have been ignored

from '%s'

DESCRIPTION

You receive this message in conjunction with PARA-010. You read a binary parasitics (SBPF) file and there were multiple occurrences of some nets in that file, which is illegal. Because of this problem, any effects of coupling were ignored for the file being read. If you were using *-keep_capacitive_coupling*, no new coupling capacitors would be added. If you were not using *-keep_capacitive_coupling*, no coupling capacitors would be reduced. They are simply ignored.

WHAT NEXT

It is not recommended that you continue at this point. See the documentation for PARA-010 for mode details.

SEE ALSO

read_parasitics (2). **PARA-010** (n).

PARA-020 (warning) -keep_capacitive_coupling not specified for
 a design which already has coupling.

DESCRIPTION

You receive this message from the **read_parasitics** command if you did not specify the **-keep_capacitive_coupling** option, but you previously issued a **read_parasitics** command to read an SPEF file (for the same design) and did use the **-keep_capacitive_coupling** option. This message warns you about a possible inconsistency between multiple **read_parasitics** commands.

WHAT NEXT

If you intended not to use the **-keep_capacitive_coupling** option, no action is required on your part. Otherwise, reissue **read_parasitics** and use the **-keep_capacitive_coupling** option.

PARA-027 (error) Cannot specify both the -coupling_reduction_factor and

the -keep_capacitive_coupling options.

DESCRIPTION

The **read_parasitics** command found that both the **-coupling_reduction_factor** and the **-keep_capacitive_coupling** options are set.

WHAT NEXT

Choose either the **-coupling_reduction_factor** or the **-keep_capacitive_coupling** option, but not both. If you specify the **-coupling_reduction_factor** option, the coupling capacitors are reduced to ground with the factor specified by the *factor* value, which conflicts with the use of the **-keep_capacitive_coupling** option. If you intend to keep the coupling capacitors, you do not need to specify the **-keep_capacitive_coupling** option.

SEE ALSO

read_parasitics (2).

PARA-040 (warning) Coupling capacitor (%s %s %g) on net %s is discarded because %s

DESCRIPTION

The **read_parasitics** command found a problem with a coupling capacitor and the capacitor was discarded. The reason is given in the message. Typical reasons include missing objects (nets, pins), both nodes being in the same net (self-coupling of nets is not supported), or a capacitance value less than or equal to zero.

Note that in the case of self-coupling, this message will be issued whether or not the **-keep_capacitive_coupling** option is specified.

WHAT NEXT

Examine the Standard Parasitic Exchange Format (SPEF) file for correctness.

SEE ALSO

read_parasitics (2).

PARA-041 (warning) Coupling capacitor (%s %s %g) on net %s

is reduced because %s

DESCRIPTION

You receive this message if the **read_parasitics** command found a coupling capacitor in a SPEF file which specifies a nonexistent aggressor sub-node. This error could be caused by a large RC network that was discarded by PrimeTime. This message warns you that the coupling capacitor connected being reduced (grounded).

WHAT NEXT

This is a warning message only. If it is acceptable to you that the specified coupling capacitor is grounded, no action is required on your part. Otherwise, check the consistency between the netlist and SPEF file, and check for the presence of a large RC network. Make any changes necessary, then reexecute **read_parasitics**.

PARA-043 (warning) Invalid coupling capacitor (%s %s %g) on net %s:
%s

DESCRIPTION

While reading a SPEF file, the **read_parasitics** command found an invalid coupling capacitor. This is usually due to a semantic error in the specification of the capacitor.

WHAT NEXT

The reason is given in the body of the message.

SEE ALSO

read_parasitics (2).

PARA-044 (error) Invalid %s (%s %g) on net %s:
%s

DESCRIPTION

The **read_parasitics** command found a capacitor or resistor which is invalid. This is usually due to a mismatch between the netlist and the parasitics file. The reason is

given in the body of the message.

WHAT NEXT

Examine the parasitics file for correctness.

SEE ALSO

read_parasitics (2).

PARA-045 (information) Merging parallel capacitor on net %s from %s %s with value %g: new total value %g.

DESCRIPTION

The **read_parasitics** command found a capacitor in parallel with another capacitor. This could be due to duplicate entries in a parasitics file, or a reduced coupling capacitor in a SPEF file.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2).

PARA-046 (warning) No matching coupling capacitor found with value %g for
victim net %s and
aggressor net %s:
Ground this coupling capacitor.

DESCRIPTION

The **read_parasitics** command found a coupling capacitor in the SPEF file in a victim D_NET which does not have a complimentary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is grounded.

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

SEE ALSO

read_parasitics (2).

PARA-047 (warning) Net %s has been annotated with %s %s using the %s command. This takes precedence over values from parasitics.

DESCRIPTION

The **read_parasitics** command found a network which already has annotated lumped capacitance or resistance set using the **set_load** or **set_resistance** commands, respectively. Lumped values from these commands take precedence over the values from parasitics files.

WHAT NEXT

To use the total capacitance or resistance read in from a parasitics file, you must remove the existing values by using the **remove_capacitance** or **remove_resistance** command.s PrimeTime then reverts to the detailed (or other) RC network.

SEE ALSO

read_parasitics (2), **remove_capacitance** (2), **remove_resistance** (2), **set_load** (2), **set_resistance** (2).

PARA-050 (information) Merged %d parallel coupling capacitors to total %g pf
 between file nodes '%s' and '%s'

.

DESCRIPTION

While reading a SPEF file, the **read_parasitics** command found parallel coupling capacitors between two nets which needed to be merged. These parallel coupling capacitors are replaced by a single coupling capacitor with the capacitance equal to

the sum of the capacitance of the parallel coupling capacitors. The number of capacitors, and the resulting total capacitance, are shown in the message.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2).

PARA-051 (warning) Self-coupling for net '%s' is discarded

DESCRIPTION

The **read_parasitics** command found coupling from a net to itself in a Synopsys Binary Parasitics Format (SBPF) file. PrimeTime does not support self-coupling, so this coupling is discarded. Note that this message will be issued whether or not the **-keep_capacitive_coupling** option is specified.

WHAT NEXT

No action is necessary. However, the user should determine if the application which wrote the binary parasitics file has a mode which will suppress self-coupling.

SEE ALSO

read_parasitics (2).

PARA-052 (warning) Cannot use -increment with reduced parasitics.
Net '%s' will be overwritten with %s parasitics from '%s'

DESCRIPTION

The **read_parasitics** command was used with the **-increment** option, and the net in question already has parasitics. This message is issued if the current file has reduced parasitics for the net, or if the net has reduced parasitics and the current file has detailed parasitics for the net. In any of these cases, the parasitics for the net are removed, and the parasitics from the file overwrite what was there. The **-increment** option only works for detailed parasitics.

WHAT NEXT

No action is necessary. However, the user should determine if the usage of the -`increment` option is correct.

SEE ALSO

`read_parasitics` (2).

PARA-053 (error) %s '%s' exists but is not connected to net '%s'

DESCRIPTION

The `read_parasitics` command was used to read binary parasitics. There is a mismatch between the binary parasitics file and the netlist. The data in the file indicates that the named pin or port is connected to the specified net, but it is not. This error will prevent the parasitics from being annotated on this net.

WHAT NEXT

Ensure that you are applying the correct binary parasitics file to the correct netlist.

SEE ALSO

`read_parasitics` (2).

PARA-060 (warning) failed to re-anchor parasitics on net '%s'

DESCRIPTION

An `insert_buffer` command was issued to buffer either the load or driver side pin of a net with parasitics. The parasitics are re-anchored on either the driver or load side of the buffer being inserted. If the re-anchoring failed all the parasitics of the orignial net will be removed. When this happens both the driver and load side nets of the inserted buffer will have no parasitics.

WHAT NEXT

Parasitics will only be preserved if a single load or driver pin is being buffered. Although multiple pins can be buffered parasitics will not be preserved if more than one pin is buffered.

Use set_load to try and compensate for the removed parasitics.

SEE ALSO

insert_buffer

PARA-061 (warning) failed to re-anchor parasitics on net '%s'

DESCRIPTION

A **remove_buffer** command was issued and parasitics were present on the driver and/or load side nets connected to the buffer. The parasitics with the worst ground capacitance are moved to the net resulting after the buffer removal. If the re-anchoring failed all the parasitics of the driver and/or load side nets originally connected to the buffer will be removed. When this happens the resulting net after the buffer removal will have no parasitics.

WHAT NEXT

Use report_net to examine the pins of load and driver side nets of the buffer being removed.

Use set_load to try and compensate for the removed_parasitics

SEE ALSO

remove_buffer

PARA-062 (error) -original_file_name used without -eco.

DESCRIPTION

The **original_file_name** can only be used along with the **eco** option to specify which original parasitic file that the given eco file corresponds to.

WHAT NEXT

Use -eco switch also if you are reading ECO parasitics. If not, do not use -original_file_name option.

SEE ALSO

read_parasitics

PARA-063 (error) An ECO file cannot be read without reading original parasitics in SPEF or in version 3 (or later) of SBPF.

DESCRIPTION

The **-eco** option is used to load parasitics incrementally for an ECO change after original analysis is performed. The original parasitics should be present before one can read the ECO parasitics. Also, even if the original parasitics were read using version 2 or version 1 of SBPF, ECO operation cannot be applied. Only the version 3 or later versions of SBPF can be used for ECO operations.

WHAT NEXT

Read the original parasitics before reading the ECO parasitics.

SEE ALSO

read_parasitics

PARA-064 (error) Cannot auto-determine original file name for the ECO.

DESCRIPTION

The **-eco** option is used to load ECO parasitics corresponding to a particular extraction database. In the current session, parasitics were read in using multiple files. The attempt to auto-determine the original file name failed. Use **-original_file_name** option to distinguish which parasitic file that this ECO file corresponds to.

WHAT NEXT

Give the **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-065 (error) The specified original file cannot be found.

DESCRIPTION

The specified original file can not be found. If you used **-path** option while reading the original file, please issue the same **-path** for reading the ECO file also.

WHAT NEXT

Check the file name given to **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-066 (information) Attempting to read the ECO file to determine original file name.

DESCRIPTION

The **-eco** option is specified without specifying the **-original_file_name** option. Since parasitics are annotated into the current session using multiple parasitic files, it is necessary to determine which file does the ECO file correspond to. An attempt is being made to determine this information by looking at the ECO file.

WHAT NEXT

If you do not want PTSI to auto determine this information, please provide **-original_file_name** option.

SEE ALSO

read_parasitics

PARA-067 (information) Attempting to read the parasitic file to auto-determine location transformation factors.

DESCRIPTION

The **-path** and **-increment** options are specified to read a parasitic file with locations without specifying the locations transformation factors. An attempt is

being made to determine this information by looking at the parasitic file.

WHAT NEXT

This is just information message, no action required.

SEE ALSO

read_parasitics

PARA-068 (information) Locations of block %s are being transformed for '%s' rotation, '%s' flip, '%i' X offset and '%i' Y offset.

DESCRIPTION

This message gets issued only when you are reading parasitics with locations turned on via the variable 'read_parasitics_load_locations'. It was determined that the given block is rotated, flipped and/or offset before being placed at the chip-level. Hence, the locations will be automatically transformed to global co-ordinates. Global co-ordinates are determined by looking at the file that was read in without the -path option.

WHAT NEXT

This is just an information message.

SEE ALSO

read_parasitics (2)

PARA-069 (error) Invalid '%s' scale factor '%f'.

DESCRIPTION

A parasitic scale factor is defined as a floating point number greater than ZERO. You get this message when you specified a parasitic scale factor that is less than or equal to ZERO.

WHAT NEXT

Make sure you specify correct scale factors and re-run the command.

PARA-070 (error) There are no parasitics loaded.

DESCRIPTION

You have attempted to perform an operation like scale_parasitics that requires parasitics to have been loaded but no parasitics are set on this current design.

WHAT NEXT

Read the parasitics first and re-run the command.

SEE ALSO

`read_parasitics` (2) `scale_parasitics` (2)

PARA-071 (error) No net-specific scaling has been done.

DESCRIPTION

You have attempted to reset scaling for few nets. But, reset_scale_parasitics on certain number of nets works only if there has been some previous net-specific scaling done. This message indicates that no such scaling has been done previously.

WHAT NEXT

You may not want to issue reset_scale_parasitics, you may want to use scale_parasitics instead with factors equal to 1.0.

SEE ALSO

`scale_parasitics` (2) `reset_scale_parasitics` (2)

PARA-072 (warning) No net-specific scaling has been done for

net '%s'.

DESCRIPTION

```
You have attempted to reset/report scaling for few nets. But, reset_scale_parasitics
or report_scale_parasitics on certain number of nets works only if there has been
some previous net-specific scaling done. This message indicates that no such scaling
has been done previously.
```

WHAT NEXT

```
You may not want to issue reset_scale_parasitics, you may want to use
scale_parasitics instead with factors equal to 1.0.
```

SEE ALSO

scale_parasitics (2) **reset_scale_parasitics** (2) **report_scale_parasitics** (2)

PARA-073 (error) No scaling has been done.

DESCRIPTION

```
You have attempted to reset scaling of parasitics. But, reset_scale_parasitics works
only if there has been some previous parasitic scaling done. This message indicates
that no such scaling has been done previously.
```

WHAT NEXT

```
You may not want to issue reset_scale_parasitics.
```

SEE ALSO

scale_parasitics (2) **reset_scale_parasitics** (2)

PARA-074 (error) Invalid ECO SBPF found.

DESCRIPTION

```
You have attempted to read an ECO SBPF file. PTSI determined that the ECO file does
not correspond to the original parasitic file. No coupling will be read from this
current file.
```

WHAT NEXT

You may not want to make sure you are using correct ECO SBPF file.

SEE ALSO

read_parasitics (2)

PARA-075 (error) Could not resolve net '%s'.

DESCRIPTION

This message gets issued when you are reading parasitics and a net name is found in the parasitic file that could not be resolved to any real net in the design. This happens when your physical design does not match the logical design. Net is searched by the net name and may also be searched by pin names associated on the net. This message tells you that all the searching did not the net name to any net or it resolved it to more than one net in the design.

WHAT NEXT

Make sure your parasitic file matches the design.

SEE ALSO

read_parasitics (2)

PARA-076 (error) Failed to create on-disk-caching files.

DESCRIPTION

The program failed to create temporary files for on disk caching. This can be due a number of reasons like the lack of write permissions on the specified cache directory, lack of disk space and so on.

WHAT NEXT

Verify the permissions, disk space and reissue the command

PARA-077 (information) Coupling separations are set on the

design that might overwrite the annotated cross-couplings.

DESCRIPTION

This message gets issued to inform you that you have set coupling separations for cross-talk or noise analysis and are reading parasitics. The coupling separation constraints take precedence and will overwrite the annotated cross-couplings for the specific nets.

WHAT NEXT

This is just an information. No action is required.

SEE ALSO

`read_parasitics` (2) `set_coupling_separation` (2) `report_si_delay_analysis` (2) `report_si_noise_analysis` (2)

PARA-078 (error) Could not find pin/port '%s' in design.

DESCRIPTION

You get this message when you are trying to read parasitics and a specified pin/port cannot be found in the design.

WHAT NEXT

Check the parasitic file/parasitic extractor for errors.

SEE ALSO

`read_parasitics` (2)

PARA-079 (error) Could not find net connected to pin/port '%s' in design.

DESCRIPTION

You get this message when you are trying to read binary parasitics and an unconnected pin/port is being annotated in the design.

WHAT NEXT

Check the parasitic file/parasitic extractor for errors.

SEE ALSO

read_parasitics (2)

PARA-080 (error) Cannot read variation-aware parasitics when parasitics are already present.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the design is already annotated with parasitics. This is a limitation for now, and will be supported in future.

WHAT NEXT

Remove the annotated parasitics and re-issue the read_parasitics command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-081 (error) Cannot read regular parasitics as variation-aware parasitics are already annotated on the design.

DESCRIPTION

You get this message when you are trying to read non-variation aware parasitics and variation-aware parasitics are already annotated on the design.

WHAT NEXT

Remove the annotated parasitics and re-issue read_parasitics command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-082 (error) Cannot open parasitic corner file '%s'.

DESCRIPTION

You get this message when you issue set_parasitic_corner command and the corner file cannot be opened for reading.

WHAT NEXT

Check the file permissions and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-083 (error) Unexpected data at line number '%d'.

DESCRIPTION

You get this message when you issue set_parasitic_corner and the parasitic corner file has unexpected contents.

WHAT NEXT

Check the file contents and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-084 (error) Variation-aware parasitics are not loaded.

DESCRIPTION

You get this message when you perform an operation that requires variation-aware parasitics to be set and there are no such parasitics currently annotated.

WHAT NEXT

Read the variation-aware parasitics and re-issue the command.

PARA-085 (error) Parasitic corner is not set previously.

DESCRIPTION

You get this message when you issue 'remove_parasitic_corner' to remove the
parasitic corner set for analysis in the presence of variation-aware parasitics and
the tool determines that no parasitic corner was set previously.

WHAT NEXT

No action is required.

SEE ALSO

remove_parasitic_corner (2) **set_parasitic_corner** (2) **read_parasitics** (2)
report_annotated_parasitics (2)

PARA-086 (error) Parasitic corner cannot be found.

DESCRIPTION

You get this message when you issue 'set_parasitic_corner' to set the parasitic
corner but the specified corner name cannot be found in the specified corner file.

WHAT NEXT

Check the corner file and re-issue the command.

SEE ALSO

set_parasitic_corner (2) **remove_parasitic_corner** (2) **read_parasitics** (2)
report_annotated_parasitics (2)

PARA-087 (warning) Variation multiplier value for '%s' is outside

the bounds at line '%d'.

DESCRIPTION

You get this message when you issue 'set_parasitic_corner' to set the parasitic
corner but the specified corner in the corner file contains invalid variation
multiplier values. These values are supposed to be within -3.0 to +3.0.

WHAT NEXT

Check the corner file.

SEE ALSO

set_parasitic_corner (2) **remove_parasitic_corner** (2) **read_parasitics** (2)
report_annotated_parasitics (2)

PARA-088 (error) Corner file does not match the base corner - aborting the reading. This is occuring while reading ground capacitances/resistances of net '%s'.

DESCRIPTION

You get this message when you are trying to read multiple corner parasitics but it
is found that the current corner topology does not match the base corner.

WHAT NEXT

Check the corner parasitic file and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-089 (warning) Ignoring the temperature parameter or unknown process variation parameter '%s'.

DESCRIPTION

You get this message when you are trying to read a corner file for variation-aware

parasitics but the variation parameters given in the file do not match with the defined parasitic parameters. This can also happen for temperature corner setting because PrimeTime VX does not currently support temperature as a variation.

WHAT NEXT

You may want to check the corner parasitic file.

SEE ALSO

set_parasitic_corner (2) **report_annotated_parasitics** (2)

PARA-090 (error) The "-create_default_variations" option can be used only along with "-keep_variations" option.

DESCRIPTION

You get this message when you are trying to read parasitics without keeping variation sensitivities but trying to generate default variation parameters.

WHAT NEXT

Re-issue the command without the "-create_default_variations" option.

SEE ALSO

read_parasitics (2)

PARA-091 (warning) Failed to create node map information for the parasitic file.

DESCRIPTION

You get this message when you are trying to read parasitics with keeping coupling but PT was unable to create node map information between the parasitic file and PT. This node map information is usually not needed for the operation of PT, unless when you try to read in an ECO parasitic file via "read_parasitics -eco" in future.

WHAT NEXT

You do not need to do anything.

PARA-092 (error) Cannot read variation-aware parasitics as regular parasitics are already annotated on the design.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and non-variation-aware parasitics are already annotated on the design.

WHAT NEXT

Remove the annotated parasitics and re-issue read_parasitics command.

SEE ALSO

`read_parasitics` (2) `remove_annotated_parasitics` (2)

PARA-093 (error) Number of variation parameters do not match. Aborting the reading.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

`read_parasitics` (2) `remove_annotated_parasitics` (2)

PARA-094 (error) Number of variation parameters do not match. Aborting the reading.

DESCRIPTION

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

read_parasitics (2) **remove_annotated_parasitics** (2)

PARA-095 (error) Number of corners do not match for multi-corner read.

DESCRIPTION

You get this message when you are trying to read multi-corner binary parasitic file but the number of corners from the file do not match what is set previously. Aborting the read.

WHAT NEXT

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-096 (information) Scaling parasitics to operating

temperature of '%f'.

DESCRIPTION

```
You get this message when you are trying to read variation-aware parasitic files
that have temperature sensitivities. If the operating condition temperature is
different than the (global) extraction temperature, then this message is issued to
inform you that the parasitics will be scaled to the given operating temperature.
```

WHAT NEXT

```
No need of any action.
```

SEE ALSO

`read_parasitics` (2)

PARA-097 (error) All instance paths in the -path option should correspond to valid and same sub-design.

DESCRIPTION

```
You get this message when you are trying to read parasitic files with a list of
paths specified in the -path option and not all the paths correspond to the same sub
design or some of the paths do not correspond to a valid hierarchical instances.
```

WHAT NEXT

```
Reissue the command with proper paths in the -path option.
```

SEE ALSO

`read_parasitics` (2)

PARA-098 (warning) Detected semantically incorrect SPEF in coupling section.

DESCRIPTION

```
You get this message when you are trying to read parasitic files where the coupling
capacitances are written in semantically incorrect manner. According to IEEE Std
```

SPEF, coupling should be written so that current net comes first followed by coupled
net. The application will read the file but runtime may be slower. Also, the support
is not guaranteed in future versions.

WHAT NEXT

No action needed for now, but please check with the SPEF writer tool to see why it
is not following the standard.

SEE ALSO

read_parasitics (2)

PARA-099 (error) Loading locations with simultaneous hierarchy reading is currently not supported.

DESCRIPTION

You get this message when you are trying to read parasitic files by loading the
files simulataneously using multiple instances in the -path option but have also
enabled loading locations. For loading locations, you have to issue each instance
separately in -path option.

WHAT NEXT

Please re-issue read_parasitics command with one -path at a time.

SEE ALSO

read_parasitics (2)

PARA-100 (warning) No matching coupling capacitor found with value %g for
victim net %s and
aggressor net %s:
Forcing symmetry for this coupling capacitor.

DESCRIPTION

The **read_parasitics** command found a coupling capacitor in the SPEF file in a victim

D_NET which does not have a complimentary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is forced to be symmetric, that is, a coupling capacitor of that value is created between the two nets at the given nodes. If there are similar records in the two D_NETs, but the values are dissimilar, then the result will be a single coupling capacitor with a value that is the sum of the two dissimilar values.

WHAT NEXT

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

SEE ALSO

read_parasitics (2).

PARA-101 (error) read_parasitics -eco can only be used when the program is in ECO mode.

DESCRIPTION

The **read_parasitics** command with -eco option can only be used in ECO mode.

WHAT NEXT

Use set_program_options -enable_eco to enable the ECO mode.

SEE ALSO

set_program_options (2), **sh_eco_enabled** (3).

PARA-102 (information) Reading parasitics file '%s' because parasitic information is required by the multicore master.

DESCRIPTION

During a multicore analysis using PrimeTime, the master process attempts to save runtime and memory by skipping the reading of parasitics, letting the remote processes perform this task instead. This saving is possible only when a single parasitics file, of any format other than PARA, DSPF or RSPF, is used within a session and the '-keep_capacitive_coupling', '-verbose', '-syntax_only', '-

keep_variations', or '-path' options are not used with **read_parasitics**.

However, several subsequent ECO or reporting commands will force the master to read the parasitics file: **complete_net_parasitics**, **connect/disconnect_net**, **insert/ remove_buffer**, **report_annotated_parasitics**, **scale_parasitics**, **set_parasitic_corner** and **write_parasitics**.

WHAT NEXT

No action is needed but, for optimal performance, check your script to see whether the command that forces the parasitics to be read is necessary.

SEE ALSO

read_parasitics (2),

PARA-103 (information) Parasitics file '%s' will be read by the remote processes.

DESCRIPTION

During a multicore analysis using PrimeTime, this message is outputted to indicate that the remote processes will read the parasitics file directly if it has not already been done so by the master process.

WHAT NEXT

No action necessary.

SEE ALSO

read_parasitics (2), **PARA-102** (n).

PARA-104 (error) Corner file does not match the base corner - aborting the reading. This occurs while reading coupling between nets '%s' and '%s'.

DESCRIPTION

You get this message when you are trying to read multiple corner parasitics but it is found that the current corner topology does not match the base corner in coupling section.

WHAT NEXT

Check the corner parasitic file and re-issue the command.

SEE ALSO

read_parasitics (2)

PARA-105 (warning) Parasitics file '%s' was not read by the multicore master because the multi_core_read_parasitics variable is set to 'disabled'.

DESCRIPTION

During a multicore analysis using PrimeTime, this warning is outputted to indicate that the master did not read the parasitics file because the **multi_core_read_parasitics** variable is set to 'disabled'.

WHAT NEXT

To allow the master to read the parasitics file, set **multi_core_read_parasitics** to 'auto'.

SEE ALSO

read_parasitics (2),

PLIB-100 (warning) The direction of pin "%s" in cell "%s has been changed to "%s of the corresponding cell from the %s.

DESCRIPTION

The pin direction in the design is inconsistent with that defined in the library.

WHAT NEXT

Make sure the direction of pins from library and design are consistent.

PLIB-101 (error) The direction of pin "%s" in cell "%s is not consistent with that from the design!

DESCRIPTION

The pin direction in the design is inconsistent with that defined in the library.

WHAT NEXT

Make sure the direction of pins from library and design are consistent.

PLIB-102 (error) Invalid direction for pin "%s" in library cell "%s

DESCRIPTION

The pin direction of the cell defined in the library is invalid.

WHAT NEXT

Check the pin direction of the cell in the library.

PLIB-103 (error) Can't find wire load model name.

DESCRIPTION

The wire load model name specified can not be found in Synopsys DB library.

WHAT NEXT

Check the name specified for the wire load model.

PLIB-104 (error) Can't set wire load before reading the library!

DESCRIPTION

set_wire_load_model command can not be used until Synopsys DB library has been read in.

WHAT NEXT

Please read in the library first before use the command set_wire_load_model.

PLIB-105 (error) Can't find wire load model %s.

DESCRIPTION

The wire load model name specified can not be found in Synopsys DB library.

WHAT NEXT

Check the name specified for the wire load model.

PLIB-106 (error) Mismatch in function definition.

DESCRIPTION

There is parathesis mismatching in cell function definition .

WHAT NEXT

Check the integrity of the Synopsys DB library in use.

PLIB-107 (warning) Unknown function operator %c.

DESCRIPTION

There is unknown operator found in cell function definition.

WHAT NEXT

Check the integrity of the Synopsys DB library in use.

PLIB-108 (error) Can't find pin "%s" in cell "%s

DESCRIPTION

The pin specified in cell function can not be found in verilog cell definition.

WHAT NEXT

Check the consistency between library and design.

PLIB-109 (warning) Pin "%s" of cell "%s

DESCRIPTION

The specific pin in the cell is not connected in the design netlist.

WHAT NEXT

Check the consistency between the library and the design.

PLIB-110 (warning) Pin table is not specified for cell "%s

DESCRIPTION

The cell pin information was not found in the design netlist.

WHAT NEXT

Check the consistency between library and design.

PLIB-111 (error) Can't find power supply name "%s

DESCRIPTION

The specified signal level cann't not be found in the library.

WHAT NEXT

Check the integrity of the library.

PLIB-112 (warning) Illegal direction on %s %s.

DESCRIPTION

The pin direction specified in the library is illegal. The possible pin direction
can be: input output inout internal

WHAT NEXT

Check the integrity of the library.

PLIB-113 (warning) Different directions defined for %s %s.

DESCRIPTION

Different directions defined for bus or bundle pins in the library.

WHAT NEXT

```
Check the integrity of the library.
```

PLIB-114 (warning) No members defined for bundle %s.

DESCRIPTION

```
There is no member defined for bundle pin in the library.
```

WHAT NEXT

```
Check the integrity of the library.
```

PLIB-115 (error) Can't find pin "%s" in bundle "%s

DESCRIPTION

```
There is inconsistency in bundle pin definition.
```

WHAT NEXT

```
Check the integrity of the library.
```

PLIB-116 (error) Missing bus_type attribute in synopsys lib for bus %s!

DESCRIPTION

```
bus_type attribute is not specified for bus pin.
```

WHAT NEXT

```
Check the integrity of the library.
```

PLIB-117 (error) Missing type group in synopsys lib for bus type

%s!

DESCRIPTION

The specifid bus type is not defined in the library

WHAT NEXT

Check the integrity of the library.

PLIB-118 (error) Can't find pin %s in bus %s!

DESCRIPTION

There is inconsistency in bus pin definition.

WHAT NEXT

Check the integrity of the library.

PLIB-119 (warning) Can't find pin "%s" in cell "%s

DESCRIPTION

The pin specified in cell function can not be found in verilog cell definition.

WHAT NEXT

Check the consistency between library and design.

PLIB-120 (warning) "when in power table of cell %s!

DESCRIPTION

The power tables in the library are generated by power characterization tool. The when states in power table need to be mutually exclusive in order to represent power dissipation correctly during simulation.

WHAT NEXT

Please verify the power characterization procedure.

PLIB-121 (warning) Illegal power template name "%s

DESCRIPTION

The specified power template is not defined in the library.

WHAT NEXT

Check the integrity of the library.

PLIB-122 (warning) cell=%s - size of lut values doesn't fit template %s.

DESCRIPTION

The size of power lut table doesn't fit the power template table.

WHAT NEXT

Check the integrity of library.

PLIB-123 (warning) Illegal scaling_factors name: %s.

DESCRIPTION

The specified scaling_factors is not defined in the library.

WHAT NEXT

Check the integrity of library.

PLIB-124 (error) Can't find the related pin of timing group!

DESCRIPTION

The related pin is not specified for the timing arc. The attributes that can specify
the related pin are related_pin and related_bus_pins.

WHAT NEXT

Check the integrity of library.

PLIB-125 (warning) Rising and falling power table have different dimensions in cell "%s

DESCRIPTION

The 3D power table is supported in PrimeTime PX, but the rising and falling power
tables have to be in the same dimension for a cell.

WHAT NEXT

Adjust the power table in the library.

PLIB-126 (error) Can't find equal_or_opposite_out "%s 3D power table in cell "%s

DESCRIPTION

The equal_or_opposite_out pin can not be found in the 3D power table.

WHAT NEXT

Check the integrity of library.

PLIB-127 (error) No "equal_or_opposite_output the 3d power

table in cell "%s

DESCRIPTION

The equal_or_opposite_out attricute can not be found in the 3D power table.

WHAT NEXT

Check the integrity of library.

PLIB-128 (error) Can't find cell "%s

DESCRIPTION

The cell is not defined in Synopsys DB library. Missing cell timing and power tables will cause inaccurate power analysis results.

WHAT NEXT

Add the missing timing and power tables to the library.

PLIB-129 (warning) No %s specified in the library! Taking: %s = %g.

DESCRIPTION

The mentioned attribute is not specified in Synopsys DB library. PrimeTime PX will take the default value during power simulation.

WHAT NEXT

Add the attribute into the library.

PLIB-130 (error) Illegal default_operating_conditions name: '%s'.

DESCRIPTION

The attribute specified for default_operating_conditions is not recognizable by

PrimeTime PX. The following attributes are supported by PrimeTime PX: process
temperature voltage tree_type

WHAT NEXT

Check the integrity of library. If you think that the specified attricute should be
supported, please contact Synopsys support center.

PLIB-131 (warning) Voltage from config command (%g) differs from default_operating_conditions voltage (%g) by more than 5 percent! Taking %g.

DESCRIPTION

The difference between default_operating_conditions voltage and nom_voltage
specification is more than 5%.

WHAT NEXT

Check the integrity of library.

PLIB-132 (warning) Temperature from config command (%g) differs from default_operating_conditions temperature (%g) by more than 100! Taking %g.

DESCRIPTION

The difference between the absolute values of default_operating_conditions
temperature and nom_temperature specification is more than 100.

WHAT NEXT

Check the integrity of library.

PLIB-133 (error) Illegal operating_conditions name: '%s'.

DESCRIPTION

The attribute specified for operating_conditions is not recognizable by PrimeTime

PX. The following attributes are supported by PrimeTime PX: process temperature
voltage tree_type

WHAT NEXT

Check the integrity of library. If you think that the specified attricute should be
supported, please contact Synopsys support center.

PLIB-134 (warning) Time unit "%s synopsys library for PrimeTime PX, use "ns

DESCRIPTION

The unit specified for time_unit is not recognizable by PrimeTime PX. Only "ns" and
"ps" are currently supported by PrimeTime PX.

WHAT NEXT

Check the integrity of library. If you think that the specified time unit should be
supported, please contact Synopsys support center.

PLIB-135 (warning) Capacitance unit "%s the synopsys library for PrimeTime PX, use "pf

DESCRIPTION

The unit specified for capacitive_load_unit is not recognizable by PrimeTime PX.
Only "ff" and "pf" are currently supported by PrimeTime PX.

WHAT NEXT

Check the integrity of library. If you think that the specified capacitance unit
should be supported, please contact Synopsys support center.

PLIB-136 (warning) Voltage unit "%s synopsys library for

PrimeTime PX, use "V

DESCRIPTION

The unit specified for voltage_unit is not recognizable by PrimeTime PX. Only "V"
and "v" are currently supported by PrimeTime PX.

WHAT NEXT

Check the integrity of library. If you think that the specified voltage unit should
be supported, please contact Synopsys support center.

PLIB-137 (warning) Leakage power unit "%s synopsys library for PrimeTime PX, use "W

DESCRIPTION

The unit specified for leakage_power_unit is not recognizable by PrimeTime PX. The
following units are currently supported by PrimeTime PX: mW uW nW pW

WHAT NEXT

Check the integrity of library. If you think that the specified leakage power unit
should be supported, please contact Synopsys support center.

PLIB-138 (warning) Can't find library name %s.

DESCRIPTION

Could not find the named library.

WHAT NEXT

PLIB-139 (error) Failed to read synopsys library file.

DESCRIPTION

The Synopsys library name is not specified before reading in library data.

Use set link_path or target_library to specify the library to read in. For more information, please type "man link".

PLIB-140 (warning) Synopsys library file "%s

DESCRIPTION

The specified library has already been read in by PrimeTime PX. The repeating library load command will be ignored.

WHAT NEXT

Check the command usage.

PLIB-141 (error) File name too long: %s.%s.

DESCRIPTION

The length of the library file name exceeds the limit of 1024 characters that PrimeTime PX can currently handle.

WHAT NEXT

Rename the file with a shorter name.

PLIB-142 (error) Can't open file %s!

DESCRIPTION

Not able to open the specified library file for read.

WHAT NEXT

Check the library name specified.

PLIB-143 (error) Operating condition %s is not defined. Using

default.

DESCRIPTION

An operating condition is used but it is not defined in a technology library. The operating condition is specified by the command set_oprating_conditions. If the option of this command, -library, is not specified properly, e.g., the file name or library name is not correct, this error will also occur.

WHAT NEXT

Check the library to make sure it is defined. Make sure that set_oprating_conditions is used correctly.

PLIB-144 (error) The '%s' library has not been read in yet.

DESCRIPTION

The command issued tries to access a library that does not exist in the database. The following command might trigger the generation of this error: report_lib.

WHAT NEXT

Use list_libs to find all available libraries. Make sure the library name is among the ones being reported by list_libs. Please note that the library name can be different from the library filename. Load the library into the database using read_db for a db library file and then reissue the command.

MESSAGE Error: The 'cell_lib' library has not been read in yet. (SLIB-050)

PLIB-145 (information) PrimeTime PX assumes that the fanout number for all the output ports be %s.

DESCRIPTION

Fanout number of output ports may affect the back annotation by way of wire load model. PrimeTime PX has a default value.

PLIB-146 (error) Operating condition as described below is used for power calculation: File : %s Library : %s Name : %s

DESCRIPTION

This message will help you to check if the operating conditions specified for power calculation is what you intended to set. Sometimes there could be multiple libraries read in pp_shell. And each library could have a operating conditions with the same name. By default, pp_shell will use the first one it finds. Use -library option of command set_operating_conditions to solve the ambiguity problem.

WHAT NEXT

PLIB-147 (error) File "%s

DESCRIPTION

The specified library needs to have .db as file extension.

WHAT NEXT

Use the correct extension for synopsys DB library.

PLIB-148 (error) Unable to open DBVER files - $SYNOPSYS is not set.

DESCRIPTION

Need to specify environment variable $SYNOPSYS in order to access DBVER files.

WHAT NEXT

Set your environment variable $SYNOPSYS to Synopsys tools' installation root directory.

PLIB-149 (warning) Could not read library file "%s

DESCRIPTION

Not able to read information from the specified library.

WHAT NEXT

Check the integrity of the library.

PLIB-150 (warning) '%d' is not a valid argument type.

DESCRIPTION

The argument type in the library is not supported by PrimeTime PX.

WHAT NEXT

Please check the integrity of the library.

PLIB-151 (error) library name '%s' is ambiguous, use <file_name>:<library_name> to identify library

DESCRIPTION

The command issued tries to access a library by its name when at least another
library with the same name has been read. The following command might trigger the
generation of this error: report_lib.

WHAT NEXT

Use <file_name>:<library_name> as the command argument represting the library, where
<file_name> is the name of the file containing the required library. If you are not
sure which file was used to read the required library then use list_libs -file. If
libraries with the same name are read from files that also have the same name, then
use the full pathname as the library filename.

MESSAGE Error: library name 'asic_lib' is ambiguous, use
'<file_name>:<library_name>' to identify library (SLIB-104)

PLIB-152 (warning) Can not find library cell '%s' in technology libraries.

DESCRIPTION

The specific cell is not defined in synopsys technology library. The internal power for such cell type will be zero.

WHAT NEXT

Please check your read_db command. For more accurate power simulation results, a good and complete library is recommended.

PLIB-153 (warning) Can not find power table for library cell '%s' in technology libraries.

DESCRIPTION

The power table for the specific cell is not provided in technology library. The internal power for such cell type will be zero.

WHAT NEXT

For more accurate power simulation results, a good and complete library is recommended.

PLIB-154 (warning) No library or power table in the technology library.

DESCRIPTION

No library is specified or no power table is found in the technology library. The internal power for the whole design will be zero. Only switching power will be reported!

Since no library is loaded, the pin capacitance may not be available. So, this could cause some error for back annotations. For example: set_load -subtract_pin_load report_wire -include_pin_cap

Please check your read_db command. For more accurate power simulation results, a
good and complete library should be used.

PLIB-155 (error) No synopsys library file has been read in for reporting

DESCRIPTION

No synopsys library files have been read in. Need to read in libraries before
reporting them.

WHAT NEXT

Please read in the libraries either using read_db or link command.

PLIB-156 (error) Could not find library '%s'.

DESCRIPTION

The specific library with the given name is not found in synopsys technology
library.

WHAT NEXT

Please check your library name. It may have been specified incorrectly. Or you may
have not read the library file with the given name.

PLIB-157 (error) There are multiple libraries for the library name of '%s'.

DESCRIPTION

Could not find a unique synopsys library. There are multiple libraries with the same
name. Do not know which library to report.

WHAT NEXT

Please give the unique name of libraries while reading in the libraries.

PLIB-158 (error) Can't find cell '%s' in library '%s'.

DESCRIPTION

```
The cell is not defined in Synopsys DB library. Missing cell timing and power tables
will cause inaccurate power analysis results.
```

WHAT NEXT

```
Add the missing timing and power tables to the library.
```

PLIB-159 (warning) Do not support old internal power tables attached to cell '%s' in technology libraries.

DESCRIPTION

```
For this release, PrimeTime PX doesn't support old internal power tables attached to
library cells in technology libraries. The internal power tables attached to library
cells will be ignored. The internal power tables attached to ports will be used.
```

WHAT NEXT

```
Check the integrity of library. If you think that the internal power tables attached
to library cells should still be supported, please contact Synopsys support center.
```

PLIB-160 (information) Do not support power calculation for DPCM library.

DESCRIPTION

```
PrimeTime PX doesn't support power calculation for DPCM model.
```

WHAT NEXT

PLIB-161 (information) The power model is different from the

delay model in the library.

DESCRIPTION

The delay and power models used in a technology library can be different. For example, you can use generic cmos delay model for timing tables and use non-linear power model for power tables in the library. Such kind of scenario is supported by PrimeTime PX. The power models supported by PrimeTime PX are non-linear power model (nlpm) and scalable polynomial power model (sppm).

WHAT NEXT

PLIB-162 (error) Can not find technology library in the design. Please read the technology library and run the tool again.

DESCRIPTION

To estimate the power the tool needs a technology library. Since, no library is read in, the tool will not be able to estimate power.

WHAT NEXT

Please read the technology library and run the tool again.

PLIB-163 (warning) There is neither 'related_outputs' nor 'related_input' specified under the cell-based internal power table attached to cell '%s' in technology libraries.

DESCRIPTION

The old style cell-based internal power tables require either related_outputs or related_input attributes to indicate the pin which the tables belong to.

WHAT NEXT

Check the integrity of library. Highly suggest switching to pin-based power model syntax.

PLIB-164 (warning) The "when" condition of an internal power

table for cell "%s contains only 0 or 1. Such "when table will be used as Non State-Dependent internal power table.

DESCRIPTION

```
The when condition of a power table should consist of valid pin states. Using
constants as the when condition is not allowed.
```

WHAT NEXT

```
Check the integrity of library and apply the proper when condition for the power
table.
```

PLIB-165 (warning) The 'when' condition of a leakage power table for cell '%s' contains only 0 or 1. Such 'when' condition is ignored. This table will be used as default leakage power table.

DESCRIPTION

```
The when condition of a power table should consist of valid pin states. Using
constants as the when condition is not allowed.
```

WHAT NEXT

```
Check the integrity of library and apply the proper when condition for the power
table.
```

PLIB-166 (warning) 'when' states are not mutually exclusive in internal power tables of cell '%s'!

DESCRIPTION

```
The power tables in the library are generated by power characterization tool. The
when states in internal power tables need to be mutually exclusive in order to
represent power dissipation correctly during simulation.
```

WHAT NEXT

```
Please verify the power characterization procedure.
```

PLIB-167 (warning) 'when' states are not mutually exclusive in leakage power tables of cell '%s'!

DESCRIPTION

```
The power tables in the library are generated by power characterization tool. The
when states in leakage power tables need to be mutually exclusive in order to
represent power dissipation correctly during simulation.
```

WHAT NEXT

```
Please verify the power characterization procedure.
```

PLIB-168 (warning) Found overlapped rail specific internal power tables for library cell '%s'.

DESCRIPTION

```
PrimeTime PX supports rail specific internal and leakage power tables. However, the
rail specific power tables should not overlap.
```

WHAT NEXT

```
Please check the integrity of the library.
```

PLIB-169 (warning) Found overlapped rail specific leakage power tables for library cell '%s'.

DESCRIPTION

```
PrimeTime PX supports rail specific internal and leakage power tables. However, the
rail specific power tables should not overlap.
```

WHAT NEXT

```
Please check the integrity of the library.
```

PLIB-170 (warning) Power data cann't be loaded from library file

'%s'.

DESCRIPTION

```
Libraries are loaded again to read in library power data for power analysis.
However, the named library file can not be reloaded.
```

WHAT NEXT

```
Please check the integrity of the library.
```

PLIB-171 (error) No library has been loaded for power analysis.

DESCRIPTION

```
Technology libraries are required for power analysis. Power analysis can not be
continued without loading in library.
```

WHAT NEXT

```
Please check the integrity of the library.
```

PLIB-172 (error) Power calculation can not be continued without loading in library.

DESCRIPTION

```
Technology libraries are required for power analysis. Power analysis can not be
continued without loading in library.
```

WHAT NEXT

```
Please check the integrity of the library.
```

PLIB-173 (error) Can't find pg_pin '%s' for library cell '%s'.

DESCRIPTION

```
The name specified for related_pg_pin attribute is not defined as a pg_pin for the
```

named library cell.

WHAT NEXT

Check the name specified for related_pg_pin attribute.

PLIB-174 (warning) The internal power table for cell '%s' has related_ground_pin specified, but with no related_pg_pin specification.

DESCRIPTION

Distributed power tables (NLPM) are required to have related_pg_pin specification.

WHAT NEXT

Check the NLPM power tables defined in the library

PLIB-175 (warning) The leakage power table for cell '%s' has related_ground_pin specified, but with no related_pg_pin specification.

DESCRIPTION

Distributed power tables (NLPM) are required to have related_pg_pin specification.

WHAT NEXT

Check the NLPM power tables defined in the library

PLIB-176 (error) Library '%s' is not in PG pin synax. Disabling transit power analysis in PrimeTime PX ...

DESCRIPTION

Transit power analysis in PrimeTime PX provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) with NLPM power distribution tables in PG pin syntax must be provided.

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-177 (error) Missing distributed power tables for cell '%s'. Disabling transit power analysis in PrimeTime PX ...

DESCRIPTION

Transit power analysis in PrimeTime PX provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) in PG pin syntax must be provided. For cells with multiple ground pins defined in the library, NLPM power distribution tables must be provided.

WHAT NEXT

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-178 (error) Missing ground pin definition for cell '%s' in the library. Disabling transit power analysis in PrimeTime PX ...

DESCRIPTION

Transit power analysis in PrimeTime PX provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) in PG pin syntax must be provided. For cells with multiple ground pins defined in the library, NLPM power distribution tables must be provided.

WHAT NEXT

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-179 (error) Can't find pg_pin '%s' for library cell '%s'.

DESCRIPTION

The name specified for related_ground_pin attribute is not defined as a pg_pin for the named library cell.

WHAT NEXT

Check the name specified for related_ground_pin attribute.

PRPT-098 (warning) Cell "%s

DESCRIPTION

PrimeTime-PX does not calculate power for constant cells. **report_power_calculation** command does not work for constant cells.

WHAT NEXT

Please specify non-constant cell object for **report_power_calculation** command.

PRPT-099 (error) report_power_calculation command is only allowed in the activity based power analysis flow. Please set **power_analysis_mode** to **averaged**

DESCRIPTION

The report_power_calculation command is not allowed in the time-based power analysis flow. If **power_ui_backward_compatibility** is set to true, then the variable **power_force_saif_flow** can be set to true to cause the tool to run the activity based power analysis flow during **update_power**.

WHAT NEXT

set the power analysis mode to **averaged** and re-run the command.

PRPT-100 (error) Could not get %s!

DESCRIPTION

The program is not able to get some necessary information for generating the power .rpt file.

WHAT NEXT

Action based on the message text.

PRPT-101 (error) Run out of memory!

DESCRIPTION

```
The program is not able to allocate enough memory during report generation.
```

WHAT NEXT

```
Action based on the message text.
```

PRPT-102 (warning) Could not find module "%s" in the specified block "%s

DESCRIPTION

```
The program is not able to locate the specified module in the design by its name.
```

WHAT NEXT

```
Please check if the instand name specified in analyze_power -inst option is a valid
instance name in your design.
```

PRPT-103 (warning) Could not find module "%s

DESCRIPTION

```
The program is not able to locate the specified module in the design by its name.
```

WHAT NEXT

```
Please check if the instand name specified in analyze_power -inst option is a valid
instance name in your design.
```

PRPT-104 (error) Could not open file "%s

DESCRIPTION

```
The program is not able to open the file for reporting.
```

WHAT NEXT

Check if you have the write permission in the current directory.

PRPT-105 (error) Could not open file "%s

DESCRIPTION

The program is not able to append additional information at the end of .rpt file.

WHAT NEXT

Check if the .rpt file is in the current run directory with open permission.

PRPT-106 (error) Failed to create a signal for fsdb dumping.

DESCRIPTION

The program is not able to create signal handlers during power histogram generation.

WHAT NEXT

Report this error to Synopsys Customer Service Center.

PRPT-107 (error) Can't report %s before reading the pif files!

DESCRIPTION

The design should be read first before dumping data.

WHAT NEXT

Use 'read_pif' to read in the design first.

PRPT-108 (warning) Net %s does not exist!

DESCRIPTION

The net specified cann't be found in the design.

WHAT NEXT

Check the node name specified in command 'report_net'.

PRPT-109 (error) String exceeds limit during generating file "%s

DESCRIPTION

The string was too long and exceeded the buffer limit - 2048 Bytes during generating histogram report file.

WHAT NEXT

Contact your local Synopsys Support Center.

PRPT-110 (warning) Histogram report file "%s on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

DESCRIPTION

The .out histogram report file will be closed if it is approaching the file size limit. No more power histogram data will be written out after that point. However, the time-based power histogram will still be calculated for the rest of simulation and peak powers will be reported in .rpt file.

The current size limit for .out file is 2GB.

WHAT NEXT

There are several ways to reduce the histogram report file size: 1. use "-inst" option to select instance block(s) for power analysis 2. use "-level" option to print instances from root down to the specified level 3. use "-time" option to choose the specific time window(s) for power analysis 4. increase sampling interval to reduce the amount of data

PRPT-111 (error) Not able to get the status for file "%s

DESCRIPTION

There was an error occurred during getting file size for histogram report file.

WHAT NEXT

Make sure not to remove/touch the file during the run

PRPT-112 (error) Not able to create a buffered file system for "%s

DESCRIPTION

The program is not able to open the file for reporting.

WHAT NEXT

Contact your local Synopsys Support Center.

PRPT-113 (error) Net name is not specified!

DESCRIPTION

PrimeTime PX should be told which net to report.

WHAT NEXT

Refer to man page of report_wire.

PRPT-114 (warning) Cannot report power for cell "%s it's not covered by update_power.

DESCRIPTION

The cell is not covered at the power calculating stage. So there is no power to report. To set update_power coverage, refer to update_power man page, -instance option description.

WHAT NEXT

Reset the power coverage and calculate power again.

PRPT-115 (error) Power is not calculated. Please run update_power before report_power.

DESCRIPTION

It is required that update_power be run before report_power.

WHAT NEXT

Refer to man pages of update_power and report_power.

PRPT-116 (error) There is no current design specified for reporting.

DESCRIPTION

There is inconsistancy in the design data structure.

WHAT NEXT

Make sure the pif files are read correctly. Verify the integrity of the pif files, regenerate pif if needed.

PRPT-117 (warning) The total power is below reporting threshold of %.1f. Please check your setup.

DESCRIPTION

The total power of the design is less than the reporting threshold specified in report_power command (default: 0.0).

WHAT NEXT

Please check your design setup and adjust the reporting threshold.

PRPT-118 (warning) Sampling interval %g for waveform display is too small. Reset to %gns.

DESCRIPTION

```
It is required that sampling interval be no smaller than 0.01ns.
```

WHAT NEXT

PRPT-119 (warning) The digits after the second decimal point of sampling interval are ignored.

DESCRIPTION

WHAT NEXT

PRPT-120 (error) String exceeds limit during generating file "%s.out"!

DESCRIPTION

```
The string was too long and exceeded the buffer limit - 2048 Bytes during generating
histogram report file.
```

WHAT NEXT

```
Contact your local Synopsys Support Center.
```

PRPT-121 (warning) Waveform report file "%s.out" has been closed on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

DESCRIPTION

```
The .out histogram report file will be closed if it is approaching the file size
limit. No more power histogram data will be written out after that point. However,
```

the time-based power histogram will still be calculated for the rest of simulation
and peak powers will be reported in .rpt file.

The current size limit for .out file is 2GB.

WHAT NEXT

There are several ways to reduce the histogram report file size: 1. use "-inst"
option to select instance block(s) for power analysis 2. use "-level" option to
print instances from root down to the specified level 3. use "-time" option to
choose the specific time window(s) for power analysis 4. increase sampling interval
to reduce the amount of data

PRPT-122 (warning) Waveform report file "%s.fsdb" has been closed on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

DESCRIPTION

The .out histogram report file will be closed if it is approaching the file size
limit. No more power histogram data will be written out after that point. However,
the time-based power histogram will still be calculated for the rest of simulation
and peak powers will be reported in .rpt file.

The current size limit for .fsdb file is 2GB.

WHAT NEXT

There are several ways to reduce the histogram report file size: 1. use "-inst"
option to select instance block(s) for power analysis 2. use "-level" option to
print instances from root down to the specified level 3. use "-time" option to
choose the specific time window(s) for power analysis 4. increase sampling interval
to reduce the amount of data

PRPT-123 (error) Not able to get the status for file "%s.out

DESCRIPTION

There was an error occurred during getting file size for histogram report file.

WHAT NEXT

Make sure not to remove/touch the file during the run

PRPT-124 (warning) Mode expression is not true for the given set of vectors. Therefore, power estimation is not performed. All the power numbers will be reported to be zero.

DESCRIPTION

```
Given mode expression does not evaluate to true for the given set of vectors. Since
the given mode is not excited no power will be consumed by the design.
```

WHAT NEXT

```
Please check the set of vectors, and the modal condition.
```

PRPT-125 (error) Cannot report power as rail sensitive command (e.g. set_current_rail or create_power_rail_mapping) has been issued after command update_power. Please rerun update_power to recalculate power consumption data. Or you can "set pwr_force_reporting true" to generate power report anyway.

DESCRIPTION

```
This error message can be happened for a multi-rail design. Commands
set_currentr_rail and create_power_rail_mapping can affect the power analysis
results calculated by PrimeTime PX. If any of the rail sensitive commands has been
issued after command update_power, PrimeTime PX will not report the power analysis
results unless user has set variable pwr_force_reporting to be true.
```

WHAT NEXT

```
1. rerun update_power to recalculate power consumption or 2. set pwr_force_reporting
to be true to generate power report anyway.
```

PRPT-126 (error) No object list provided to report_power_calculation command. Please refer to command

usage for more information on options.

DESCRIPTION

```
Object list is a require argument to report_power_calculation command. Without this
argument the command will not know the objects for which the power calculation
information need to be reported.
```

WHAT NEXT

```
Please refer to command usage for more information on options.
```

PRPT-127 (warning) Object "%s net or cell. No power calculation information will be reported.

DESCRIPTION

```
The object is neither a port, pin, net or a cell. In order to report power
calculation information, object has to be one of these.
```

WHAT NEXT

```
Please check if the correct object list is provided to the command.
```

PRPT-128 (warning) Leakage power table not found for cell: %s (%s) state: "%s

DESCRIPTION

```
No matching leakage power table was found for the specified cell with the specified
state condition.
```

WHAT NEXT

```
Please check if the correct options are specified in the command. Type "man
report_power_calculation" to get more information on command usage.
```

PRPT-129 (warning) Cell "%s have power table in the

technology library.

DESCRIPTION

Only leaf-level cell object has corresponding power tables defined in technology library. The report_power_calculation command can only be issued for objects that are associated with leaf cells. This excludes reporting for hierarchical cells.

WHAT NEXT

Please specify leaf cell object for report_power_calculation.

PRPT-130 (warning) Please specify the related pin for output toggle pin %s of cell: %s (%s).

DESCRIPTION

If the toggle pin is an output pin, the option -path_source is required to specify the related input pin for such output toggle. The report_power_calculation command uses path source information to pick the correct internal power table and get the input transition value if needed. If the toggle pin is an input pin, option -path_source is not needed.

WHAT NEXT

Please specify the related pin for the specified toggle pin through option -path_source.

PRPT-131 (warning) Related pin %s not found in cell: %s (%s).

DESCRIPTION

The specified related pin through option -path_source was not found in the cell.

WHAT NEXT

Please check the pin name specified in option -path_source.

PRPT-132 (warning) Pin direction unknown for pin %s in cell: %s

(%s).

DESCRIPTION

```
The specified toggle pin is neither input, inout, or output pin. The
report_power_calculation doesn't know how to report power calculation information
associated with it.
```

WHAT NEXT

```
Please check the property of the pin in the design and report this error to
Synopsys.
```

PRPT-133 (warning) Internal power table not found for cell: %s (%s) pin: %s related_pin: %s state: "%s

DESCRIPTION

```
No matching internal power table was found for the specified cell pin with the
specified related pin and state condition.
```

WHAT NEXT

```
Please check if the correct options are specified in the command. Type "man
report_power_calculation" to get more information on command usage.
```

PRPT-134 (warning) Options -state_condition, -path_source, -rise, -fall, -negative_unateness and -verbose are not valid for net objects.

DESCRIPTION

```
The options in the above list is not valid options for net objects. They will be
ignored during report_power_calculation.
```

WHAT NEXT

```
Please check if the correct options are specified in the command. Type "man
report_power_calculation" to get more information on command usage.
```

PRPT-135 (warning) Options -path_source, -rise, -fall and -negative_unateness are not valid for cell objects unless -verbose option is used.

DESCRIPTION

```
The options in the above list is not valid options for cell objects. They will be
ignored during report_power_calculation.
```

WHAT NEXT

```
Please check if the correct options are specified in the command. Type "man
report_power_calculation" to get more information on command usage.
```

PRPT-136 (warning) Internal power table not found for cell: %s (%s) pin: %s state: "%s

DESCRIPTION

```
No matching internal power table was found for the specified cell pin with the state
condition.
```

WHAT NEXT

```
Please check if the correct options are specified in the command. Type "man
report_power_calculation" to get more information on command usage.
```

PRPT-137 (information) -verbose option overwrites -state_condition option. It is equivalent to "-state_condition all -path_source all

DESCRIPTION

```
Once -verbose option is specified, -state_condition option will be ignored.
```

WHAT NEXT

```
Type "man report_power_calculation" to get more information on command usage.
```

PRPT-138 (information) -verbose option overwrites -path_source option. It is equivalent to "-state_condition all -path_source all

DESCRIPTION

Once -verbose option is specified, -path_source option will be ignored.

WHAT NEXT

Type "man report_power_calculation" to get more information on command usage.

PRPT-139 (error) Object '%s' is not a %s.

DESCRIPTION

The -only argument of the report_power command should contain a list of cells of the -cell flag is specified; a list of nets of the -net flag is specified; and a list of cells and nets if both -net and -cell are specified.

WHAT NEXT

Re-invoke the command with a valid object list with the -only argument.

PRPT-140 (error) No valid %s specified.

DESCRIPTION

The -only argument needs a list of cells if -cell is specified; a list of nets of -net is specified; and a list of nets and cells if both -cell and -net are specified. Note that if both -cell and -net are specified the -only argument should contain at least one cell and at least one net.

WHAT NEXT

Re-invoke the command with a valid list of objects in the -only argument and with a valid combination of the -cell and -net flags.

PSW

PSW-100 (warning) Can not find instance "%s" in the design. Ignoring the switching information of nets/ports under this instance.

DESCRIPTION

The instance got from the SAIF file can not be found in the netlist provided by the
user. Therefore, the switching information (probability and toggle count present in
SAIF file) of the nets/ports, hierarchically under this instance can not be
asserted. The read_saif will ignore this instance cand continue to read the
switching information of other instances.

WHAT NEXT

Make sure that strip name given by option -instance_name is correct. Also, if the
SAIF file is used for the wright design.

PSW-101 (error) Can not find top level cell. Aborting reading SAIF file.

DESCRIPTION

SAIF file reader asserts the switching information on the i instances/nets/ports
which are hierarchically either at the same or lower level than the top level cell.
Since, SAIF reader can not find the top level cell (or current design) it can not
find the elements of the design and hence can not assert switching information.

WHAT NEXT

Make sure that the correct netlist is read and also the correct top level design is
set using the command current_design. Also, check if the SAIF file is used for the
wright design.

PSW-102 (warning) Design name from SAIF file "%s" and top

level design name from netlist "%s" are not same.

DESCRIPTION

```
The design name from the header of the SAIF file and the top level design name of
the netlist does not match. The SAIF reader will ignore the design name from SAIF
file and will keep on reading the SAIF file with the top level design name from
netlist as the correct one.
```

WHAT NEXT

```
Make sure that the correct netlist is read for this SAIF file. Also, check if the
SAIF file is used for the wright design.
```

PSW-103 (warning) Direction of SAIF file is not "backward". Please make sure if correct SAIF file is read.

DESCRIPTION

```
The direction of SAIF file is other than backward. PrimeTime PX reads only backward
SAIF file. Assuming the direction to be backward and continue to read the SAIF file.
```

WHAT NEXT

```
Check if reading the correct SAIF file.
```

PSW-104 (warning) SAIFVERSION is "%s". Supported versions are "%s". Please check if the correct SAIF file is used for this design.

DESCRIPTION

```
The version of the SAIF file is different from the supported versions. This is not a
cause of concern. Just letting the user know if they using the proper application to
generate the SAIF file.
```

WHAT NEXT

```
Check if reading the correct SAIF file.
```

PSW-105 (warning) Can not open file "%s" for reading. Please provide the correct file name.

DESCRIPTION

The file can not be open for reading.

WHAT NEXT

Check if reading the correct SAIF file.

PSW-106 (warning) Time unit is not provided in SAIF file. USing default time unit of "%s".

DESCRIPTION

Time unit is not defined in SAIF file. This time unit denotes the unit of the simulation time. Therefore, will assume the default time unit.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-107 (error) Time unit "%s" provided in SAIF file is wrong. It must be one of "ns", "us", "ms", "ps", "s", and "fs".

DESCRIPTION

Time unit defined in SAIF file should be one of "ns", "us", "ms", "ps", "s", and "fs". Can not resolve the time unit, hence the SAIF reader can not continue.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-108 (error) Time unit scale factor of "%d", provided in SAIF

file is wrong. It must be one of "1", "10", and "100".

DESCRIPTION

```
Time unit scalar factor defined in SAIF file should be one of "1", "10", and "100".
Not able to resolve the time unit scale factor, therefore can not continue reading
SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-109 (error) Simulation time duration "%f" provided in SAIF file is negative. Please check the SAIF file.

DESCRIPTION

```
The duration of simulation time period defined in SAIF file is negative. The
simulation time period should be positive. The SAIF reader will stop reading SAIF
file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-110 (warning) Instance "%s" is hierarchical. Can not put state and path dependent switching information on the instance.

DESCRIPTION

```
The state and path dependent switching information can only be put on the non-
hierarchical (leaf-level) instances. In order to put state and path dependent
switching information SAIF reader requires power table information from the
technology library cell. Since, the instance is hierarchical, it is not mapped to
any technology library cell. The SAIF reader will ignore the switching information
for state and path, and continue to read other switching information in SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-111 (warning) Instance "%s" does not map to technology cell in the library. Can not put state and path dependent switching information on the instance.

DESCRIPTION

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the instance is not mapped to any technology library cell, this information is not available. The SAIF reader will ignore the switching information for state and path, and continue to read other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-112 (error) Program run out of memory.

DESCRIPTION

No more memory available.

WHAT NEXT

Reduce the size of your design and run the tool again.

PSW-113 (warning) For instance "%s", can not find power table in technology library associated with pin "%s", having when condition "%s". Hence, switching information will not be asserted for this power arc.

DESCRIPTION

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given pin, it can not assert switching information for this power arc. The SAIF reader will ignore the switching information for the power arc and continue to read other switching information in SAIF file.

Check if the SAIF file was generated correctly.

PSW-114 (warning) For instance "%s", can not find pin "%s" in the design.

DESCRIPTION

Can not find the pin, therefore switching information on the pin will not be asserted. However, the SAIF reader will continue to read the SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-115 (warning) For instance "%s", can not find pin "%s" in technology library.

DESCRIPTION

Can not find the pin in the techonlogy library cell to which the instance is mapped to, therefore switching information on the pin will not be asserted. However, the SAIF reader will continue to read the SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-116 (warning) For instance "%s", can not find power arc in technology library associated with target pin "%s", and related pin "%s", having when condition "%s". Hence, switching information will not be asserted for this power arc.

DESCRIPTION

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given target and

related pin, it can not assert switching information for this power arc. The SAIF
reader will ignore the switching information for the power arc and continue to read
other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-117 (warning) Can not find the local net for pin "%s". Hence, switching information is not asserted on the pin.

DESCRIPTION

Internally in the SAIF reader the switching information for a pin/port is stored on
the net to which this pin is connected to. Since, this pin is not connected to any
net, the SAIF reader will ignore the switching information for the pin. However it
will continue to read other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-118 (warning) Can not find the global net for pin "%s". Hence, switching information is not asserted on the pin.

DESCRIPTION

Internally in the SAIF reader the switching information for a pin/port is stored on
the net to which this pin is connected to. Since, this pin is not connected to any
net, the SAIF reader will ignore the switching information for the pin. However it
will continue to read other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-119 (error) Pin "%s", has both state and path dependent

switching information. It can have only one of these two.

DESCRIPTION

```
In a technology library cell a pin can have only one of: state dependent (SD), path
dependent (PD), or state and path dependent (SDPD) power table. However, this pin
has two or more of the above combination. Since, this scenario should not happen,
the SAIF reader can not assert switching information on the pin and will stop
reading SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-120 (warning) Can not find the global net for net "%s". Hence, switching information is not asserted on the net.

DESCRIPTION

```
Internally in the SAIF reader the switching information for a net is stored on the
global net to which this net is connected to. Since, this net is not connected to
any global net, the SAIF reader will ignore the switching information for the net.
However it will continue to read other switching information in SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-121 (warning) Can not find net/pin "%s" in the design. Hence, can not assert switching information on net/pin.

DESCRIPTION

```
Can not find the net/pin, therefore switching information on the net/pin will not be
asserted. However, the SAIF reader will continue to read the SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-122 (warning) Virtual instance "%s" does not map to technology cell in the library. Can not assert switching information on the nets/ports of the instance.

DESCRIPTION

```
In order to put switching information on a instance SAIF reader requires instance to
be mapped to technology library cell. Since, the virtual instance is not mapped to
any technology library cell, this information is not available. The SAIF reader will
ignore the switching information for this virtual instance, and continue to read
other switching information in SAIF file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-123 (warning) Virtual instance "%s" is hierarchical. Can not assert switching information on the nets/ports of instance.

DESCRIPTION

```
The virtual instance defined in SAIF file has to be non-hierarchical. Since, the
instance is hierarchical, the SAIF reader will ignore the switching information for
net/ports of instance, and continue to read other switching information in SAIF
file.
```

WHAT NEXT

```
Check if the SAIF file was generated correctly.
```

PSW-124 (warning) Virtual instance "%s" is defined to be sequential in SAIF file. However, it is mapped to non-sequential cell in technology library. Hence, switching information is not asserted on nets/ports of this instance.

DESCRIPTION

```
There is a mismatch bewtween the virtual instance defined in SAIF file and what it
has been mapped to in technology library. Therefore, the SAIF reader will ignore the
switching information for net/ports of instance, and continue to read other
```

switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-125 (warning) Virtual instance "%s" is defined to be tri-state in SAIF file. However, it is mapped to non tri-state cell in technology library. Hence, switching information is not asserted on nets/ports of this instance.

DESCRIPTION

There is a mismatch bewtween the virtual instance defined in SAIF file and what it has been mapped to in technology library. Therefore, the SAIF reader will ignore the switching information for net/ports of instance, and continue to read other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-126 (warning) For instance "%s", can not find leakage power table for state with when condition "%s". Hence, not asserting switching information for this state.

DESCRIPTION

In order to put switching information on leakage state of a instance, SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given leakage state, it can not assert switching information on this leakage state. The SAIF reader will ignore the switching information for the leakage state and continue to read other switching information in SAIF file.

WHAT NEXT

Check if the SAIF file was generated correctly.

PSW-127 (error) RTL object name is not given. Please provide RTL object name by using -rtl option.

DESCRIPTION

RTL object name is required parameter for set_rtl_to_gate_name command. Without RTL object name the command will not know one of the mapping parameter between RTL object and gate level object.

WHAT NEXT

Please provide RTL object name by using -rtl option.

PSW-128 (error) Gate level object name is not given. Please provide gate level object name by using -gate option.

DESCRIPTION

Gate level object name is required parameter for set_rtl_to_gate_name command. Without gate level object name the command will not know one of the mapping parameter between RTL object and gate level object.

WHAT NEXT

Please provide gate level object name by using -gate option.

PSW-129 (error) Gate level object "%s Therefore, will not be able to set mapping bewteen RTL and gate level objects.

DESCRIPTION

Gate level object can not be found in the netlist. Without gate level object the command will not know one of the mapping parameter between RTL object and gate level object.

WHAT NEXT

Please check if correct gate level object name is provided.

PSW-130 (error) No switching activity has been annotated. It could be the name of the current design given by option -strip_path is incorrect or the time window specified by -time is out of range.

DESCRIPTION

No switching activity has been annotated. It could be the name of the instance of the current design given by option -strip_path is incorrect or the time window specified by -time is out of range.

WHAT NEXT

Please check SAIF/VCD file and give the correct -strip_path or -time option.

PSW-131 (error) No object list provided to get_switching_activity command. Please refer to command usage for more information on options.

DESCRIPTION

Object list is a require argument to get_switching_activity command. Without this argument the command will not know the objects for which the switching activity information need to be retrieved.

WHAT NEXT

Please refer to command usage for more information on options.

PSW-132 (warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to retrieve switching activity information.

DESCRIPTION

The object is neither a port, pin, net or a cell. In order to retrieve switching activity information, object has to be one of these. The command will return value of -2 for toggle rate, glitch rate, and static probability, to indicate this.

Please check if the correct object list is provided to the command.

PSW-133 (warning) Need to provide state condition by using -state option, if path condition is provided using -path option.

DESCRIPTION

If path condition is provided using -path option, then state condition should also be provided using -state option. Using -path option indicate that user is interested in getting state dependent path dependent switching activity information. The command will return value of -2 for toggle rate and glitch rate to indicate this.

WHAT NEXT

Please provide state condition with -state option and run the command again.

PSW-134 (warning) -rise|-fall options only work when state condition is provided by using -state option. Ignoring -rise|-fall options.

DESCRIPTION

The transition edge type can be rise or fall. Therefore either -toggle_rate or -glitch_rate option should be provided as rise or fall is associated with a transition. Moreover, rise or fall transition values can be different only for state condition toggle or glitch rates. On a simple net/pin the number of rise and fall transitions will be equal. Hence, for a net/pin number of rise and fall transitions can be computed by dividing toggle rate or glitch rate by 2. Therefore, for -rise|-fall option to make sense, state condition should be provided. If -rise|-fall option is true and state condition is not given -rise|-fall options will be ignored.

WHAT NEXT

Please refer to man page of the command for more information on options.

PSW-135 (warning) Can not get net connected to the pin "%s". Therefore, will not be able to retrieve switching activity

information.

DESCRIPTION

For a pin switching activity information is stored on the net to which it is connected to. Since, the pin is not connected to any net, the switching activity information for this pin can not be retrieved. The command will return value of -2 for toggle rate, glitch rate and static probability to indicate this.

WHAT NEXT

Please check if the correct pin object is provided to the command.

PSW-136 (warning) Pin "%s" is a port. A port can not have state condition associated with it.

DESCRIPTION

Pin is a port and a port can not have state condition associated with it. Therefore, the switching activity information can not be retrieved for the given state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

WHAT NEXT

Please check if the correct pin object is provided to the command.

PSW-137 (warning) Instance "%s" is hierarchical. Can not retrieve state and path dependent switching activity information from the instance.

DESCRIPTION

State and path dependent switching activity information is present only on non-hierarchical instances. Since, this instance is hierarchical the switching activity information can not be retrieved for the given state and path conditions. The command will return value of -2 for toggle rate and glitch rate to indicate this.

WHAT NEXT

Please check if the correct instance object is provided to the command.

PSW-138 (warning) Instance "%s" does not map to technology cell in the library. Can not retrieve state and path dependent switching information from the instance.

DESCRIPTION

```
State and path dependent switching activity information is present only on non-
hierarchical instances. This non-hierarchical instance should be mapped to a
technology cell in the library to associate state and path conditions. Since, this
instance is not mapped to technology cell, the switching activity information can
not be retrieved for the given state and path conditions. The command will return
value of -2 for toggle rate and glitch rate to indicate this.
```

WHAT NEXT

```
Please check if the correct instance object is provided to the command.
```

PSW-139 (warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not retrieve switching activity information.

DESCRIPTION

```
The power arc associated with the state condition for the given pin can not be found
from the technology library. Therefore, can not retrieve switching activity
information for the given state condition. The command will return value of -2 for
toggle rate and glitch rate to indicate this.
```

WHAT NEXT

```
Please check if the correct pin object and state condition are provided to the
command.
```

PSW-140 (warning) For instance "%s", can not find pin with name "%s". Therefore, can not retrieve switching activity information.

DESCRIPTION

```
The pin with the given name can not be found in the netlist. Therefore, can not
```

retrieve switching activity information for the given pin. The command will return value of -2 for toggle rate and glitch rate to indicate this.

WHAT NEXT

Please check if the correct pin name is provided to the command.

PSW-141 (warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not retrieve switching activity information.

DESCRIPTION

The power arc for the given state condition and source and sink pins can not ne found in the technology library. Therefore, can not retrieve switching activity information for the state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

WHAT NEXT

Please check if the correct state condition and pin objects are provided to the command.

PSW-142 (warning) None of the options -toggle_rate, -glitch_rate, or -static_prob are true. By default assuming all three options to be true.

DESCRIPTION

Since, none of the options are true, default is to print all the three values if present.

WHAT NEXT

Please refer to man page of the command for more information on options.

PSW-143 (warning) For instance "%s", need to provide state

condition by using -state option.

DESCRIPTION

When the cell object is provided to the command, the intend of user assume to be
retrieving static probability on leakage state condition. Therefore, state condition
needs to be provided. If the user want to print static probability for default when
condition please use -state "default" option.

WHAT NEXT

Please refer to man page of the command for more information on options.

PSW-144 (warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not retrieve switching activity information for this state.

DESCRIPTION

The leakage power arc for the given state condition can not ne found in the
technology library. Therefore, can not retrieve switching activity information for
the state condition. The command will return value of -2 for toggle rate and glitch
rate to indicate this.

WHAT NEXT

Please check if the correct state condition and instance objects are provided to the
command.

PSW-145 (error) Need to specify values of toggle rate and glitch rate together. Can not set one value at a time.

DESCRIPTION

The toggle rate and glitch rate can not be set separately. This is a requirement of
the command.

WHAT NEXT

Please provide both values and run the command again. See command man page for more
information.

PSW-146 (error) Glitch rate is negative. Should be >= 0.

DESCRIPTION

The glitch rate is defined as (# of glitch transitions) or (# of glitch transitions)/(simulation time in library time unit), depending upon if period/clock is not provided or provided, respectively. From the definition, it is clear that minimum number of glitch transitions can be 0.

WHAT NEXT

Please provide correct value of glitch rate and run the command again.

PSW-147 (error) Toggle rate is negative. Should be >= 0.

DESCRIPTION

The toggle rate is defined as (# of glitch free transitions) or (# of glitch free transitions)/(simulation time in library time unit), depending upon if period/clock is not provided or provided, respectively. From the definition, it is clear that minimum number of glitch free transitions can be 0.

WHAT NEXT

Please provide correct value of toggle rate and run the command again.

PSW-148 (error) Static probability value should be >=0 and <= 1.0.

DESCRIPTION

Static probability is defined as the (one time of signal)/(simulation time). In other words it is defined as the fraction of time the signal is at logic state 1 (or high). From the definition it is clear that maximum and minimum values signal probability can have is 1.0 and 0.0 respectively.

WHAT NEXT

Please provide correct value of signal probability and run the command again.

PSW-149 (error) State condition should be provided if path condition is provided using -path option. Please provide state condition using -state option.

DESCRIPTION

If path condition is provided using -path option, then state condition should also be provided using -state option. Using -path option indicate that user is interested in getting state dependent path dependent switching activity information, and for this state condition should also be provided.

WHAT NEXT

Please provide state condition using -state option and run the command again.

PSW-150 (error) Rise ratio value should be >=0 and <= 1.0.

DESCRIPTION

Specifies the ratio of rise transitions to total transitions for the specified toggle/glitch rate with annotating pins that are characterized with both rise and fall internal power. The ratio_value argument is a floating point number between 0.0 (all transitions are falling) and 1.0 (all transitions are rising). You need to specify a toggle rate in order to use this option. The default value is 0.5.

WHAT NEXT

Please provide correct value of rise ratio and run the command again.

PSW-151 (error) The value of period provided is negative. Should be > 0.

DESCRIPTION

Specifies the time period for which the number of transitions given by the -toggle_rate tr_value and -glitch_rate gr_value occur; When this argument is used, the tr_value/gr_value are divided by the given period value. It is clear from the definition that the period should be greater than 0.

Please provide correct value of period and run the command again.

PSW-152 (error) -hier option works only when select types are provided using -select option.

DESCRIPTION

-hier option specifies that all the objects in all the hierarchy that satisfy the selection criteria will be annotated. It can be used only with the -select argument.

WHAT NEXT

Please provide select types using -select argument and run the command again. Please refer to command man page for more information.

PSW-153 (error) -instance option works only when select types are provided using -select option.

DESCRIPTION

-hier option specifies that all the objects in the given list of instances that satisfy the selection criteria will be annotated. It can be used only with the -select option.

WHAT NEXT

Please provide select types using -select argument and run the command again. Please refer to command man page for more information.

PSW-154 (error) At a time can provide either select types or object list.

DESCRIPTION

The object list option for explicitly specifying the objects to be annotated, and the -select option for implicitly specifying the objects to be annotated, are mutually exclusive. They can not be specified together.

WHAT NEXT

```
Please provide either select types using -select option or object list, and run the
command again. Please refer to command man page for more information.
```

PSW-155 (error) Neither object list or select types are provided. Please provide one of them and run the command again.

DESCRIPTION

```
Either the object list for explicitly specifying the objects to be annotated, or the
select types for implicitly specifying the objects to be annotated, should be
provided. .
```

WHAT NEXT

```
Please provide either select types using -select option or object list, and run the
command again. Please refer to command man page for more information.
```

PSW-156 (error) Both period and clock name are provided using -period and -clock options respectively. Can provide only one of them at a time.

DESCRIPTION

```
Both -period and -clock options specifed the time period for which the number of
transitions occur. Therefore, if both options are specified the command will not
know which period to use. Hence, can specify either -period or -clock options, not
both.
```

WHAT NEXT

```
Please use only one of -period or -clock options, and run the command again. Please
refer to command man page for more information.
```

PSW-157 (error) More than one clock is provided. Multiple

clocks are not supported.

DESCRIPTION

```
More than one clock is provided using -clock option. If nore than one clocks are
provided, the command will not know which clock period should be used. Therefore,
only one clock should be provided by -clock options.
```

WHAT NEXT

```
Please provide only one clock name using -clock options, and run the command again.
Please refer to command man page for more information.
```

PSW-158 (error) Can not find the clock with name "%s".

DESCRIPTION

```
Can not find the clock with the given name.
```

WHAT NEXT

```
Please provide correct clock name using -clock options, and run the command again.
Please refer to command man page for more information.
```

PSW-159 (error) Period of the clock "%s" is 0. Please provide different clock.

DESCRIPTION

```
Time period of the clock with the given name is 0. Time period specifies the period
for which the number of transitions occur. Therefore, period can not be 0.
```

WHAT NEXT

```
Please check if correct clock name is provided. Moreover, a different clock name can
be provided using -clock options, and command can be run again. Please refer to
command man page for more information.
```

PSW-160 (warning) Wrong select type "%s" is provided using -

select option.

DESCRIPTION

Possible select types are "regs/tris/inputs/outputs/inouts/ports/nets". When the -select option is used with one or more of the above options, all the objects in the current instance or list of instances that satisfy the selection criteria will be annotated with the specified switching activity.

WHAT NEXT

Please provide correct select types using -select option and run the command again. Please refer to command man page for more information.

PSW-161 (warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

DESCRIPTION

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

WHAT NEXT

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-162 (warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

DESCRIPTION

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

WHAT NEXT

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-163 (warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to set switching activity information.

DESCRIPTION

```
The object is neither a port, pin, net or a cell. In order to set switching activity
information, object has to be one of these.
```

WHAT NEXT

```
Please check if the correct object list is provided to the command.
```

PSW-164 (warning) For instance "%s", can not find pin with name "%s". Therefore, can not set switching activity information.

DESCRIPTION

```
The pin with the given name can not be found in the netlist, therefore switching
information can not be set on the pin.
```

WHAT NEXT

```
Please check if the correct pin name is provided is provided to the command by -path
option. Please refer to command man page for more information.
```

PSW-165 (warning) Can not get net connected to the pin "%s". Therefore, will not be able to set switching activity information.

DESCRIPTION

```
For a pin switching activity information is stored on the net to which it is
connected to. Since, the pin is not connected to any net, the switching activity
information for this pin can not be set.
```

WHAT NEXT

```
Please check if the correct pin object is provided to the command.
```

PSW-166 (warning) Pin "%s" is a port. A port can not have state condition associated with it.

DESCRIPTION

```
Pin is a port and a port can not have state condition associated with it. Therefore,
the switching activity information can not be set on the given state condition.
```

WHAT NEXT

```
Please check if the correct pin object is provided to the command.
```

PSW-167 (warning) Instance "%s" is hierarchical. Can not set state and path dependent switching activity information on the instance.

DESCRIPTION

```
State and path dependent switching activity information is present only on non-
hierarchical instances. Since, this instance is hierarchical the switching activity
information can not be set for the given state and path conditions.
```

WHAT NEXT

```
Please check if the correct instance object is provided to the command.
```

PSW-168 (warning) Instance "%s" does not map to technology cell in the library. Can not set state and path dependent switching information on the instance.

DESCRIPTION

```
State and path dependent switching activity information is present only on non-
hierarchical instances. This non-hierarchical instance should be mapped to a
technology cell in the library to associate state and path conditions. Since, this
instance is not mapped to technology cell, the switching activity information can
not be set for the given state and path conditions.
```

Please check if the correct instance object is provided to the command.

PSW-169 (warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not set switching activity information.

DESCRIPTION

The power arc associated with the state condition for the given pin can not be found
from the technology library. Therefore, can not set switching activity information
for the given state condition.

WHAT NEXT

Please check if the correct pin object and state condition are provided to the
command.

PSW-170 (warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not set switching activity information.

DESCRIPTION

The power arc for the given state condition and source and sink pins can not ne
found in the technology library. Therefore, can not set switching activity
information for the state condition.

WHAT NEXT

Please check if the correct state condition and pin objects are provided to the
command.

PSW-171 (warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not

set switching activity information for this state.

DESCRIPTION

The leakage power arc for the given state condition can not ne found in the
technology library. Therefore, can not set switching activity information for the
state condition.

WHAT NEXT

Please check if the correct state condition and instance objects are provided to the
command.

PSW-172 (error) -period or -clock option can only be used if toggle and glitch values are provided using -toggle_rate and -glitch_rate options, respectively.

DESCRIPTION

-period or -clock options specify the time period for which the number of
transitions given by the -toggle_rate and -glitch_rate options occur. If number of
transitions are not given then the time period will not be used and hence not
required.

WHAT NEXT

Please provide number of transitions using -toggle_rate and -glitch_rate options,
and run the command again. Please refer to command man page for more information.

PSW-173 (warning) No object is selected to set the specified switching activity.

DESCRIPTION

No objects can be found in the design to satisfy the criteria defined by the options
given to the set_switching_activity command.

WHAT NEXT

Give the correct options to the command.

PSW-174 (error) State condition should be provided if path condition is provided using -path option. Please provide state condition using -state option.

DESCRIPTION

```
-path option works only if state condition is provided using -state option. Both the
options are required for finding state dependent path dependent power arc. Using -
path option user is specifying the swicting activity information on state dependent
path dependent power arc to be reset.
```

WHAT NEXT

```
Please provide the state condition and run the command again. Please refer to the
command man pages for more information.
```

PSW-175 (error) State condition, using -state option, can be only be provided if the object list is non empty.

DESCRIPTION

```
-state option works only if the object list is provided. Using -state option
indicates that user wants to reset either state dependent or state dependent path
dependent information. For this the exact instance or pin object has to be provided
to the command and this can only be done through object list.
```

WHAT NEXT

```
Please provide object list and run the command again. Please refer to the command
man pages for more information.
```

PSW-176 (error) At a time can provide either instance list or object_list, not both.

DESCRIPTION

```
The object list option for explicitly specifying the objects to be annotated, and
the -instance option for implicitly specifying the objects to be annotated, are
mutually exclusive. They can not be specified together.
```

Please provide either object list or instance list and run the command again. Please refer to the command man pages for more information.

PSW-177 (error) Both state condition and instance list are provided using -state and -instance options respectively. Can provide only one of them at a time.

DESCRIPTION

-state option works only if the object list is provided. Using -state option indicates that user wants to reset either state dependent or state dependent path dependent information. For this the exact instance or pin object has to be provided to the command and this can only be done through object list.

WHAT NEXT

Please provide either state condition or instance list and run the command again. Please refer to the command man pages for more information.

PSW-178 (error) -hier option works only when instance list is provided using -instance option.

DESCRIPTION

-hier option specifies that all the objects in all the hierarchy that will be annotated. It can be used only with the -instance option.

WHAT NEXT

Please provide instance list using -instance option and run the command again. Please refer to command man page for more information.

PSW-179 (warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to reset switching activity

information.

DESCRIPTION

```
The object is neither a port, pin, net or a cell. In order to reset switching
activity information, object has to be one of these.
```

WHAT NEXT

```
Please check if the correct object list is provided to the command.
```

PSW-180 (warning) Instance "%s" can not be found in netlist. Therefore, will not be able to reset switching activity information.

DESCRIPTION

```
The instance provided by the -instance option can not be found in the netlist. The
command will ignore this instance and continue with other instances if provided.
```

WHAT NEXT

```
Please check if correct instance is provided. Please refer to command man page for
more information.
```

PSW-181 (warning) For instance "%s", can not find pin with name "%s". Therefore, can not reset switching activity information.

DESCRIPTION

```
The pin with the given name can not be found in the netlist, therefore switching
information can not be reset on the pin.
```

WHAT NEXT

```
Please check if the correct pin name is provided is provided to the command by -path
option. Please refer to command man page for more information.
```

PSW-182 (warning) Can not get net connected to the pin "%s".

Therefore, will not be able to reset switching activity information.

DESCRIPTION

```
For a pin switching activity information is stored on the net to which it is
connected to. Since, the pin is not connected to any net, the switching activity
information for this pin can not be reset.
```

WHAT NEXT

```
Please check if the correct pin object is provided to the command.
```

PSW-183 (warning) Pin "%s" is a port. A port can not have state condition associated with it.

DESCRIPTION

```
Pin is a port and a port can not have state condition associated with it. Therefore,
the switching activity information can not be reset on the given state condition.
```

WHAT NEXT

```
Please check if the correct pin object is provided to the command.
```

PSW-184 (warning) Instance "%s" is hierarchical. Can not reset state and path dependent switching activity information on the instance.

DESCRIPTION

```
State and path dependent switching activity information is present only on non-
hierarchical instances. Since, this instance is hierarchical the switching activity
information can not be reset for the given state and path conditions.
```

WHAT NEXT

```
Please check if the correct instance object is provided to the command.
```

PSW-185 (warning) Instance "%s" does not map to technology

cell in the library. Can not reset state and path dependent switching information on the instance.

DESCRIPTION

```
State and path dependent switching activity information is present only on non-
hierarchical instances. This non-hierarchical instance should be mapped to a
technology cell in the library to associate state and path conditions. Since, this
instance is not mapped to technology cell, the switching activity information can
not be reset for the given state and path conditions.
```

WHAT NEXT

```
Please check if the correct instance object is provided to the command.
```

PSW-186 (warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not reset switching activity information.

DESCRIPTION

```
The power arc associated with the state condition for the given pin can not be found
from the technology library. Therefore, can not reset switching activity information
for the given state condition.
```

WHAT NEXT

```
Please check if the correct pin object and state condition are provided to the
command.
```

PSW-187 (warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not reset switching activity information.

DESCRIPTION

```
The power arc for the given state condition and source and sink pins can not ne
found in the technology library. Therefore, can not reset switching activity
information for the state condition.
```

Please check if the correct state condition and pin objects are provided to the
command.

PSW-188 (warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not reset switching activity information for this state.

DESCRIPTION

The leakage power arc for the given state condition can not ne found in the
technology library. Therefore, can not reset switching activity information for the
state condition.

WHAT NEXT

Please check if the correct state condition and instance objects are provided to the
command.

PSW-189 (warning) Switching activity for constant net %s is ignored.

DESCRIPTION

The specified net is a constant net, meaning it is connected to VDD (logic 1) or VSS
(logic 0), or it is set by set_case_analysis. The toggle rate for the net is always
0.0. The static probability is 1.0 if it is logic 1, or 0.0 if it is logic 0. The
switching activity set by user's set_switching_activity or read_saif is not correct.
PrimeTime PX will reset it.

WHAT NEXT

This is a warning message. Make sure you specify the switching activity is correct.

PSW-190 (warning) Invalid switching activity annotation on

constant net %s is being ignored.

DESCRIPTION

```
The design contains logic 0 or 1 nets, or cell pins driven by such nets, that have
been annotated with invalid switching activity. Basically, for constants the
annotated toggle rate value must be 0. The static probability for logic 1 objects
must 1.0 and that of logic 0 must be 0.0.
```

```
Since the user annotation is clearly invalid, it is ignored and the correct
switching activity values will be used for power calculation purposes.
```

WHAT NEXT

```
This is a warning message. The invalid user annotation is being ignored during power
calculation.
```

PSW-191 (warning) Net %s has user asserted toggle rate but not the static probability. For propagation the tool will use default static probability and user asserted toggle rate for this net.

DESCRIPTION

```
Ideally the net should have either both the toggle rate and static probability
values either specified by the user or not specified by the user. When one value is
specified by the user and other is not we make some assumptions for propagation of
these values. In the case of the toggle rate user specified and static probability
not, we use default static probability value and user specified toggle rate value,
on this net, for propagation. If the static probability value is user specified and
toggle rate value is not, then we ignore static probability value, on this net, for
propagation.
```

WHAT NEXT

```
This is a warning message. Make sure specifying only one value (either toggle rate
or static probability) is intended behavior.
```

PSW-192 (warning) Net %s has user asserted static probability but not the toggle rate. For propagation the tool will ignore static

probability for this net.

DESCRIPTION

```
Ideally the net should have either both the toggle rate and static probability
values either specified by the user or not specified by the user. When one value is
specified by the user and other is not we make some assumptions for propagation of
these values. In the case of the toggle rate user specified and static probability
not, we use default static probability value and user specified toggle rate value,
on this net, for propagation. If the static probability value is user specified and
toggle rate value is not, then we ignore static probability value, on this net, for
propagation.
```

WHAT NEXT

```
This is a warning message. Make sure specifying only one value (either toggle rate
or static probability) is intended behavior.
```

PSW-193 (warning) Both -gate and -rtl options are given. Command will report gate level SAIF information.

DESCRIPTION

```
By default if both -gate and -rtl options are given to the command, command assumes
that the user wants to report gate level switching activity information. In other
words, the command will assume that -rtl opttion was not given.
```

WHAT NEXT

```
Please see the command man page for more information.
```

PSW-194 (warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

DESCRIPTION

```
The instance provided by the -instance option can not be found in the netlist. The
command will ignore this instance and continue with other instances if provided.
```

WHAT NEXT

```
Please check if correct instance is provided. Please refer to command man page for
```

more information.

PSW-195 (error) No switching activity information is annotated on the design. Therefore, can not report switching activity statistics.

DESCRIPTION

Since the user has not annotated switching activity information on nets/cells, the command will not report switching activity statistics.

WHAT NEXT

Please annotate the design before using the command.

PSW-196 (error) Simulation period is negative. Should be >= 0.

DESCRIPTION

The tool internally stores the switching activity information in terms of signal probability and transition density. For writing out SAIF file the tool needs the simulation period for converting signal probability into one time (time for which the signal has logic state 1) and zero time (time for which the signal has logic state 0), and for converting transition density into toggle count. Simulation period is the duration for which the design is simulated for. It can not be negative.

WHAT NEXT

Please provide correct value of simulation period and run the command again.

PSW-197 (error) Derating factor is negative. Should be >= 0.

DESCRIPTION

The derating factor is used for converting total glitch rate into inertial glitch portion. Since total number of glitches can not be negative, derating factor can not be negative.

WHAT NEXT

Please provide correct value of derating factor and run the command again.

PSW-198 (error) Can not get the full file name for writing.

DESCRIPTION

The command can not get the full file name for writing SAIF information. Full file name is required for write_saif command.

WHAT NEXT

Please check the writing permissions and run the command again.

PSW-199 (warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

DESCRIPTION

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

WHAT NEXT

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-200 (warning) Instance "%s" is non hierarchical. The list of instances should only contain hierarchical instances. Therefore, switching activity information will not be reported for this instance.

DESCRIPTION

The instance list provided by the -instance option should contain only hierarchical instances. The command will ignore this instance and continue with other instances if provided.

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-201 (error) The list of SAIF files and weights is empty. Please provide the list of SAIF files and their weights.

DESCRIPTION

For merging the SAIF files the command requires the list of SAIF files and their corresponding weights.

WHAT NEXT

Please provide the list of SAIF files and weights, and run the command again.

PSW-202 (error) In the list of SAIF files and weights, either -input option is not given or the order of -input and -weight options is incorrect.

DESCRIPTION

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. So, either -input option is not given or the order of -input and -weight options is incorrect. -input option should always precedes -weight option for a given SAIF file.

WHAT NEXT

Please provide the correct list of SAIF files and weights, and run the command again.

PSW-203 (error) In the list of SAIF files and weights, either -weight option is not given or the order of -input and -weight

options is incorrect

DESCRIPTION

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. So, either -weight option is not given or the order of -input and -weight options is incorrect. -input option should always precedes -weight option for a given SAIF file.

WHAT NEXT

Please provide the correct list of SAIF files and weights, and run the command again.

PSW-204 (error) The value of weight should be between 0 and 100.

DESCRIPTION

The value of weight should be between 0 and 100.

WHAT NEXT

Please specify the correct weight value and run the command again.

PSW-205 (error) There should be equal number of -input and -weight options in the list of SAIF files and weights.

DESCRIPTION

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. -input option is always followed by -weight option. Therefore, there should be equal number of -input and -weight options.

WHAT NEXT

Please specify the correct list of SAIF files and weights and run the command again.

PSW-206 (error) The sum of all weight values should euqal to

100.

DESCRIPTION

The list of all weight values should be equal to 100.

WHAT NEXT

Please specify the correct weight values and run the command again.

PT-001 (fatal) %s is not enabled.

DESCRIPTION

The application tried to reserve the specified license, but it was not available.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

PT-002 (error) Unrecognized feature name '%s'.

DESCRIPTION

You tried to get or remove a license that does not exist in the key file.

WHAT NEXT

Verify that the key file is up to date and that the feature name is spelled correctly.

PT-003 (information) You already have a '%s' license.

DESCRIPTION

You tried to get a license that is already checked out.

WHAT NEXT

Verify that the feature name is spelled correctly in case it was a different feature that you wanted to get.

PT-004 (error) You don't have a '%s' license to remove.

DESCRIPTION

```
You tried to remove a license that is not checked out.
```

WHAT NEXT

```
Verify that the feature name is spelled correctly in case it was a different feature
that you wanted to remove.
```

PT-005 (error) Can't remove your '%s' license: %s.

DESCRIPTION

```
You tried to remove a license that is locked by the application. For example, this
might be the license that is required to launch the application, or the license
might be required by a design that is in memory. The message will indicate the
condition that triggered it.
```

WHAT NEXT

```
Action based on the message text.
```

PT-006 (error) %s is not supported on '%s' platform.

DESCRIPTION

```
This is an error message indicating the command or option is not supported on the
specified platform.
```

WHAT NEXT

```
Please check the command manpage or product manuals for supported platforms. Make
sure you run this command on the platforms that are supported.
```

PT-007 (warning) %s will be obsoleted and removed from future releases

of %s starting %s on %s platforms.

DESCRIPTION

```
This is a warning message indicating the specified command, option or variable is in
the process of being obsoleted and will not be supported in future releases on the
specified platform.
```

WHAT NEXT

```
Please check the command/variable manpages, product manuals or release notes for
more details about the obsolescence, and whether there are alternative approaches or
replacements for this feature being obsoleted.
```

PT-008 (error) %s has been obsoleted since %s release and is no longer supported on %s platforms.

DESCRIPTION

```
This is an error message indicating that the specified command, option or variable
has been obsoleted and no longer supported on the specified platform.
```

WHAT NEXT

```
Please check the command/variable manpages, product manuals or release notes for
more details about the obsolescence, and whether there are alternative approaches or
replacements for this feature being obsleted.
```

PT-009 (warning) The BC_WC analysis mode will be phased out in future releases.

DESCRIPTION

```
The analysis mode you are setting, best case - worst case, is potentially inaccurate
and should be avoided for sign-off. It will be obsoleted in a future release of
PrimeTime.

For a thorough analysis, both setup and hold times should be checked at each corner
of interest using the on_chip_variation analysis mode. In the BC_WC analysis mode,
two corners are analyzed simultaneously. Hold times are checked at the fast (min)
corner, and setup times are checked at the slow (max) corner. In the fast corner,
fast slews are propagated along both the launch and capture sides of hold timing
paths. As a result, worst-case slow timing cannot be guaranteed on the hold capture
```

paths. In the slow corner, slow slews are propagated along both the launch and capture sides of setup timing paths. Again, worst-case fast timing cannot be guaranteed on the setup capture paths. In addition, the BC_WC analysis is incomplete because setup times are not cross-checked in the fast corner, and hold times are not cross-checked in the slow corner.

WHAT NEXT

Migrate flows and scripts to avoid setting BC_WC analysis mode.

PT-010 (error) %s is not enabled.

DESCRIPTION

The application tried to reserve the specified license, but it was not available.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

PT-014 (information) Successfully checked out feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-015 (information) Started queuing for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-016 (information) Still waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-017 (information) Timeout while waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in pt_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PT-018 (n).

PT-018 (information) License queuing is enabled.

DESCRIPTION

You receive this message because you have enabled licensing queuing.

The license queuing is enabled by setenv SNPSLMD_QUEUE TRUE

When enabled the following timeouts can be adjusted:

Timeout for the initial license: setenv SNPS_MAX_WAITTIME <number of seconds>

Timeout for all subsequent licenses: setenv SNPS_MAX_QUEUETIME <number of seconds>

Defaults are equivalent to setenv SNPS_MAX_WAITTIME 259200 setenv SNPS_MAX_QUEUETIME 28800

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

PTANA-001 (error) Cannot change the state of fast analysis mode because
  %s.

DESCRIPTION

This error message is issued when the attemp to change the state of fast analysis
mode fails due to the reason indicated. Most often, it happens when you are trying
to either enable or disable fast analysis mode after designs and/or libraries have
already been loaded into PrimeTime.

WHAT NEXT

Please verify the reason indicated by the error message, make sure you issue the
command 'set_program_options' earlier, e.g. before any library/design is loaded.

PTANA-002 (information) Fast analysis mode is %s.

DESCRIPTION

This information message is issued when the state of fast analysis mode is changed.

WHAT NEXT

PTANA-003 (error) %s.

DESCRIPTION

This is a generic error message.

WHAT NEXT

Please note and confirm the specific reason indicated by the error message, modify
your setting(s) accordingly, re-issue the command(s).

PTANA-004 (warning) The value of variable %s cannot be changed under fast analysis mode.

DESCRIPTION

In fast analysis mode, the values of some variables are fixed in a range.

WHAT NEXT

PTE-001 (Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

This error occurs when any arc does not exist between the two pins specified by the -from option and the -to option of set_disable_timing or remove_disable_timing commands.

WHAT NEXT

Make sure the pins really exist on the cell or the libcell.

PTE-003 (warning) Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these disabled timing arcs.

DESCRIPTION

This message is displayed when timing arcs are disabled by tool to break combinational feedback loops or when propagating constant value due to case analysis. It is not displayed for arcs that are manually disabled with the **set_disable_timing** command.

WHAT NEXT

If you want to manually break a timing loop, examine the design to see why there is combinational feedback, then choose a different point at which to break the loop. To do this, use the **set_disable_timing** command instead of letting the tool automatically break the loop. To see details on the timing loops in the design, use **check_timing -inlcude loops -verbose**.

EXAMPLE MESSAGE

Warning: Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these disabled timing arcs. (PTE-003)

PTE-004 (error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

DESCRIPTION

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, nor can you have a generated clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

PTE-005 (information) Invalidating all auto-disabled timing arcs.

DESCRIPTION

Some arcs have been enabled, forcing the tool to do loop detection from scratch. The tool therefore enables all auto-disabled arcs.

WHAT NEXT

To view all timing loops in your design, use **check_timing -loops**. To manually break the loops, use **disable_timing**.

PTE-006 (error) Cannot specify '%s' as the group name.

DESCRIPTION

Some path groups are internal and cannot be modified by you.

WHAT NEXT

Use **group_path** with a valid group name.

PTE-007 (warning) Attempting to remove a clock gating check

that was not previously set.

DESCRIPTION

Removal of clock gating check on an object is valid only if a clock gating check was set before on that object.

WHAT NEXT

This command will be ignored. Please check the spelling of the object for the **remove_clock_gating_check** command.

PTE-008 (error) No%s timing arc in cell '%s(%s)' from pin %s'%s' to pin '%s'.

DESCRIPTION

Some cell timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-009 (warning) No %s arcs from pin '%s'.

DESCRIPTION

Delay annotation does not match netlist. The message is issued because some timing arcs specified in the SDF file, or by set_annotated_delay command cannot be found in the current design.

This can happen for example when SDF file was written for one design and applied with read_sdf to a different design.

The message is also issued if set_annotated_delay command is used to annotate timing arcs that do not exit. For example due to incorrect directions of ports, such as bidirectional pin u1/PAD being connected to a net with single input port IN. Then command set_annotated_delay -net -from u1/PAD 10.2 results in PTE-009 because arc u1/PAD to IN does not exits.

The message is automatically suppressed when annotating only delta delay.

WHAT NEXT

If the message occurs during read_sdf then check that your SDF file is up-to-date with your design. If the missing arc is due to false path (e.g., in the example above the path from u1/PAD to IN would never be functionally sensitized) then suppress the message.

SEE ALSO

read_sdf (2), **set_annotated_delay** (2), **suppress_message** (2), **si_enable_analysis** (3).

PTE-010 (error) No %s arcs to pin '%s'.

DESCRIPTION

Some timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-011 (warning) No%s timing arc in cell '%s(%s)' with condition '%s' from pin %s'%s' to pin '%s'.

DESCRIPTION

Some timing arcs specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check if your SDF file is up-to-date with your design.

PTE-012 (warning) A non-unate path in clock network detected. Propagating noninverting sense for clock '%s' to endpoints through pin '%s'.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks

normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. Since it is ambiguous PrimeTime always uses the noninverting sense of clock at clock pins down stream from these pins.

WHAT NEXT

If you want to analysis both the inverted and non_inverted clock from this point set the variable timing_non_unate_clock_compatibility to false. If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-013 (warning) Some clock relationships result in a common base period which require
  clock waveforms to be expanded more than 1000 times. PrimeTime limits
  clock waveforms expansion to be no more than 1000. Please check your
  clocks and apply set_false_path between unrelated clock domains.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

If the large base period is due to the fact that clock periods do not divide evenly then PrimeTime tries to tweak the periods so that they divide evenly. Use **report_clock** to find out the exact clock period used. In any case, the PrimeTime restricts clock waveform expansion to no more than 1000.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-014 (error) No net timing arc from pin '%s' to pin '%s'.

DESCRIPTION

There were no timing arcs between the specified pins. You received this error
because the net timing arcs specified in the SDF cannot be found in the current
design, or the entered command requires the existance of a timing net arc between
the two pins.

WHAT NEXT

Check if both nets are connected to the same net. If the error is issued during
reading of a SDF file, make sure that the SDF file is up-to-date with your design.

PTE-015 (error) Net delay from pin '%s' to pin '%s' cannot be
annotated because of a timing assertion on hierarchical pin '%s'.

DESCRIPTION

When a timing assertion such as create_clock or a max_delay is specified on a
hierachical pin, SDF annotation cannot be performed between the 'from_pin' and
'to_pin' of the net. This is because of the net segmentation performed on the
hierarchical pin which is inbetween the 'from_pin' and 'to_pin'.

WHAT NEXT

It is recommened that you do not specify timing assertion on hierarchical pins.

PTE-016 (information) Expanding clock '%s' to base period of %.2f
(old period was %.2f, added %d edges).

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be
related if they are respectively related to a third clock. For example, if CLK1 is
related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is,
CLK1 is related to CLK3 even though there may not be a true path between them. Using

the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set) and expands the clock waveforms to the base period.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

PTE-017 (information) Inferring %d clock-gating checks.

DESCRIPTION

PrimeTime automatically checks setup and hold violations on gating inputs. This ensures that the clock signal is not interrupted or clipped by the gate. Disable clock gating checks by setting the variable timing_disable_clock_gating_checks to true.

WHAT NEXT

To disable automatic inferring of clock-gating checks, set the environment variable timing_disable_clock_gating_checks to true.

PTE-018 (information) Abandoning fast timing updates.

DESCRIPTION

PrimeTime has a built-in efficient algorithm to update the timing of a design, after it has been timed at least once, to accommodate a change that requires this update.

When the user makes a change that invalidates the timing of the design such as new assertions, exceptions, etc, PrimeTime automatically tries to do an incremental update_timing whenever a query is made that requires a timing update. When the number and severity of changes made since the last update is small, the incremental update provides over 10X runtime improvement over the initial timing update.

However, when those changes are large, the incremental update becomes inefficient. To ensure that the incremental update does not result in any slowdown, PrimeTime automatically switches to update from scratch a larger portion of the design than the portion immediately affected by the changes. This message informs the user of this switching. The incremental update remains faster than the update executed after an update_timing -full command.

PrimeTime provides the variable 'timing_update_effort', which can be set to "low", "medium", and "high" to control the switch to full timing updates. It is unlikely that the user would need to change the default setting of the variable. See the

manual page for this variable for more information.

WHAT NEXT

Use 'set timing_update_effort low' if timing_update_effort is medium. Use 'set
timing_update_effort medium' if timing_update_effort is high.

PTE-019 (error) report_delay_calculation is not enabled for library '%s'.

DESCRIPTION

The delay calculation report shows detailed performance information about library
cells. By default, cell delay reporting is disabled. The technology library vendor
can enable delay calculation for a library by specifying the following in the **.lib**
source:

```
library_features(report_delay_calculation);
```

WHAT NEXT

Contact your library vendor to request a library with this feature enabled.

PTE-020 (error) The master clock %s has %d edges in a period. Cannot
 do frequency multiplication.

DESCRIPTION

If the master clock of a generated clock has more than 3 edges in a
 period, you cannot generate a frequency multiplied clock from that master
 clock.

WHAT NEXT

You can use -edges option to generate the clock.

PTE-021 (error) The generated clock '%s' is in the fanout of

clock
 source %s.

DESCRIPTION

A generated clock can only be in the fanout of a clock source from which it is
generated. Here the generated clock is found to be in the fanout of some other clock
source.

WHAT NEXT

Generate this clock from a clock in whose fanout it is in.

PTE-022 (error) Generated clock '%s' is not in the fanout of its master clock.

DESCRIPTION

The generated clock is not in the fanout of the master clock with respect to which
it has been defined. A generated clock must be in the fanout of its master clock.

WHAT NEXT

Please check the design and redefine the generated clock to be in the fanout of its
master clock.

PTE-023 (warning) The generated clock '%s' has not been expanded,
 please create or activate its master clock.

DESCRIPTION

A generated clock will not expand if the master clock from which it is generated has
not been created or activated. Also if the master clock was given with a -
master_clock but does not reach the pin given with -source, this message will be
given.

WHAT NEXT

Please create or activate the master of the generated clock or change the -source

pin given. Use the **report_clock** command to see if the master clock is created or inactive.

SEE ALSO

create_clock(2), set_active_clocks(2), report_clock(2).

PTE-024 (error) The following generated clocks '%s' form a loop.

DESCRIPTION

The generated clock listed are defined in a loop. A loop of generated clocks is formed in that there is a circular dependency of generated clock to master clock.

For example, if A and B are generated clocks, and A is generated from B, and B is generated from A, there is a circular dependency.

WHAT NEXT

Remove cirular dependency in the generated clock sources.

PTE-025 (error) The master of the generated clock '%s' is not connected to any clock source.

DESCRIPTION

The master clock of a generated clock must be either a clock source, or must be connected to a clock source. If it is neither, it is an error.

WHAT NEXT

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source.

PTE-026 (information) Found %d generated clock master pins

that are not connected to clock sources.

DESCRIPTION

It gives a summary of the number of generated clock master pins that are not
connected to clock sources.

WHAT NEXT

For a more detailed description of which generated clock master pins are not
connected to any source, do check_timing -with -verbose option.

PTE-027 (information) Found %d loops in the generated clock network.

DESCRIPTION

This message gives a summary of the number of loops in the generated clock network.
If there is a circular dependency of generated clock sources and its master, there
will be a loop in the generated clock network.

WHAT NEXT

To get a more detailed description of where the generated clock loops are, use
check_timing -verbose.

PTE-028 (warning) The variables timing_disable_bus_contention_check
  and timing_disable_floating_bus_check are both set to true. Reverting the
  setting of these variables to the default (false) value.

DESCRIPTION

It is a contradiction to set the variables timing_disable_bus_contention_check and
timing_disable_floating_bus_check both to true. This is because setting the variable
timing_disable_bus_contention_check implies that the user guarantees that on all
multi-driven tri-state busses, disabling of the old drivers in the previous clock
cycle is done before the enabling of the new drivers in the current clock cycle.
This contradicts what is implied by setting the variable

timing_disable_floating_bus_check that enabling of the new drivers occurs before disabling of the old drivers. PrimeTime detects this contradiction and resets the value of the two variables to the default (false) value. In most cases, the user need not adjust these default values.

WHAT NEXT

Change your script to set both variables timing_disable_bus_contention_check and timing_disable_floating_bus_check to false, or to set only one of them to true.

PTE-030 (warning) No annotated %ss from '%s' to '%s'

DESCRIPTION

You attempted to remove an annotated delay or check between two pins and there was no annotation to remove.

WHAT NEXT

Verify that the -from and/or -to arguments in the command are correct.

PTE-031 (Warning) No annotated timing checks were removed

DESCRIPTION

The remove_annotated_check command did not find any checks to remove. If you did not limit the scope of the objects searched, then there are no checks in the design. If you did limit the search to a set of pins, cells, etc., then there are no checks on the objects which you specified.

WHAT NEXT

PTE-032 (Error) Cannot %s annotated check from '%s' to '%s':%s

DESCRIPTION

An attempt to set or remove an annotated check failed because the from and to pins specified are on different cells.

```
Specify pins which are on the same cell.
```

PTE-033 (warning) Some related clocks cannot be expanded to a common clock period
within the expansion limit of 100 times per pair of related clock.
The subject clocks are: %s, %s, ...

DESCRIPTION

```
Two clocks are related if there exists a true path between them. They can also be
related if they are respectively related to a third clock. For example, if CLK1 is
related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is,
CLK1 is related to CLK3 even though there may not be a true path between them. Using
the relatedness relation, PrimeTime partitions the clocks in the design into
mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a
base period (over all the clocks in the set) and expands the clock waveforms to the
base period.

The timing analysis when this warning is present can potentially miss some paths
from being analyzed since some clock pulse relations would not be known.

If the large base period is due to the fact that clock periods do not divide evenly
then PrimeTime tries to tweak the periods so that they divide evenly. Use
report_clock to find out the exact clock period used. In any case, the PrimeTime
restricts clock waveform expansion to no more than 100 times per pair clocks.

Sometimes unexpected clock relationships due to automatically inferred clock-gating
checks may cause a very large base period. You can disable clock-gating checks by
setting the environment variable timing_disable_clock_gating_checks to "true".
```

WHAT NEXT

```
Use set_false_path to declare that timing paths between unrelated clocks are false.
```

PTE-035 (warning) Dynamic loop breaking causes report_timing to
track a large number of paths; PrimeTime may run out of memory.
Please consider manually breaking some loop paths before

issuing report_timing.

DESCRIPTION

You receive this message if the **timing_dynamic_loop_breaking** variable is set to *true* and your design contains a large number of loops, long paths in the loops, and many non-unate arcs in the path. In this case, the **report_timing** command could consume a large amount of memory, eventually causing PrimeTime to run out of memory.

WHAT NEXT

There are two potential solutions, as follows:

1. Manually break some long loops, then reexecute **report_timing**.

2. Reset the **timing_dynamic_loop_breaking** variable to *false* to return to static loop breaking mode, then reexecute **report_timing**. While in dynamic loop breaking mode, use **report_constraint -all_violators** to verify if there are more constraining paths than static loop breaking mode reports. **report_constraint -all_violators** consumes less memory and always works in dynamic loop breaking mode.

PTE-036 (warning) User specified '%s' in set_clock_gating_check command
  overwrites what the logic function of the cell or pin implies
  that clock gating check at pin '%s' should be against the '%s' of the clock.

DESCRIPTION

You receive this message if you execute **set_clock_gating_check** with the **-high** or **-low** option, and this specification is different from the PrimeTime inference based on the logic function of the cell. This message warns you that your current specification takes precedence over the PrimeTime inference.

WHAT NEXT

Verify that your specification of **-high** or **-low** is correct; the PrimeTime inference is usually accurate. If you are satisfied that your specification is correct, no action is required on your part. Otherwise, reexecute the **set_clock_gating_check** command and do not specify **-high** or **-low** so that the PrimeTime inference remains.

PTE-037 (information) Issuing set_operating_conditions for

setting analysis mode on_chip_variation.

DESCRIPTION

You receive this message when PrimeTime puts the design in on_chip_variation
analysis mode during linking a design. PrimeTime issues a **set_operating_conditions**
command with **-analysis_type on_chip_variation**, using best-case and worst-case
operating conditions that are the same as the default operating condition in the
main library.

WHAT NEXT

This is an informational message only; no action is required on your part.

PTE-038 (warning) Net "%s" has many driver/load combinations (%d); expect performance degradation.

DESCRIPTION

You receive this message if the **update_timing** command finds a net with a large
number of driver/load combinations. This message warns you that PrimeTime could run
out of memory, because creating net arcs for each driver/load pair is very memory-
intensive. You should expect a performance degradation.

WHAT NEXT

PrimeTime can, under certain conditions, reduce the timing arcs in the net's fanin
to alleviate the problem. This can be achieved by setting
timing_reduce_multi_drive_net_arcs to true. Please refer to the man page for
timing_reduce_multi_drive_net_arcs(3) for more details.

PTE-039 (information) Issuing set_operating_conditions corresponding to timing_slew_propagation_mode setting.

DESCRIPTION

You receive this message when you set the **timing_slew_propagation_mode** variable to
worst_arrival and have specified a single operating condition using
set_operating_conditions -analysis_type single. PrimeTime cannot compute accurate
transition time for hold timing paths if the analysis type is *single*. In this case,
PrimeTime issues this message and executes a **set_operating_conditions** command with **-
analysis_type on_chip_variation**, using best-case and worst-case operating conditions
that are the same as the single operating condition under which you set the

variable.

Conversely, if you set the **timing_slew_propagation_mode** variable back to its default value of *worst_slew*, PrimeTime again issues this message and executes a **set_operating_conditions** command with **-analysis_type single**.

In both cases, PrimeTime echoes the exact command that was issued.

WHAT NEXT

This is an informational message only; no action is required on your part. However, you can avoid receiving this message by changing your script to use a **set_operating_conditions -analysis_type on_chip_variation** command with an appropriate operating condition.

PTE-040 (Warning) Source Latency defined on pin/port '%s' will overwrite the clock source latency for clock '%s' .

DESCRIPTION

You receive this message if clock source latency is defined for both a clock and its port (source pin). In this case, the source latency for the port takes precedence, because it is more specific.

WHAT NEXT

If it is acceptable to you for the source latency on the specified pin/port to overwrite the clock source latency, no action is required on your part. Otherwise, reexecute the **set_clock_latency** command with the required specifications.

PTE-041 (warning) Unable to find specified driving cell for port '%s':
expected %s/%s %s -> %s.

DESCRIPTION

The driving cell information for the specified port indicates that the port should inherit its drive capability from a certain library cell. This error indicates that the application was unable to locate a matching library cell, a pin on that library cell, or an arc between the pins. This might happen if the **link_path** variable does not contain the library for that cell, or if the cell name or pin name is incorrect. The driving cell information, set by the **set_driving_cell** command, is specified in the text of the message, and you can see it by using the **report_port** command with the **-drive** option.

WHAT NEXT

If the driving cell requires a library that has not been identified in the link path, the **link_path** variable should be changed to include that library. Otherwise, check the information for errors in the library name, library cell name, or library cell pin name.

SEE ALSO

report_port (2), **set_driving_cell** (2), **link_path** (3).

PTE-042 (warning) Conflicted logic driving pin %s, setting resolved logic value %s on pin %s.

DESCRIPTION

You receive this message because, during the propagation of case analysis or logic constants, update_timing detects two conflicting logic values propagated to a pin. (The update_timing may occur as a result of executing the **update_timing** command or other commands, such as **report_timing**.)

For example, if two strong drivers drive a net with one carrying case analysis **0** and the other carrying case analysis **1**, then a logic conflict would arise.

In these situations, **update_timing** resolves the logic conflict to **0** and continues propagating this forward in the design. The message warns you that a logic conflict has occurred at the specified pin and that it has been resolved to the specified logic value.

WHAT NEXT

The case analysis values that propagated to the pin in question should be changed to prevent the logic conflict from arising, if the resolved value propagated forward is unsuitable. To identify the case values causing the problem, perform the following steps:

1. Enable the generation of a case analysis propagation log file by setting the **case_analysis_log_file** variable to a filename of your choice.

2. Reexecute update_timing, and review the log file to determine the reason for the conflicting values.

3. Correct the problem and reexecute **update_timing**.

SEE ALSO

set_case_analysis (2), **report_timing** (2), **update_timing** (2), **case_analysis_log_file** (3).

PTE-044 (warning) In the data check from reference pin '%s' to constraint

  pin '%s', multiple clocked signals arrive at the reference pin.
  The signal driven by clock '%s' is selected by default. You can use
  set_data_check -clock to select the clock.
  timing_enable

DESCRIPTION

You receive this message during data checks performed by **update_timing**, if your
design contains multiple clocks per register, the
timing_enable_multiple_clocks_per_reg variable is set to false, and you did not
specify a clock using **set_data_check -clock**. For these conditions, PrimeTime selects
a random clock among all clocks that arrive at the reference pin, and issues this
message.

PrimeTime supports multiple clocks when the **timing_enable_multiple_clocks_per_reg**
variable is at its default setting of true. Normally, if your circuit contains more
than one clocked signal that arrives at a reference pin, you should leave this
variable at its default setting of true to analyze all clocks, or specify which
clock you want to use with **set_data_check -clock**. You can use the **-clock** option even
if you are using a library cell for the data check.

If only one clock arrives at the reference pin, you do not need to specify the
clock.

WHAT NEXT

If it is acceptable to you for the specified clock to be used by default, no action
is required on your part. Otherwise, verify that you intended for multiple clocked
signals to arrive at the reference pin of the specified data check. If not, adjust
your design accordingly.

If so, do one of the following:

• If you want all clocks to be analyzed simultaneously, set the
timing_enable_multiple_clocks_per_reg variable to true.

• If you want to select one clock to be analyzed, use **set_data_check -clock** to
select the clock to be used.

Finally, reexecute **update_timing**.

PTE-045 (warning) The generated clock '%s' does not have a valid master clock because its master clock has been removed.

DESCRIPTION

When a generated clock is created using -add option , it's master clock must be specified using -master_clock option. But if at a later time, the master clock is deleted then the dependent generated clocks would not have a valid master.

WHAT NEXT

Please make sure if the deletion of master clock is really intended. If it was intended, define a master clock for the generated clock, otherwise the generated clock would not be expanded.

SEE ALSO

create_generated_clock (2)

PTE-046 (information) Reducing %d parallel drivers:
   Reduction at net: '%s'
   Reduced to timing arcs from cell: '%s'

DESCRIPTION

The parallel timing arcs through the specified net will be reduced to a single driver cell for timing analysis purposes. This optimization is triggered when the variable timing_reduce_multi_drive_net_arcs is set to true.

WHAT NEXT

Refer to the man pages of timing_reduce_multi_drive_net_arcs(3) and timing_reduce_multi_drive_net_arcs_threshold(3) for more details.

PTE-047 (information) Cannot reduce parallel timing arcs at net '%s'

which has %d drivers x loads
Reason: Driving cell %s%s%s

DESCRIPTION

Even though the net drivers-loads product exceeds the threshold value set in
timing_reduce_multi_drive_net_arcs_threshold(3), the cells driving this net will not
be reduced for the reason specified.

WHAT NEXT

For more details regarding the restrictions on clock network parallel buffers
collapse, check the man pages for timing_reduce_multi_drive_net_arcs.

PTE-048 (information) No net arcs %s pin '%s' due to multi-drive timing arcs reduction

DESCRIPTION

The necessary timing arc to annotate does not exist because it was subject to
parallel drivers reduction instigated by setting *timing_reduce_multi_drive_net_arcs*
to true. Annotations specified as such will be ignored.

WHAT NEXT

For more details regarding reducing multi-drivers in the clock network, check the
man pages for *timing_reduce_multi_drive_net_arcs*. These messages may be suppressed
using the following command: "suppress_message PTE-048".

PTE-049 (warning) power rails of operating condition on port '%s' are incompatible with power rails of driving cell '%s'. Driving cell ignored.

DESCRIPTION

The power rails specified in the library of a driving cell must be a subset of those
specified in the operating condition. Rails are matched by name, and the order of
rails much also be identical.

Consider another operating condition or driving cell.

SEE ALSO

report_port (2), **set_operating_condition** (2), **create_operating_condition** (2), **set_driving_cell** (2),

PTE-051 (warning) Using minimum CRP value due to mismatch in the launching and %s clock edges at the common point.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. This message will occur for one of two reasons. One, the transition sense of the launching and capturing clocks at the common point differ. For example, a rising clock edge through the common point triggers the launching register and a falling clock edge through the common point triggers the capturing register. Two, the capturing register is a level-sensitive latch. In this case two CRP values will be calculated, one corresponding to the opening edge and one corresponding to the closing edge. This means that there will be a mismatch in one of these CRP values and the minimum CRP value will be used.

WHAT NEXT

For the case when the capturing device is a level-sensitive device the report should clearly indicate what edge is using the minimum CRP.

SEE ALSO

timing_remove_clock_reconvergence_pessimism (3), **report_crpr** (2).

PTE-052 (warning) For computing a common base period for a number of clocks
PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times. Since the largest period is too large compared to the smallest period,

no common base period is possible satisfying these limits, and
PrimeTime has taken the largest period as the common base
period
but still has not expanded the smallest period beyond its limit.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be
related if they are respectively related to a third clock. For example, if CLK1 is
related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is,
CLK1 is related to CLK3 even though there may not be a true path between them. Using
the relatedness relation, PrimeTime partitions the clocks in the design into
mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a
base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is
evenly divisible by every clock in the set. Since clock periods can be arbitrary
floating-point numbers, this may require some adjustments to the clock periods.
Moreover, to prevent the common base period from becoming too large, PrimeTime must
restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period: (1) The
largest clock period is so large compared to the smallest clock period that no
common base period can be computed satisfying the limits. In this case, PrimeTime
takes the largest clock period as the common base period but still does not expand
the smallest period beyond its limit; (2) A common base period is computed but it
has to be decreased to satisfy the limits; and (3) A common base period is computed
and it already satisfies the limits. This warning message handles the first case.

Sometimes unexpected clock relationships due to automatically inferred clock-gating
checks may cause a very large common base period. You can disable clock-gating
checks by setting the environment variable timing_disable_clock_gating_checks to
"true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-053 (warning) For computing a common base period for a number of clocks
PrimeTime limits the waveform expansion of the smallest
period to be no more than %d times and the waveform
expansion of the largest period to be no more than %d times.

PrimeTime has computed a common base period bounded by these limits.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, this may require some adjustments to the clock periods. Moreover, to prevent the common base period from becoming too large, PrimeTime must restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period: (1) The largest clock period is so large compared to the smallest clock period that no common base period can be computed satisfying the limits. In this case, PrimeTime takes the largest clock period as the common base period but still does not expand the smallest period beyond its limit; (2) A common base period is computed but it has to be decreased to satisfy the limits; and (3) A common base period is computed and it already satisfies the limits. This warning message handles the second case.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large common base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

WHAT NEXT

Use **set_false_path** to declare that timing paths between unrelated clocks are false.

PTE-054 (Information) Zero transition time used at to pin of annotated arcs. Delays on not annotated delay arcs will be estimated using best available slew.

DESCRIPTION

This message is issued when more than 95 percent of delay arcs on a design have annotated values and **timing_use_zero_slew_for_annotated_arcs** is set to *auto*, or when **timing_use_zero_slew_for_annotated_arcs** has been set to **always. This functionality is intended for use only on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.**

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-055 (warning) Variable "%s" must be set before link

DESCRIPTION

The PrimeTime variable indicated can only be consumed before the design is linked. That is, the current change in value will only be honored the next time the link_design command is invoked.

WHAT NEXT

Please verify that the current setting is correct. If so, either invoke the link_design command or move the variable setting to a position prior to invoking the link_design command and rerun your script.

SEE ALSO

timing_propagate_through_unclocked_registers (3)

PTE-056 (Warning) Due to the value set by timing_crpr_threshold_ps, the CRP displayed in the timing_report will lie in the range: %g < CRP < %g.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. In order to reduce the computational complexity of deriving a CRP value during update_timing, different compute mechanisme are utilized in the production of the CRP values for **report_timing** and **report_crpr**. This may result in a difference between the CRP values produced by report_timing and report_crpr. The difference will not be greater than the value of the variable, **timing_crpr_threshold** and will lie in the range: CRP(report_crpr)-threshold < CRP < CRP(report_crpr). Hence, the value of CRP used in report_timing, if different to report_crpr, will always be more pessimistic.

WHAT NEXT

If more accuracy is required in the CRP value issued by **report_timing** set the variable **timing_crpr_threshold_ps** to a lower value and execute a full **update_timing**. Setting the variable ftiming_crpr_threshold_ps to a low value will result in significantly increased runtime and memory usage.

`report_crpr` (2), `timing_remove_clock_reconvergence_pessimism` (3), `timing_crpr_threshold_ps` (3).

PTE-057 (Warning) Transition times on not annotated delay arcs have been set to zero. Cannot perform max_transition checking.

DESCRIPTION

This message issues if a zero value is used for transition time on the load pins of fully delay annotated arcs. For this reason, **report_constraint -max_transition** is disabled.

Fully annotated arcs are those with values for both rise and fall either read from an SDF file, or set with the command **set_annotated_delay**.

Zero transition times are used when more than 95 percent of delay arcs on a design have annotated values and the varibale **timing_use_zero_slew_for_annotated_arcs** is set to **auto**, or when **timing_use_zero_slew_for_annotated_arcs** is set to **always** (irrespective of the percentage of annotated delay arcs).

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality. Setting this this variable to **never will re-enable calculation of slews, and max_transition constraint checking.**

PTE-058 (Warning) timing_use_zero_slew_for_annotated_arcs will be disabled when slew propagation mode is not *worst_slew*.

DESCRIPTION

The functionality enabled by **timing_use_zero_slew_for_annotated_arcs** is compatible only with *worst_slew* slew propagation and will not be invoked when **timing_slew_propagation_mode** is set to anything other than *worst_slew*.

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-059 (Error) timing_use_zero_slew_for_annotated_arcs cannot be enabled unless timing_slew_propagation_mode is worst_slew.

DESCRIPTION

The functionality enabled by **timing_use_zero_slew_for_annotated_arcs** is compatible only with **worst_slew B slew propagation mode.**

WHAT NEXT

Setting **timing_slew_propagation_mode to worst_slew** will allow **timing_use_zero_slew_for_anntoated_arcs** to be enabled. See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

PTE-060 (warning) No clock-gating check is inferred for clock %s
 at pins %s and %s of cell %s.

DESCRIPTION

Unless the variable **timing_disable_clock_gating_checks** is set to true, PrimeTime automatically infers clock-gating checks. For this cell, PrimeTime cannot infer a clock-gating check. This happens because the logic of this cell does not provide enough information to determine whether to perform a gating check on the high level or low level of the input clock signal.

WHAT NEXT

Use **set_clock_gating_check** with either the **-high** or **-low** option to specify the level of the clock.

PTE-061 (Warning) Since the launching device is a level-sensitive latch and the variable timing_early_launch_at_borrowing_latches is set to TRUE, the

CRP for any paths launched from the latch data pin will be zero.

DESCRIPTION

You receive this message when you execute the **report_crpr** command. Since the same (early) clock arrival time is used to both launch and capture data at a level-sensitive latch with borrow, normal application of CRPR may be optimistic. For this reason the CRP is set to zero for such paths. For more details see the man page for the variable **timing_early_launch_at_borrowing_latches**.

WHAT NEXT

In order to apply CRPR to paths launched from a borrowing data pin set the variable **timing_early_launch_at_borrowing_latches** to FALSE. This is recommended for PrimeTime to minimize the overall pessimism throughout a latch-based design.

SEE ALSO

report_crpr (2), **timing_remove_clock_reconvergence_pessimism** (3), **timing_early_launch_at_borrowing_latches** (3).

PTE-062 (information) Accepted db inherited disable timing arcs to break loops.

DESCRIPTION

Accepted db inherited disable timing arcs to break loops due to a true value of the variable **timing_keep_loop_breaking_disabled_arcs**. Variable **timing_keep_loop_breaking_disabled_arcs** is false by default.

There may still be loops in the design that the db inherited disabled timing arcs did not break, they are broken using the default loop breaking technique.

There is a difference between DC and PT where additional set_case_analysis and set_disable_timing commands will not remove db inheritied disabled timing arcs.

A boolean attribute **is_db_inherited_disabled** has been added to the class timing_arcs, where true indicates an arc is a db inherited disabled arc.

The command **remove_disable_timing** may be used to remove db inherited disabled timing arcs, since these arcs are considered to be under user control.

To remove all db inherited disable timing arcs for loop breaking, issue command **remove_disable_timing** [get_timing_arcs -of [get_cell *] -filter "is_db_inherited_disabled == true"]

report_disable_timing (2), **timing_keep_loop_breaking_disabled_arcs** (3).

PTE-063 (warning) Resetting value of variable timing_keep_loop_breaking_disabled_arcs will have no effect.

DESCRIPTION

Resetting value of variable **timing_keep_loop_breaking_disabled_arcs** will have no effect after accepting db inherited disable timing arcs to break loops. This value of this variable is only checked during linking.

If the user wishes to remove the db inherited disable timing arcs, issue command **remove_disable_timing** [get_timing_arcs -of [get_cell *] -filter "is_db_inherited_disabled == true"]

SEE ALSO

report_disable_timing (2), **timing_keep_loop_breaking_disabled_arcs** (3).

PTE-064 (information) Related clock set %d includes clock '%s' with period %.2f.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message says that this clock is a member of this clock set.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

SEE ALSO

set_clock_groups (2), **set_false_path** (2).

PTE-065 (information) Related clock set %d has base period %.2f.

DESCRIPTION

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message shows the base period of this clock set.

WHAT NEXT

It is recommened that you mark paths between unrelated clocks as false.

SEE ALSO

set_clock_groups (2), **set_false_path** (2).

PTE-066 (Warning) Zero transition time will be used at to pins of annotated arcs since more than 95 percent of delay arcs are annotated. Delays on not annotated delay arcs will be estimated using best available slew.

DESCRIPTION

If more than 95 percent of delay arcs on a design have annotated values, the SDF flow is automatically switched on during the timing update or during the execution of **report_annotated_delay**. Note that issuing **read_sdf** with the **-verbose** option will implicitly call **report_annotated_delay**. Switching on of the SDF flow will result in faster performance of update_timing, at the expense of no longer calculating the slews on the load pins of annotated arcs.

This functionality is intended for use on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.

WHAT NEXT

See man page of **timing_use_zero_slew_for_annotated_arcs** for more details on this functionality.

To avoid the SDF flow being automatically switched on, set
timing_use_zero_slew_for_annotated_arcs to *never*.

PTE-067 (warning) Setting this variable to a lower value can cause a significant performance degradation during a timing update.

DESCRIPTION

You receive this message when setting the variable **timing_crpr_threshold_ps**. Turning CRPR on can cause a noticable performance degradation both in terms of CPU and capacity. Further to this, setting the variable to values lower than the default (20ps) can further degrade performance with little corresponding increase in the accuracy of the CRP calculation. See the man page for **timing_crpr_threshold_ps** for more details.

WHAT NEXT

The recommended setting for the variable **timing_crpr_threshold_ps** is about one half of the stage (gate plus net) delay of a typical stage in the clock network.

PTE-068 (information) Using CRPR on a pre-layout clock network can cause performance degradation during a timing update.

DESCRIPTION

You receive this message during a timing update. The CRPR algorithm is optimized for post layout clock networks. Because of this fact it is not recommended to use this algorithm on a pre-layout (pre-clock tree synthesis) clock network as it can lead to degradation in both CPU performance and in capacity.

WHAT NEXT

In order to alleviate performance concerns turn CRPR off by setting the variable **timing_remove_clock_reconvergence_pessimism** to false.

SEE ALSO

timing_remove_clock_reconvergence_pessimism (3).

PTE-069 (error) The requested clock sense at pin '%s' for clock '%s' does not exist. Propagating the '%s' sense of the clock through this pin.

DESCRIPTION

There is a 'set_clock_sense' directive at the pin given and the requested clock sense does not exist at the pin for the given clock. This may be due to a conflicting 'set_clock_sense' directive on a previous pin or it may be because the only clock paths to that pin are not of the sense requested.

WHAT NEXT

Remove the conflicting 'set_clock_sense' directives.

PTE-070 (information) A non-unate path in clock network detected. Propagating both inverting and noninverting senses of clock '%s' from pin '%s'.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. This is an informational message that such a pin has been detected and that PrimeTime is propagating both senses of clock.

WHAT NEXT

If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-071 (warning) The '%s' edge of clock '%s' through pin '%s' causes the clock to both rise and fall.

A generated clock is needed at this pin.

DESCRIPTION

```
The clock tree for the specified clock contains two half unate paths such that the
clock edge given causes both a rising and falling clock edges and the other edge of
clock causes no change. This type of edge relationship requires that a generated
clock be added. In the 'create_generated_clock' command, use of non-monitomic edges
such as (1 1 3) or (2 2 4).
```

WHAT NEXT

```
Place a generated clock at the given pin.
```

PTE-072 (Warning) SI analysis is not enabled, therefore the adaptive CRPR engine will not be used.

DESCRIPTION

```
You receive this message during a timing update if the variable
timing_crpr_enable_adaptive_engine is set to TRUE and SI analysis is turned off
(si_enable_analysis). The adaptive CRPR engine applicable only when SI is turned on
therefore will have no effect on the non-SI timing update.

See the man page for timing_crpr_enable_adaptive_engine for more details.
```

WHAT NEXT

```
If the users intention is to perform an SI analysis then set the variable
si_enable_analysis to TRUE. Otherwise turn off the adaptive CRPR engine by setting
timing_crpr_enable_adaptive_engine to FALSE.
```

SEE ALSO

```
timing_crpr_enable_adaptive_engine (3), timing_remove_clock_reconvergence_pessimism
(3).
```

PTE-073 (Warning) Turning off Adaptive CRPR.

DESCRIPTION

```
You receive this message during a timing update if the variable
timing_crpr_enable_adaptive_engine is set to TRUE and either the max SI iteration
```

count (set by **si_xtalk_exit_on_max_iteration_count**) or the max SI incremental iteration count (set by **si_xtalk_exit_on_max_iteration_count_incr**) is set to 1.

The adaptive CRPR engine requires at least two SI iterations to perform its analysis. Because of this the adaptive engine is turned off and standard CRPR analysis is performed.

See the man page for **timing_crpr_enable_adaptive_engine** for more details.

WHAT NEXT

Set the variable **si_xtalk_exit_on_max_iteration_count** to at least 2 and repeat the timing update.

SEE ALSO

si_xtalk_exit_on_max_iteration_count (3) **timing_crpr_enable_adaptive_engine** (3), **timing_remove_clock_reconvergence_pessimism** (3).

PTE-074 (warning) At pin '%s' clock '%s' does not have the needed %s edge.

DESCRIPTION

The clock tree contains half unate timing arcs or disable timing commands that have disabled the needed rise or fall edge. The register clock pin given will not have the clock assigned to it and will not be timed.

WHAT NEXT

Alter clock network to propagate the needed clock edge to this register.

PTE-075 (warning) Generated clock '%s' has no path to its master clock.

DESCRIPTION

The generated clock has no path to the master clock on which it has been defined. This may be because there is no physical path, or because the generated clock has been defined as a -combinational and the generated clock is not in the direct fanout of the master clock. A propagated source latency of zero will be use from the master clock to the generated clock.

WHAT NEXT

Please check the design and redefine the generated clock to be in the fanout of its
master clock.

DESCRIPTION

To conserve memory, PrimeTime retains arrival, required and slack information only
where necessary to service the timing update and standard reporting requirements.
This warning was issued to indicate that the command the user issued does not work
under the current analysis settings.

WHAT NEXT

No explicit action is required on your part - under these circumstances PrimeTime
adjusts the analysis settings as needed, updates timing and proceeds with the
execution of the command.

SEE ALSO

timing_save_pin_arrival_and_slack (3) **timing_save_pin_arrival_and_required** (3)

DESCRIPTION

This command requires that additional slack-related info be available throughout the
design for execution. To produce this information, an additional timing update will
be incurred. In order to avoid the extra CPU cost of this additional update the
variable should be set to TRUE before the initial timing update in this flow.

WHAT NEXT

The optimal flow for any commands requiring pin arrivals and slacks is to set the
associated variable to TRUE before the initial timing update. This prevents the need
for additional work before and command requiring arrivals and slacks is executed.

PTE-079 (Warning) The %s attribute does not exist on the given pin because %s is set to FALSE.

DESCRIPTION

To conserve memory, PrimeTime retains arrival, required and slack information only
where necessary to service the timing update and standard reporting requirements.
This warning was issued to indicate that the attribute the user queried does not

exist for the given pin under the current analysis settings.

WHAT NEXT

Set the variable appearing in the warning message to TRUE.

SEE ALSO

timing_save_pin_arrival_and_slack (3) **timing_save_pin_arrival_and_required** (3)

PTE-080 (Error) pulse clock sense merging at pin: '%s' for clock: '%s' The clock will not propagate forward from this pin.

DESCRIPTION

A pulse clock is combinationally combining with another sense of the same clock.
PrimeTime does not resolve this conflict. Any registers down stream from this point
will be have this clock assigned to them.

WHAT NEXT

Resolve the conflict by specifying the sense of the clock used through this pin by
using the command 'set_clock_sense'.

PTE-081 (error) Can not honor set_clock_sense -pulse option at pin '%s'. Clock '%s' is missing needed rise and/or fall, or has conflicting high or low pulse types at this pin

DESCRIPTION

The user has specified a set_clock_sense -pulse option at the given pin. The needed
clock senses were not available at this pin. For example, a
'rise_triggered_high_pulse' expects to find a clock source rise to this pin rise
path and a clock source rise to this pin fall path. If both paths can not be found
this message will be issued. There can be conflict between the pulse type
propagating and that set by set_clock_sense -pulse. For example, if the propagating
pulse is high and user sets a low pulse type at a pin, then this message will be
issued. The pulse clock assignment for registers down stream from this pin will not
be correct.

Change the options to the command 'set_clock_sense'.

PTE-082 (warning) Connected pin groups were detected that may generate a very large
number of loops. Please check the validity of this feedback logic by
inspecting the connected pin groups above. Dynamic loop breaking is
being disabled.

DESCRIPTION

```
The design contains one or more regions of logic which have combinational feedback.
PrimeTime has identified these regions of connected pin groups which have the
potential to generate a large number of combinational loops. Because the number of
loops increases exponentially with the number of pins, these regions have the
potential to exceed the limits of the machine during dynamic loop breaking. Dynamic
loop breaking is being disabled.
```

WHAT NEXT

```
Check the listed pin groups to ensure that the combinational feedback loops are
expected and correct in the design. If they are unavoidable, manually disable
dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.
```

PTE-083 (warning) Connected pin groups were detected that generate a large number of
loops. Here is the connected pin group that has generated the
largest number of loops so far. Dynamic loop breaking will
continue, which may exceed the machine's capabilities.

DESCRIPTION

```
The design contains one or more regions of logic which have combinational feedback.
PrimeTime has identified a region of logic which has a very large number of
```

combinational loops. The pins in this group will be reported, and PrimeTime will continue to attempt dynamic loop breaking. This may result in exceeding the limits of the machine. The system may become unstable and an "out of memory" error may occur.

WHAT NEXT

Check the listed pin groups to ensure that the combinational feedback loops are expected and correct in the design. If they are unavoidable and dynamic loop breaking proves to be too costly, manually disable dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.

PTE-084 (warning) Parasitics on the net "%s" have been overridden, because the net is part of an ideal network.

DESCRIPTION

This message is displayed during a timing update for ideal nets that have parasitics annotated. The effect of leaving ideal networks in the design is that the parasitics are ignored and the net delay is ideal. This may obscure timing violations.

WHAT NEXT

To display the ideal networks is the design use the **report_ideal_network** command. To remove ideal networks that are not intended use the **remove_ideal_network** command.

SEE ALSO

remove_ideal_network (2), **report_ideal_network** (2).

PTE-085 (Warning) the calculated SHPR curve is not monotonic.

DESCRIPTION

The calculated interdependent setup/hold curve is not monotonic. The results of setup_hold_pessimisim_reduction (SHPR) may be inaccurate.

WHAT NEXT

Check SHPR library data of setup/hold value and make sure they are characterized properly.

PTE-086 (Warning) Target constraint value is beyond the boundary of characterized SHPR library. Using nearest boundary value instead.

DESCRIPTION

The target constraint value, wich is required by SHPR optimization parameter, is beyond the boundary of characterized SHPR library. To avoid optimism, PrimeTime use the nearest boundary value as the updated target constraint value.

WHAT NEXT

Check SHPR library data of setup/hold value and make sure they are characterized properly and the characterization scale covers the target constraint value.

PTE-087 (Warning) %s constraint set on %s '%s' will be ignored.

DESCRIPTION

Pulse clock constraint set on the design, lib cell, instance or clock will be ignored. This can due to the fact that the design may not have any pulse generator cells, the constrained lib cell may not be a pulse generator or is not instantiated in the design, the constrained instance is not a pulse generator or the clock may not driving any pulse generators.

WHAT NEXT

PTE-088 (Information) report_analysis_coverage was reported with timing_enable_pulse_clock_constraints variable set to FALSE.

DESCRIPTION

timing_enable_pulse_clock_constraints was set to FALSE during report_analysis_coverage for -check_type min_pulse_width and then set to its preset value i.e. TRUE after reporting.

PTE-089 (Warning) Abandoning distributed timing update.

DESCRIPTION

PrimeTime was unable to successfully perform a distributed timing update and has set the **multi_core_enable_analysis** variable to FALSE.

WHAT NEXT

PTE-090 (Error) No output clock defined on the output '%s' of the PLL.

DESCRIPTION

You receive this message if the design has a PLL and there is no clock defined on the output that is connected to the feedback pin of the PLL.

WHAT NEXT

You should define a generated clock at the output of every PLL using the **create_generated_clock** command with the required specifications.

PTE-091 (Error) The feedback pin '%s' has no path to its PLL output clock.

DESCRIPTION

You receive this message if the design has a PLL and the feedback path is not connected correctly. Ideally, the feedback pin of a PLL should be connected to an output pin of the PLL. In addition, a generated clock should be defined on the output that is connected to the feedback pin.

WHAT NEXT

You should check that there is a path from the output of the PLL to the feedback pin. In addition, define a generated clock at the output of every PLL using the **create_generated_clock** command with the required specifications.

PTE-092 (Warning) The timing arcs from the reference pin to the output pin of the PLL '%s' are not unate. Not performing the PLL adjustment.

DESCRIPTION

```
You receive this message if the library model of the PLL does not have unate arcs
from the reference clock pin to the output clock pin.
```

WHAT NEXT

PTE-093 (Warning) the -delay_calculation_only_mode flag is ignored because of the current variable settings.

DESCRIPTION

```
You may receive this message in the following case(s):
```

timing_use_zero_slew_for_annotated_arcs == always

timing_use_zero_slew_for_annotated_arcs == auto and more
```
        than 95 percent of delay arcs on a design have annotated values"
```

WHAT NEXT

```
See man page of
```
timing_use_zero_slew_for_annotated_arcs `for more details.`

PTE-094 (Warning) the si_xtalk_exit_on_max_iteration_count variable is ignored; only one iteration is performed

DESCRIPTION

```
You receive this warning because the
```
-delay_calculation_only_mode `option of the`
write_sdf `command is exclusive with:`

si_enable_analysis==true and **si_xtalk_exit_on_max_iteration_count**>1

```
Since only one iteration is performed, the results may be less accurate (but always
```

pessimistic.)

WHAT NEXT

Do nothing if this behavior is acceptable to you or remove the **-delay_calculation_only_mode** option if you insist in running multiple SI iterations. Note the general issue that using SDF generated after several SI iterations can lead to optimistic results if not done properly.

PTE-095 (Error) Generated clock is not defined on the output pin of the PLL connected to the feedback pin; not performing the PLL correction.

DESCRIPTION

You receive this error because PLL cell output defined using **-pll_output** connected to the feedback pin defined using **-pll_feedback** does not have a generated clock defined on it.

Since the generated clock is not defined, no PLL correction would be performed.

WHAT NEXT

If you want to perform PLL correction, define a generated clock at the PLL output connected to the feedback pin of the PLL.

PTE-096 (Warning) The variable multi_core_enable_analysis has been automatically set to FALSE as the following flow is not supported - '%s'. The update will now complete in scalar mode and no remote processes will be launched.

DESCRIPTION

You have attempted to perform a distributed update_timing but PrimeTime has detected a flow which is not supported in distributed mode. All remote_processes will be killed and your update will now complete as a scalar update.

WHAT NEXT

You can continue with your timing analysis. All commands will execute in scalar mode.

PTE-097 (fatal) An exceptionally long combinational path with greater than 25,000 pins is encountered. PrimeTime will exit its current session.

DESCRIPTION

```
PrimeTime does not time paths that have exceptionally large combinational depth for
reasons of memory efficiency.
```

WHAT NEXT

```
Consider breaking combinational paths that span across more than 25,000 pins. Note
that there can be multiple paths which have such exceptionally large combinational
depths and all such paths need to be broken to correctly time the design.
```

PTECO-001 (error) Cannot change the state of ECO mode because
   %s.

DESCRIPTION

This error message is issued when the attemp to change the state of ECO mode fails
due to the reason indicated. Most often, it happens when you are trying to either
enable or disable ECO mode after designs and/or libraries have already been loaded
into PrimeTime.

WHAT NEXT

Please verify the reason indicated by the error message, make sure you issue the
command 'set_program_options' earlier, e.g. before any library/design is loaded.

PTECO-002 (information) ECO mode is %s, and the behaviors of the following ECO commands are changed: "read_parasitics -eco".

DESCRIPTION

This information message is issued when the state of ECO mode is changed.

WHAT NEXT

Please verify if the commands listed in the message are really needed or not needed
in the script.

PTECO-003 (error) %s.

DESCRIPTION

This is a generic error message.

WHAT NEXT

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

PTGUI-100 (warning) A timing update is required before timing data
in the current design can be displayed in the GUI.

DESCRIPTION

The variable timing_save_pin_arrival_and_slack was found set to FALSE. To display data in the GUI, the slack and arrival window attribute data must be present for pins that are not endpoints. For this reason, a timing update will be required before data can be displayed on the current design.

To make such updates unnecessary in the future, please set timing_save_pin_arrival_and_slack to TRUE before running the last timing analysis prior to starting the GUI. Runtime for PrimeTime timing analysis may increase when this variable is set to TRUE, but it will save the time when you start the GUI.

WHAT NEXT

For more information please refer to PrimeTime User Guide and the man page for timing_save_pin_arrival_and_slack.

PTGUI-101 (warning) Disabling GUI due to an invalid value
for shell environment variable DISPLAY.

DESCRIPTION

The shell environment variable DISPLAY is used to identify a X server to use for GUI display. This variable was either blank or set to an invalid X server name. All GUI features will be disabled.

To enable GUI features, please set the DISPLAY variable to a valid value before starting PrimeTime.

PTGUI-102 (warning) Disabling GUI due to missing symbol library

in the installation.

DESCRIPTION

The symbol library used to display logical schematic views in PrimeTime GUI could not be opened for reading. All GUI features will be disabled.

To enable GUI features, please ensure that the the Synopsys root in use has been properly installed before starting PrimeTime.

PTHC-001 (information) %s.

DESCRIPTION

This is just a generic informational message.

WHAT NEXT

No action needed.

PTHC-002 (waring) %s.

DESCRIPTION

THis is a generic warning message.

WHAT NEXT

Please note and confirm the specific reason indicated by the warning message, modify setting(s) accordingly, re-issue the command(s) if necessary.

PTHC-003 (error) %s.

DESCRIPTION

This is a generic error message.

WHAT NEXT

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

PTHC-004 (error) Cannot change the state of high capacity mode because

%s.

DESCRIPTION

This error message is issued when the attemp to change the state of high-capacity
mode fails due to the reason indicated. Most often, it happens when you are trying
to either enable or disable high capacity mode after designs and/or libraries have
already been loaded into PrimeTime.

WHAT NEXT

Please verify the reason indicated by the error message, make sure you issue the
command 'set_program_options' earlier, e.g. before any library/design is loaded.

PTHST-100 (warning) %d errors were detected during the Tcl command evaluation.

DESCRIPTION

While evaluating the Tcl command string given as the **-tcl_cmd** option with each object in the collection, a number of errors were encountered.

WHAT NEXT

For more information see the **create_histogram** command man page.

SEE ALSO

create_histogram (2).

PTIO

PTIO-1 (error) Cannot open file '%s' for %s.

DESCRIPTION

The specified file could not be opened for reading or writing. If reading, the file may not exist, or might have incorrect permissions. If writing, you may not have access to the directory.

WHAT NEXT

Verify the file name, directory name, and permissions.

PTIO-2 (error) %s for '%s' failed:
 %s

DESCRIPTION

A problem occured when reading or writing a file. For example, when writing an SDF file, you ran out of disk space. The message will indicate the command and problem.

WHAT NEXT

Action based on the problem, indicated in the message.

PTIO-3 (error) Failed to create directory '%s'.

DESCRIPTION

The specified directory could not be created by Primetime. You may not have access to the directory.

WHAT NEXT

Verify the permissions and reissue the command

PTIO-4 (error) The remote process expected directory '%s' to

'%s'

DESCRIPTION

While the slave process was performing an operation, it expected the directory specified to exist or non-exist as indicated. The master process is responsible for manipulating the directories but failed to complete the operation.

WHAT NEXT

Verify the permissions and reissue the command.

PTSR

PTSR-001 (error) The directory '%s' already exists.

DESCRIPTION

```
The specified directory to save the application session data already exist. If you
want to overwrite the data in the directory, use -replace option.
```

WHAT NEXT

```
Verify the directory name.
```

PTSR-002 (information) Cleaning and overwriting all data in the existing directory '%s'.

DESCRIPTION

```
The specified directory to save the PrimeTime session data already exists and -
replace option is specified to overwrite the data in the directory.
```

```
Please use -replace with great caution, because it will try to remove all the
existing data, including all files and sub-directories, already present in the
target directory. If the target directory is logically the parent directory of
current working directory or the directory from which the current session has been
launched, the behavior is undefined.
```

WHAT NEXT

```
Please confirm that it is safe for the application to delete the specified directory
before issue the commond with -replace option.
```

PTSR-003 (error) %s.

DESCRIPTION

```
As indicated by the message, something is wrong during the save/restore operation,
```

WHAT NEXT

```
Please confirm the reason indicated by the message, fix the problem and try again.
```

PTSR-004 (information) %s.

DESCRIPTION

As indicated by the message, some potentially risky operations have been performed during the save/restore.

WHAT NEXT

Please confirm the indicated operation.

PTSR-005 (error) Mismatch of technology library. The library '%s' does not match between saved image and the one being currently loaded. Restore will be aborted.

DESCRIPTION

As indicated by the message, technology libraries are either recompiled or a different version of the library is being read.

WHAT NEXT

Check your technology libraries (look in lib_map file) and redo restore_session.

PTSR-006 (error) Required library '%s' not found. Restore will be aborted.

DESCRIPTION

The given technology library was not found. This is required to perform restore.

WHAT NEXT

Check your technology libraries (look in lib_map file) and redo restore_session.

PTSR-007 (error) The library file '%s' could not be restored.

DESCRIPTION

```
The given technology library could not be restored. This is required to perform
restore.
```

WHAT NEXT

```
Check your technology libraries (look in lib_map file) and redo restore_session.
```

PTSR-008 (error) Cannot save design data to directory '%s'.

DESCRIPTION

```
As indicated by the message, the application is unable to save the design data in
the specified directory. Usually, the target directory should not be the current
directory, or a directory which is parent of the current working directory, or a
directory which is a subdir of some unexisting directory.
```

WHAT NEXT

```
Please confirm the indicated reason, fix the prolem and try again.
```

PTSR-009 (warning) Can not save variable '%s': unsupported %s

DESCRIPTION

```
As indicated by the message, the application is unable to save the specified
variable. The type of data listed is not supported by the save_session command.
```

WHAT NEXT

```
If the variable is needed in the restored session issue the needed commands to re-
create the variable.
```

PTSR-010 (error) The session was not saved with the current

version of application.

DESCRIPTION

```
The directory given to the restore_session command was not written by the current
version of application. To see what version it was written with look at the file
<directory>/README.
```

WHAT NEXT

```
Use the same version of PrimeTime/PrimePower to restore a session as was used to
save the session.
```

PTSR-011 (error) The session directory is corrupted

DESCRIPTION

```
The directory given to the restore_session command is not complete. One or more
files do not contain the expected data.
```

WHAT NEXT

```
The session directory can not be used. Please re-run the original script.
```

PTSR-012 (error) Expected to find '%s' but found '%s' in the lib_map file.

DESCRIPTION

```
The directory given to the restore_session command has corrupted lib_map file. One
or more technology library files are missing/changed in position.
```

WHAT NEXT

```
Please re-run the restore_session after fixing the ascii lib_map file.
```

PTSR-013 (error) Cannot read the saved session files becuase

they were not generated by the same product.

DESCRIPTION

```
The directory given to the restore_session command was not generated by the same
product. To see what product generated this session, please refer to file
<directory>/README.
```

WHAT NEXT

```
Use the same version and the same product to restore a session as was used to save
the session.
```

PTSR-014 (information) The library location '%s' is changed to '%s' in the lib_map file.

DESCRIPTION

```
This is an information message that the lib_map file was edited to change the
location of the technology libraries.
```

WHAT NEXT

```
No action is required, this is just information.
```

PTSR-015 (error) Cannot restore the session saved with version '%s',
 which is different from the current version '%s'.

DESCRIPTION

```
The directory given to the restore_session command was not written by the current
version of application. To see what version it was written with look at the file
<directory>/README.
```

WHAT NEXT

```
Use the same version of PrimeTime/PrimePower to restore a session as was used to
save the session.
```

PTSR-016 (error) Clean up partially restored design data...

DESCRIPTION

As indicated by the message, some potentially risky operations have been performed
during the save/restore and resulted in the restore failing.

WHAT NEXT

Please confirm the indicated operation.

PTSR-017 (information) Could not remove previously added hosts as they are either still on line or are currently being launched.

DESCRIPTION

As indicated by the message, prevously added hosts could not be removed. Therefore,
the number of hosts added for the restored session will exceed the number of hosts
required.

WHAT NEXT

No action is required.

PTSR-018 (warning) The -only_used_libraries option is not supported in multi_core_enable_analysis mode and will be ignored.

DESCRIPTION

As indicated by the message, the -only_used_libraries option is not supported when
multi_core_enable_analysis is set to true. This option will be ignored when saving
the session. As a result, all libraries loaded will be required when the session is
restored.

WHAT NEXT

No action is required.

SEE ALSO

save_session (2)

PWR-001 (error) Power analysis is disabled.

DESCRIPTION

You received this error message because the **power_enable_analysis** variable has been set to **false** while the command requires power analysis.

WHAT NEXT

First, determine whether you want to perform power analysis. If you do, then set **power_enable_analysis** to **true**.

PWR-002 (error) Cannot proceed without power analysis feature.

DESCRIPTION

You received this error message because the command requires power analysis feature. The first power related command brings out the power analysis feature. This command cannot be the first command.

WHAT NEXT

Make sure you set the variable power_enable_analysis to true at the begining of your script. Make sure you have PrimeTime PX license. Look at the man page of this command, and use it correctly.

PWR-003 (information) Setting timing_save_pin_arrival_and_slack to TRUE.

DESCRIPTION

You receive this informational message because sometimes in power extention mode, the timing_save_pin_arrival_and_slack variable must be set to TRUE for accurate power analysis.

WHAT NEXT

This is an informational message. No action is required on your part.

SEE ALSO

power_enable_analysis (3), **timing_save_pin_arrival_and_slack** (3).

PWR-004 (error) Save and restore failed for user options.

DESCRIPTION

You received this error message because save and restore of user options did not behavior correctly.

WHAT NEXT

Check whether same versions of PrimeTime PX were used for save and restore.

PWR-005 (error) Run out of memory.

DESCRIPTION

You received this error message because the program runs out of memory.

WHAT NEXT

Check whether the machine has the memory large enough to run the application.

PWR-006 (error) Event file (VCD or its equivalent) was not properly set for time based power analysis.

DESCRIPTION

You received this error message because time based power analysis did not find the correponding event information specified by read_vcd command.

WHAT NEXT

Check whether read_vcd command was specified or ran correctly. This command is

required before update_power for time based power analysis.

PWR-007 (warning) VCD coverage on the design is too small. Power may be underestimated.

DESCRIPTION

You received this warning message because the annotated event coverage from VCD or its equivalent was too small. the activities of some parts of the design were not captured in the current VCD.

WHAT NEXT

Check read_vcd command, especially the -strip_path and -path options to see whether VCD events were applied to the proper hierachy of the design.

PWR-008 (error) The value of power_ui_backward_compatibility variable in the restore seesion is not the same as that in the save session.

DESCRIPTION

power_ui_backward_compatibility variable determines whether PrimeTime is to use the UI of 2008.06 or current release. You received this error message because the saving and restoring power related sessions used different values for this variable, which is not allowed in PrimeTime PX.

WHAT NEXT

Change the variable so that save and restore sessions use the same version of PrimeTime PX UI.

PWR-100 (error) Cannot open "%s

DESCRIPTION

Not able to open the specified PIF file for reading.

Check your read_pif command for the correct design_label.

PWR-101 (warning) Cannot open %s for write, write to stdout instead.

DESCRIPTION

Failed to open the file for writing. The results will be printed to screen.

WHAT NEXT

Action based on the message.

PWR-102 (error) Current instance index %d exceeds total instance count %d. Please verify your PIF files and try again.

DESCRIPTION

The number of instance read has already exceeded the total instance count. The pif files are corrupted.

WHAT NEXT

Verify the integrity of the pif files, regenerate pif if needed.

PWR-103 (warning) "%s No power will be reported for instance "%s

DESCRIPTION

The cell type of the instance at the leaf level is not defined in your HDL code. Power consumption for this particular instance will not be calculated.

WHAT NEXT

Check your HDL code.

PWR-104 (error) Port %s is not found in cell %s!

DESCRIPTION

The port specified in the delay path is not found in the cell definition.

WHAT NEXT

Check the Verilog model for the cell.

PWR-105 (error) Failed in reading from "%s Please verify your PIF files and try again.

DESCRIPTION

The program failed to read the first line of information from the specified PIF file.

WHAT NEXT

Verify the integrity of your PIF files and regenerate PIF files if needed.

PWR-106 (error) "%s Please wait for .pif1 to be completed and re-run PrimeTime PX.

DESCRIPTION

The program failed to read the necessary information from .pif1 file.

WHAT NEXT

Please check if the Verilog/vhdl simulation has finished generating .pif1 file. If not, please wait, otherwise, verify your PIF files and regenerate them if needed.

PWR-107 (error) Failed in reading %s from "%s Please verify

your PIF files and try again.

DESCRIPTION

```
The program failed to read the necessary information from the PIF file.
```

WHAT NEXT

```
Verify the integrity of your PIF files and regenerate PIF files if needed.
```

PWR-108 (error) The design files are in old PIF version %s. Please re-run simulation and re-generate PIF files.

DESCRIPTION

```
PrimeTime PX is no longer support PIF version prior to 4.0.1.
```

WHAT NEXT

```
Re-run simulation and re-generate PIF files.
```

PWR-109 (error) CHKSUM on "%s

DESCRIPTION

```
The program failed checksum test on PIF file.
```

WHAT NEXT

```
Verify the integrity of your PIF files and regenerate PIF files if needed.
```

PWR-110 (error) Mismatching instance count in PIF files. Please verify your PIF files and try again.

DESCRIPTION

```
The total number of instance found in .pif1 file does not match with the total
instance count recorded. The pif files are corrupted.
```

PWR-111 (error) Not valid instance found for net "%s Please verify your PIF files and try again.

DESCRIPTION

The instance found on the net has invalid id. The pif files are corrupted.

WHAT NEXT

Verify the integrity of your PIF files and regenerate PIF files if needed.

PWR-112 (error) Failed to create handle to read from file "%s Please verify your PIF files and try again.

DESCRIPTION

The program has problem in reading from PIF file. Most likely, the pif files are corrupted.

WHAT NEXT

Verify the integrity of your PIF files and regenerate PIF files if needed.

PWR-113 (warning) File "%s

DESCRIPTION

HDL Simulation is still running, and it hasn't finished dumping all the events into event PIF file(s) yet. PrimeTime PX is capable of starting power simulation before HDL simulation finishes. But make sure to choose the analyze window within the period that events have been captured in PIF files Otherwise, the results can be off.

WHAT NEXT

Choose the appropriate time window in 'analyze_power' command.

PWR-114 (warning) CHKSUM on "%s If your PIF files were not generated by the latest PIF generation executable, please ignore this message.

DESCRIPTION

```
The program failed checksum test on PIF file.
```

WHAT NEXT

```
Verify the integrity of your PIF files and regenerate PIF files if needed.
```

PWR-115 (warning) No event was found in "%s

DESCRIPTION

```
No event was read in the event PIF file.
```

WHAT NEXT

```
1. Wait little longer for the HDL simulation to dump more events into the event PIF
file. 2. Verify the integrity of your event PIF file.
```

PWR-116 (error) No event was found in "%s

DESCRIPTION

```
No event was read in the event PIF file.
```

WHAT NEXT

```
Verify the integrity of your PIF files and regenerate PIF files if needed.
```

PWR-117 (error) Event PIF file has not been closed yet! Use 'analyze_power' command to specify the time window for power

analyze, as you are using a set of unfinished PIF files!

DESCRIPTION

```
HDL Simulation is still running, and it hasn't finished dumping all the events into
event PIF file(s) yet. PrimeTime PX is capable of starting power simulation before
HDL simulation finishes. But make sure to choose the analyze window within the
period that events have been captured in PIF files Otherwise, the results can be
off.
```

WHAT NEXT

```
Choose the appropriate time window in 'analyze_power' command.
```

PWR-118 (error) Data miss-matching found in .pif1 file. Please verify your PIF files and try again.

DESCRIPTION

```
The program found miss-matching data in .pif1 file.
```

WHAT NEXT

```
Verify the integrity of your PIF files and regenerate PIF files if needed.
```

PWR-119 (error) Cannot open "%s

DESCRIPTION

```
Not able to open the specified wire cap file for reading.
```

WHAT NEXT

```
Check your read_wire_cap command for the correct file name.
```

PWR-120 (warning) Cannot read in net name and capacitance

value from file %s line %ld. This line is skipped.

DESCRIPTION

```
Failed to read net name and capacitance value from the wire cap file.
```

WHAT NEXT

```
Check your wire cap file for the correct syntax.
```

```
Example of specifying net capacitance in wire cap file: top.inst.u2.Z 0.01
top.inst.u1.u0.Z 0.01
```

PWR-121 (warning) Cannot find net '%s' in the design read from file %s line %ld. This line is skipped.

DESCRIPTION

```
The net read from the wire cap or spf file can not be found in the design captured
in PIF files.
```

WHAT NEXT

```
Check the content in your wire cap or spf file for the correct net name.
```

```
Example of specifying net capacitance in wire cap file: top.inst.u2.Z 0.01
top.inst.u1.Z 0.02
```

```
Example of specifying net capacitance in spf file: *|NET A 1.01230E-04PF *|NET B
1.39876E-05PF
```

PWR-122 (warning) Capacitance of net '%s' is not set.

DESCRIPTION

```
The net capacitance is not set in the wire cap file. You can also use
'set_wire_load' to set the wire load model, or use 'set_load' to set the load on the
net. The default net capacitance is 0.
```

WHAT NEXT

```
Action based on the message.
```

PWR-123 (error) Cannot open "%s

DESCRIPTION

Not able to open the specified file for reading.

WHAT NEXT

Check the file name given in the command.

PWR-124 (warning) Capacitance unit '%s' is unrecognizable at line %ld. Use default 'pf'.

DESCRIPTION

The supported net capacitance units are 'pf', 'ff' and 'nf'.

WHAT NEXT

Check your spf file for the correct capacitance unit.

PWR-125 (warning) '%s' is not complete! It's only run to simulation time %g ns.

DESCRIPTION

HDL Simulation is still running, and it hasn't finished dumping all the events into event PIF file(s) yet. PrimeTime PX is capable of starting power simulation before HDL simulation finishes. But make sure to choose the analyze window within the period that events have been captured in PIF files Otherwise, the results can be off.

WHAT NEXT

Choose the appropriate time window in 'analyze_power' command.

PWR-126 (error) PIF event file "%s

DESCRIPTION

HDL Simulation is still running, and it hasn't dumped any event into specified event PIF file.

WHAT NEXT

Wait for a while and try again. If you think that this can be an error, check your $gen_pif task.

PWR-127 (error) Cannot open "%s

DESCRIPTION

Not able to open the specified event PIF file for reading.

WHAT NEXT

Check your read_pif command for the correct file name.

PWR-128 (error) Cannot open "%s

DESCRIPTION

Not able to open the specified event PIF file for reading.

WHAT NEXT

Check your read_pif command for the correct file name.

PWR-129 (error) Cannot open "%s

DESCRIPTION

Not able to open the specified event PIF file for reading.

Check your read_pif command for the correct file name.

PWR-130 (error) Invalid net ID "%d Please verify your PIF files and try again.

DESCRIPTION

The net ID read from event PIF file for the specific event is either negative or exceeds the total number of nets in the design. The event pif file is corrupted.

WHAT NEXT

Verify the integrity of the pif files, regenerate pif if needed.

PWR-131 (error) Can't find module with index '%d'! Please verify your PIF files and try again.

DESCRIPTION

Data read from PIF files are not consistant.

WHAT NEXT

Verify the integrity of the pif files, regenerate pif if needed.

PWR-132 (error) Symbol length %d is too long! Please verify your PIF files and try again.

DESCRIPTION

Data read from PIF files are not correct.

WHAT NEXT

Verify the integrity of the pif files, regenerate pif if needed.

PWR-133 (error) There are mismatches in the PIF files! Please verify your PIF files and try again.

DESCRIPTION

```
Data read from PIF files are not consistant.
```

WHAT NEXT

```
Verify the integrity of the pif files, regenerate pif if needed.
```

PWR-134 (error) File "%s" is not in DSPF format which is not supported. Please use DSPF and try again.

DESCRIPTION

```
The read_spf command reads capacitances from a file only in Standard Parasitic
Format form.
```

WHAT NEXT

```
Make sure the file is in DSPF format. Refer to read_spf man page.
```

PWR-135 (error) Syntax error in DSPF file "%s".

DESCRIPTION

WHAT NEXT

```
Make sure the file is in DSPF format. Refer to read_spf man page.
```

PWR-136 (warning) Name "%s" is too long.

DESCRIPTION

```
The matching pattern are too long to process. It exceeds the buffer limit - 2048
Bytes.
```

PWR-137 (error) Current design is not defined.

DESCRIPTION

The current design is not defined. Some commands require that the current design is set.

WHAT NEXT

Use current_design command to set current design.

PWR-138 (error) Cannot find design '%s'.

DESCRIPTION

There is no design with that name is in memory.

WHAT NEXT

Read in the design or reenter the command with a different name.

PWR-139 (error) Cannot find %s '%s' in design '%s'

DESCRIPTION

The specified object cannot be found in the given design or the PIF design if the last %s is not given.

WHAT NEXT

PWR-140 (error) Cannot set current instance to leaf instance

'%s'.

DESCRIPTION

```
The current instance must be a hierarchical instance.
```

WHAT NEXT

PWR-141 (error) "%s" value must be positive.

DESCRIPTION

WHAT NEXT

PWR-142 (error) The pif design has already been loaded.

DESCRIPTION

```
The command read_pif has been used to read a pif design prior to the command that
caused this error information. Currently, pp_shell can only accommodate one pif
design at one time. That is, read_pif command can be used only once.
```

WHAT NEXT

```
If another design is desired, quit and restart pp_shell.
```

PWR-143 (error) Design is not linked. Cannot continue.

DESCRIPTION

```
The command or the command with some specific options cannot proceed without linked
design.
```

```
Note that when we say "Design is not linked", sometimes it is just the library is
not read.
```

WHAT NEXT

```
Use link or read_db to read libraries and link the design.
```

PWR-144 (warning) set_ideal_transition: Net "%s" is not an ideal net. The command on this net is ignored.

DESCRIPTION

set_ideal_transition command only works for ideal nets. If the specified nets are not ideal nets, the command is ignored.

WHAT NEXT

Use set_ideal_net to specify the nets as ideal nets before using this command.

PWR-145 (warning) set_ideal_load: Net "%s" is not an ideal net. The command on this net is ignored.

DESCRIPTION

set_ideal_load command only works for ideal nets. If the specified nets are not ideal nets, the command is ignored.

WHAT NEXT

Use set_ideal_net to specify the nets as ideal nets before using this command.

PWR-146 (warning) Current design is already set. Cannot be changed!

DESCRIPTION

For PIF flow, current design is always *pp_root*. For VCD flow, once the current design is linked, it cannot be changed again.

PWR-147 (error) Can't find %s '%s' in %s '%s'.

DESCRIPTION

```
(internal use)
```

WHAT NEXT

PWR-148 (error) Can not find cell "%s" in the current design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files are read correctly. Verify the integrity of the pif files,
regenerate pif if needed.
```

PWR-149 (error) There is no cell in the design, please check your design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files are read correctly. Verify the integrity of the pif files,
regenerate pif if needed.
```

PWR-150 (error) There is no design, please check your design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files are read correctly. Verify the integrity of the pif files,
regenerate pif if needed.
```

PWR-151 (warning) There is no port on design "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-152 (error) There is unknown direction on pin "%s" in design "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-153 (error) There is no cell in the current design, please

check your current design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-154 (error) Can find design which instantiate cell "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-155 (warning) There is no net connected to cell "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-156 (error) There is no net in the current design, please

check your design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-157 (warning) There is no cell connected to net "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-158 (error) There is mismatch of cell number connected to net "%s".

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-159 (error) Can not find net "%s" in the current design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-160 (error) There is no port in the design.

DESCRIPTION

```
There is inconsistancy in the design data structure.
```

WHAT NEXT

```
Make sure the pif files and the library files are read correctly. Verify the
integrity of the pif files, regenerate pif if needed. Verify the integrity of the
library files.
```

PWR-161 (error) PIF version "%s" is not recognizable by pp_shell version "%s Please make sure to use the PLI library and the pp_shell from the same release. Re-run simulation and re-generate PIF files if needed.

DESCRIPTION

```
There is version inconsistency between PIF files and pp_shell. The PIF files could
be generated by a later version of PrimeTime PX PLI library.
```

WHAT NEXT

```
Please make sure to use the PLI library and the pp_shell from the same release. Re-
run simulation and re-generate PIF files if needed.
```

PWR-162 (warning) PIF version "%s" is not the same as pp_shell version "%s

DESCRIPTION

There is version inconsistency between PIF files and pp_shell.

WHAT NEXT

Please make sure to use the PLI library and the pp_shell from the same release. Re-run simulation and re-generate PIF files if needed.

PWR-163 (error) Can't use "%s

DESCRIPTION

It is required that the design be read first in PrimeTime PX.

WHAT NEXT

Use command 'read_verilog', 'read_vhdl' or 'read_db' to read in the design first.

PWR-164 (error) lack design name in current_design

DESCRIPTION

It is required that a design name must be provided for the current_design command.

WHAT NEXT

provide the design name with current_design

PWR-165 (error) design "%s

DESCRIPTION

The specified design is not found.

```
make sure the design is already read and also check spelling.
```

PWR-166 (warning) Please make sure SBPF file contains lumped cap information.

DESCRIPTION

```
PrimeTime PX currently can only process lumped capacitance. SBPF file, unlike SPEF
file, contains either lumped or decoupling capacitance, but not both. If the SBPF
file was written by PrimeTime, it most probably does not contain lumped capacitance.
PrimeTime PX IS able to read the file, but the power result could be inaccurate.
```

WHAT NEXT

PWR-167 (warning) No power information at the %s '%s'.

DESCRIPTION

```
(internal use)
```

WHAT NEXT

PWR-168 (waning) No timing window at the pin '%s'.

DESCRIPTION

```
(internal use)
```

WHAT NEXT

PWR-169 (error) Error when reading '%s' from %s.

DESCRIPTION

```
(internal use)
```

PWR-170 (error) Cannot output average waveform because %s

DESCRIPTION

For the given reason, average power waveform cannot be output.

WHAT NEXT

Make sure 1) the clock is correctly specified; 2) the specified clock is created; 3) the specified clocks are synchronous; 4) PrimeTime license is available; and then try again.

PWR-171 (warning) No clock specified. %s

DESCRIPTION

For the signals for which user has not specified switching activity values, PrimeTime PX internally calculates their values. For switching activity calculation PrimeTime PX uses clock period. Sinc clock is not specified, PrimeTime PX will use default value.

WHAT NEXT

Make sure 1) the clock is correctly specified; 2) the specified clock is created; 3) the specified clocks are synchronous; 4) PrimeTime license is available; and then try again.

PWR-172 (error) Failed to check out license for PrimeTime PX.

DESCRIPTION

The application failed to check out the licenses required to enable this product. It may be that all the licenses are in use or the site is not licensed to use this product.

WHAT NEXT

Make sure that the required feature is in the key file.

Contact your local Synopsys Support Center.

PWR-173 (error) Synopsys root is not set.

DESCRIPTION

1. if ran through pp_shell: Synopsys root should be set during installation by environment variable $SYNOPSYS or the command path. This indicates a bad installation.

2. if ran through pp_shell_exec: $SYNOPSYS variable or -root_path command line option should be set in order to find installed files.

WHAT NEXT

1. for case 1 above: Check your installation procedure, contact Synopsys support center if needed.

2. for case 2 above: Please set either $SYNOPSYS environment variable or -root_path command line option to the root of the installed Synopsys software.

PWR-174 (error) Can't %s before reading pif files!

DESCRIPTION

It is required that the design be read first in PrimeTime PX.

WHAT NEXT

Use command 'read_pif' to read in the design first.

PWR-175 (warning) Effort level '%s' is not supported! Command 'set_ana_effort' is ignored.

DESCRIPTION

The valid option for 'set_ana_effort' command is medium or high.

WHAT NEXT

Use the valid option for 'set_ana_effort'. Type "man set_ana_effort" for more information.

PWR-176 (warning) Effort level '%s' is not supported!

DESCRIPTION

The valid option for 'analyze_power -effort' is 'medium' or 'high'.

WHAT NEXT

Type "man analyze_power" for more information.

PWR-177 (error) Only a single character among 01*xX can be used for 'set_match_xstate'.

DESCRIPTION

The valid option for 'set_match_xstate' command is '0', '1', 'X', or 'x'.

WHAT NEXT

Use the valid option for 'set_match_xstate'. Type "man set_match_xstate" for more information.

PWR-178 (error) Only one single character can be used for hier_sep.

DESCRIPTION

The symbol for hierarchical seperator should be one single character.

WHAT NEXT

Type "man set_hier_sep" for more information.

PWR-179 (error) link_path or link_library variable is not set.

DESCRIPTION

Variable link_path or link_library needs to be set when reading library.

Type "man link" for more information.

PWR-180 (error) Incorrect time values in -time "%s" or "%s

DESCRIPTION

The time values specified for 'analyze_power' command cann't be negative.

WHAT NEXT

Provide the time window period for 'analyze_power' command.

PWR-181 (warning) Net %s does not exist!

DESCRIPTION

The net specified cann't be found in the design.

WHAT NEXT

Check the port names specified in command 'set_load' and 'set_input_transition'.

PWR-182 (warning) Invalid load capacitance unit '%s', use the default 'pf'.

DESCRIPTION

The unit used in the wire cap file is not supported by PrimeTime PX.

WHAT NEXT

Check your wire cap file.

PWR-183 (warning) Invalid option specified for 'analyze_power

-sortby'.

DESCRIPTION

The option specified for '-sortby' is invalid. The valid options are 'power',
'toggle', 'name'.

WHAT NEXT

Use the valid option for '-sortby' Type "man analyze_power" for more information.

PWR-184 (warning) histogram sampling interval cann't be negative. '-histogram' option is ignored.

DESCRIPTION

Histogram sampling interval should be a positive number.

WHAT NEXT

Provide the correct sampling interval for '-histogram' option.

PWR-185 (warning) The digits after the second decimal point of histogram sampling interval will be ignored. Waveform displaying tool may give incorrect results.

DESCRIPTION

The minimum time precision for displaying power histogram is 0.1ns. Using smaller
sampling interval than 0.1ns will result in incorrect waveform displayed by waveform
tool. Since power histogram is an average power consumption over the period of
sampling interval, use sampling interval smaller than 0.1ns can also cause PrimeTime
PX to give incorrect histogram power numbers.

WHAT NEXT

Use sampling interval larger than 0.1ns. If you do think that you need finer
resolution for histogram sampling interval, call Synopsys Service Center.

PWR-186 (error) Design label unspecified!

DESCRIPTION

```
Design needs to be specified for PrimeTime PX run.
```

WHAT NEXT

```
Use command 'read_pif' to specify the design label.
```

PWR-187 (error) PIF files are too old to use the -module_instance option! Please create your PIF files again with latest PrimeTime PX.

DESCRIPTION

```
PIF files are too old to use the -module_instance option!
```

WHAT NEXT

```
Create PIF files again with latest PrimeTime PX.
```

PWR-188 (warning) '%s' is not supported in %s mode. It is ignored.

DESCRIPTION

```
Each command has its own availablity, like read_pif only works for gate mode and
read_saif only works for RTL mode. This warning indicates a command used in an
inappropriate mode.

Warning: 'read_saif' is not supported in gate mode. It is ignored. (PrimeTime PX-
017)
```

WHAT NEXT

```
Look at the AVAILABILITY section in the command's man page.
```

PWR-189 (warning) '%s' of '%s' is not supported in %s mode. It

is ignored.

DESCRIPTION

Each command's option has its own availablity, like the "-gate_clock" option in
update_power only works in the RTL mode. This warning indicates a command's option
used in an inappropriate mode.

Warning: '-gate_clock' of 'update_power' is not supported in gate mode. It is
ignored. (PrimeTime PX-018)

WHAT NEXT

Look at the AVAILABILITY section in the command's man page.

PWR-190 (error) Can not find library file "%s".

DESCRIPTION

The library file name given are incorrect or the search path for this library file
are not given or the path is not correct.

WHAT NEXT

Give correct library file name or path name and run again.

PWR-191 (error) The interactive mode is not supported in RTL analysis.

DESCRIPTION

The interactive mode is only supported in gate level analysis.

WHAT NEXT

Write a shell script for RTL analysis.

PWR-192 (Warning) set_load in the wire_cap file is no longer

supported. Instead, make use of the set_load command.

DESCRIPTION

WHAT NEXT

```
Use built-in shell command 'source' to read the file.
```

PWR-193 (Error) Options '%s' and '%s' of command '%s' are mutually exclusive.

DESCRIPTION

```
The options cannot be specified at the same time.
```

WHAT NEXT

PWR-194 (Error) The %s given for option '%s' is incorrect!

DESCRIPTION

```
The option has a range of value or some specific values to specify.
```

WHAT NEXT

```
Check the man page of the command for legal values.
```

PWR-195 (Warning) The given strip_path %s cannot match net name '%s'. Ignored!

DESCRIPTION

```
PrimeTime PX cannot find the the strip_path specified by the user from the net name
given in the parasitics file. It will give up striping off anything from the net
name and use the net name as it is to search the net in the design.
```

Make sure you give the right strip_path.

PWR-196 (Error) Wire Load Model name must be specified.

DESCRIPTION

When you want to use wire load model for back annotation, make sure you read in the library and give the name of the wire load model.

WHAT NEXT

PWR-197 (Error) Option '%s' must be specified in combination with option '%s'.

DESCRIPTION

WHAT NEXT

PWR-198 (error) Can not find net "%s" in the current design.

DESCRIPTION

There is inconsistancy in the design data structure.

WHAT NEXT

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-199 (error) Can not find current design.

DESCRIPTION

No designs has been read in the memory.

Make sure the designs are read correctly. Verify the integrity of the designs.

PWR-200 (error) Command '%s' is obsolete. Use '%s' instead.

DESCRIPTION

Some old commands are obsolete. This message tells you what command to use instead.

WHAT NEXT

Use the alternative command instead.

PWR-201 (error) There is no interrupted power calculation thread pending.

DESCRIPTION

The resume_power_calculation command can be used only after update_power is interrupted.

WHAT NEXT

Use the update_power command instead.

PWR-202 (warning) After interruption, something in the environment has changed that may affect the way of power calculation. Use -force option if you still want to resume.

DESCRIPTION

If, after power calculation is interrupted, the timing information, parasitics, vcd file, and/or waveform options have changed, and then you type resume_power_calculation, power will not be calculated in the same way as before. Therefore, resuming power calculation is not recommended.

Use -force option if you still want to resume. Otherwise, do update_power from
start.

PWR-203 (warning) The option 'set_waveform_options -effort high' is ignored because this is not a VCD flow.

DESCRIPTION

The option -effort of command set_waveform_options only works for VCD flow. So for
non-VCD flows, the value for this option is ignored.

WHAT NEXT

PWR-204 (error) The %s command can only be used after power calculation.

DESCRIPTION

Some commands can only be used after the update_power command has been successfully
run through.

WHAT NEXT

Run update_power command first.

PWR-205 (error) Can't annotate power on cell %s.

DESCRIPTION

Power can only be annotated on leaf cell or unresolved cell. The cell you specified
is a hierarchical cell and is not an unresolved cell.

WHAT NEXT

Give the correct cell name.

PWR-206 (error) Cannot find current design when running update_power command or analyze_power command.

DESCRIPTION

```
Failed to get current design netlist from the memory. It is required that the design
be read first in PrimeTime PX.
```

WHAT NEXT

```
Use command 'read_pif' to read in the design first.
```

PWR-207 (error) Negative start time or time interval (start_time >= end_time) in option "-time {%g, %g}" of update_power or analyze_power commands.

DESCRIPTION

```
Incorrect time window. It is required that the start time be no less than 0 and the
end time no less than the start time.
```

WHAT NEXT

```
Give correct time window and try again.
```

PWR-208 (warning) Invalid option "-sortby %s" in update_power or analyze_power command, option ignored.

DESCRIPTION

```
Currently, the option "-sortby" is not supported by PrimeTime PX. The option is
ignored.
```

WHAT NEXT

```
None.
```

PWR-209 (warning) Invalid option "-histogram %g" in

update_power command or analyze_power command, option ignored.

DESCRIPTION

```
Currently, the option "-histogram" is not supported by PrimeTime PX. The option is
ignored.
```

WHAT NEXT

```
None.
```

PWR-210 (error) Invalid option "-mode %s" in update_power or analyze_power command, option ignored.

DESCRIPTION

```
The boolean expression for -mode option is incorrect.
```

WHAT NEXT

```
Refer to PrimeTime PX Manual for correct boolean expression.
```

PWR-211 (error) Boolean function is too long in -mode option of update_power or analyze_power command.

DESCRIPTION

```
The string is too long and exceeds the buffer limit - 2048 Bytes.
```

WHAT NEXT

```
Try to make the boolean function short and run again.
```

PWR-212 (error) Unknown function operator "%c" in "-mode"

option of update_power or analyze_power command.

DESCRIPTION

The boolean expression for -mode option is incorrect.

WHAT NEXT

Refer to PrimeTime PX Manual for correct boolean expression.

PWR-213 (error) Invalid "-time or analyze_power command.

DESCRIPTION

Incorrect time window given.

WHAT NEXT

Refer to PrimeTime PX Manual or manpage of update_power for how to specify time window by -time option.

PWR-214 (error) Lack the VCD file name

DESCRIPTION

The VCD file name in report_vcd_hierarchy is missed.

WHAT NEXT

Add the VCD file name or issue read_vcd before report_vcd_hierarchy.

PWR-215 (error) No rail name is specified for command set_current_rail. Please refer to command usage for more information.

DESCRIPTION

Design power rail name must be sepecified for command set_current_rail.

Type 'man set_current_rail' for more information

PWR-216 (error) Power rail "%s Please verify the design rail name.

DESCRIPTION

Power rails in the design are defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_rail command to select the rail of interest. To list all the defined power rails, use command report_power_rail_mapping.

WHAT NEXT

Check the power rail defined in the design and make sure that the name is correctly spelt. For more information about commands create_power_rail_mapping and report_power_rail_mapping, please type 'man create_power_rail_mapping' and 'man report_power_rail_mapping'.

PWR-217 (error) Design power rail name must be specified for command create_power_rail_mapping. Please refer to command usage for more information.

DESCRIPTION

Design power rail name must be specified for command create_power_rail_mapping.

WHAT NEXT

Type 'man create_power_rail_mapping' for more information

PWR-218 (warning) Power rail "%s Please verify the library rail name.

DESCRIPTION

The specific library rail name is not defined in the technology libraries which are

linked with the design.

WHAT NEXT

Check the rail names defined in the technology libraries and make sure that the name
is correctly spelt.

PWR-219 (error) There is no design power rail defined in this design. This command is ignored. Use command create_power_rail_mapping to define design power rails.

DESCRIPTION

Power rails in the design are defined by command create_power_rail_mapping. Then the
defined design rail can be used in set_current_rail command to select the rail of
interest. To list all the defined power rails, use command
report_power_rail_mapping.

WHAT NEXT

Type 'man create_power_rail_mapping' for more information

PWR-220 (error) There is only one design power rail defined in this design. Command set_current_rail has no effect on single rail design. This command is ignored. Use command create_power_rail_mapping to define design power rails.

DESCRIPTION

Power rails in the design are defined by command create_power_rail_mapping. Then the
defined design rail can be used in set_current_rail command to select the rail of
interest. To list all the defined power rails, use command
report_power_rail_mapping.

WHAT NEXT

Type 'man create_power_rail_mapping' for more information

PWR-221 (error) Internal error: library power rail "%s for cell %s

(%s). Please contact Synopsys Customer Support Center.

DESCRIPTION

An internal rare error has occurred. This cell is supplied by multi-voltages, but
the specific power rail is not found in its definition from the technology library.

WHAT NEXT

Contact Synopsys Customer Support Center.

PWR-222 (information) Different library rails are mapped to the same design rail for cell "%s" ("%s

DESCRIPTION

Different library power rails can be mapped to different design power rails at
instance basis in PrimeTime PX. Command create_power_rail_mapping can be used to
define the design power rails and create such rail mapping.

WHAT NEXT

PWR-223 (error) Can not find net "%s

DESCRIPTION

The net name used in the boolean expression for -off_condition option is not defined
in the current design.

WHAT NEXT

Check the boolean expression for -off_condition option in command
create_power_rail_mapping.

PWR-224 (error) Invalid specification in option "-off_condition

%s create_power_rail_mapping, please check.

DESCRIPTION

```
The specification for -off_condition option is not valid boolean expression.
```

WHAT NEXT

```
Check the boolean expression for -off_condition option in command
create_power_rail_mapping.
```

PWR-225 (error) Boolean function is too long in -off_condition option of command create_power_rail_mapping. The maximum acceptable number of characters is %d.

DESCRIPTION

```
The length limit for the boolean expression is currently set to be 2048 characters.
```

WHAT NEXT

```
Check the boolean expression for -off_condition option in command
create_power_rail_mapping. Please contact Synopsys Customer Support Center if
needed.
```

PWR-226 (error) Unknown function operator "%c create_power_rail_mapping.

DESCRIPTION

```
The operator used in the boolean expression for -off_condition option is not
support. The supported operators list is: (, ), !, +, *, &, |, ^, '.
```

WHAT NEXT

```
Check the boolean expression for -off_condition option in command
create_power_rail_mapping.
```

PWR-227 (warning) The state probability of net "%s is not set.

Set to be 0.5.

DESCRIPTION

An internal rare error has occurred. The state probability of nets should have been
set before power calculation starts in PrimeTime PX's SAIF based flow.

WHAT NEXT

Contact Synopsys Customer Support Center.

PWR-228 (warning) The state probability of net "%s is %.3f, which is not allowed. Set to be 1.0.

DESCRIPTION

An internal rare error has occurred. The state probability of a net cann't exceed
1.0.

WHAT NEXT

Contact Synopsys Customer Support Center.

PWR-229 (warning) No rail specific power table is defined for library cell "%s

DESCRIPTION

"related_pg_pin" or "power_level" (old syntax name) attribute can be specified in
internal and leakage power tables to indicate power consumptions associated with
different power rails in a cell. This enables PrimeTime PX to report power
consumption at rail basis.

WHAT NEXT

Provide more accurate power characterization data in the library.

PWR-230 (warning) Rail specific power tables are not fully

defined for library cell "%s

DESCRIPTION

```
"related_pg_pin or "power_level" (old syntax name) attribute can be used in internal
and leakage power tables to indicate power consumptions associated with different
power rails in a cell. This enables PrimeTime PX to report power consumption at rail
basis. The number of rail specific power tables should match the number of power
rails defined for the cell in the library.
```

WHAT NEXT

```
Check power tables in the library
```

PWR-231 (warning) Rail specific power tables are over specified for library cell "%s

DESCRIPTION

```
"related_pg_pin or "power_level" (old syntax name) attribute can be used in internal
and leakage power tables to indicate power consumptions associated with different
power rails in a cell. This enables PrimeTime PX to report power consumption at rail
basis. The number of rail specific power tables should match the number of power
rails defined for the cell in the library.
```

WHAT NEXT

```
Check power tables in the library
```

PWR-232 (error) Can not open file "%s" for reading.

DESCRIPTION

```
The file can not be open for reading.
```

WHAT NEXT

```
Check if the correct name mapping file is provided.
```

PWR-233 (error) Gate level object "%s Therefore, will not be

able to set mapping bewteen RTL and gate level objects.

DESCRIPTION

Gate level object can not be found in the netlist. Without gate level object the
command will not know one of the mapping parameter between RTL object and gate level
object.

WHAT NEXT

Please check if correct gate level object name is provided.

PWR-234 (warning) Can't find module "%s" in the specified block "%s

DESCRIPTION

Not able to find the instances specified by analyze_power -inst option in the
design. The design block information is captured in PIF files through simulation.

WHAT NEXT

1. Find the design block name specified by $gen_pif task in your Verilog/vhdl test
bench code. 2. Check if the instances specified by analyze_power -inst option do
exist in the design block.

PWR-235 (warning) Can't find module "%s

DESCRIPTION

Not able to find the instances specified by analyze_power -inst option in the
design. The design information is captured in PIF files through simulation.

WHAT NEXT

Check your design to verify if the instances specified by analyze_power -inst option
do exist.

PWR-236 (error) No valid block is specified, please check your

analyze_power command!

DESCRIPTION

```
Not able to find any instance specified by analyze_power -inst option in the design.
The design information is captured in PIF files through simulation.
```

WHAT NEXT

```
1. Find the design block name specified by $gen_pif task in your Verilog/vhdl test
bench code. 2. Check if the instances specified by analyze_power -inst option do
exist in the design block.
```

PWR-237 (error) Can't find user specified block "%s in the design, please check your $gen_pif task!

DESCRIPTION

```
Not able to find the instances specified by $gen_pif task in the design.
```

WHAT NEXT

```
Check if the instances specified by $gen_pif task do exist.
```

PWR-238 (error) Analyze window (%g, %g) mismatches with the simulation activity window (%g, %g).

DESCRIPTION

```
The analyze window specified by 'analyze_power -time' option mismatches with the
simulation window captured by $gen_pif task. Mismatched window will cause incorrect
power simulation results.
```

WHAT NEXT

```
1. Check your $gen_pif task for pif generation 2. Choose the time window within the
simulation time window.
```

PWR-239 (warning) Analyze window (%g, %g) starts ealier than

the simulation activity window (%g, %g).

DESCRIPTION

```
The analyze window specified by 'analyze_power -time' option mismatches with the
simulation window captured by $gen_pif task. Mismatched window will cause incorrect
power simulation results.
```

WHAT NEXT

```
1. Check your $gen_pif task for pif generation 2. Choose the time window within the
simulation time window.
```

PWR-240 (warning) Analyze window (%g, %g) finishes later than the simulation activity window (%g, %g).

DESCRIPTION

```
The analyze window specified by 'analyze_power -time' option mismatches with the
simulation window captured by $gen_pif task. Mismatched window will cause incorrect
power simulation results.
```

WHAT NEXT

```
1. Check your $gen_pif task for pif generation 2. Choose the time window within the
simulation time window.
```

PWR-241 (error) Unknown port direction!

DESCRIPTION

```
The port direction in the cell is unknown. The supported port direction types are:
input, output and inout.
```

WHAT NEXT

```
Report this error to Synopsys Customer Service Center.
```

PWR-242 (warning) Power simulation has been interrupted!

DESCRIPTION

If a user presses Ctrl-C in the middle of PrimeTime PX run, power simulation will be interrupted. pp_shell will do a wrap-up and report the simulation results up to this point.

WHAT NEXT

PWR-243 (warning) Window [%g, %g] negative or too narrow to be simulated!

DESCRIPTION

The analyze window specified by 'analyze_power -time' option gives too little the room to run simulation.

WHAT NEXT

Choose a more reasonable time window in 'analyze_power' command..

PWR-244 (warning) Analyze window has been adjusted to be (%g, %g).

DESCRIPTION

The analyze window specified by 'analyze_power -time' option mismatches with the simulation window captured by $gen_pif task. This analyze window has been adjusted according to the simulation window to give more accurate power results.

WHAT NEXT

1. Check your $gen_pif task for pif generation 2. Choose the analyze time window within the simulation time window.

PWR-245 (warning) User specified switching activity information present on the design. However, using event based flow for

power estimation as -saif switch is not used with the command.

DESCRIPTION

```
Both event file and user specified switching activity information is present on the
design. However, since -saif switch is not used with the command, by default the
command will use event based flow for power estimation.
```

WHAT NEXT

```
Check if you are using wright flow for power estimation.
```

PWR-246 (warning) Neither event file or switching activity data present for power estimation. The command will propagate switching activity values for power calculation.

DESCRIPTION

```
Since, neither event file or switching activity data is present on the design, the
command will propagate switching activity values for power calculation.
```

PWR-247 (warning) Event end time %g is less than analysis start time %g

DESCRIPTION

```
event end time in VCD is less than the analysis start time. The VCD file doesn't
your analysis window.
```

WHAT NEXT

```
your test bench to make sure your simulation is run long enough.
```

```
your PrimeTime PX run script to make sure you specify the correct "-time" values
update_power.
```

PWR-248 (error) Can not find any event in the event file.

DESCRIPTION

```
An event happens when the value at any net or pin changes. From the VCD file given,
no event can be found.
```

WHAT NEXT

```
Check -strip_path and -path in read_vcd to make sure correct paths are specified.
```

```
Check testbench and make sure to dump every leaf cell's events. For example, use
$dumpvar(0).
```

PWR-249 (warning) End time of the analysis window {%g %g} is earlier than the first event time (%g)

DESCRIPTION

WHAT NEXT

PWR-250 (warning) Start time of the analysis window {%g %g} is earlier than the first event time (%g).

DESCRIPTION

WHAT NEXT

PWR-251 (error) No design has been specified for power analysis.

DESCRIPTION

```
Failed to get current design netlist from the memory. It is required that the design
be read first in PrimeTime PX.
```

Use command 'read_pif' to read in the design first.

PWR-252 (warning) Power simulation has been interrupted.

DESCRIPTION

WHAT NEXT

PWR-253 (warning) End time of the analysis window {%g, %g} is later than the last event time (%g).

DESCRIPTION

WHAT NEXT

PWR-254 (error) Invalid direction on lib_pin "%s" in lib_cell "%s".

DESCRIPTION

Normally the direction attribute of a lib_pin has one of three values: in, out, inout. This error happens when the real value is none of these.

WHAT NEXT

Check the library file.

PWR-255 (error) No activity is available in the VCD file for the given time interval for power calculation.

DESCRIPTION

Incorrect time window. The times specified must include VCD activity.

Check the VCD file to make sure that activity is dumped during the time window
specified. Give the correct time window and try again.

PWR-256 (warning) There is no waveform options specified for update_power -waveform command. Use the default waveform options.

DESCRIPTION

When using update_power -waveform, set_waveform_options should be used before to
specify the waveform options. Otherwise, use the default waveform options.

WHAT NEXT

Refer to set_waveform_options and update_power man pages.

PWR-257 (warning) set_waveform_options has been set, but create_power_wavefroms is not used.

DESCRIPTION

In order to create waveform file, after set_waveform_options command, use
create_power_waveforms, instead of update_power.

WHAT NEXT

Refer to set_waveform_options and create_power_waveforms man pages.

PWR-258 (error) (read_vcd) Cannot open file "%s

DESCRIPTION

Not able to open the specified VCD file for reading.

WHAT NEXT

Check your read_vcd command for the correct file_name.

PWR-259 (error) (read_vcd) Unknown time unit.

DESCRIPTION

```
The time unit given is not recognizable.
```

WHAT NEXT

```
Check your VCD file.
```

PWR-260 (error) (read_vcd) Can not find cell "%s" in design "%s

DESCRIPTION

```
The cell read from vcd file cannot be found in the specified design.
```

WHAT NEXT

```
Make sure the VCD file is created correctly, and the path and strip_path option are
given appropiately.
```

PWR-261 (error) (read_vcd) Can not find the top cell in design "%s

DESCRIPTION

```
The top cell read from vcd file cannot be found in the specified design.
```

WHAT NEXT

```
Make sure the VCD file is created correctly, and the path and strip_path option are
given appropiately.
```

PWR-262 (error) (read_vcd) Syntax error. $scope and

$upscope are not in pair. Ignoring the extra $upscope.

DESCRIPTION

WHAT NEXT

```
Check the VCD file.
```

PWR-263 (warning) (read_vcd) Can not find net or port "%s in cell "%s

DESCRIPTION

```
The net or port of a certain cell read from the VCD file can not be found in the
same cell of the design loaded in pp_shell.
```

WHAT NEXT

```
Make sure the VCD file is created correctly, and the path and strip_path option are
given appropiately.
```

PWR-264 (error) (read_vcd) Variable length %d of identifer %s does not match the length of the vector %d.

DESCRIPTION

WHAT NEXT

```
Check the VCD file.
```

PWR-265 (error) (read_vcd) Strip path "%s matched in the VCD file.

DESCRIPTION

```
PrimeTime PX cannot find the the strip_path specified by the user from the net name
given in the VCD file. It will give up reading anything from the VCD file for this
net.
```

Make sure you give the right strip_path.

PWR-266 (error) read_vcd command is not used in the PrimeTime PX VCD flow.

DESCRIPTION

PrimeTime PX has two flow. One is VCD flow and the other is PIF flow. In the VCD flow, PrimeTime PX reads in the HDL netlist and VCD file while in the PIF flow it just reads in PIF files. This error occurs when VCD file is not read in the VCD flow.

WHAT NEXT

Please read in VCD file using read_vcd command before update_power.

PWR-267 (warning) The net "%s" is not covered by VCD file "%s

DESCRIPTION

The signal changes for the reported net is not recorded in the VCD file. This will lead power calculation inaccurate. Most likely the power number is less than it should be.

WHAT NEXT

Please check $dumpvars in Verilog testbench to make sure all nets are dumpped.

PWR-268 (error) Wrong input "%s Valid inputs are "low" or "high".

DESCRIPTION

The option -effort accepts two variables of values "low" and "high". The "high" value is given if the user wants to use the new algorithm, which is cpu and memory intensive, for waveform generation. The "low" value is given if the user wants to use the old algorithm for waveform generation.

Please choose the correct variable value to the option and run the command again.

PWR-269 (error) Cannot turn on power analysis when variation analysis is on

DESCRIPTION

Power analysis and variation analysis are currently mutually exclusive. Power analysis cannot be enabled while variation analysis is on.

WHAT NEXT

Turn off variation analysis first then turn on power analysis.

PWR-270 (error) Power analysis license is not available.

DESCRIPTION

You received this error message because either a Primepower license or a PrimeTime-PX license is not available.

WHAT NEXT

Make you have either a Primepower or a PrimeTime-PX license and no one else is using it.

PWR-271 (error) Can't create power group '%s' because of name conflict.

DESCRIPTION

Power group cannot be created because the name of the power group to be created is conflicting to an existing power group.

WHAT NEXT

Try another group name.

PWR-272 (error) There is no predefined power group called '%s'.

DESCRIPTION

Only predefined power groups have default list of cells. The specified power group is not a predefined power group.

WHAT NEXT

Use correct predefined power group name or create your own power group.

PWR-273 (error) Power group '%s' does not exist.

DESCRIPTION

There is no power group with the specified name. If the name is a predefined power group, it must have been removed.

WHAT NEXT

Make sure to give the correct name.

PWR-274 (information) Average waveform period is %f ns.

DESCRIPTION

The average waveform period is the common base period of all clocks specified to generate the average waveform.

WHAT NEXT

PWR-275 (error) Cannot generate Average waveform because its period is too big.

DESCRIPTION

The average waveform period is the common base period of all clocks specified to generate the average waveform. You are recieving this message because the common

base period of the specified clocks is too big. Most probably the clocks are not synced with one another very well. Generating a waveform for such a big period could be a waste of runtime and memory.

To solve the problem, you should split the specified clocks into different groups, with clocks in each group syncing up very well with each other, and then generate waveforms for each group.

If you really want to generate average waveform for such a big period, change the value of the variable power_average_waveform_limit. For details, refer to the man page of that variable.

WHAT NEXT

Re-specify clocks or change the value of power_average_waveform_limit.

PWR-276 (error) Clock network power has not been estimted.

DESCRIPTION

You are trying to include estimted clock network power in the power report, but the clock network power has not been estimated yet.

WHAT NEXT

Try estimate_clock_network_power before report_power.

PWR-277 (error) Missing close blacket in power off expression "%s

DESCRIPTION

Missing close blacket in the boolean expression for -off_condition option in command create_power_rail_mapping.

WHAT NEXT

Check the boolean expression for -off_condition option in command create_power_rail_mapping.

PWR-278 (warning) The hierarchical cell '%s' is an empty cell

DESCRIPTION

The reported cell is a hierarchical cell but without any instances in its master
reference design. It will be considered as a black box during power calculation.

WHAT NEXT

Check the netlist to make sure that's correct. Make sure VCD, SAIF or
set_switching_activity cover the output pins of the reported cell, otherwise the
tool will set the default switching activity for them.

PWR-279 (error) Can't find reference clock for cycle accurate peak power analysis in current design.

DESCRIPTION

This message indicates that Primetime-PX can not find the reference clock for cycle
accurate peak power analysis. Cycle accurate peak power analysis needs a reference
clock to determine the cycle period or multiples of the cycle period over which the
power values are averaged. The reference clock name can be specified by the -
cycle_accurate_clock option in **create_power_wavforms** command. If the option is not
used, the tool will try to find a reference clock automatically. If no clock can be
found, the **create_power_waveforms** command will stop emit this error message.

WHAT NEXT

Check whether the current design has any related clocks.

PWR-280 (information) Clock %s is selected as the reference clock for cycle accurate peak power analysis of the current design.

DESCRIPTION

This message indicates that Primetime-PX will use this clock as the reference clock
for cycle accurate peak power analysis.

None.

PWR-281 (error) Can't use -interval option for cycle accurate peak power analysis.

DESCRIPTION

This message indicates that *-interval* option is used with *-cycle_accurate* option in the **create_power_waveforms** command. Please use *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* to determine the sampling interval for cycle accurate peak power instead.

WHAT NEXT

Use *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* to specify the sampling interval.

PWR-282 (error) Can't use -clocks option for cycle accurate peak power analysis.

DESCRIPTION

This message indicates that *-clocks* option is used with the *-cycle_accurate* option in the **create_power_waveforms** command. Please use *-cycle_accurate_clock* to specify the reference clock instead.

WHAT NEXT

Use *-cycle_accurate_clock* to specify the reference clock.

PWR-283 (error) Can't use -cycle_accurate_cycle_count option without -cycle_accurate option in create_power_waveform command.

DESCRIPTION

This message indicates that *-cycle_accurate_cycle_count* option is used in the

`create_power_waveforms` command, but *-cycle_accurate* option is not specified. The *-cycle_accurate_cycle_count* option is only allowed for cycle accurate peak power analysis. Please use the *-cycle_accurate* option in the **create_power_waveforms** command to turn on the cycle accurate peak power analysis.

WHAT NEXT

Use *-cycle_accurate* option along with *-cycle_accurate_cycle_count* option in the **create_power_waveforms** command.

PWR-284 (error) Can't use -cycle_accurate_clock option without -cycle_accurate option in the create_power_waveform command.

DESCRIPTION

This message indicates that the *-cycle_accurate_clock* option is used in the **create_power_waveforms** command, but the *-cycle_accurate* option is not specified. The *-cycle_accurate_clock* option is only allowed for cycle accurate peak power analysis. Please use the *-cycle_accurate* option in **create_power_waveforms** to turn on the cycle accurate peak power analysis.

WHAT NEXT

Use *-cycle_accurate* option along with *-cycle_accurate_clock* option in **create_power_waveforms**.

PWR-285 (warning) The value of -interval in create_power_waveforms is not correct.

DESCRIPTION

This message indicates that the value of -interval option in create_power_waveforms is not correct. This can happen when you use a zero delay VCD (read_vcd -zero_delay) and you either don't set -interval or set the value of -interval is too small. For a zero delay VCD, you need to set the interval value greater than a fast clock period since the power analysis for the zero delay VCD can only give a cycle accurate result.

WHAT NEXT

Set a correct interval value. Otherwise, the tool will set/reset the interval value. You can check power report to make sure the value set by the tool is what you

expect.

PWR-286 (error) The cycle accurate power analysis cannot be used in vector free or SAIF based flow.

DESCRIPTION

The cycle accurate power analysis can only be used in VCD based flow. It cannot be used in vector free or SAIF based flow.

WHAT NEXT

Remove -cycle_accurate option from create_power_waveforms command.

PWR-287 (error) Can't find any cell in the transient fanout of the specified sources.

DESCRIPTION

This message indicates **report_power -from** failed to find any cell in the transient fanout cone of the specified sources. The sources specified with *-from* option of **report_power** command need to be valid cell, net, pin or port objects. If the *-groups* option is also specified, the source object should be in the power groups.

WHAT NEXT

Check whether the specified sources are valid. If not, fix it and run the command again.

PWR-288 (error) The _FANOUT_TREE_ power group exists.

DESCRIPTION

_FANOUT_TREE_ power group is reserved for the feature of **report_power -from**. If the power group was already created by user, there will be conflicts.

WHAT NEXT

Remove or rename the user defined _FANOUT_TREE_ power group and run the command again.

PWR-289 (error) Can't find main library for the design.

DESCRIPTION

The error happens when there is no cell in the design which can find the corresponding library cell. This is usually caused by incorrect link_library paths or invalid technology libraries.

WHAT NEXT

Check whether link_path is correct and technology libraries are correctly loaded and re-run the case.

PWR-290 (error) Power value is required for 'set_annotated_clock_network_power' command.

DESCRIPTION

The error happens when **set_annotated_clock_network_power** command did not specify any power value, neither the default power value nor the power values specified by *-switching*, *-internal* or *-leakage* options. The command needs to accept at least one power value.

WHAT NEXT

Add power value(s) to the command and re-run the case.

PWR-291 (error) Can't find clock '%s' in current design.

DESCRIPTION

The error happens when **set/remove_annotated_clock_network_power** command specified the clock with the *-clock* option. But the clock with this name can't be found in the current design.

WHAT NEXT

Check the clock name in SDC, correct it and re-run the case.

PWR-292 (warning) Power has already been annotated on the

whole clock network. Ignore clock based power annotation.

DESCRIPTION

The warning happens when **set_annotated_clock_network_power** command has already annotated the power on the whole clock network. Clock based annotation with *-clock* will be ignored under such a circumstance.

WHAT NEXT

If you would like to do clock based power annotation, use **remove_annotated_clock_network_power** on the design first.

PWR-293 (error) No power has been annotated on the clock network.

DESCRIPTION

The error happens when **remove_annotated_clock_network_power** command can not find any annotated clock network power on the design.

WHAT NEXT

Remove the command from in the context of the script.

PWR-294 (error) No power has been annotated on the clock network for clock '%s'.

DESCRIPTION

The error happens when **remove_annotated_clock_network_power** command can not find any annotated clock network power for the clock specified by the *-clock* option.

WHAT NEXT

If you would like to remove all the annotated clock power, use **remove_annotated_clock_network_power** without *-clock* option.

PWR-295 (warning) Annotated clock network power exists.

Ignore estimated clock network power.

DESCRIPTION

Annotated clock network power has higher priority than the estimated clock network power. If both are activated in the **report_power** command. The estimated clock network power will be ignored.

WHAT NEXT

Use either annotated or estimated clock network power, not both.

PWR-296 (error) Group based power reports must contain 'clock_network' group when annotated clock network power is used.

DESCRIPTION

When power is annotated for the clock network, **report_power -group groups** command must contain the 'clock_network' group.

WHAT NEXT

If you don't want to report power with annotated clock network power, use **remove_annotated_clock_network_power** command before the **report power** command.

PWR-297 (warning) '%s' has already been annotated on the clock network. Overide it.

DESCRIPTION

If the power has already been annotated on the clock network, the succeeding commands will override it. The overiding behavior only happens on switching, internal and leakage power separately. Default power is treated as internal power.

WHAT NEXT

Check whether the command overriding is intended and fix them if it's not.

PWR-298 (error) Clock based power reports are not allowed when there is annotated power on the whole clock network.

DESCRIPTION

The error happens when there is annotated power on the whole clock network but **report_power** has the *-clocks* option. In this situation, there is no power information for each clock domain of the clock network. So PrimeTime-PX can't generate a valid report.

WHAT NEXT

Use **remove_annotated_clock_network_power** to remove the annotated clock network power. Then, use **set_annotated_clock_network_power -clock clk_name** to annotate clock based power on clock network, or remove *-clocks* option from **report_power** and re-run the case.

PWR-299 (error) Only one clock object is allowed for the '-clock' option.

DESCRIPTION

set/remove_annotated_clock_network_power command only allows to specify one clock domain. The error happens when more than one clock objects are specified with *-clock* option for the command.

WHAT NEXT

If annotated clock network power is needed for more than one clock domains, use multiple **set/remove_annotated_clock_network_power** commands.

PWR-300 (warning) Cell '%s(%s)' drives %d loads.

DESCRIPTION

The warning occurs when the cell drives a large fanout. An example is, a clock gating cell drives a large number of sequential cells before the clock network is implemented. The large fanout can affect the power calculation. Event based power analysis will do some special handling for the large fanout drivers and their loads.

PWR-301 (warning) %d high fanout drivers are detected. Power analysis may be affected by high fanout drivers.

DESCRIPTION

The warning gives the number of high fanout drivers in the design. Event based power analysis in PrimeTime-PX will do some special handling for large fanout drivers and their loads.

WHAT NEXT

Set the high fanout nets as ideal nets, or let PrimeTime-PX handle them.

PWR-302 (warning) Inout port %s of library cell %s has neither functionality nor state and path dependent power table. Assume it's an input.

DESCRIPTION

PrimeTime-PX relies on the three state enable function of the cell or the when state of power tables to decide whether an inout pin works as an input or output. The warning indicates that both functionality and when state of power tables are missing. In this case, PrimeTime-PX will assume the inout pin works as input.

WHAT NEXT

To model the behavior and power more acccurately, please specify the funcionality or generate state and path dependent power tables for the cell and run PrimeTime-PX again.

PWR-401 (error) Power features are not supported for the

format '%s'

DESCRIPTION

You received this message because you executed the **extract_model** command and specified an option **-power** with the **-format** option that included an argument other than *lib*. Power features are not supported in any format other than *lib*, so only the timing model will be written in those formats.

WHAT NEXT

If the *lib* format was not used, re-execute **extract_model** including the *lib* argument with the **-format** option.

PWR-402 (error) Clock is not defined

DESCRIPTION

extract_model -power will attach power tables to clock pins. So at least one clock must be defined.

WHAT NEXT

Use create_clock or create_generated_clock to define clock(s).

PWR-403 (error) Should set either period or ratio in set_simulation_clock

DESCRIPTION

You should set either period or ratio in set_simulation_clock to a value greater than or equal to 0.

WHAT NEXT

Check your scipt to make sure you specify -priod or -ratio for set_simulation_clock.

PWR-404 (error) Cannot set both peiod or ratio in

set_simulation_clock

DESCRIPTION

In set_simulation_clock, you can either specify -period or -ratio. You cannot specify both.

WHAT NEXT

Check your set_simulation_clock and make sure you only specify either -period or -ratio.

PWR-405 (error) Cannot specify period without clock in set_simulation_clock

DESCRIPTION

In set_simulation_clock command, you cannot specify -period without clock. Without clock you can only specify -ratio which is a global scaling ratio for all clocks.

WHAT NEXT

Check your set_simulation_clock command.

PWR-406 (warning) The net %s has no base clock for power calculation.

DESCRIPTION

For vector free power analysis and clock scaling, PrimeTime PX uses the base clock to set and/or scale switching activity. This message indicates the reported net has no base clock. So the tool will use the fastest clock in the design.

WHAT NEXT

Use check_power's no_base_clock to check your design. You can also use set_switching_activity to directly set the switching activity.

PWR-501 (error) Power rail mapping command can not be

combined with power domain commands.

DESCRIPTION

Power domains can define the power intention for a multi-voltage design. The power
rail mapping commands can be replaced by power domain TCL commands. Combining power
rail mapping commands with power domain commands is not allowed.

WHAT NEXT

For more information about power domain commands, please type 'man
create_power_domain'.

PWR-502 (warning) The library cell '%s' does not have 'primary_power' or
 'primary_ground' defined in the library.

DESCRIPTION

It is required to have 'primary_power' and 'primary_ground' defined in the PG pin
library.

WHAT NEXT

PWR-503 (error) The legacy power rail mapping commands can not be launched as default. Set variable "power_domains_compatibility

DESCRIPTION

UPF is an industrial standard for specifying power design intent as an extension to
logic specification. The legacy power rail mapping commands will continue to be
supported. However, combining power rail mapping commands with UPF commands is not
allowed.

WHAT NEXT

For more information about UPF commands, please type 'man create_power_domain'.

PWR-504 (error) The domain based power reporting can not be launched in non-UPF mode. Apply UPF commands to the design and set variable "power_domains_compatibility to enable UPF mode.

DESCRIPTION

UPF is an industrial standard for specifying power design intent as an extension to
logic specification. The domain based power reporting is designed to be used in UPF
mode.

WHAT NEXT

For more information about UPF commands, please type 'man create_power_domain'.

PWR-601 (Information) Running %s analysis...

DESCRIPTION

PrimeTime PX is running power analysis in the specified mode. For more information
on analysis mode, please check out the man page for power_analysis_mode.

PWR-901 (error) Number of annotated nets from VCD is too low (< 95%) to calculate peak power.

DESCRIPTION

The number of annotated nets from VCD is too low (less then 95%) to calculate peak
power.

The VCD file might come from RTL simulation in which case peak power calculation
(create_power_waveforms) is allowed only if you use -cycle_accurate which enables
cycle-accurate peak power analysis. See create_power_waveforms man page.

If you don't want the peak power, you can use update_power for average power
calculation for RTL VCD. To generate average cycle waveform and its peak power, set
the variable power_force_saif_flow to TRUE.

WHAT NEXT

Use report_switching_activity to check the annotated activity and also check the VCD

file. If it's a RTL VCD, make sure to add -cycle_accurate option to
create_power_waveforms.

PWR-902 (error) Average activity report not compatible with other options.

DESCRIPTION

The -average_activity flag allows for averaging toggle rates and glitch rates. The -state_cond, -source_pins, -rise, -fall flags cannot be used in conjunction with the -average_activity_flag.

WHAT NEXT

Remove incompatible flags

PWR-903 (error) Filter options not allowed together with other specified options.

DESCRIPTION

The filter options -exclude, -exclude_source, -include_only, -include_only_source cannot be used together with any of the -state_cond, -source_pin, -rise, -fall options.

WHAT NEXT

Remove the incompatible options.

PWR-904 (error) Cannot run get_switching_activity on pins with given options

DESCRIPTION

The command **get_switching_activity** cannot operate on pins of the design if the -average_activity, -exclude, -exclude_source, -include_only, -include_only_source, or -sort options have been used.

Remove the options, or try get_switching_activity on nets, or on hierarchical cells
(for -average_activity).

PWR-905 (error) Only one of -average_activity, -coverage, -list_not_annotated, -list_annotated, -list_zero_activity, -list_low_activity, -list_by_source may be used in a single call to report_switching_activity.

DESCRIPTION

Only one of -average_activity, -coverage, -list_not_annotated, -list_zero_activity,
-list_low_activity, -list_by_source may be used in a single call to
report_switching_activity.

WHAT NEXT

Instead of requesting multiple reports with report_switching_activity, simply run
the command multiple times, and request a different report with each command.

PWR-906 (error) report_switching_activity list options do not support -hierarchical

DESCRIPTION

The list options for report_switching_activity provide lists of nets. Reporting
hierarchically is not supported.

WHAT NEXT

Remove the -hier flag from the command.

PWR-907 (error) The primary_clock option is only supported with the -average_activity report.

DESCRIPTION

The primary_clock option only has meaning with the -average_activity report. It is

an error to use the -primary_clock option with a different report request.

WHAT NEXT

Remove the -primary_clock option.

PWR-908 (error) Option toggle_limit has no effect with other options chosen

DESCRIPTION

The option -toggle_limit only has an effect when the -coverage option or the -list_low_activity option are used with the command report_switching_activity.

WHAT NEXT

Remove the -toggle_limit option from the report_switching_activity command.

PWR-909 (error) The option -sort has no effect with other options chosen.

DESCRIPTION

For the command report_switching_activity, the -sort option only has an effect when the option -average_activity is chosen.

WHAT NEXT

Remove the -sort option.

PWR-910 (error) Clock '%s' not found.

DESCRIPTION

A proper clock name must be specified with the -primary_clock option.

WHAT NEXT

Make sure that the clock you intend to use as the primary clock exists in the

design.

PWR-911 (error) Uknown source in '%s'

DESCRIPTION

An unrecognized source was specified with the -list_by_source option for the report_switching_activity command.

Possible sources are the following:

saif, vcd, default, propagated, set_switching_activity, set_case_analysis, annotated.

WHAT NEXT

.

PWR-912 (error) Uknown source in '%s'

DESCRIPTION

An unrecognized source was specified with the -list_by_source option for the report_switching_activity command.

Possible sources are the following:

saif, vcd, default, propagated, set_switching_activity, set_case_analysis, annotated.

WHAT NEXT

.

PWR-913 (error) Unknown source or group '%s'

DESCRIPTION

An unrecognized source or group was specified with the report_switching_activity command in relation to one of the filter options -exclude, -exclude_source, -include_only, -include_only_source

Possible sources are the following:

```
file, default, propagated, set_switching_activity, set_case_analysis, annotated,
no_switching_activity.
```

```
Possible groups are the following:
```

```
sequential, combinational, black_box, tri_state, primary_input, rtl
```

WHAT NEXT

.

PWR-914 (error) Source string too long.

DESCRIPTION

```
The source list string for the report_switching_activity command was unexpectly
long.
```

WHAT NEXT

PWR-915 (error) The exclude options 'extended_clock' and 'buffer_tree' are not yet implemented for the Beta version of PT-PX

DESCRIPTION

WHAT NEXT

```
Wait until the release version to use these features.
```

PWR-916 (error) Unknown source specification or exclusion

group specified.

DESCRIPTION

WHAT NEXT

PWR-917 (error) The option -sort has no effect with other options chosen.

DESCRIPTION

For the command report_switching_activity, the -sort option only has an effect when the option -average_activity is chosen.

WHAT NEXT

Remove the -sort option.

PWR-918 (error) Unknown sort method

DESCRIPTION

For the command report_switching_activity, the -sort option sorts net lists or hierarchical block lists.

For net lists, -sort net_toggle_rate or -sort name can be used

For hierarchical block lists, -sort net_toggle_rate sorts over the average toggle rate in the cell. -sort name and -sort hierarchy can also be used.

WHAT NEXT

Remove the -sort option or change the -sort argument.

PWR-919 (error) No such clock found for -only_related_clock

option

DESCRIPTION

```
For the command report_switching_activity or get_switching_activity, the clock
specified by the -only_related_clock option could not be found in the design.
```

WHAT NEXT

```
Verify that the given clock exists in the design, or remove the -only_related_clock
option.
```

PWR-920 (error) cannot use -leakage_only flag with peak power analysis or when waveforms are requested.

DESCRIPTION

```
The -leakage_only flag for report_power can only be used with average power
analysis.
```

WHAT NEXT

PWR-921 (warning) Timing will not be updated prior to power analysis, and timing is not up-to-date.

DESCRIPTION

```
Timing will not be updated prior to power analysis. This can happen when either the
-no_propagation flag was used, or leakage variation analysis is being used.

If the -no_propagation flag has been used, but timing is not up-to-date, then
changes in clocks or case_analysis will not be reflected in the switching activity
for power analysis. Changes in switching activity will not be propagated. Default
power groups may not be correct.

Power groups may not be correct. In particular, without timing information, the tool
will not properly distinguish between objects in the sequential and register groups.
```

WHAT NEXT

```
Either avoid using the -no_propagation flag with report_power, or make sure that
changes made to the design and the constraints will not affect switching activites.
```

```
Avoid relying on power breakdowns into power groups.
```

PWR-922 (warning) There were %d nets without switching activities. No activity will be propagated. Default activity will be used on these nets.

DESCRIPTION

```
When the -no_propagation flag is used, propagation is skipped. Nets without
activities will be treated as if they had default activity.
```

WHAT NEXT

```
To take advantage of more acurate state-dependent power analysis, either apply
activities to the design with a SAIF file, or avoid use of the -no_propagation flag.
```

PWR-923 (error) Only static probability can be reported for a cell when the -state_condition argument is used.

DESCRIPTION

```
The get_switching_activity command does not support the use of -state_condition and
either -toggle_rate or -glitch_rate when applied to a cell. This is because only
leakage power is associated with the state of a cell.
```

WHAT NEXT

```
Remove the -toggle_rate or -glitch_rate flag
```

PWR-924 (error) This command can only be used in upf mode.

DESCRIPTION

```
The command set_supply_net_probability can only be used when upf compatability mode
is on.
```

WHAT NEXT

```
Set the variable power_domains_compatibility to FALSE and avoid use of commands
```

incompatible with upf mode.

PWR-925 (error) Options "%s

DESCRIPTION

The command report_power cannot be used with the specified features while the
variable power_enable_leakage_variation_analysis is set to true.

WHAT NEXT

Set the variable power_enable_leakage_variation_analysis to FALSE or remove the
options from report power and try again.

PWR-926 (error) Leakage variation analysis failed. No report can be generated

DESCRIPTION

The report_power command tried to access the results of leakage variation analysis.
But no results were found, indicating that the analysis failed.

WHAT NEXT

Determine the cause of why leakage variation analysis failed, and rerun the
analysis. If the leakage variation report is not wanted, set the variable
power_enable_leakage_variation_analysis to FALSE and rerun report_power.

PWR-927 (error) Unknown interpolation method "%s

DESCRIPTION

The variable **power_leakage_variation_interpolation_methods** should only be set to one
of the values "exp", "linear_add", "linear_factor", "quadratic".

WHAT NEXT

Changes the value of the variable **power_leakage_variation_interpolation_methods**.

PWR-928 (error) Option %s is not permitted when leakage variation is not being used.

DESCRIPTION

Certain options to report_power are only allowed to be used when the leakage variation feature is being used.

WHAT NEXT

To turn on the leakage variation feature, set the variable **power_enable_leakage_variation_analysis** to TRUE. Please see the man page for this variable and for report power for more details.

PWR-930 (error) Inconsistent or overlapping time windows

DESCRIPTION

The time windows used for activity analysis using the -time option of the command **create_activity_waveforms** must be nonoverlapping. They must be list in order from earliest to latest.

Bad example : **-time {0 100 50 200}** Good example : **-time {0 100 110 200}**

WHAT NEXT

Reorganize the time windows so that they are nonoverlapping and listed from earliest to latest. Alternatively, remove the time option and run the analysis on the whole VCD.

PWR-931 (error) Inappropriate -interval option

DESCRIPTION

The **-interval** option for the **create_activity_waveforms** command indicates the time, in nanoseconds, over which the activity is aggregated. If the value is two small (less than 10 vcd timesteps) or two large (more than a trillion timesteps), this error is generated.

WHAT NEXT

Choose an approriate value for the interval.

PWR-932 (error) VCD file contains wire/reg at line %d not included in the VCD header

DESCRIPTION

The VCD header should include all wires and reg identifiers. This erro is produced when the VCd includes a value change for a wire or reg not previously identified in the header. This indicates that the VCD is malformed.

WHAT NEXT

Probably the simulator which produced the VCD has an issue.

PWR-933 (Warning) VCD file has reg/wire id '%s' defined multiple times with inconsistent size at VCD line number %d, for wire named '%s'.

DESCRIPTION

The indicated reg/wire was defined several different times in the VCD header, and had different sizes indicated in the VCD header. This can happen if the reg/wire is listed under several different hierarchical blocks in the VCD, and it is listed as having different sizes in different places.

In this case, any extra bits in the reg/wire may end up having zero toggles. This can affect the average toggle rate for a module.

In the VCD file, the following line defines s reg/wire:

$var reg 6 id wire_name [5:0] $end

Where *id* is a unique id for a signal, and *wire_name* is a (possibly non-unique) name for the signal.

Multiple definitions can have the same *id*. In this case, PTPX treats them as the same signal. In this way, reg/wires can be defined multiple times.

Note that if a vpd or fsdb file was used as input, the VCD line number will not be meaningful for the input file.

WHAT NEXT

PWR-934 (warning) large number of events necessitates some

time shifting for event energy in the waveform

DESCRIPTION

This warning can happen during **update_power** with large designs in some cases.

This warning is only issued once per session. If this happens multiple times, the user will be warned only at the first time it occurs in a session.

Internally, PrimeTime-PX keeps track of a time window of switching events. In some large cases, when the window is large (maybe due to large maximum cell delay), or when there are a lot of events in a short period of time, the internal buffers can get too large. To prevent overflows, PrimeTime-PX will immediately print out it's stored buffers to the power waveforms. It is possible that in doing this, PrimeTime-PX may have to print out part of the waveform before all data for the time window is known. In this case, any switching energy discovered later will be shifted later in time.

Average power calculations will not be affected, since all switching energy is accounted for. However, it is possible that if this happens at a peak, the peak may be lost due to shifting the energy to a later time.

WHAT NEXT

Inspect the waveform after is is created. Re-run power analysis using the -time option with a small time window near the peaks.

PWR-935 (error) write_activity_waveforms must be run before report_activity_waveforms

DESCRIPTION

Analysis on a VCD file must be run before the report on the activity can be generated

WHAT NEXT

Run write_activity_waveforms.

PWR-936 (error) vector length in activity file is not consistent for

object %s at VCD line number %d.

DESCRIPTION

```
The VCD file has a vector with inconsistent length.

Example:

$var reg 4 a a [5:0] $end

This should be:

$var reg 6 a a [5:0] $end

Note that the VCD line number may not be the same as the fsdb line number if you
used fsdb as input.
```

WHAT NEXT

```
Regenerate VCD file.
```

PWR-937 (Warning) The option -exclude_cells was used, but no corresponding modules were found in the VCD.

DESCRIPTION

```
The -exclude_cells option is used to exclude some modules from the VCD during time-
based activity analysis. If the -exclude_cells option is used, but none of the
specified modules were found in the VCD, then this warning is generated. However,
activity analysis is not prevented by this warning.
```

WHAT NEXT

```
Check to see that the correct VCD is being used. Check to make sure the spelling of
module names in the -exclude_cells list is correct.
```

PWR-940 (error) Leakage variation analysis cannot be run with create_power_waveforms or the event based power flow.

DESCRIPTION

```
The variable power_enable_leakage_variation_analysis has been set, but the event-
based flows in PrimeTime-PX cannot be used foor leakage variation analysis.
```

Try report_power instead to run leakage variation analysis.

PWR-941 (error) Clock gate reporting failed.

DESCRIPTION

Clock gate savings reporting failed.

WHAT NEXT

Nothing.

PWR-942 (Warning) Could not find a %s pin on cell %s.

DESCRIPTION

During clock gate savings analysis, a cell was found, and a particular pin on the cell was searched for but could not be found.

If the cell is an ICG cell, but it is not used as a clock gate, this error will be generated because the clock pins on the cell could not be determined using timing information. Even if the cell is part of the clock tree, if (for instance) the enable on the cell is tied high, then the cell is not be used as a clock gate, and this warning will be reported.

If this warning is reported, the given cell will be excluded from the report and from any averaged reported by the command.

WHAT NEXT

No suggestion.

PWR-943 (error) Could not find a clk_in pin on cell %s involved in clock gating.

DESCRIPTION

During clock gate savings analysis, a cell was found to be involved with clock gating, but no clk_in pin could be found.

No suggestion.

PWR-944 (error) Could not run command because power is not up-to-date

DESCRIPTION

Something went wrong when running power analysis.

WHAT NEXT

Investigate and successfully run update_power. Then try again the command that issued the error.

PWR-946 (Warning) Identified cell %s is not used as a clock gate and will be skipped.

DESCRIPTION

A leaf cell passed to report_clock_gate_savings was expected to be a clock gate in the design, but was not.

WHAT NEXT

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-947 (Warning) Identified cell %s is not used as a register and will be skipped.

DESCRIPTION

A leaf cell passed to report_clock_gate_savings was expected to be a register in the design, but was not.

WHAT NEXT

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-948 (error) Sorting option %s is not valid unless used with option %s

DESCRIPTION

A -sort_by option was given that is not valid in combination with the other options used.

WHAT NEXT

Change the requested sorting option, or remove the -sort_by option entirely.

PWR-949 (error) No design objects were found for analysis.

DESCRIPTION

During report_clock_gate_savings, no design objects of the type required (either registers or clock gates) were found for analysis.

WHAT NEXT

Check the options used. It may be that the cell_list used was too restrictive. Also check the current_instance to make sure the instance being analyzed is the desired instance.

PWR-950 (error) The value for option peak_window should be a multiple of the interval.

DESCRIPTION

The peak_window option for the command **write_activity_waveforms causes the tool to identify a high ativity in a larger window than the interval. The window size indicated should be a multiple of the interval size.**

Adjust the requested peak_window size to be a multiple of the interval size.

PWR-951 (error) The value for option peak_window is unreasonable

DESCRIPTION

The peak_window option for the command **write_activity_waveforms causes the tool to identify a high ativity in a larger window than the interval. The window size indicated should be larger than the interval size, but limited to no more than a few thousand times the size of the interval. If a larger peak_window is desired, the interval size should be increased as well. If a smaller peak_window is desired, the interval should be smaller also.**

WHAT NEXT

Adjust the requested peak_window size or the interval size.

PWR-952 (error) Hierarchical cell %s cannot be processed by get_switching_activity unless the -average_activity flag is used.

DESCRIPTION

The activity of hierarchical cells can only be reported if the command is instructed to average the activity over the nets in the cell.

If the activity of each net in the hierarchical cell is desired, the following command can be used:

```
pt_shell> current_instance my_hier_cell
my_hier_cell
pt_shell> get_switching_activity [get_net -hier *]
```

WHAT NEXT

Use leaf cells only, or apply the -average_activity flag

PWR-953 (Warning) For clock %s, the toggle rate %g is inconsistent with the toggle rate implied by the clock period, %g.

There may be inconsistency between annotated activity and the sdc. Using %g.

DESCRIPTION

During report_clock_gate_savings default report, the toggle savings for registers is computed from the toggle rate on the primary clock as compared to the toggle rate on the clk pin of the register. In finding the toggle rate of the clock, there was an inconsistency between the clock period, and the toggle rate on the clock net, which may have been annotated.

This situation can arise if the sdc clock was different than that used by simulation to generate the vectors.

When these toggle rates are inconsistent, the annotated value is used.

WHAT NEXT

Check to see if the sdc and simulation used different clock periods.

PWR-961 (error) Please set the variable power_analysis_mode instead of using the command set_power_analysis_mode.

DESCRIPTION

The power analysis mode is controlled by a variable, power_analysis_mode. Accidentally using the command set_power_analysis_mode is a mistake.

WHAT NEXT

The user should use .fBset power_analysis_mode.fP instead.

PWR-970 (Error) Attribute not available while leakage variation analysis is enabled.

DESCRIPTION

The requeste attribute is not available while leakage variation analysis is enabled.

WHAT NEXT

Turn off leakage variation analysis by setting
`power_enable_leakage_variation_analysis` to false. Alternately, you can request the
`leakage_power` attribute for the object, which will contain a quantile value.

SEE ALSO

`power_enable_leakage_variation_analysis`

QTM-1 (error) Cannot create the QTM model '%s' before saving the existing one.

DESCRIPTION

You have tried to create a new QTM model before saving the current QTM model.

WHAT NEXT

Save the current QTM model using **save_qtm_model** and then create a a new QTM model.

QTM-2 (error) There is no QTM model that is currently being defined.

DESCRIPTION

You are using a QTM command without actually creating a QTM model.

WHAT NEXT

Use **create_qtm_model** to create a new QTM model. All QTM commands have to be between a **create_qtm_model** and **save_qtm_model** command.

QTM-3 (error) Unable to load the library '%s'

DESCRIPTION

QTM is unable to load the library you have specified. Perhaps you have not read in the library.

WHAT NEXT

Please make sure that the library is read in using the **read_db** command. QTM will not be able to auto load the library even if the library is in the search path.

QTM-4 (warning) Technology library '%s' has been already been loaded

DESCRIPTION

```
You have already defined the technology library. The existing technology library
will be replaced with the new one.
```

WHAT NEXT

```
If you do not intend to overwrite the existing technology library please reload the
existing technology library
```

QTM-5 (warning) The parameter '%s' has already been set to '%f',
 overriding with the new value.

DESCRIPTION

```
The global parameter has already been set, the existing value will be overridden
with the new value.
```

WHAT NEXT

```
If you do not want to override the existing value of the global parameter, please
set it back to the old value.
```

QTM-6 (warning) The parameter '%s' has already been set to '%s';
  overriding with the new value.

DESCRIPTION

```
The global parameter has already been set, the existing one is overridden with the
new value.
```

WHAT NEXT

```
If you do not want the overridden value, please replace it with the existing value.
```

QTM-7 (error) The option '%s' cannot be used in conjunction with '%s'

DESCRIPTION

The two options cannot be used together. Please use either one of them.

WHAT NEXT

Please use either one of the two options.

QTM-8 (error) To use option '%s', you must also use the option '%s'.

DESCRIPTION

The two options have to be used together, you cannot use one of them alone.

WHAT NEXT

Use the two options together.

QTM-9 (error) To use option '%s', a library should have been specified, but no library has been specified for this model

DESCRIPTION

You are attempting to use a lib_cell, but you have not set the technology library.

WHAT NEXT

Please set the technology library with **set_qtm_technology** with the -library option to set the technology library.

QTM-10 (warning) The path type '%s' has already been defined,

redefining the path type with the new one.

DESCRIPTION

```
The path type has already been defined. The existing path type definition will be
replaced by the new path type definition.
```

WHAT NEXT

```
If you do not want the existing path type definition to be replaced by the new one,
give unique names to the two different path types.
```

QTM-11 (error) The library cell '%s' is not present in the technology
library you have specified.

DESCRIPTION

```
The specified lib_cell is not present in the technology library.
```

WHAT NEXT

```
Please provide the correct lib_cell name.
```

QTM-12 (error) The '%s' pin '%s' you have specified, is not present
in the cell '%s'.

DESCRIPTION

```
The input/output pin name specified is not present in the lib_cell.
```

WHAT NEXT

```
Please provide the correct input/output pin name for the lib_cell you are using.
```

QTM-13 (warning) Fanout count not specified for the path type

'%s';
  using the default fanout of %d.

DESCRIPTION

```
You have not specified the fanout count for the path type definition. The tool uses
a default count of 1.
```

WHAT NEXT

```
If you do not want to use the default fanout count (of 1), please provide the fanout
count using the -fanout option.
```

QTM-14 (warning) The drive type '%s' has already been defined; redefining the drive type with the new one.

DESCRIPTION

```
The drive type has already been defined. The existing drive type definition will be
replaced by the new drive type definition.
```

WHAT NEXT

```
If you do not want the existing drive type definition to be replaced by the new one,
give unique names to the two different drive types.
```

QTM-15 (warning) The load type '%s' has already been defined; redefining the load type with the new one.

DESCRIPTION

```
The load type has already been defined. The existing load type definition will be
replaced by the new load type definition.
```

WHAT NEXT

```
If you do not want the existing load type definition to be replaced by the new one,
give unique names to the two different load types.
```

QTM-16 (warning) The port '%s' has already been created in the model.
Replacing the original port with the new port.

DESCRIPTION

A QTM port with the same name already exists; the original port will be replaced with the new port.

WHAT NEXT

If you want the original port direction, recreate the port.

QTM-17 (error) Must specify one of '%s', or '%s' options

DESCRIPTION

Must use either one of the two options in the command.

WHAT NEXT

Please use one of the two options in the command.

QTM-18 (error) The '%s' QTM parameter '%s' used has not been defined

DESCRIPTION

The QTM parameter you are using has not been defined. Please define the QTM parameters before using them. For e.g., if you are using a path type A in defining a timing arc, please define the path type A before using it in the timing arc.

WHAT NEXT

Please define the QTM parameters (path type, drive type, load type) before using them.

QTM-19 (error) The port '%s' used in the arc is not defined

DESCRIPTION

```
The port referred in the arc has not been defined.
```

WHAT NEXT

```
Please define the ports before using them in the timing arcs.
```

QTM-20 (error) The '%s' port for a '%s' arc must be a '%s' port , but port '%s' is of type '%s'.

DESCRIPTION

```
The port type for the type of arc you are defining is not of the correct type.

For a setup arc, the from port must be of type clock and the to port must be of type
input/inout.

For an edge delay arc, the from port must be of type clock and the to port must be
of type output/inout.

For a combinational delay arc, the from port must be of type input/inout and the to
port must be of type output/inout.
```

WHAT NEXT

```
Create the arc between valid type of ports as explained above.
```

QTM-21 (error) The port '%s' is not a bus, but you have implied a bus structure.

DESCRIPTION

```
You have implied a bus structure for the port, but the port is not a bus.
```

WHAT NEXT

```
If the port is intended to be a bus, define the port to be of bus type, else use the
port in a non bussed fashion.
```

QTM-22 (error) The bus index specified %d:%d for the bus '%s', is out of
the bus array bounds %d:%d.

DESCRIPTION

The indicies used for the bus is not within the array bounds of the bus.

WHAT NEXT

Please check the array bounds of the bus and use the indicies with the array bounds.

QTM-23 (error) The arc that is an edge arc (launch) has
more than one port (%d) as the from port.

DESCRIPTION

An edge delay arc can originate from a single port. In the edge delay arc you have defined, there is more than one 'from' port.

WHAT NEXT

If you want to define more than one edge delay arc to the same port, define different timing arcs, do not combine them in one.

QTM-24 (error) The global '%s' parameter has not been defined, you cannot
define a '%s' arc

DESCRIPTION

Before defining setup/hold/edge delay timing arcs, the corresponding global parameter have to be defined.

Before defining setup arcs, define the global parameter, global setup time using **set_qtm_global_parameter** with -setup option.

Before defining hold arcs, define the global parameter, global hold time using **set_qtm_global_parameter** with -hold option.

Before defining edge delay arcs, define the global parameter, global clock to output time using **set_qtm_global_parameter** with -clk_to_output option.

WHAT NEXT

Define the corresponding global parameter before defining the setup/hold/edge delay arcs.

QTM-25 (error) Cannot get clock pin for the cell '%s'.

DESCRIPTION

The cell does not have a clock pin. If you are defining global setup/hold/ clk_to_output time using a lib_cell, the lib_cell should have the corresponding arc types, which means that the cell must have a clock pin too.

WHAT NEXT

Please use a lib_cell that has an arc corresponding to the global parameter you are defining.

QTM-26 (error) Cannot find a '%s' arc in the cell '%s' from the clock pin '%s'.

DESCRIPTION

If you are defining global parameter (setup/hold/clk_to_output) using lib_cell, the lib_cell must have corresponding arc. Further, if you specify the clock pin, there must be a corresponing arc from the clock pin.

WHAT NEXT

Please provide a lib_cell and a clock pin which has a timing arc corresponding to the global parameter you are defining. For example, If you are defining global setup time, the lib_cell must have a setup arc whith regard to the clock pin. If you are defining global hold time, the lib_cell must have a hold arc with regard to the clock pin. If you are defining global clk_to_output time, the lib_cell must have a clk_to_output arc originating from the clock pin.

QTM-27 (error) Cannot find the pin '%s' in the cell '%s'

DESCRIPTION

Cannot find the pin specifed in the lib_cell.

WHAT NEXT

Please check the pin name and give a valid pin name in present in the lib_cell.

QTM-28 (error) Pin '%s' is not of type '%s'

DESCRIPTION

The pin is not of the type desired.

WHAT NEXT

Provide a pin in the lib_cell which is of the type desired.

QTM-29 (error) Could not find arc of type '%s' coming %s the pin %s.

DESCRIPTION

QTM expects a timing arc to come into/go out of the specified pin. It did not find an arc of the corresponding type at the pin.

WHAT NEXT

Please specify a pin in the lib_cell to satisfy the above requirement.

QTM-30 (error) Could not find arc from clock '%s' to the output pin '%s'.

DESCRIPTION

The lib_cell does not have an edge delay arc from the clock pin to the output pin.

Choose the clock pin and output pin such that there is an edge delay arc from the
clock pin to the output pin.

QTM-31 (error) The port '%s' is not defined in the QTM model.

DESCRIPTION

The port you are referring to has not been defined in the QTM model.

WHAT NEXT

Please define the port before referring to the port.

QTM-32 (error) The port '%s' for which the drive is defined is neither an output port nor an inout port.

DESCRIPTION

Drive can be defined only on the output/inout ports.

WHAT NEXT

Please define drives only for output ports.

QTM-33 (error) The drive type '%s' used is not defined

DESCRIPTION

The drive type you have referenced has not been defined.

WHAT NEXT

Please define the drive type before refering to the drive type.

QTM-34 (error) The port '%s' for which the load is defined is not

an input port, a clock port, or an inout port.

DESCRIPTION

A load can be defined only on input/clock/inout ports, and not on output ports.

WHAT NEXT

Define the loads only on input/clock/inout ports.

QTM-35 (error) The load type '%s' used is not defined.

DESCRIPTION

The load type referenced has not been defined.

WHAT NEXT

Please define the load type first before referring to it.

QTM-36 (error) There is no pin '%s' of type %s in the cell '%s'.

DESCRIPTION

The input or output pin specified is not present.

WHAT NEXT

THe pin you specified is not present or the direction of the pin might not be right.

QTM-37 (error) No arc exists from '%s' to '%s' in the lib_cell %s.

DESCRIPTION

Could not find a combinational arc between the two specified pins.

WHAT NEXT

Please specify the pins between which there is a combinational arc.

QTM-38 (information) Path Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s
   Delay : %f.

DESCRIPTION

This is an informational message that provides the details of the path type defined.

WHAT NEXT

This is not an error message.

QTM-39 (information) Load Type: %s, Cell: %s, Pin: %s.

DESCRIPTION

This is an informational message which provides the details of the load type defined.

WHAT NEXT

This is an information message.

QTM-40 (information) Drive Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s .

DESCRIPTION

This is an informational message which prints the details of the drive type defined.

WHAT NEXT

This is an informational message.

QTM-41 (information) Parameter: %s, Cell: %s, Clock Pin: %s, Input

Pin: %s, Constraint Value : %f.

DESCRIPTION

This informational message prints out the details of the global parameter defined.

WHAT NEXT

This is an informational message.

QTM-42 (information) Parameter: clk_to_output, Cell: %s, Clock Pin: %s, Output Pin: %s
Delay Value : %f

DESCRIPTION

This informational message prints the details of the clk_to_output parameter defined.

WHAT NEXT

This is an informational message.

QTM-43 (error) Parameter '%s' cannot be a negative number

DESCRIPTION

The parameter cannot have a negative value

WHAT NEXT

You have entered a negative for a parameter which is invalid. Please enter a value greater than 0 for the parameter

QTM-44 (error) Port '%s' not defined to be a clock

DESCRIPTION

For a constraint/clk_to_output arc, the from port must be a clock.

WHAT NEXT

Create the constraint/clk_to_output arc staring from a clock port.

QTM-45 (error) Port '%s' not of the type input/inout.

DESCRIPTION

The 'to' port of a constraint arc must be of the type input/inout. Any other port direction is illegal.

WHAT NEXT

Create the constraint arc ending in an input/inout port.

QTM-46 (error) Port '%s' not of the type output/inout.

DESCRIPTION

The 'to' port of a delay arc must be of the type output/inout.

WHAT NEXT

Create the delay arc ending in an output/inout port.

QTM-47 (error) Port '%s' not of the type input/inout.

DESCRIPTION

The 'from' port of a delay arc must be of the type input/inout.

WHAT NEXT

Create the delay arc starting from an input/inout port.

QTM-48 (warning) The port '%s' has invalid name.

DESCRIPTION

A QTM port with an invalid name is being created. Examples, are " ", "/".

WHAT NEXT

Check the name of the port that you are creating. If the ports are defined in a
list, check the list.

QTM-49 (warning) Wire Load Model '%s' does not exist in the library.

Using 0 capacitance.

DESCRIPTION

The Wire Load Model specified must exist in the technology library.

WHAT NEXT

Specify a valid Wire Load Model name.

QTM-50 (error) Input transitions have already been defined for drive type '%s'.

DESCRIPTION

The drive type you have referenced has been defined with rise and/or fall input
transitions. You cannot specify the transition again for the port.

WHAT NEXT

Please define another drive type without transition specification before refering to
it for this port.

QTM-51 (error) %s.

DESCRIPTION

This is a general error message due to some unexpected command options, and/or
settings in creating the QTM.

WHAT NEXT

Please correct the indicated error and try again.

QTM-52 (error) Attribute '%s' for object class '%s' %s type '%s'.

DESCRIPTION

This is an error message indicating the specified attribute for the indicated QTM
object class has already been defined to the given type, or it is an application
reserved attribute of the specified type.

WHAT NEXT

Please correct the indicated error and try again.

QTM-53 (information) Defining new attribute '%s' of type '%s' for object class '%s'.

DESCRIPTION

This is an informational message indicating the specified attribute for the QTM
object class has been successfully defined.

WHAT NEXT

No user action necessary.

QTM-54 (error) %s '%s' has not been defined.

DESCRIPTION

```
This is a general error message indicating the specified object has not been defined
in the QTM, therefore it cannot be refered to in other commands.
```

WHAT NEXT

```
Please correct the indicated error and try again.
```

QTM-55 (error) No attribute named '%s' is defined for object class '%s'.

DESCRIPTION

```
This is an error message indicated the named attribute for the specifed object class
has not been defined yet.
```

WHAT NEXT

```
Please define the attribute for the QTM object class before set it on objects.
```

QTM-56 (error) Attribute named '%s' for object class '%s' is not defined as type '%s'.

DESCRIPTION

```
This is an error message indicated the named attribute for the specifed object class
has not been defined yet.
```

WHAT NEXT

```
Please define the attribute for the QTM object class before set it on objects.
```

QTM-57 (warning) Attribute '%s' is not defined for %s%s.

DESCRIPTION

```
This is a warning message indicating that the named attribute for the specifed
object/class has not been defined yet.
```

WHAT NEXT

```
Please define the attribute for the QTM object class before set or remove it on
objects.
```

QTM-58 (information) Attribute '%s' has already been set on%s'%s'
and is now replaced with the new value.

DESCRIPTION

```
This is an informational message indicating that the named attribute for the
specifed object/class has not been re-defined, so the value is updated.
```

WHAT NEXT

```
No user action is necessary.
```

QTM-59 (error) The specified value '%s' does not match the defined
data type '%s'.

DESCRIPTION

```
This is an error message indicating the given attribute value does not match the
type defined for the attribtue.
```

WHAT NEXT

```
Please correct the indicated error and try again.
```

QTM-60 (information) Attribute '%s' successfully removed for '%s'.

DESCRIPTION

This is an informational message indicating the specified attribute for the QTM object has been successfully removed.

WHAT NEXT

No user action necessary.

QTM-61 (error) Cannot find a proper timing arc in the specified lib cell to define the drive.

DESCRIPTION

This is an error message indicating that PrimeTime cannot find a proper delay arc in the specified cell to be used in defining the drive. There are 2 possible reasons for this: 1. the absense of a proper delay arc to be used as a driving arc. 2. there are ambiguities in deciding a specific arc that can be used to define the drive.

WHAT NEXT

If the error is caused by absense of proper timing arcs in the lib cell, please choose another lib cell with arcs providing the intended driving characteristics. If the error is caused by ambiguity, please use options such as -input_pin and -output_pin to tell PrimeTime exactly which timing arc should be used to define the drive.

QTM-62 (warning) Defining '%s' attribute on %s disables %s, %s.

DESCRIPTION

This is a general warning message. It may not be an error requiring corrective action, but it provides important information for your reference.

For example, the 'function' attribute for lib_pin, even thought QTM allows 'function' attribute be defined for ports, but it treats the boolean logic expressions as string literals, does not perform any syntax check, and only writes QTM with such attributes to .lib format, the correctness of the attributes therefore

only enforeced when compiled by LibraryCompiler.

WHAT NEXT

Please note and confirm the indicated reason/action and make any changes if necessary.

QTM-63 (error) Attribute '%s' for object class '%s' can not be defined for %s '%s', %s.

DESCRIPTION

This is an error message indicated the named attribute for the specifed object class is not applicable to the named object.

WHAT NEXT

Please correct the definition of the attribute for the indicated QTM object and try again.

RC-001 (error) The parasitics of the net '%s' could not be completed.

DESCRIPTION

There are some dangling nodes in the partially annotated parasitics of the net.

WHAT NEXT

You must correct the parasitics file and try to complete the net again.

RC-002 (warning) The net '%s' controls only a subset of the drivers of the multi-driven net '%s', so detailed RC delay calculation cannot be used.

DESCRIPTION

A net is controlling the switching activity of only a subset of the drivers of a multi-driven net; the switching activity of the remaining drivers is uncertain, so detailed RC delay calculation cannot be used. Instead, the load will be assumed to be the total capacitance of the multi-driven net divided by the number of drivers.

WHAT NEXT

Ensure all drivers are switched by each from-net (i.e. that they are wired in parallel), or annotate delays and transition times if you seek greater accuracy than the lumped fallback analysis can provide.

SEE ALSO

DES-023 (n), **RC-003** (n), **set_annotated_delay** (2), **set_annotated_transition** (2).

RC-003 (warning) The net '%s' connects to more than one pin and/or arc on a driver of the multi-driven net '%s', so detailed RC

delay calculation cannot be used.

DESCRIPTION

A net is ambiguously controlling the switching activity of the drivers of a multi-driven net, so detailed RC delay calculation cannot be performed. Instead, the load will be assumed to be the total capacitance of the multi-driven net divided by the number of drivers.

WHAT NEXT

Ensure all drivers are switched by each from-net in a unique way, or annotate delays and transition times if you seek greater accuracy than the lumped fallback analysis can provide.

SEE ALSO

DES-023 (n), **RC-002** (n), **set_annotated_delay** (2), **set_annotated_transition** (2).

RC-004 (warning) Failed to compute C-effective for the timing arc
  %s (%s%s)
  %s
  %s

DESCRIPTION

This message warns you that the cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so a lumped capacitance is being used to compute the cell delay. To ensure conservative results, the total capacitance of the RC network is used in max analysis mode, and zero capacitance in min analysis mode. If the library data for the total or zero capacitance is unphysical, the warning message RC-008 is issued at the end of a timing update to inform you that the min and/or max bounds on correct results cannot be guaranteed.

Reasons for this failure fall into three classes: library-related, parasitics-related, and design-related. Each is discussed in text that follows, along with possible solutions.

Library-Related Problems

One of the following messages is appended to this warning to explain the library-related reason for the C_effective failure:

1. "because the library data indicates a non-positive drive resistance"

This message is appended if the cell delay and/or output transition time does not increase with increasing output load capacitance. This condition can be caused by extrapolating too far outside the library table, or by problems in the table itself.

Solution: Check the timing arc on a lumped load using the **set_load** and **report_delay_calculation** commands; you might have to annotate delays and transition times until the library data can be fixed by the library vendor. Typically, extrapolations disappear when buffer trees are applied to large fanout networks.

2. "because the library data is inconsistent with a linear-driver model"

This message is appended if the parameters of the linear-driver model cannot be determined for this timing arc and/or RC network. Usually the trip-point variables have not been set correctly, or the library data is artificial. If generic_cmos library models are being used, ensure that the later slew trip-point is the same as the delay trip-point.

Solution: Double-check the settings of the RC delay-calculation thresholds using attributes or the **report_driver_model** command; if the library does not set these you will have to set the shell variables (c.f. DES-021). The attributes have the same names as the shell variables and are annotated on the design. If the thresholds are correct, then there is a problem with the library data. If you have access to the library source, ensure that any generic_cmos library models present are used correctly (the later slew trip-point must be the same as the delay trip-point). If nonlinear delay models (a.k.a. tables) are used, confirm that the data was derived from transistor simulation with sufficient accuracy; sometimes libraries are characterized with insufficient accuracy or the data has been manually manipulated in some way. If you do not have access to the library source, then you can try as a temporary measure (i.e. until the library can be fixed) to relax PrimeTime's effective-capacitance error tolerance; increase the value of the hidden shell variable **rc_ceff_delay_min_diff_ps** from its default value of 0.25 to 0.5 or greater. Please note that relaxing this error tolerance will help avoid falling-back to lumped RC delay-calculation in RC-004 cases, but it will also adversely impact accuracy for those delay-calculations without RC-004 messages.

Parasitics-Related Problems

One of the following messages is appended to this warning to explain the parasitics-related reason for the C_effective failure:

1. "because C_total is less than or equal to zero"

This message is appended if the total capacitance of the RC network is not positive, so that there is no way to determine an effective capacitance.

Solution: Check the network using **report_net -connections -verbose** and correct the parasitics file if necessary.

RC

2. "because the RC network has an invalid reduced-order model"

This message is appended usually if the annotated connectivity does not match the logical connectivity; for example, if there is an unconnected pin in the design.

Solution: Look for earlier **link_design** (LNK) warnings pertaining to the problematic net. In rarer situations, there might be a non-positive resistive and/or capacitive path to ground. Check the network with **report_net -connections -verbose** and correct the parasitics file if necessary.

3. "because the RC network has an invalid pole-residue model"

This message is appended if the network has poles and residues that do not generate a converging waveform. Usually this is caused by problems in the network definition has problems.

Solution: Check the network with **report_net -connections -verbose** and correct the parasitics file if necessary. This reason applies only to pi-models (for example, RSPF and RNETs in SPEF).

Design-Related Problems

The following message is appended to this warning to explain the design-related reason for the C_effective failure:

"because the from_pin is unconnected"

This message is appended if a driving arc on a multi-driven network has an unconnected from_pin. In this case, there is no way of knowing the behavior of that arc relative to the other driving arcs of the network; this will prevent RC cell delay calculation from being performed. In this case, you should receive a link warning message, LNK-022, for the unconnected pin; this RC-004 warning message; and a multi-drive warning message, RC-007.

Solution: Connect the from_pin or use commands **set_case_analysis** or **set_disable_timing** to fully qualify the unconnected arc.

TIMING ARC NOTATION

The timing arc is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell name, "2" denotes the cell instance name, "3" denotes the from-pin, "4" denotes the to-pin, "5" denotes the sense direction (min/max rising/falling), and "6" denotes the sense type and unateness.

If the timing arc is through a port with a driving cell, then the message will show the name of the port and the direction (min/max rising/falling). You can use the **report_port -drive** command to get more information about the driving cell(s) set on the port.

RC-005 (warning) Failed to compute the %s RC network delay
from the pin '%s'
to the pin '%s'
in the network '%s'.

DESCRIPTION

The RC network delay for the specified timing arc could not be computed. Common
reasons for this are as follows:

1. Unsupported multi-drive scenarios

Support for RC networks with multiple strong drivers is currently limited to the
case where all drivers are wired in parallel. Thus, if a from-pin on a driver
connected to a network does not connect to a from-pin on all other drivers,
PrimeTime cannot perform RC delay calculation.

Solution: Directly annotate the delays and slews.

2. Networks without timing arcs

You can define networks that have only driver pins or only load pins. If no pins are
bidirectional, PrimeTime cannot perform RC delay calculation. You receive this
warning message if you attempt to report from or to one of these pins.

3. Extremely under-driven networks

Networks that are extremely large for their drivers might not converge to one or
more RC delay calculation thresholds. This sometimes occurs before layout for nets
(for example, clock trees) when buffer insertion has not yet been performed.

Solution: Either adjust the RC threshold variables or directly annotate the delays
and slews.

4. Incompatible voltage-swings

If the driver and load assume different voltage-swings, it is possible that the load
waveform trip-point voltages are not sufficiently covered by the driver voltage-
swing.

Solution: Verify whether the voltage-swing differences are valid. If so, different library trip-points must be used to ensure sufficient coverage. If the voltage-swing differences are invalid, then the design must be fixed. Another common cause of this problem is using a library without a default operating condition; when this occurs one can either fix the library or use the **set_operating_conditions** command on the affected cells. You can see what trip-points are provided by libraries for the delay calculation by using the **report_delay_calculation -thresholds** command, or you can examine the threshold information for a specific library by using the **report_lib** command. See the man page for **lib_thresholds_per_lib** for more information.

WHAT NEXT

Check the network against the above situations and follow the suggested solutions.

SEE ALSO

lib_thresholds_per_lib (3), **rc_slew_lower_threshold_pct_rise** (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3), **report_delay_calculation** (2), **report_lib** (2), **set_annotated_transition** (2), **set_annotated_delay** (2), **set_operating_conditions** (2).

RC-006 (warning) The current wireload mode is %s, 'enclosed' mode is used instead to complete parasitics.

DESCRIPTION

You receive this message if you execute **complete_net_parasitics** or **read_parasitics -complete_with** and the wire load mode is not set or is set to *segmented*. The only allowed wire load modes for completion of parasitics are *top* or *enclosed*. This message warns you that the *enclosed* mode is being used.

WHAT NEXT

If it is acceptable to you for the *enclosed* wire load mode to be used to complete net parasitics, no action is required on your part. Otherwise, perform the following steps:

1. Use the **set_wire_load_mode** command to set the mode to *top*.

2. Remove the parasitics using **remove_annotated_parasitics**.

3. Using the **read_parasitics** command, read all the parasitics that were read before the first completion.

4. Complete the parasitics with **complete_net_parasitics** or **read_parasitics -**

complete_with.

RC-007 (warning) Failed to compute C-effective for the %s multi-driven net '%s' driven by cell arcs controlled by the from-net '%s'

DESCRIPTION

This message warns you that the cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific set of timing arcs, so the total capacitance is being used. Reasons for this failure fall into two classes, library-related and parasitics-related. For information about these, see the manual page for message RC-004.

An additional multi-drive-specific reason for failure could be that the collective action of multiple drivers causes the output waveform to switch faster than the library delay returned for zero output capacitance. This is a fundamental limitation of using gate-level models in multi-drive analysis. When this situation occurs, PrimeTime uses driver models with zero load to preserve the max bound on timing results; note that there is no adequate fallback for preserving the min bound. For more information, see the manual page for message RC-008.

WHAT NEXT

Validate the driver arcs in question with lumped output capacitances; use a value equal to the total capacitance of the multi-driven net divided by the number of strong drivers. Also, detect any multi-driven networks that have large input skew, such that a driver output pin transitions before its input pin does. If the output switches faster than the library delay with zero load, use annotated delays and slews from simulation when high accuracy is needed.

RC-008 (warning) The type of RC delay calculation problem(s) that
have occured prevents the %s results from bounding

the correct values.

DESCRIPTION

When RC delay calculation fails, PrimeTime performs an analysis to determine whether
the choice of fallback value will continue to preserve the reported min and max
bounds on the correct value. This message is displayed when the specified bound(s)
cannot be guaranteed.

The most common cause of this situation is a library table extrapolation that
returns a negative slew; in that case, a zero delay and zero slew are propagated and
the min-max bounds cannot be guaranteed.

Another cause of this situation is a multi-driven network that switches faster than
the library delay returned for zero output capacitance. If this occurs during min
analysis, there is no way to guarantee that propagating a zero delay and zero slew
preserves the min bound.

WHAT NEXT

Fix the library or change the design to avoid library extrapolations. If you have a
multi-driven network that is failing delay calculation with drivers that can have
negative delay, use annotated delays and slews from simulation to obtain a valid min
bound.

SEE ALSO

RC-004 (n), **RC-005** (n), **RC-007** (n).

RC-009 (warning) The drive-resistance for the timing arc %s (%s%s) is much less than the network impedance to ground; PrimeTime has adjusted the drive-resistance to improve accuracy.

DESCRIPTION

PrimeTime builds a driver model from library data in order to perform RC delay
calculation. The driver model consists of a voltage ramp in series with a resistor;
the resistor helps smooth out the voltage ramp so that the resulting driver waveform
has similar curvature to that of an actual transistor driver. When the drive
resistor is much less than the impedance of the network to ground, the smoothing
effect is reduced, causing RC delay calculation to be potentially inaccurate. This

condition can occur when a very strong driver is connected to a very resistive network. This condition does not arise out of a problem with library data.

When this condition occurs, PrimeTime adjusts the drive resistance to improve accuracy; however, note that even with this adjustment the resulting accuracy might be insufficient. By default, extra pessimism is sought in min analysis mode by not using slew-degradation.

If you wish to turn-on slew degradation in min analysis mode, set the value of the shell variable **rc_degrade_min_slew_when_rd_less_than_rnet** to true.

Also by default, PrimeTime will issue the RC-009 message only for the subset of these conditions where net-delays are greater than driver transition times. This is because these net-delays have depended upon the portion of the driver waveform most affected by drive-resistance, namely that near and beyond the later slew trip-point.

If you wish to see the RC-009 message whenever PrimeTime overrides the drive-resistance (i.e. without the just-mentioned filtering), set the value of the shell variable **rc_filter_rd_less_than_rnet** to false.

With some designs you may get flooded with RC-009 messages. This can occur for two reasons.

The first is that PrimeTime uses a threshold parameter to determine when to override the drive-resistance, and the default value assumes well-distributed RC extraction (i.e. that very resistive nets are extracted with many RC segments). As a rule of thumb, there should not be more than 100 ohms per segment. If you are using too few RC segments, and you do not wish to increase the extraction resolution, then you can either (a) qualify PrimeTime's accuracy in RC-009 mode and suppress the messages with the **suppress_message** command, or (b) change the value of the shell variable **rc_rd_less_than_rnet_threshold** to optimize accuracy for your desired extraction methodology.

The second reason for getting flooded with RC-009 messages is that there may just be a lot of very strong drivers connected to very resistive nets in the design. If this is so, then you can either (a) qualify PrimeTime's accuracy in RC-009 mode and suppress the messages, or (b) annotate delays and slews on the arcs of concern. Another, albeit seldomly possible solution is to use weaker/smaller drivers.

You can shut-off the RC-009 feature completely by setting the shell variable **rc_adjust_rd_when_less_than_rnet** to false.

WHAT NEXT

Simulate the indicated timing arc with the network load to determine whether the accuracy of the PrimeTime result is sufficient. Typically the number of these conditions in a design is very small, and the resulting delay calculations are overly pessimistic. You can back-annotate the simulator results with SDF, or use a weaker driver and/or less resistive network in the design.

TIMING ARC NOTATION

The timing arc is displayed by the warning message with the following six parts:

```
(1) 2/3-->4 (5 6)
```

In the above, "1" denotes the library cell name, "2" denotes the cell instance name,
"3" denotes the from-pin, "4" denotes the to-pin, "5" denotes the sense direction
(min/max rising/falling), and "6" denotes the sense type and unateness.

If the timing arc is through a port with a driving cell, then the message will show
the name of the port and the direction (min/max rising/falling). You can use the
report_port -drive command to get more information about the driving cell(s) set on
the port.

SEE ALSO

read_sdf (2), **report_delay_calculation** (2), **report_driver_model** (2),
set_annotated_delay (2), **set_annotated_transition** (2), **suppress_message** (2),
rc_adjust_rd_when_less_than_rnet (3), **rc_degrade_min_slew_when_rd_less_than_rnet**
(3), **rc_filter_rd_less_than_rnet** (3), **rc_rd_less_than_rnet_threshold** (3).

RC-010 (warning) Fast multi-drive analysis is being used for the multi-driven net '%s' driven by cell arcs controlled with the from-net '%s' [#drivers=%d, #loads=%d, arcs%smatch, opconds%smatch; r/f spreads: slew=%g/%g, skew=%g/%g]

DESCRIPTION

This message warns you that an approximate analysis technique is being applied to
the specified multi-drive scenario. The 'fast multi-drive analysis' can reduce
runtime by many orders of magnitude for massively multi-driven networks. However,
the analysis assumes that all driver timing arcs, operating-conditions, input-slews,
and input-skews are identical. The analysis also assumes the effective-capacitance
is the same for all drivers.

This analysis mode is activated when the number of strong (i.e. non-3state) drivers
on a net exceeds the number specified with the shell variable
rc_driver_count_threshold_for_fast_multidrive_analysis. Setting this variable to
zero shuts the feature off completely.

WHAT NEXT

Ensure the disparity in driver characteristics is sufficiently small to yield
reasonably accurate results. The spreads in operating-conditions and input-slews
should cause small spreads in output-delay and output-slew. The spread in input-
skews should be small as compared to the delays through the network.

If the accuracy of this analysis is insufficient, you can either shut this feature
off or annotate delays and slews onto the network. Note that full-accuracy analysis

of multi-driven nets in PrimeTime scales as the product #drivers x #loads.

MESSAGE NOTATION

This warning message includes some useful information about the multi-drive scenario in order to aid the user in deciding whether fast multi-drive analysis is appropriate. This information includes the number of drivers, the number of loads, whether the driver library timing arcs all match, whether the driver operating conditions all match, and the rise/fall spreads in input-slew and input-skew (in library units).

SEE ALSO

rc_driver_count_threshold_for_fast_multidrive_analysis (3).

RC-011 (warning) An extrapolation far outside the library characterization range has been detected and the delay calculation uses the last library index incremented by %s %s

DESCRIPTION

This message occurs when RC delay-calculation is attempted using slew or load that is much larger than the maximum library slew or load indices of a cell or a pin, or much smaller than the minimum library slew or load indices of a cell or a pin. Extrapolations can cause inaccurate and even unphysical data;

Presently this message is only issued when Composite Current-Source (CCS) driver modeling is used.

For driver slews, driver loads and receiver loads that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%, and the RC-011 message is issued.

For receiver slews that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%. For these cases,the RC-011 messages are not issued since they have minimum or no impact on timing results, if the related driver slew RC-011 messages are addressed.

For slews or loads that are below the minimum library index by more than 80%, delay calculation uses the last library index decremented by 80%, and RC-011 messages are not issued, since they have minimum or no impact on timing results.

WHAT NEXT

The timing arc and pin should be characterized with enough capacitance and slew indices to cover the design, or the design should be changed to stay within the library slew and capacitance characterization ranges.

The following guidelines can be used to address RC-011 messages

Guidelines for Characterizing Design Rule Constraints The max_transition pin attributes are normally present on the input and output pins of library cells. For input pins, the max_transition attribute value should not exceed the maximum slew index in the nonlinear delay model (NLDM) and Composite Current Source (CCS) driver and CCS receiver_capacitance2 tables. The lowest value of the maximum slew index between the NLDM and CCS tables should be used as a reference. The tables used as reference are for the rising and falling timing arcs from the relevant input pin for which the max_transition attribute is being characterized. You should take both the arc-based and pin-based tables into account. The max_capacitance pin attributes are normally present on the output pins of library cells. For output pins, the max_capacitance attribute value should not exceed the maximum load index in the NLDM and CCS driver as well as CCS receiver_capacitance1 and receiver_capacitance2 tables. You should use the lowest value of the maximum load index between the NLDM and CCS tables as a reference. The tables used as reference are for the rising and falling timing arcs to the relevant output pin for which the max_capacitance attribute is being characterized. You should take both the arc-based and pin-based tables into account.

Guidelines for Fixing RC-011 Warning Messages If the libraries used in the design follow the guidelines outlined in the Guidelines for Characterizing Design Rule Constraints section, all RC-011 messages are addressed by fixing the max_transition and max_capacitance violations reported by the report_constraint command. If the libraries are not compliant with these guidelines, you should consider RC-011 warning messages to be important. You need to address the DRCs in the design to fix these warnings.

TIMING ARC NOTATION

The timing arc/pin is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell/pin name, "2" denotes the cell/pin instance name, "3" denotes the from-pin of a cell, "4" denotes the to-pin of a cell, "5" denotes the sense direction (min/max rising/falling), and "6" denotes the sense type and unateness.

If the timing arc is through a port with a driving cell, then the message will show the name of the port and the direction (min/max rising/falling). You can use the **report_port -drive** command to get more information about the driving cell(s) set on the port.

SEE ALSO

report_net (2), **report_delay_calculation** (2).

RC-104 (warning) Failed to compute the cell timing arc
%s (%s%s)
%s
%s

DESCRIPTION

This message warns you that the RC delay calculation based on composite current-source (CCS) data failed to compute for a specific timing arc, so a lumped capacitance is being used to compute the cell delay. To ensure conservative results, the total capacitance of the RC network is used in max analysis mode, and zero capacitance in min analysis mode. If the delay and/or slew library data for the total or zero capacitance is unphysical, the warning message RC-008 is issued at the end of a timing update to inform you that the min and/or max bounds on correct results cannot be guaranteed.

This is the CCS version of the RC-004 warning message.

Reasons for this failure fall into three classes: library-related, parasitics-related, and design-related. Each is discussed in text that follows, along with possible solutions.

Library-Related Problems

One of the following messages is appended to this warning to explain the library-related reason for the delay-calculation failure:

1. "because there is a problem with the driver's CCS data"

This message is appended if the delay-calculation does not produce a full-swing transition on all the netlist pins, or if the threshold voltages for such pins are not all reached. This condition can be caused by the final voltage level that is obtained from integrating the library CCS current data does not get close to the voltage set on the pins, or the final voltage does not drive the net to the second slew trip point of a load pin, or data extrapolating too far outside the library table, or by problems in the table itself.

Solution: Check the timing arc on a lumped load using the **set_load** and **report_delay_calculation** commands; you might have to annotate delays and transition times until the library data can be fixed by the library vendor. Typically, extrapolations disappear when buffer trees are applied to large fanout networks.

Solution: Double-check the settings of the RC delay-calculation thresholds using attributes or the **report_delay_calculation -thresholds** command; if the library does not set these you will have to set the shell variables (c.f. DES-021). The attributes have the same names as the shell variables and are annotated on the design. If the thresholds are correct, then there is a problem with the library data.

Parasitics-Related Problems

One of the following messages is appended to this warning to explain the parasitics-related reason for the delay-calculation failure:

1. "because C_total is less than or equal to zero"

This message is appended if the total capacitance of the RC network is not positive, so that there is no way to perform a valid delay calculation.

Solution: Check the network using **report_net -connections -verbose** and correct the parasitics file if necessary.

2. "because the RC network has an invalid reduced-order model"

This message is appended usually if the annotated connectivity does not match the logical connectivity; for example, if there is an unconnected pin in the design.

Solution: Look for earlier **link_design** (LNK) warnings pertaining to the problematic net. In rarer situations, there might be a non-positive resistive and/or capacitive path to ground. Check the network with **report_net -connections -verbose** and correct the parasitics file if necessary.

Design-Related Problems

One of the following messages is appended to this warning to explain the design-related reason for the delay-calculation failure:

1. "because some load-pin thresholds are not covered"

This message is appended if load pin delay or slew threshold is outside the range of the driver output voltage.

Solution: Double-check the load pin thresholds. For example, you can run **report_delay_calculation -thresholds** command.

TIMING ARC NOTATION

The timing arc is displayed by the warning message with the following six parts:

(1) 2/3-->4 (5 6)

In the above, "1" denotes the library cell name, "2" denotes the cell instance name, "3" denotes the from-pin, "4" denotes the to-pin, "5" denotes the sense direction (min/max rising/falling), and "6" denotes the sense type and unateness.

If the timing arc is through a port with a driving cell, then the message will show the name of the port and the direction (min/max rising/falling). You can use the **report_port -drive** command to get more information about the driving cell(s) set on the port.

SEE ALSO

RC-004 (n), **RC-008** (n), **DES-021** (n), **rc_slew_lower_threshold_pct_rise** (3), **rc_slew_lower_threshold_pct_fall** (3), **rc_slew_upper_threshold_pct_rise** (3), **rc_slew_upper_threshold_pct_fall** (3), **rc_input_threshold_pct_rise** (3), **rc_input_threshold_pct_fall** (3), **rc_output_threshold_pct_rise** (3), **rc_output_threshold_pct_fall** (3), **rc_slew_derate_from_library** (3), **report_net** (2), **report_delay_calculation** (2), **set_annotated_transition** (2), **set_annotated_delay** (2), **set_load** (2).

RMDB

RMDB-1 Failed to Initialize MWX Api's (error) code '%d' .

DESCRIPTION

WHAT NEXT

RMDB-2 (error) Failed to open lib '%s'.

DESCRIPTION

WHAT NEXT

RMDB-3 (warning) The logic db and CEL view netlist data maybe out of sync. Please sync up in milkyway before running read_mdb.

DESCRIPTION

WHAT NEXT

RMDB-4 (error) Failed to open lib '%s'.

DESCRIPTION

WHAT NEXT

RMDB-5 (info) The logic db and CEL view netlist data maybe out

of sync. Please sync up in milkyway before running read_mdb.

DESCRIPTION

WHAT NEXT

RMDB-6 (error) internal error reading the cells.

DESCRIPTION

WHAT NEXT

RMDB-7 (error) Failed to get instance name.

DESCRIPTION

WHAT NEXT

RMDB-8 (error) Failed to get cell instance name.

DESCRIPTION

WHAT NEXT

RMDB-9 (error) Failed to get cell instance name.

DESCRIPTION

WHAT NEXT

RMDB-10 (error) Failed to get the instance location for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-11 (error) Failed to get the instance orientation for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-12 (error) Failed to get the instance restriction for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-13 (error) Failed to get the instance restriction for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-14 (error) Failed to get the instance '%s' .

DESCRIPTION

WHAT NEXT

RMDB-15 (error) Failed to get the instance location for '%s' .

DESCRIPTION

RMDB-16 (error) Failed to get the instance orientation for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-17 (error) Failed to get the instance restriction for '%s' .

DESCRIPTION

WHAT NEXT

RMDB-18 (error) Failed to set the route data for net_name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-19 (warning) Via name '%s' not found in Technology file .

DESCRIPTION

WHAT NEXT

RMDB-20 (warning) Via name '%s' not found in Technology file .

DESCRIPTION

WHAT NEXT

RMDB-21 (error) Failed to set the groute data for net_name

'%s'.

DESCRIPTION

WHAT NEXT

RMDB-22 (info) path not supported for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-23 (error) Failed to convert the sites .

DESCRIPTION

WHAT NEXT

RMDB-24 (warning) Split clock net not supported.

DESCRIPTION

WHAT NEXT

RMDB-25 (info) Pin got '%d' .

DESCRIPTION

WHAT NEXT

RMDB-26 (warning) No pins found in the design .

RMDB-27 (error) in setting the pin attributes .

RMDB-28 (warning) Ignoring nondefault rule '%s' .

RMDB-29 (warning) Group '%s' without region .

RMDB-30 (error) Failed to Initialize MWX Api's (error) code '%d'

.

DESCRIPTION

WHAT NEXT

RMDB-31 (error) Failed to open library .

DESCRIPTION

WHAT NEXT

RMDB-32 (warning) Failed to create obstruction for layer '%s'.

DESCRIPTION

WHAT NEXT

RMDB-33 (info) Signal Nets will be ignored for the design .

DESCRIPTION

WHAT NEXT

RMDB-34 (warning) No nets found in the design .

DESCRIPTION

WHAT NEXT

RMDB-35 (error) Failed to get net from the design.

DESCRIPTION

WHAT NEXT

RMDB-36 (info) Creating physical only net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-37 (warning) Failed to create a physical only net '%s' .

DESCRIPTION

WHAT NEXT

RMDB-38 (warning) Failed to create non default rule for net

'%s'.

DESCRIPTION

WHAT NEXT

RMDB-39 (warning) Failed to get routing attribute for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-40 (error) Current design is not linked .

DESCRIPTION

WHAT NEXT

RMDB-41 (error) Failed to Initialize MWX Api's (error) code '%d'

.

DESCRIPTION

WHAT NEXT

RMDB-42 (error) Failed to set the current design '%s' .

DESCRIPTION

WHAT NEXT

RMDB-43 (info) Creating physical only cell '%s'.

DESCRIPTION

WHAT NEXT

RMDB-44 (error) Internal error to get the DB cell instance '%s' .

DESCRIPTION

WHAT NEXT

RMDB-45 (error) Failed to set the conversion factor.

DESCRIPTION

WHAT NEXT

RMDB-46 (error) Internal error Failed to add layer '%s' .

DESCRIPTION

WHAT NEXT

RMDB-47 (error) in setting the layer attribute .

DESCRIPTION

WHAT NEXT

RMDB-48 (warning) Failed to set tracks .

DESCRIPTION

WHAT NEXT

RMDB-49 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-50 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

RMDB-51 (warning) Failed to set the non default rules.

DESCRIPTION

RMDB-52 (warning) Route guides created in the non routing

layer '%s' are not supported .

DESCRIPTION

WHAT NEXT

RMDB-53 (error) Internal error in routing obstructions .

DESCRIPTION

WHAT NEXT

RMDB-54 (error) Failed to open library '%s' with cell '%s'.

DESCRIPTION

WHAT NEXT

RMDB-55 (error) Unable to set the design '%s'.

DESCRIPTION

WHAT NEXT

RMDB-56 (error) Top design is not set correctly .

DESCRIPTION

WHAT NEXT

RMDB-57 (info) Reading Cell information from MDB.

RMDB-58 (warning) Failed to create power/ground net .

DESCRIPTION

WHAT NEXT

RMDB-59 (info) Reading Route information from MDB.

DESCRIPTION

WHAT NEXT

RMDB-60 (info) Creating physical port for '%s'.

DESCRIPTION

WHAT NEXT

RMDB-61 (warning) Failed to create physical port '%s'.

DESCRIPTION

WHAT NEXT

RMDB-62 (warning) Failed to get port location for port '%s'.

DESCRIPTION

RMDB-63 (error) Failed to set port location for port '%s'.

DESCRIPTION

WHAT NEXT

RMDB-64 (info) Signal Nets will be ignored for the design .

DESCRIPTION

WHAT NEXT

RMDB-65 (warning) Failed to create non default rule for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-66 (warning) Failed to get routing attribute for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-67 (warning) Failed to get routing attribute for physical

net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-68 (error) Failed to get the layer name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-69 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-70 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-71 (error) Failed to get the layer name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-72 (warning) Net type cannot be global route type for net

name '%s' .

DESCRIPTION

WHAT NEXT

RMDB-73 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-74 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-75 (error) Failed to get the layer name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-76 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-77 (error) Error in setting the route segment for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-78 (warning) clock skew not supported .

DESCRIPTION

WHAT NEXT

RMDB-79 (warning) Shield net not supported for read_mdb .

DESCRIPTION

WHAT NEXT

RMDB-80 (warning) Failed to set wires for vias on net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-81 (error) Failed to get the via name '%s'.

DESCRIPTION

WHAT NEXT

RMDB-82 (error) Failed to set the route via for net '%s'.

DESCRIPTION

RMDB-83 (error) Failed to set the route via for net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-84 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-85 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

RMDB-86 (error) Cannot get via for '%s'.

DESCRIPTION

WHAT NEXT

RMDB-87 (error) Cannot create library via in design for '%s'.

DESCRIPTION

WHAT NEXT

RMDB-88 (error) Cannot create design via for '%s'.

DESCRIPTION

WHAT NEXT

RMDB-89 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

RMDB-90 (error) Turn Vias are not supported at this time .

DESCRIPTION

WHAT NEXT

RMDB-91 (info) Stack Vias and Turn vias not supported.

DESCRIPTION

WHAT NEXT

RMDB-92 (error) Routing via not translated .

DESCRIPTION

WHAT NEXT

RMDB-93 (error) Via '%s' not translated .

DESCRIPTION

WHAT NEXT

RMDB-94 (Info) SDC information is not read by read_mdb.

DESCRIPTION

The SDC information is not read from the Milkyway database by read_mdb command. The designer has to explicitly read the SDC data from the Milkyway database.

WHAT NEXT

read_sdc(2)

RMDB-95 (error) Directory not writable '%s' .

DESCRIPTION

WHAT NEXT

RMDB-96 (warning) SDC file exists at '%s'.

DESCRIPTION

WHAT NEXT

RMDB-97 (warning) Could not reset incremental SDC flag in Milkyway.

DESCRIPTION

This warning message informs you that although the incremental Synopsys Design Constraints (SDC) may be written out, the flag for incremental SDC in Milkyway cannot not be reset.

Upon further use of this Milkyway database, it may appear that there is no

```
incremental SDC written out.
```

WHAT NEXT

```
This is a warning message only. No action is required on your part.
```

SEE ALSO

`read_mdb` (2).

RMDB-98 (error) Incremental SDC could not be found.

DESCRIPTION

```
This error message appears when there is an error in finding incremental Synopsys
Design Constraints (SDC) in the Milkyway design database.
```

WHAT NEXT

```
Determine if the incremental SDC can be written out using Astro, and annotate that
SDC to the design in the tool by sourcing that SDC.
```

SEE ALSO

`read_mdb` (2).

RMDB-99 (error) The specified cell '%s' doesn't exists in design library '%s'.

DESCRIPTION

WHAT NEXT

RMDB-100 (warning) Failed to set the min/max layer for net '%s'

.

DESCRIPTION

WHAT NEXT

RMDB-101 (error) Unable to create net %s.

DESCRIPTION

```
Read_mdb failed to create a net. Probably the hierarchy information in CEL view is
incorrect.
```

WHAT NEXT

```
Please run astRepairHierPreservation in Astro and rerun read_mdb command.
```

RMDB-103 (error) Port instance %s of cell inst %s not connected to hier net. Please run astRepairHierPreservation in Astro to fix.

DESCRIPTION

WHAT NEXT

RMDB-104 (error) Port instance %s of cell inst %s not connected to hier net. Please run astRepairHierPreservation in

Astro to fix.

DESCRIPTION

WHAT NEXT

RMDB-105 (error) Found new hierarchy %s in MW..

DESCRIPTION

Read_mdb unable to update the milkyway library because of the inconsistencies between the LOGIC view and CEL view.

WHAT NEXT

Fix the MDB and rerun read_mdb command.

There also exists a work-around. You can set variable "mw_create_netlist_from_CEL" to true so that the inconsistent LOGIC view will be ignored. Do not forget to explicitly load the SDC after read_mdb.

RMDB-106 (error) Failed to open the main library '%s'.

DESCRIPTION

Read_mdb cannot open the given MDB library.

WHAT NEXT

Double check the library name and path are correct and you have write permission.

RMDB-107 (error) Failed to open cell '%s' in view '%s' .

DESCRIPTION

Read_mdb unable to open the given cell for write.

WHAT NEXT

Make sure you have write permission to the cell. Also check the mw_reference_library variable to make sure that all the libraries are added correctly.

RMDB-108 (warning) Please update Hierarchy in Astro before running read_mdb.

DESCRIPTION

You get this error because Milkyway does not have a flag set which shows that the hierarchy perservation is not updated.

WHAT NEXT

Run astRepairHierPreservation in Astro before you save the cell and then run read_mdb.

RMDB-109 (error) Failed to close cell .

DESCRIPTION

Read_mdb unable to close the cell that opened earlier. This should be an internal error.

WHAT NEXT

Please check Synopsys for solutions.

RMDB-110 (error) Failed to open cell '%s' in view '%s' .

DESCRIPTION

WHAT NEXT

RMDB-111 (error) Failed to close cell .

DESCRIPTION

WHAT NEXT

RMDB-112 (error) Failed to get the Instances in the design .

DESCRIPTION

Read_mdb failed to get the instance from milkyway library.

WHAT NEXT

Make sure your milkyway library is correct and rerun read_mdb.

RMDB-113 (warning) No cell boundary defined for the design.

DESCRIPTION

Read_mdb could not get the boundary definition from the MDB.

WHAT NEXT

Make sure the boundary is defined before run read_mdb.

RMDB-114 (error) No sites found in the design .

DESCRIPTION

Read_mdb could not find the sites defined for current design.

WHAT NEXT

Make sure the site is defined before run read_mdb.

RMDB-115 (error) Failed to get the site row basearray.

DESCRIPTION

Read_mdb unable to get the site row base array. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-116 (error) Failed to get the site for design.

DESCRIPTION

Read_mdb unable to get the site data from the library. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-117 (error) Failed to set the site '%s' in the db .

DESCRIPTION

WHAT NEXT

RMDB-118 (warning) No tracks in the design.

DESCRIPTION

Read_mdb unable to get the track. This usually means that the MDB library was not correctly prepared.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-119 (error) Failed to set the track '%s' .

DESCRIPTION

read_mdb could not set the track. This could happened if running out of memory.

WHAT NEXT

Rerun the command with more memory.

RMDB-120 (warning) Maximum number of pins exceeded the equivalent pin class.

DESCRIPTION

The equivalent pin class number exceeded the predefined maximum number in MDB. This mostly happened because of some internal error.

WHAT NEXT

Make sure your MDB library is correct before call read_mdb. As a workaround, you can

```
also try to manually reduce the pin number.
```

RMDB-121 (warning) Maximum number of pins exceeded the equivalent pin class of 1000.

DESCRIPTION

```
Read_mdb limits the number of equivalent pin class to 1000. If the actual number is
more than this, the pin information could not be saved into the db.
```

WHAT NEXT

```
Reduce the equivalent pin class number and rerun read_mdb.
```

RMDB-122 (warning) Pin '%s' not connected to any Net.

DESCRIPTION

```
The given pin is not connected to any net in the MDB library.
```

WHAT NEXT

RMDB-123 (error) Failed to set the rule '%s'.

DESCRIPTION

WHAT NEXT

RMDB-124 (warning) Poly shaped blockages are not supported.

DESCRIPTION

```
DB library does not support poly-shaped blockages. Read_mdb will drop these
blockages if any.
```

RMDB-125 (warning) No group associated with the region .

DESCRIPTION

WHAT NEXT

RMDB-126 (warning) No cells found in the group.

DESCRIPTION

WHAT NEXT

RMDB-127 (warning) No group associated with the region .

DESCRIPTION

WHAT NEXT

RMDB-128 (warning) No cells found in the group.

DESCRIPTION

WHAT NEXT

RMDB-129 (warning) Failed to set the min/max layer for net '%s' .

DESCRIPTION

```
Read_mdb unable to set the min/max layer for the given net. This could happen if
read_mdb cannot get the specified layer.
```

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-130 (error) No nets in the design .

DESCRIPTION

Read_mdb could not find any nets defined in current design. No route information
will be updated.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-131 (error) Failed to get the Net '%s'.

DESCRIPTION

Read_mdb could not find the specified net in the design.

WHAT NEXT

RMDB-132 (error) Failed to get the Net '%s'.

DESCRIPTION

WHAT NEXT

RMDB-133 (error) Unable to create net %s.

DESCRIPTION

read_mdb failed to create a new net. Probably the hierarchy information in CEL view
is incorrect.

Please run astRepairHierPreservation in Astro.

RMDB-134 (info) Sourcing SDC from file %s.

DESCRIPTION

WHAT NEXT

RMDB-135 (error) Linking the design failed .

DESCRIPTION

read_mdb failed to link the design internally. No physical information could be transfered from the MDB library.

WHAT NEXT

Make sure to provide all the necessary libraries. Also check the link command for necessary steps.

RMDB-136 (error) Polygon with odd points!. Dropping last co-ordinate.

DESCRIPTION

WHAT NEXT

RMDB-137 (warning) Round type wire extensions are not supported.

DESCRIPTION

Round type wire extensions are not supported by DB library. Read_mdb will not be able to keep this extension info.

RMDB-138 (info) Incremental SDC is at %s.

DESCRIPTION

An incremental Synopsys Design Constraints file is written in your current working
directory with the name shown. You need to manually source this file to annotate
this SDC to the design. If the switch -update_sdc is provided to read_mdb, the SDC
will be automatically sourced. Incremental SDC are SDC constraints that were created
during an Astro session and are additional to the existing SDC constraints that
describe the constraints of the design.

WHAT NEXT

Source the incremental SDC which is shown, if you want the incremental SDC annotated
on your design. If you have specified the switch -update_sdc to read_mdb, no action
is required by you on this message.

RMDB-140 (error) Internal error in initializing the milkyway host.

DESCRIPTION

WHAT NEXT

RMDB-141 (Warning) Failed to open cell '%s' in view '%s'.

DESCRIPTION

The specified cell doesn't exist on the specified milkyway libraries.

WHAT NEXT

1. Check the mw_reference_library variable to make sure that all the libraries are
added correctly.

RMDB-142 (information) The LOGIC view does not exist. The

tool is creating it in the memory database from a CEL view.

DESCRIPTION

```
This message advises you that the LOGIC view for the specified cell does not exist
in the library. The tool uses the netlist by default and the Synopsys Design
Constraints (SDC) information is not translated. The reason for this action is
because this library was created by using a directory from another tool.
```

WHAT NEXT

```
This is only an informational message. No action is required.
```

```
However, if the result is not what you intended, you can explicitly read the SDC
information from the other tool into the tool that is generating the message. You
can run the change_names command to ensure that your data is consistent with the SDC
that is output from the system.
```

SEE ALSO

```
change_names(2)
```

RMDB-143 (error) dixi2ax_mwUnInit called without Initializing.

DESCRIPTION

WHAT NEXT

RMDB-144 (warning) Failed to read the GCEL grid from milkway design library.

DESCRIPTION

WHAT NEXT

RMDB-145 (warning) Failed to create placement obstruction for

the design.

DESCRIPTION

Read_mdb unable to create the placement obstruction for current design.

WHAT NEXT

Make sure the MDB library is correct before call read_mdb.

RMDB-146 (warning) Failed to attach the TLu+ file for design '%s'.

DESCRIPTION

read_mdb unable to attach the TLu+ file to the design library.

WHAT NEXT

Please manually set the environment variable "tlu_plus_library" with correct value.

RMDB-147 (error) Non-rectangular edge for polygon.

DESCRIPTION

WHAT NEXT

RMDB-148 (warning) Less than 4 points: ignoring POLYGON definition.

DESCRIPTION

WHAT NEXT

RMDB-149 (information) Unable to get direction for port,

assuming INPUT.

DESCRIPTION

read_mdb failed to get the port direction, so just assume it is INPUT.

WHAT NEXT

SEE ALSO

RMDB-150 (information) Unable to get direction for ref port.

DESCRIPTION

read_mdb failed to get the port direction from MDB. Set the direction to UNKNOWN in DB.

WHAT NEXT

SEE ALSO

RMDB-151 (warning) Failed to get port type.

DESCRIPTION

read_mdb failed to get the port type from MDB.

WHAT NEXT

Check if the port type exists in the MDB and rerun read_mdb.

RMDB-152 (warning) Failed to get hierarchical net name.

DESCRIPTION

```
read_mdb unable to get the hierarchical net name from Milkyway library. This could
be an internal error.
```

WHAT NEXT

```
Please try astRepairHierPreservation in Astro.
```

SEE ALSO

RMDB-153 (warning) More than one base array found.

DESCRIPTION

```
Read_mdb got more than one base array for the given design from MDB library.
```

WHAT NEXT

SEE ALSO

RMDB-154 (warning) Core area may not be set correctly.

DESCRIPTION

```
read_mdb failed to get the core area for the given design.
```

WHAT NEXT

```
Check the mdb library and rerun read_mdb.
```

RMDB-155 (warning) Failed to create routing obstruction.

DESCRIPTION

WHAT NEXT

RMDB-156 (information) Updating netlist from Milkyway database.

DESCRIPTION

This information message occurs when the tool is updating a netlist from the Milkyway database.

This message does not occur if the Milkyway database was initially created using a Jupiter or Astro flow.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

mw_create_netlist_from_CEL(2)

RMDB-157 (information) Processing master '%s'.

DESCRIPTION

This information message occurs when the **read_mdb** command is processing the specified design master.

WHAT NEXT

This is only an information message. No action is required.

RMDB-158 (error) Failed to get cell name.

DESCRIPTION

WHAT NEXT

RMDB-159 (error) Failed to initiate an iterator through ports in the cell.

DESCRIPTION

WHAT NEXT

RMDB-160 (error) Failed to initiate an iterator through cell instances in the cell.

DESCRIPTION

WHAT NEXT

RMDB-161 (error) Failed to initiate an iterator through port instances in the cell.

DESCRIPTION

WHAT NEXT

RMDB-162 (error) Voltage area %s contains no hierarchical

objects.

DESCRIPTION

```
read_mdb could not find any hierarchical cell belong to the given voltage area. This
usually means that the voltage attribute was not correctly set for the cells.
read_mdb does not recognize the voltage attribute set only to the leaf cells.
```

WHAT NEXT

```
Update the voltage area attribute for the hierarchical cells and do read_mdb again.
```

RMDB-163 (warning) Exclusive plan group '%s' is translated to non-exclusive bounds in the tool.

DESCRIPTION

```
This warning occurs because the tool does not support exclusive plan groups. These
plan groups are treated as non-exclusive plan groups (bounds) for reading and
writing purposes. Any subsequent writing would transfer the exclusive plan groups to
non-exclusive bounds in this tool.
```

```
The hardness level of the bound is determined by the rigidity on the plan group. The
tool considers anything other than rigidity of 10 to be soft bounds.
```

WHAT NEXT

```
You can create non-exclusive plan groups for a smooth flow between JXT/Astro. You
can also convert all of the exclusive plan groups to voltage areas before doing any
reading.
```

RMDB-164 (info) Successfully read SDC file attached to CEL view.

DESCRIPTION

```
JupiterXT and Astro can attach the SDC file to the CEL view. Read_mdb will read the
attachment and invoke 'read_sdc' to import the SDC constraints. This message
indicates this operation has completed successfully.
```

WHAT NEXT

SCOPE

SCOPE-002 (error) File '%s' is not the expected format of binary scope data file.

DESCRIPTION

```
You receive this message to inform you that the file specified to provide block-
level scope data is not recoganized by PrimeTime as the expected binary format.
```

WHAT NEXT

```
Please make sure the file is the right format and contains the scope data.
```

SCOPE-003 (information) Loading scope data from file '%s'.

DESCRIPTION

```
You receive this message to inform you that the scope constraint data used to do
scope check for the specified blocks are loaded from the given file.
```

WHAT NEXT

```
No user action is needed if the file contains the intended scope data.
```

SCOPE-004 (information) Checking the hierarchical scope of block '%s' as an %s.

DESCRIPTION

```
You receive this message to inform you that the scope checks will be performed for
the cell by treating the cell as the indicated model type.
```

WHAT NEXT

```
No user action is needed.
```

SCOPE-005 (information) Overwriting existing file '%s'...

DESCRIPTION

```
You receive this message to inform you that the scope data captured for the
specified block is being written into the indicated file. Since the file already
exists, so the original data in the file will be overwritten.
```

WHAT NEXT

```
No user action is needed.
```

SCOPE-006 (wanring) Scope data for block '%s' as %s model and
scenario '%s' already exists in the output file '%s', replace the existing data.

DESCRIPTION

```
You receive this message to inform you that the scope data captured for the
specified block as the indicated model type and scenario name already present in the
indicated file, and the existind data will be overwritten and replaced with the
newly captured scope data.
```

WHAT NEXT

```
No user action is needed.
```

SCOPE-007 (error) No valid cell instances to perform the scope check.

DESCRIPTION

```
You received this message because there are no valid cell instance to perform the
scope check.
```

WHAT NEXT

```
Please make sure the cell instances are specified correctly.
```

SCOPE-008 (error) No scope data found in file '%s'.

DESCRIPTION

```
You received this message because there are no valid scope data found in the given
file.
```

WHAT NEXT

```
Please make sure the file contains proper scope data to perform check.
```

SCOPE-009 (error) No scope data defined in file '%s' to check for block/cell '%s' as %s model in scenario '%s'.

DESCRIPTION

```
You received this message because there are no valid scope data found in the
specified file for the given block and scenario.
```

WHAT NEXT

```
Please make sure the file contains proper scope data to perform check.
```

SCOPE-010 (error) Cannot find cell instance named '%s' in the design.

DESCRIPTION

```
You received this message because there are no cells found in the current design
with the specified name to do scope check.
```

WHAT NEXT

```
Please make sure the cell names are correct.
```

SCOPE-011 (error) Cannot determine the model type for cell

instance '%s'.

DESCRIPTION

You received this message because PrimeTime cannot determine the exact timing model
type for the specified cell/block instance and therefore cannot perform correct
scope check for it.

WHAT NEXT

Please make sure the cell names are correct.

SCOPE-012 (warning) Cannot find any pin named '%s' within the cell/block
'%s' at top-level.

DESCRIPTION

You received this message because PrimeTime cannot find a pin as named within the
hierarchy of the cell/block instance to do scope check for it. This can happen when
the cell name is wrong, or the indicated pin is not contained in the model for the
original block.

WHAT NEXT

Please make sure the cell names are correct, and the pin present in the model for
the original block.

SCOPE-013 (information) No scope constraints defined for the input data
signals of cell or block '%s'.

DESCRIPTION

You received this message because PrimeTime cannot find any scope information on the
data signals of the indicated cell/block and therefore will not perform and scope
checks for them. This can happen when there is no input data signals on the cell, or
the input data signals are ignored when capturing the scope for the block.

Please check that proper information is captured in the scope file for the block when the model for the block is generated.

SCOPE-014 (wrning) No top-level clocks propagate to pin '%s'.

DESCRIPTION

You received this message because PrimeTime cannot find any clocks defined at the top-level propagate to the pin as indicated. This can happen when there are missed clock definitions at top-level or redundant clock definitions at block-level when the model and scope data was generated.

WHAT NEXT

Please check that clocks are properly defined at both the block and top level.

SCOPE-015 (information) %s.

DESCRIPTION

This is a general informational message to indicate the progress and/or status of the command execution

WHAT NEXT

No user action is needed.

SCOPE-016 (warning) Ignoring a duplicated instance name for cell/block '%s', scope check for the block is done only once.

DESCRIPTION

This is a warning message because the indicated cell/block instance have been specified multiple times, only one will be checked.

WHAT NEXT

Please specify a cell instance only once in the -instance option to avoid the the warning message.

SCOPE-017 (warning) %s.

DESCRIPTION

```
This is a general warning message for some potential siginificant issues found when
performing scope checks.
```

WHAT NEXT

```
Please check for any problems indicated by the message and verify the design
settings and command options to avoid the warning message.
```

SCOPE-018 (warning) Unexpected %s range %8.4f(min)->%8.4f(max)
  %s %s, min value is greater than max.

DESCRIPTION

```
This is a warning message for a situation in which the min bound of a scope range is
greater than the max bound, it may be caused by some inproper settings for timing
analysis.
```

WHAT NEXT

```
Please check for any setup related issues that may cause the indicated problem and
verify/correct the design settings.
```

SCOPE-019 (error) Cannot check the scope for cell/block instance '%s',
 it is a black-box and not properly linked.

DESCRIPTION

```
You received this message because the specified cell/block instance is found to be a
black-box in the current design. It is not properly resolved during the design link
time.
```

WHAT NEXT

```
Please make sure the library or design source for the named cell is provided and
```

properly linked.

SCOPE-020 (error) %s.

DESCRIPTION

This is to inform the user that the tool has encountered a general error as indicated

WHAT NEXT

Please make sure the error is fixed and try issue the command again.

SCOPE-021 (error) Scope file '%s' is created by %s version of PrimeTime and can no longer be read in for analysis.

DESCRIPTION

You receive this message to inform you that the file specified for PrimeTime to load scope data from is a binary scope file, but created by a certain version of PrimeTime as specified which is no longer being supported by the current version of PrimeTime.

For example, a scope file created by the first beta version of the hierarchical block scope analysis feature for PrimeTime, i.e. 2004.06-Beta3, is not supported by the 2004.06 production and later releases.

However, this is only a special case. In general, scope files will be kept backward compatible. This means a later release of PrimeTime will understand and make use of the scope files created by previous releases of PrimeTime. Therefore, the scope files do not need to be re-generated with each releases of PrimeTime in general.

WHAT NEXT

Please re-create the scope file with the new version of PrimeTime, so it can be read in for scope checking and analysis.

SDC

SDC-1 (information) Setting sdc_version outside of an SDC file has no effect

DESCRIPTION

You set the **sdc_version** variable outside of the context of an SDC file. In that context, changing the variable has no effect.

WHAT NEXT

No action necessary.

SDC-2 (warning) SDC version in file (%s) does not match the version you requested
 from read_sdc (%s). Some constraints and options may not function.

DESCRIPTION

The version indicated by the setting of the **sdc_version** variable in your SDC file does not match the version requested by the **read_sdc** command.

WHAT NEXT

Ensure that you select the correct version when issuing the **read_sdc** command.

SDC-3 (warning) Constraint '%s' is not supported by %s.

DESCRIPTION

Not all Synopsys Design Constraints are supported by all applications. The specified constraint is not supported by the current application, and it is ignored. For example, test constraints are not recognized by PrimeTime. One SDC-3 message is issued per instance of the constraint which is ignored. Then, after **read_sdc** completes, an SDC-4 summary message will tell you how many of each constraint was ignored.

SDC-4 (information) Ignored %d unsupported '%s' constraint%s.

DESCRIPTION

This is a summary message indicating how many instances of a particular constraint were ignored by **read_sdc** because the constraint is unsupported.

WHAT NEXT

SDC-5 (error) Errors reading SDC file:
 %s.
 Use error_info for more info.

DESCRIPTION

This message is generated by **read_sdc** when an syntax error occurs during the read. The specific error is shown in the text of the message.

WHAT NEXT

You can use **error_info** to help trace the cause of the error. For example, it might show the file and line number of the syntax error.

SDF-001 (error) SDF version '%s' is not supported. The following SDF versions are supported: '%s'.

DESCRIPTION

The SDF version is not supported.

WHAT NEXT

Use an SDF version which is supported.

SDF-002 (error) Error in SDF file '%s' near line %d : wrong divider '%s'.

DESCRIPTION

Only dividers '.' and '/' are allowed by SDF.

WHAT NEXT

Use a supported DIVIDER symbol in SDF.

SDF-003 (warning) No library was found on the search path; time unit '%s'
 is assumed.

DESCRIPTION

There was no library found on the search path.

WHAT NEXT

Verify the search path with **list search_path** and verify the link library is under the search path. The link library is specified with **link_library**. Use **link** to verify the design has necessary libraries on the search path. Read the timing file once again after fixing the link errors.

SDF-004 (warning) The library '%s' has no time unit specified, '%s' is assumed.

DESCRIPTION

```
The library has no time unit specified. By default the time unit is nanosecond and
time scale is 1. The only valid library time unit for the sdf format are 0.001,
0.01, 0.1, 1, 10, and 100. The time unit is specified in the library with the
attributes time_scale and time_unit_name. For example, a library with timing values
in 10 picosecond units is specified with the attributes: time_scale = 10 and
time_unit_name = ps. read_timing assumes the technology library time unit is 1ns.
The time unit in the sdf file is specified with 'timescale' construct.
```

WHAT NEXT

```
If this assumption is incorrect, modify the scale and time unit of the sdf timing
file before reading it in the Design Compiler product.
```

SDF-005 (warning) No library was found on the search path; time unit '%s'
   is assumed.

DESCRIPTION

```
There was no library found on the search path.
```

WHAT NEXT

```
Verify the search path with list search_path and verify the link library is under
the search path. The link library is specified with link_library. Use link to verify
the design has necessary libraries on the search path. Read the timing file once
again after fixing the link errors.
```

SDF-006 (warning) The SDF file contains delays for the design '%s',
   which is different from the current design '%s'.

DESCRIPTION

```
The current design and the design that the sdf file was written for are not the
```

same. The 'design' construct in the sdf file contains the name of the design for which the timing file was written. This name should be the same as the **current_design**.

WHAT NEXT

Verify the sdf file was created for the current design, the 'design' construct in the sdf file must contain the name of the current design. Check the usage of the **read_timing** command, you might need to use the **-path** option.

SDF-007 (error) There is '%s'.

DESCRIPTION

There is no current design. SDF file cannot be read if the design is not previously read.

WHAT NEXT

Prior to reading the SDF file, you must read the netlist.

SDF-008 (error) Error in SDF file %s Line %d: %s at or near token '%s'.

DESCRIPTION

A syntax error has been found when reading the SDF file.

WHAT NEXT

Fix the SDF file at the given line and reload the SDF.

SDF-009 (error) Cannot find hierarchical path '%s'.

DESCRIPTION

Cannot find the specify hierarchical path to which SDF delays must be annotated.

Find the correct hierarchical path.

SDF-010 (error) Hierarchical path '%s' corresponds to design '%s', and not to design '%s' as you specified with option -design.

DESCRIPTION

The specified hierarchical path, to which SDF delays should be annotated, corresponds to a design whose name is different from the -design option you specified.

WHAT NEXT

Find the correct design corresponding to the given hierarchical path, or do not specify the design name and the tool will derive it.

SDF-011 (error) Cannot find instance '%s'. All delays related to that instance are ignored.

DESCRIPTION

This instance specified in the SDF file cannot be found in the current design.

WHAT NEXT

Check that the SDF file is correct and corresponds to the current design.

SDF-012 (warning) Library cell '%s' is not used in the current design.

DESCRIPTION

This library cell specified in the SDF file cannot be found in the current library.

WHAT NEXT

Check that the SDF file is correct and corresponds to the current design.

SDF-013 (warning) SDF variables '%s' are obsolete. Please use option 'read_sdf %s'.

DESCRIPTION

```
The Design Compiler sdfin_* variables are obsolete in PrimeTime. Use the equivalent
command line options of command 'read_sdf':

sdfin_top_instance_name <path_name> : read_sdf -strip_path <path_name>

sdfin_fall_net_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_rise_net_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_fall_cell_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_rise_cell_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>

The following sdfin_* variables are obsolete:

sdfin_min_rise_net_delay sdfin_min_fall_net_delay sdfin_min_rise_cell_delay
sdfin_min_fall_cell_delay
```

WHAT NEXT

```
Remove the use of sdfin_* variable and add the equivalent command line option to the
read_sdf command.
```

SDF-014 (warning) SDF variables '%s' are obsolete.

DESCRIPTION

```
The Design Compiler sdfin_* variables are obsolete in PrimeTime. Use the equivalent
command line options of command 'read_sdf':

sdfin_top_instance_name <path_name> : read_sdf -strip_path <path_name>

sdfin_fall_net_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_rise_net_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_fall_cell_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_rise_cell_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>

The folowing sdfin_* variables are obsolete:

sdfin_min_rise_net_delay sdfin_min_fall_net_delay sdfin_min_rise_cell_delay
sdfin_min_fall_cell_delay
```

WHAT NEXT

```
Remove the use of sdfin_* variable and add the equivalent command line option to the
```

read_sdf command.

SDF-015 (error) Cannot open file '%s'.

DESCRIPTION

The file name provided to **read_sdf** or **write_sdf** cannot be opened.

WHAT NEXT

Validate that the file name is correct. Or, for writing SDF, check that the
directory where you want to write the SDF is opened for writing.

SDF-016 (warning) Timing check arc to internal pin '%s' of libcell '%s'
is not compressed in SDF file.

DESCRIPTION

The timing check arc is not compressed when both from pin and to pin are internal
pins. Also, timing check arc from or to internal pin for NOCHANGE is not compressed.

WHAT NEXT

This is the limitation of current implementation of SDF export.

SDF-017 (error) write_constraints option '%s' not supported in PrimeTime.

DESCRIPTION

The given option used for write_constraints is not supported in PrimeTime.

WHAT NEXT

Check in the PrimeTime User Guide the options supported for write_sdf_constraints.

SDF-018 (warning) There is no delay to write in SDF.

DESCRIPTION

Because there are no delays to write in the SDF, the SDF file is not created.

WHAT NEXT

The most common reason for not having any delay written in SDF is because the design was not linked correctly and have only black boxes.

SDF-019 (warning) The %s of cell '%s' from '%s' to '%s' could not be annotated.

DESCRIPTION

There are more delay arcs or timing check information in SDF than what can be annotated based on the library timing arcs and timing checks. For example, if both rise and fall values exist in SDF for a timing arc which only has a rise value, then the SDF reader will warn that the fall value from SDF cannot be annotated. Another example is when the timing check in the library has data edge and SDF does not, then only the appropriate edge will be annotated.

Note: The timing check portion of this warning is suppressed when reading SDF version one.

WHAT NEXT

Your SDF file can be incorrect, or your library is missing some timing arcs or has incorrect timing checks to match the transition delays specified in SDF.

SDF-020 (error) Unable to open SDF mapping file %s.

DESCRIPTION

PrimeTime was unable to open the SDF mapping file for reading.

WHAT NEXT

Check whether the SDF mapping file exists and has read permissions.

SDF-021 (error) Error reading SDF mapping file %s. Mapping info for only %d cells read.

DESCRIPTION

```
The SDF mapping file has improper syntax. Mapping information for cells which was
specified before the cell at which error occured will be stored and used while
mapping their instances, rest of the file is not read.
```

WHAT NEXT

```
Check whether the SDF mapping file has correct syntax.
```

SDF-022 (error) Unsupported operator used in an expression in SDF mapping file.

DESCRIPTION

```
SDF mapping file contains an unsupported operator.
```

WHAT NEXT

```
See the list of supported operators in the SDF mapping file syntax, and re-write the
expression using only supported operators.
```

SDF-023 (warning) Arc corresponding to label %s on library cell %s not found. Functions that access delays with this label will return 0.0.

DESCRIPTION

```
No arc corresponding to the label exists.
```

WHAT NEXT

```
Check the SDF mapping file.
```

SDF-024 (warning) No library cell named %s found.

DESCRIPTION

```
SDF mapping file had mapping information for a cell, which was not found in any of
the loaded libraries.
```

WHAT NEXT

```
Check the SDF mapping file and correct the library cell name. If the library cell
name is correct, ensure that you have loaded the library prior to using the
"write_sdf -map" command.
```

SDF-025 (error) Value '%d' of level is not greater or equal to 1.

DESCRIPTION

```
The level of hierarchy must be greater than or equal to 1. Level 1 means to include
arcs that start or end at the level of the top design or the instance specified by -
instance. Level N means to include arcs that start or end at the level of the top
design or the instance specified with -instance and at all levels of hierarchy up to
N.
```

WHAT NEXT

```
If you want to include arcs at all levels of the circuit, do not use -level option.
If you want only arcs immediately inside a hierarchical cell, use -level 1 -instance
<cell>.
```

SDF-026 (warning) The SDF file is version 3.0. Current SDF-3.0 supported constructs are: %s.

DESCRIPTION

```
Currently read_sdf has a limited support for SDF 3.0. Only the specified subset of
SDF 3.0 constructs are supported.
```

WHAT NEXT

```
Remove the unsupported SDF 3.0 constructs to avoid any syntax error.
```

SDF-027 (warning) '%s' is not supported with the -include option for SDF version '%s'

DESCRIPTION

You received this message because you executed the **write_sdf** command and specified the SDF constructs **SETUPHOLD** and/or **RECREM** with the -include option. In addition you specified a version using the -version option or alternatively you specified no version and the default of version 2.1 was specified for you. The SDF version you specified does not support **SETUPHOLD** and/or **RECREM**.

WHAT NEXT

Reexecute **write_sdf** and specify a valid version for the constructs as follows **SETUPHOLD**, version 2.1 , version 3.0 **RECREM**, version 3.0

SDF-028 (warning) No delays were found for either ABSOLUTE or INCREMENT

DESCRIPTION

You received this message because no delays were found after either ABSOLUTE or INCREMENT in the SDF file read in by **read_sdf**. This is non spec compliant SDF but the error is ignored and the remainder of the file is read in as normal.

WHAT NEXT

Check that your SDF writer has not ommitted any delays which should have appeared in the empty space after either ABSOULTE or INCREMENT .

SDF-029 (warning) Primetime may not be able to fully annotate SDF generated with the -no_internal_pins option

DESCRIPTION

You received this message because you wrote SDF using write_sdf with the -no_internal_pins option. Primetime does not support the reading of SDF generated with the -no_internal_pins option.

To generate SDF which can be read back in to primetime, use write_sdf without the -no_internal_pin option. If you wish to exclude just internal pins which are checkpins from the SDF, use the -exclude checkpins option, Primetime will be able to fully annotate this SDF.

SDF-030 (warning) Port construct being used.

DESCRIPTION

The port construct is being used instead of the interconnect construct at the reported locations.

SDF-031 (information) Using one port statement for %d net arcs at pin %s.

DESCRIPTION

The port construct is being used instead of the interconnect construct at the reported locations.

SDF-032 (information) Cell delay values of cells %s are being aligned.

DESCRIPTION

The cell delay values of the reported cells are being aligned.

SEE ALSO

sdf_align_multi_drive_cell_arcs(2)

SDF-033 (warning) Both port and interconnect statements have

been used at pin %s.

DESCRIPTION

The net arcs to the specified pin have been written out using both port and interconnect statements. It was not possible to just use a port construct as the net arc delay spread was too great. If cell alignment has been enabled, it will not succeed at this cell pin due to combined port and interconnect usage.

WHAT NEXT

To use only port statements, the **sdf_enable_port_threshold** value will have to be raised. For more details regarding port construct usage and the restrictions on clock network parallel buffers collapse, check the man pages for **sdf_enable_port_construct** and **sdf_align_multi_drive_cell_arcs**.

SDF-034 (warning) The %s construct is not supported for %s sdf delay reading mode.

DESCRIPTION

Only net arc delays can be specified in the sdf file in this mode. All delays referring to other constructs will be ignored. The **port** and **interconnect** are the only supported constructs in this mode.

WHAT NEXT

Read in non-net arc delays using regular read_sdf.

SDF-035 (error) The ABSOLUTE construct is not supported in %s sdf delay reading mode.

DESCRIPTION

Only net arc delays with INCREMENT construct can be specified in the sdf file in this mode. All delays referring to other constructs will be ignored.

WHAT NEXT

Use INCREMENT construct in this mode.

SDF-036 (warning) The sum of the %s values in the cell '%s' for the arc between pins '%s' and '%s' is negative, which is not allowed. To make it positive, the %s value has been adjusted from %f to %f.

DESCRIPTION

This warning message occurs when the sum of the setup and hold values is negative for a given arc. Note that negative values for either the setup time or hold time are allowed; however, their sum must always be greater than 0.

WHAT NEXT

This is a warning message only. No action is required because the %s time has been automatically adjusted to give a positive sum for the setup and hold times.

SDF-037 (warning) Circular timing arcs were detected in the cell '%s' while writing SDF. The pin '%s' is in the loop. SDF information for the cell may contain errors.

DESCRIPTION

The cell pin has circular timing arcs. A circular timing arc occurs when an inout or output pin is related to itself though other inout or output pins. A change in one pin belonging to a circular timing arc continually loops around. Circular timing arcs do not make sense and are probably mistakes.

When writing SDF, timing information for the pin in a circular timing arc might be incorrectly determined.

WHAT NEXT

Check the cell library file and verify the questionable circular timing arcs.

SDF-038 (error) The delta_net_delays_only option can only be used when coupling capacitances are read along with parasitics

and SI analysis is enabled in PrimeTime.

DESCRIPTION

The delta_net delay option of write_sdf writes the delta delays on the interconnects and therefore coupling capaacitances should be read from the parasitics file and, to annotate delta delays on the nets, SI analysis mode should be enabled.

WHAT NEXT

Use -keep_capacitive_coupling with read_parasitics and set si_enable_analysis variable to TRUE

SEC-0 (error) Software is not licensed for this machine.

DESCRIPTION

```
Could not find a valid matching key in the key file for this feature
```

WHAT NEXT

```
Check to see that the machine hostid, using the machine_id utility provided by
Synopsys, matches the hostid in the key file for the feature.
```

SEC-1 (error) %s

DESCRIPTION

```
The key file with all of the license information cannot be opened.
```

WHAT NEXT

```
Check directory and file read permissions.
```

SEC-2 (error) Cannot open key file '%s' or a licensing environment parameter has not been set correctly.

DESCRIPTION

```
The keyfile cannot be read.
```

WHAT NEXT

```
Check the location of the keyfile to see if a keyfile is present and it is readable.
```

SEC-3 (error) Encryption file header is corrupt.

DESCRIPTION

WHAT NEXT

SEC-4 (error) Unknown encryption method.

DESCRIPTION

The application is trying to match the encryption with that in the keyfile. The encryption being used is not correct.

WHAT NEXT

Make sure that the executable is not corrupt or has not been changed.

SEC-5 (warning) License for '%s' expires within %2d days.

DESCRIPTION

The license for the listed feature is going to expire within 2 days.

WHAT NEXT

Contact your Synopsys support representative.

SEC-6 (warning) License for '%s' has expired.

DESCRIPTION

The license for the listed feature has expired.

WHAT NEXT

Please contact your Synopsys support representative.

SEC-10 (error) Software is not licensed for this machine.

DESCRIPTION

There was a problem matching the key file information to the machine you are trying to run the software on.

Possible causes are bad encryption code and the hostid specified in the license file does not match the node on which the software is running.

WHAT NEXT

Check to see if the hostid in the key file matches the machine hostid.

Check to make sure that the key certificate encryption code exactly matches the key file encryption code.

Contact your Synopsys support representative.

SEC-11 (error) Software is not yet enabled or has expired.

DESCRIPTION

The feature trying to be used does not have a valid license. Either the date may be wrong or the encryption may be wrong.

WHAT NEXT

Check the start date of the feature. It may not have been reached. Contact your Synopsys support representative.

SEC-12 (error) Can't communicate with the license server.

DESCRIPTION

The machine you are running the software on is having trouble communicating with the license server.

The attempt to the connect to the vendor daemon on all SERVER nodes was unsuccessful.

WHAT NEXT

Check to make sure that the daemon name in the license file FEATURE line matches the

vendor daemon name.

Check to see that the ethernet device can be located.

Check network connections from node running software to server node(s).

Contact local System Adminitrator.

SEC-13 (error) The date/time difference between your host and the license
 server host is too great.

DESCRIPTION

The date/time difference between your host and the license server host cannot be
greater than 4 hours.

WHAT NEXT

Contact local System Administrator to synch client/host times.

SEC-14 (error) Key file syntax error: %s.

DESCRIPTION

The start or expiration date is invalid.

WHAT NEXT

Check the dates in the license file.

Contact your Synopsys support representative.

SEC-15 (error) Key file '%s' has an unrecognized format.

DESCRIPTION

The keyfile is unreadable.

WHAT NEXT

Check the permissions on the file. It may also not be a text file.

SEC-16 (error) Can't read the '%s' file.

DESCRIPTION

The file /dev/kmem or /vmunix is not readable on this system.

WHAT NEXT

Contact you local System Administrator.

SEC-17 (error) Internal licensing error number %d: %s.

DESCRIPTION

A possible reason is a bad encryption handshake with the server. The client performs an encryption handshake operation with the daemon prior to any licensing operations. This handshake operation failed.

A possible reason is the feature database got corrupted in the daemon. The daemon's run-time feature data-structures have somehow become corrupted. This is an internal daemon error.

A possible reason is that there is no TCP/IP service "license." This happens if a SERVER line does no specify a TCP/IP port number, and the TCP service does not exist. There is no socket to talk to the server on.

WHAT NEXT

Make sure that there is a socket number in the SERVER line of the key file. Also check with your system administrator.

SEC-18 (error) Unknown internal licensing error number: %d.

DESCRIPTION

Unknown error has occurred.

WHAT NEXT

Check the status of the license server and the vendor daemon. Try bringing down the
license server and bringing it back up again.

SEC-20 (error) This site is not authorized for license(s): %s

DESCRIPTION

This site is not licensed to use this product.

WHAT NEXT

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features.

Contact your local Synopsys Support Center.

SEC-21 (error) Failed to checkout license for feature(s): %s

DESCRIPTION

The application failed to check out the licenses required to enable this product. It
may be that all the licenses are in use or the site is not licensed to use this
product.

WHAT NEXT

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features and to
find the current users of the features.

Contact your local Synopsys Support Center.

SEC-22 (information) %s feature '%s'.

DESCRIPTION

This is an informational message indicating the feature that has been queued, checked-out, or checked-in.

WHAT NEXT

If the feature has been queued for sometime, then you can find out the current users of this feature (by using the lmstat -A command) and request them to release it.

SEC-23 (information) Waiting for required feature(s). (%s)

DESCRIPTION

This is an informational message that is displayed periodically when the process is queued for required set of features. You can find out the current users of all the required features by using the lmstat -A command.

WHAT NEXT

Request the current users to release the licenses, if possible.

Let the process wait in queue for indicated period of time to acquire the license.

SEC-50 (error) All '%s' licenses are in use.

DESCRIPTION

The maximum number of licenses has been reached.

WHAT NEXT

Contact your Synopsys support representative to order more licenses.

SEC-51 (error) This site is not licensed for '%s'.

DESCRIPTION

A possible cause is that no such feature exists. The feature could not be found in the license file.

A possible problem is that the version is not supported at the server end. The version specified in the checkout request is greater than the highest version number the daemon supports.

A possible problem is that the server does not support this feature or the feature has expired or has not yet started (on the server node).

WHAT NEXT

Check to make sure that the license file supports this version.

SEC-52 (error) Requested more licenses for '%s' than supported in the key file.

DESCRIPTION

A checkout request was made for more licenses than are supported in the license key file.

WHAT NEXT

Make sure that you hvae enough licenses in the keyfile.

SEC-53 (error) The end-user license options EXCLUDE you from using '%s'.

DESCRIPTION

The user/host/display has been excluded from this feature by an end-user's daemon option file.

WHAT NEXT

Contact your local System Administrator to have your name removed from the EXCLUDE list in the options file.

SEC-54 (error) The end-user license options don't INCLUDE you for using '%s'.

DESCRIPTION

```
The user/host/display has NOT been included in this feature by an end-user's daemon
option file.
```

WHAT NEXT

```
Contact your local System Administrator to include you in the options file.
```

SEC-55 (error) Can't remove your '%s' license. You must always have one or
 more of the following license(s): %s.

DESCRIPTION

```
A request was received to remove a license that is necessary for the application to
be run. At least one of these licenses is required for the application to be
running.
```

WHAT NEXT

```
Make sure that you are removing the right license.
```

SEC-80 (information) Attempting to reacquire license for '%s'; wait %d minutes.

DESCRIPTION

```
The node has lost communication with the license server and is attempting to
reacquire a license. It will try to reestablish connection every minute for the
first X minutes (default is 10, but it will use the number supplied with the -
timeout option). It will retry for four days.
```

WHAT NEXT

```
Contact your local system administrator to check to see whether the license server
or network is hung.
```

SEC-81 (information) Reacquired license for '%s' after %d minutes.

DESCRIPTION

```
The application lost the license due to some reason. It could be that the vendor
daemon died or the license daemon died and it was brought back up again. The
application tries to reconnect to the daemon a few times.
```

WHAT NEXT

```
Make sure that the license and vendor daemons are running.
```

SEC-82 (warning) License server is busy, retrying.

DESCRIPTION

```
The application server is "busy" trying to connect. The license server is busy
establishing a quorum of server nodes so that licensing can start.
```

WHAT NEXT

```
Wait a few minutes. If the license daemon does not start up, bring it down and back
up again. It could also be that one of the servers in the redundant server
configuration is down.
```

SEC-83 (warning) Timeout value must be between %d and %d; using default of %d.

DESCRIPTION

```
The timeout value used is not correct.
```

WHAT NEXT

```
Use the correct timeout value.
```

SEC-84 (warning) Unable to obtain a license for '%s'. Obtained a license for '%s' instead.

'%s' contains these features:%s.

DESCRIPTION

Not all licenses for the application could be checked out.

WHAT NEXT

Check the keyfile amd make sure that you have the licenses for all the features in
the product.

SEC-85 (error) Communication with the license server failed; error number %d.

DESCRIPTION

Bad return from server. The port number returned from lmgrd is invalid. An attempted
connection to a vendor daemon did not result in a correct acknowledgement from the
daemon. The daemon did not send back a message within the timeout interval. A
message from the daemon had an invalid checksum.

Cannot read from server. The process cannot read data from the daemon within the
timeout interval. The connection was reset by the daemon (usually because the daemon
exited) before the process attempted to read data.

Cannot write to server The process could not write data to the daemon after the
connection was established.

Feature checkin failed at daemon end The checkin request did not receive proper
reply from the vendor daemon (the license might still be considered in use).

WHAT NEXT

Make sure that the port number and the path to the daemon in the keyfile are
correct. Either the daemon is down or the machine is not alive. Try checkin again or
try removing the license for that feature.

SEC-86 (error) This site is not licensed for third party software; error number %d.

DESCRIPTION

A possible cause is that no such feature exists. The feature could not be found in

the license file.

A possible problem is that the server does not support this feature or the feature
has expired or has not yet started (on the server node).

WHAT NEXT

Check to make sure that the license file supports this version.

SEC-87 (error) Unable to obtain license for '%s'. Feature is suppressed.

DESCRIPTION

The functionality cannot be invoked for this product package. Possible cause is the
functionality is not supposed to be supported for this product package, eventhough
the license key is available.

WHAT NEXT

If the functionality should be within the product package, contact your Synopsys
support representative.

SEC-88 (warning) Unable to set precedence for key '%s'. Cyclic dependency detected.

DESCRIPTION

Cyclic dependency on the prerequisite licenses detected. Some features may not
execute because of inability to obtain license. If you encounter this warning,
please report it to your Synopsys sypport representative.

WHAT NEXT

Contact your Synopsys support representative.

SEC-89 (information) Unable to set precedence for key '%s'.

Precedence already exists.

DESCRIPTION

```
Order of prerequisite licenses has already existed. Re-setting the precedence is
redundant, and does not cause any harm.
```

WHAT NEXT

```
Contact your Synopsys support representative to ensure that the redundant order
setting is removed in the next product release.
```

SEC-100 (error) This can only be used with software that is network licensed.

DESCRIPTION

```
The application is licensed to run only with network licensing. You may be running
the application by using a node locked license.
```

WHAT NEXT

```
Check the keyfile being used.
```

SEC-101 (information) No one is using any feature from the license server.

DESCRIPTION

```
No features from the keyfile are being used.
```

WHAT NEXT

```
Nothing needs to be done.
```

SEC-102 (error) Unable to get an optimize license.

DESCRIPTION

```
The license cannot be obtained.
```

WHAT NEXT

```
Check the keyfile for this feature. Check the location of the keyfile, default or
SYNOPSYS_KEY_FILE.
```

SEC-103 (error) You must have a Design-Analyzer or one of the optimize licenses to use this feature.

DESCRIPTION

```
The keyfile must have a Design-Analyzer or an optimize license to use this
application.
```

WHAT NEXT

```
Check to see if the keyfile has these features. Check whether the correct keyfile is
being used.
```

SEC-104 (information) Checking out the license '%s'.

DESCRIPTION

```
This is a message from the daemon that the license for this feature is being checked
out.
```

WHAT NEXT

```
Check whether you are using this feature. If so, nothing needs to be done.
```

SEC-105 (information) Checking in the license '%s'.

DESCRIPTION

This is a message from the daemon that the license for this feature is being
released.

WHAT NEXT

Nothing need to be done.

SEC-106 (information) Checking out '%s' implies that '%s' is also available. Checking '%s' back in to avoid duplicate license checkout.

DESCRIPTION

The new license key, "DesignWare", is issued to replace the following old license
keys: "DesignWare-Foundation", "SynLib-ALU", "SynLib-AdvMath", "SynLib-Control",
"SynLib-FltTol", "SynLib-Seq". When the new key is checked out, no old key will be
checked out. If any of the old keys are already checked out, they are checked back
in to avoid having duplicate licenses checked out.

This is a message from the daemon that the license for the specified feature is
being released, because it is not needed.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEDF-1 (error) Unable to open file '%s'.

DESCRIPTION

`The EDIF file you tried to open does not exist or has incorrect permissions.`

WHAT NEXT

`Verify the file name and permissions.`

SEDF-2 (information) Ignoring unrecognized construct '%s' at line %d in '%s' (and all future occurrences).

DESCRIPTION

WHAT NEXT

SEDF-3 (error) Unmatched right parenthesis at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-4 (error) Missing %s parenthesis

at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-5 (error) Net connection failed
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-6 (error) Misplaced percent sign
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-7 (error) Unrecognized token '%s'
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-9 (error) Expected %s

at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-10 (error) Incorrect number of elements in %s construct at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-11 (error) Argument %d for %s construct is invalid at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-12 (error) array name '%s' does not match bus_extraction_style '%s' at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-13 (error) Unexpected %s

at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-14 (error) In rename, '%s' inconsistent with bus extraction style
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-15 (error) ASCII character is not between 0 and 127
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-16 (error) Invalid %s token
at line %d in %s.

DESCRIPTION

WHAT NEXT

SEDF-17 (warning) Duplicate base name '%s' for port bus. Using '%s' instead

at line %d in %s.

DESCRIPTION

The EDIF file contains two port bus (array) definitions which are trying to use the same base name. For example, in[3:2] and in[1:0] both want to use in as the base name. This might be an error, but for compatibility with Design Compiler, this reader will use the full name of one of the port busses as the base name. In this case, it might pick in[3:2] as the base name for one of the port busses.

WHAT NEXT

Verify that this is not a typo in the file.

SEDF-18 (error) Duplicate port name '%s' at line %d in %s.

DESCRIPTION

The EDIF file contains two scalar ports with the same name. This is an error.

WHAT NEXT

Correct the port name and re-read the file.

SDC-1 (information) Setting sdc_version outside of an SDC file has no effect

DESCRIPTION

```
You set the sdc_version variable outside of the context of an SDC file. In that
context, changing the variable has no effect.
```

WHAT NEXT

```
No action necessary.
```

SEL-001 (error) No such collection '%s'

DESCRIPTION

```
The collection which you specified does not exist.
```

WHAT NEXT

```
Verify that the collection is the one you want. It is possible that it existed, but
was transient. Transient collections are automatically garbage-collected and cannot
be relied upon across command boundaries. In order to make a collection persistent,
set it to a variable, and then use it. For example:

    set uPorts [get_ports U*]
    command_for_ports $uPorts
```

SDC-2 (warning) SDC version in file (%s) does not match the version you requested
 from read_sdc (%s). Some constraints and options may not function.

DESCRIPTION

```
The version indicated by the setting of the sdc_version variable in your SDC file
does not match the version requested by the read_sdc command.
```

Ensure that you select the correct version when issuing the **read_sdc** command.

SEL-002 (warning) Collection '%s' has inappropriate type (%s).

DESCRIPTION

The collection which you specified contains objects which are not acceptable for this command. Either the data type of the objects is incorrect, or the objects are out of context (for example, they are not in the current design).

WHAT NEXT

Check the command to determine the allowable object types for it, or specify objects that are in the correct context.

SDC-3 (warning) Constraint '%s' is not supported by %s.

DESCRIPTION

Not all Synopsys Design Constraints are supported by all applications. The specified constraint is not supported by the current application, and it is ignored. For example, test constraints are not recognized by PrimeTime. One SDC-3 message is issued per instance of the constraint which is ignored. Then, after **read_sdc** completes, an SDC-4 summary message will tell you how many of each constraint was ignored.

WHAT NEXT

SEL-003 (warning) Nothing implicitly matched '%s'

DESCRIPTION

The pattern which you specified did not match any objects of the classes acceptable for this command.

WHAT NEXT

Check the pattern to see if it is what you expected.

SDC-4 (information) Ignored %d unsupported '%s' constraint%s.

DESCRIPTION

This is a summary message indicating how many instances of a particular constraint were ignored by **read_sdc** because the constraint is unsupported.

WHAT NEXT

SEL-004 (warning) No %ss matched '%s'

DESCRIPTION

The pattern which you specified did not match any objects of the class acceptable for this command.

WHAT NEXT

Check the pattern to see if it is what you expected.

SDC-5 (error) Errors reading SDC file: %s. Use error_info for more info.

DESCRIPTION

This message is generated by **read_sdc** when an syntax error occurs during the read. The specific error is shown in the text of the message.

WHAT NEXT

You can use **error_info** to help trace the cause of the error. For example, it might show the file and line number of the syntax error.

SEL-005 (error) Nothing matched for %s

DESCRIPTION

```
The pattern(s) which you specified did not match any objects.
```

WHAT NEXT

```
Check the values which you entered.
```

SEL-006 (error) More than one object matched for '%s'.

DESCRIPTION

```
The pattern(s) which you specified matched more than one object. This command option
accepts only a single object.
```

WHAT NEXT

```
Check the values which you entered.
```

SEL-007 (error) Invalid index %d for collection %s

DESCRIPTION

```
During an iteration over a collection (with foreach_in_collection), an invalid index
was generated.
```

WHAT NEXT

```
Contact your application consultant.
```

SEL-008 (warning) Collection/attribute class '%s' has not been defined

DESCRIPTION

```
The collection class which you specified does not exist. Classes of objects include
designs, cells, etc.
```

Verify that the class name is spelled correctly, or that the class of objects is applicable for this product.

SEL-009 (warning) Collection class '%s' cannot be %s

DESCRIPTION

The collection class which you specified cannot be used for the operation you attempted. Some collection classes cannot be queried, indexed, or copied, so they cannnot be used as an argument to query_objects, index_collection, or copy_collection.

WHAT NEXT

Only use collections of this class as arguments to appropriate commands.

SEL-010 (warning) %s objects from '%s' were of the %scorrect class.

DESCRIPTION

A heterogeneous collection was passed to another command. This collection contained some objects that were of a class which is not accepted by the command. The message will indicate whether some objects or no objects were accepted by the command.

WHAT NEXT

Some commands continue to operate when only a subset of the patterns match. Other commands only perform their action when all patterns match something. So, verify that the command was applied to the objects which were expected.

SEL-011 (warning) Some objects (%s) could not be queried.

DESCRIPTION

A heterogeneous collection was passed into query_objects. This collection contained some objects that were of a class which cannot be the target of a query.

```
There is no adverse affect of this situation.
```

SEL-012 (information) Iteration for collection %s was terminated because the collection was modified or deleted.

DESCRIPTION

```
Commands in the body of a foreach_in_collection can affect the collection which is
currently in iteration. Some commands can cause objects to be removed from the
collection, and others can cause the collection to be deleted. When such events
occur, the iterator is modified and in some cases will terminate. This message
advises you of that event.

For example:

foreach_in_collection itr [get_cells *] { remove_design [current_design] }
would cause the collection of cells to be deleted, and the iteration would be
terminated.
```

WHAT NEXT

```
No action is required.
```

SEL-013 (error) Regular expression error: %s.

DESCRIPTION

```
While using a regular expression with a collection command, you entered an invalid
regular expression. For example, use of the * (zero or more) or + (one or more)
operators alone always yields the empty set; therefore, ".*" or ".+" would be
appropriate. Other errors such as unmatched parens or invalid characters within
square braces will also cause this error.
```

WHAT NEXT

```
Take action based on the error that occurred.
```

SEL-014 (error) At least one %scollection required for argument

'%s'%s

DESCRIPTION

Some commands do not allow heterogeneous collections as arguments, whereas others allow them only in some contexts. Other commands require at least one collection as an argument. You entered a variation of a command which requires at least one collection (either homogeneous, or of either type) for the named argument.

WHAT NEXT

Consult the man page from the command which failed for further information.

SEL-015 (warning) Ignored all implicit elements in argument '%s'%s

DESCRIPTION

Many commands allow implicit searches for objects - an argument can be a list of collections or patterns which are searched for in a documented set of object classes. However, in some cases, it is not possible to determine any object classes in which to search for an implicit pattern. For example, attempting to add an implicit pattern to a heterogeneous collection with **add_to_collection** would cause this warning.

WHAT NEXT

Consult the man page from the command which failed for further information.

SEL-016 (error) Name patterns are not allowed in this argument context - the pattern %s will be skipped/ignored; use only collections in this argument context.

DESCRIPTION

Many commands allow implicit searches for objects - an argument can be a list of collections or name patterns which are searched for in a documented set of object classes. However, in some cases, when there is more than one object class to be searched, it is not allowed to include name patterns, and only collections should be included in such an argument.

WHAT NEXT

In the argument context in which this error happened, remove all name patterns from the offending argument, and make sure that only collections are included in the argument. You can typically use a "get" command to convert a name pattern to a collection.

SIM

SIM-001 (error) Number of reference paths %d does not match the number of measured paths %d.

DESCRIPTION

Path comparison is done one path at a time, 1st path in the collection of reference paths with 1st path in the collection of measured paths, 2nd with 2nd etc. Therefore the number of paths in reference and measured path collections must be same.

WHAT NEXT

Make sure that you are comparing collection of same physical paths. If one collection is a superset of the other, use **foreach_in_collections** and **append_to_collections** to create a new collection with subset of path objects to compare.

SEE ALSO

foreach_in_collection (2), **append_to_collection** (2), **sim_get_recalculated_timing_paths** (2), **sim_compare_paths** (2).

SIM-002 (warning) Paths cannot be compared because %s

DESCRIPTION

Path comparison is done pin by pin. Only pins of the same name and rise/fall sense can be compared.

WHAT NEXT

Make sure that you are comparing collection of same physical paths. Use **sim_get_recalculated_timing_paths** to get collection of reference paths.

SEE ALSO

sim_get_recalculated_timing_paths (2), **sim_compare_paths** (2).

SIM-003 (information) The reference path has no simulation data

DESCRIPTION

Only segments of the reference path annotated with Spice-simulated delays are reported during the comparison. This is to avoid both long reports as well as misleading accuracy percentage of overall path delay. To force comparison on all pins of the datapath use **sim_compare_paths -entire_datapath**.

WHAT NEXT

Make sure that you are using **sim_get_recalculated_timing_paths** to get collection of reference paths.

SEE ALSO

report_timing (2), **sim_get_recalculated_timing_paths** (2), **sim_compare_paths** (2).

SIM-004 (error) Path simulation failed

DESCRIPTION

Path validation is performed by simulation of the selected path segment in transistor-level simulator and then comparing delay and transition time with PrimeTime path object. The simulation failed.

WHAT NEXT

Investigate messages in the path log directory (indicated by message "The generated spice deck is ..."). Make sure that the simulation directory is kept after simulation terminates by setting **sim_setup_simulator -preserve failed** or **sim_setup_simulator -preserve all**.

SEE ALSO

sim_setup_simulator (2), **sim_setup_library** (2), **sim_get_recalculated_timing_paths** (2), **sim_setup_distributed** (2), **sim_compare_paths** (2).

SIM-005 (error) Simulation failed because there are designs in

memory

DESCRIPTION

Validation of simulation setup and predriver characterization create their own
design based on a library cell that you want to simulate.

WHAT NEXT

Either remove all designs by **remove_design -all** and rerun this command or in case of
setup validation you can validate an existing timing path by **sim_validate_path**.

SEE ALSO

sim_setup_simulator (2), **sim_validate_path** (2), **remove_design** (2).

SIM-006 (error) Validation of simulation setup does not support sequential cells

DESCRIPTION

Validation of simulation setup supports only combinational cells.

WHAT NEXT

Use an arc of a combinational cell in **sim_validate_setup**.

SEE ALSO

sim_validate_path (2).

SIM-007 (information) Using default %s of %g library units

DESCRIPTION

Validation of simulation setup determines default load capacitance and input
transition from library data as follows: For CCS libraries middle indices of
output_current table of the first library arc selected by fBsim_validate_setup are
used. For NLD libraries default capacitance is 10 times pin capacitance of the from
pin of the first library arc selected by fBsim_validate_setup. Transistion time is
100ps.

WHAT NEXT

To use a specific value use **sim_validate_setup -transition_time <slew_value> - capacitance <cap_value>**.

SEE ALSO

sim_validate_setup (2).

SIM-008 (information) Simulator executable %s does not exit or is incorrect

DESCRIPTION

Simulator executable has to exist, be a regular file, readable and executable.

WHAT NEXT

Make sure that you can execute simulator standalone (paste the above path to your current shell). Correct the path or adjust file access permissions.

SEE ALSO

sim_setup_simulator (2).

SLG-201 (error) A library may be in only one scaling library group.

DESCRIPTION

The **define_scaling_lib_groups** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the **link_design** commands occur (either explicitly or implicitly).

If a user tries to use a library in more than one group, the SLG-201 error message will occur.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed and the SLG-202 error message is issued.

WHAT NEXT

Be sure that the set of arcs and pins is identical across the members of the scaling library groups. The positions of the arcs and pins within the libraries must be the same as well.

The output-capacitance indices used for Composite Current-Source (CCS) driver data must have identical values across the libraries as well. This is not a requirement for CCS timing receiver models or constraints. If this is not satisfied, the SLG-203 warning message will be issued.

SEE ALSO

define_scaling_lib_group (2), **SLG-201** (n), **SLG-202** (n), **SLG-203** (n). **SLG-205** (n).

SLG-202 (Error) Completion of scaling library groups failed %s.

DESCRIPTION

The **define_scaling_lib_groups** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued

after the design is read.

If a user tries to use a library in more than one group, the SLG-201 error message will occur.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed and the SLG-202 error message is issued.

WHAT NEXT

Be sure that the set of arcs and pins is present across the members of the scaling library groups. This message is issued when some of the arcs or cells are missing across the members of the scaling library groups.

The total number of output-capacitance indices for which the Composite Current-Source (CCS) driver data is present must be the same across the libraries as well; This message is issued if the number of output-capacitance indices are different across the members of a scaling group.

The output-capacitance indices used for Composite Current-Source (CCS) driver data must have identical values across the libraries as well. This is not a requirement for CCS timing receiver models or constraints; if this is not satisfied, the SLG-203 warning message will be issued.

If you are using Base-curve Technology CCS Timing libraries, also verify if the base curve information in the libraries have been discretized and normalized in identical manner. i.e. check if curve_x has identical values across the scaling libraries in a library group.

SEE ALSO

define_scaling_lib_group (2), **SLG-201** (n), **SLG-202** (n), **SLG-203** (n).

SLG-203 (warning) The members of a scaling library group have significantly different
 output-capacitance indices; this can adversely affect scaling accuracy.

DESCRIPTION

The **define_scaling_lib_groups** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the **read_db** and **link_design** commands occur (either explicitly or implicitly).

If a user tries to use a library in more than one group, the SLG-201 error message will occur.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed and the SLG-202 error message is issued.

WHAT NEXT

Be sure that the set of arcs and pins is identical across the members of the scaling library groups. The positions of the arcs and pins within the libraries must be the same as well.

The output-capacitance indices used for Base-curve Technology Current-Source (CCS) driver data must have identical values across the libraries as well. This is not a requirement for CCS timing receiver models or constraints. If this is not satisfied, the SLG-203 warning message will be issued.

SEE ALSO

define_scaling_lib_group (2), **SLG-201** (n), **SLG-202** (n), **SLG-203** (n).

SLG-204 (Warning) Some of the timing arcs cannot be uniquely determined across the scaling libraries, it is assumed that the timing arcs are defined in the same order across all the libraries.

DESCRIPTION

The **define_scaling_lib_groups** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is linked.

If a user tries to use a library in more than one group, the SLG-201 error message will occur.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if the timing arcs cannot be associated across the scaling libraries because the timing arcs cannot be identified uniquely within a library, the SLG-204 warning message is issued. Since the timing arcs cannot be uniquely identified, the arcs are assumed to be in the same order across the libraries in a library group.

Note that this is only an informational warning, the scaling relationship for the scaling library group will still be created.

WHAT NEXT

Be sure that the set of arcs that cannot be uniquely identified are present in the same order across the members of the scaling library groups.

SEE ALSO

define_scaling_lib_group (2), **SLG-201** (n), **SLG-202** (n), **SLG-203** (n).

SLG-205 (Warning) CCS Noise information is inconsistent for %s across the libraries in the scaling library group. Scaling for CCS Noise will not be supported.

DESCRIPTION

The **define_scaling_lib_groups** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

If a user tries to use a library in more than one group, the SLG-201 error message will occur.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed and SLG-202 error message is issued. If the association fails only due to missing or inconsistent CCS Noise data across the libraries, the SLG-205 warning message is issued.

WHAT NEXT

Be sure that the CCS Noise data for the set of arcs and pins is present across the members of the scaling library groups. This message is issued when some of the arcs or pins have i) missing CCS Noise model information across the members of the scaling library groups (or) ii) CCS Noise model information with the input voltage and output voltage indices not in the same percent vdd in all libraries of a scaling group (or) iii) having inconsistent or missing conditions for CCS Noise models across the members of a scaling library group (or) iv) having inconsistent ordering of conditional CCS Noise models across the members of a scaling library group.

SEE ALSO

define_scaling_lib_group (2), **SLG-200** (n), **SLG-201** (n), **SLG-202** (n), **SLG-203** (n).

SLG-206 (Warning) Completion of scaling library group failed for power analysis: %s.

DESCRIPTION

The **define_scaling_lib_group** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

After design linking occurs, the remaining libraries in scaling library group will be loaded to "complete" the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If this association fails for associating power arcs across the libraries, the SLG-206 warning message will be issued and the scaling will not be enabled for power analysis.

Note that this warning is for power anlaysis, the scaling relationship for the scaling library group will still be created. The scaling for timing analysis will not be affected. Message SLG-202 will be issued when some of the timing arcs or cells are missing across the members of the scaling library group.

WHAT NEXT

Be sure that the set of power arcs is present across the members of the scaling library group. This message is issued when some of the power arcs are missing across the members of the scaling library group.

SEE ALSO

define_scaling_lib_group (2), **SLG-202** (n).

SLG-207 (Warning) Some of the power arcs cannot be uniquely determined across the scaling libraries, it is assumed that the power arcs are defined in the same order across all the libraries.

DESCRIPTION

The **define_scaling_lib_group** command can be used to specify a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is linked.

After design linking occurs, the remaining libraries in scaling library group will be loaded to "complete" the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If the power arcs cannot be associated across the scaling libraries because the power arcs cannot be

identified uniquely within a library, the SLG-207 warning message is issued. Since
the power arcs cannot be uniquely identified, the arcs are assumed to be in the same
order across the libraries in a library group.

Note that this is only an informational warning, the scaling relationship for the
scaling library group will still be created.

WHAT NEXT

Be sure that the set of arcs that cannot be uniquely identified are present in the
same order across the members of the scaling library group.

SEE ALSO

define_scaling_lib_group (2), **SLG-204** (n), **SLG-206** (n).

SLG-208 (Error) The command define_scaling_lib_group needs to be defined before the command set_variation_library.

DESCRIPTION

The **define_scaling_lib_group** command must be issued before the command
set_variation_library.

WHAT NEXT

Define the **define_scaling_lib_group** before applying the command
set_variation_library.

SEE ALSO

define_scaling_lib_group (2), **set_variation_library** (2), **SLG-200** (n), **SLG-201** (n),
SLG-202 (n), **SLG-203** (n).

SLG-209 (Error) Invalid set of libraries passed to define_scaling_lib_group.

DESCRIPTION

A valid set of libraries should be passed to **define_scaling_lib_group**. Check the characterization operating conditions of the libraries in the group.

For example, If you want to use operating conditions between 0.8 and 0.9V and temperatures between -40 and 125 degrees, libraries characterized at all the four voltage/temperature combinations should be specified.

```
pt_shell> define_scaling_lib_group {
  lib_max_125_0.8V_cccs.db
          lib_max_125_0.9V_cccs.db
          lib_max_-40_0.8V_cccs_v2.db
          lib_max_-40_0.9V_cccs_v2.db }
```

If any of the four libraries are missing, the scaling library group would be rejected. When specifying multiple temperatures and/or voltages, all libraries on the resulting voltage/temperature grid must be provided.

WHAT NEXT

Check the characterization operating conditions of the libraries provided to **define_scaling_lib_group** and ensure that the grid is fully populated.

SEE ALSO

define_scaling_lib_group (2), **report_lib** (2).

SLG-210 (warning) More than one scaling library is in the link_path, which may introduce significant performance degradation.

DESCRIPTION

At most one library in each scaling library group should be in the link_path. If there exists more than one scaling library in the link_path, PrimeTime has to reload some libraries, which may introduce significant performance degradation.

WHAT NEXT

Remove some scaling libraries from the link_path such that only one scaling library in each library group is in the link_path.

SEE ALSO

define_scaling_lib_group (2).

SPFP-001 (error) Cannot open file '%s'.

DESCRIPTION

```
The named parasitics file cannot be opened.
```

WHAT NEXT

```
Validate that the file name is correct.
```

SPFP-002 (error) Could not determine the format of parasitics file:
 '%s'

DESCRIPTION

```
The named parasitics file was opened, but the format of the file (DSPF, RSPF, SPEF)
could not be determined.
```

WHAT NEXT

```
Validate that the file is a properly formatted parasitics file in one of the
supported formats.
```

SPFP-010 (error) %s syntax error: %s
 at line %d near '%s' in file '%s'

DESCRIPTION

```
A syntax error was found while reading the indicated type of parasitics file. A
nearby line is given to help you isolate the problem.
```

WHAT NEXT

```
This message covers a wide variety of syntax errors. Review the line number reported
in the message and determine if the writer of the parasitics file has introduced a
syntax error.
```

SPFP-011 (error) Unknown %s construct '%s'
 at line %d in file '%s'

DESCRIPTION

An unexpected or unknown construct was found while reading a parasitics file of the indicated format, This will often be followed by a general syntax error, **PARA-010**.

WHAT NEXT

Review the line number reported in the message and determine if the writer of the parasitics file has introduced an unknown construct.

SPFP-012 (warning) Missing '*|GROUND_NET' statement in SPF file '%s'
 Using 'vss', 'VSS', 'gnd' and 'GND'

DESCRIPTION

The GROUND_NET statement is missing from the named DSPF or RSPF file.

WHAT NEXT

This is just a warning to indicate that default values will be used.

SPFP-013 (warning) name DELIMITER and hierarchy DIVIDER are the same!
 Some objects may not be found, and performance may be affected.

DESCRIPTION

The hierarchy divider and pin delimiter in the named parasitics (SPEF, DSPF, RSPF) file are the same. This may not be completely supported. Some net or pin objects may not be found, and performance may be adversely affected.

WHAT NEXT

Modify your use of the application which generated the parasitics file and

regenerate it using different (or default) DELIMITER and DIVIDER. Synopsys strongly
recommends that for the best performance, you should use different characters for
the hierarchy delimiter and name delimiter.

SPFP-014 (warning) %s value %g exceeds user-defined threshold
 at line %d in file '%s'.

DESCRIPTION

You receive this message if the parasitics file contains a capacitance value (in
picofarads) or a resistance value (in ohms) that exceeds user-defined thresholds, as
specified by the **parasitics_cap_warning_threshold** and
parasitics_res_warning_threshold variables. This warning is intended to assist you
in detecting large, unexpected values generated by other applications. The specified
value is still used by the application.

WHAT NEXT

This is a warning message only; no action on your part is required. However, you can
change the thresholds by setting the **parasitics_cap_warning_threshold** and
parasitics_res_warning_threshold variables to different values, or to 0.0 (the
default) to suppress the generation of this message. For more information, see the
manual pages of these variables.

SEE ALSO

parasitics_cap_warning_threshold (3), **parasitics_res_warning_threshold** (3).

SPFP-100 (error) Expected %skeyword %s but found '%s'
 at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error where a specific
keyword was expected (for example, *D_NET), but something else was found. The file
name and line number are given so you can isolate the problem.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-101 (error) Invalid %s '%s'%s
at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in a number
of different constructs. The message will indicate the type of construct and what
part of it is invalid. Some examples include:
• You specified a DIVIDER, DELIMITER, or BUS_DELIMITER which is outside of the
allowed set of values for the construct

• Any of the header unit constructs has an invalid number or multiplier string.

• A port or D_NET connectivity entry has an invalid direction.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-102 (error) NAME_MAP syntax error at '%s'
at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in an entry
in the NAME_MAP section of the file.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-103 (error) %s requires %d or more %s's

at line %d in file '%s'.

DESCRIPTION

Many sections of the SPEF file require one or more sub sections of a specific type.
You receive this message if the SPEF file violates that semantic. Some examples
include:
• The *CAP section of a D_NET, if specified, requires one or more capacitor
elements.

• The *RES section of a D_NET, if specified, requires one or more resistor elements.

• The connectivity section of a D_NET requires one or more *P or *I sub sections.

• The *POWER_NETS and *GROUND_NETS sections, if specified, require one or more net
names.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-104 (error) %s requires %s
 at line %d in file '%s'.

DESCRIPTION

Some sections of the SPEF file require a specific sequence of sub sections. You
receive this message if the SPEF file violates that semantic. Generally, this
message is reserved for some rarely used sections of the file, like *DEFINE.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-105 (error) Invalid node name '%s'

at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in a node name, which is used in several places in the *RES and *CAP sections. The specific node name which is in error is shown in the message. A node name is either a port name, an instance pin name (an instance name or name map id, followed by the pin delimiter, followed by a pin name or name map id), or an internal node name (a net name, followed by the pin delimiter, followed by a positive integer).
The SPEF specification details the various possible forms for a node name.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-106 (error) Strict SPEF syntax error: invalid %s %s
 at line %d in file '%s'.

DESCRIPTION

Historically, there are a number of SPEF writers which write illegal SPEF. For backward compatibility with existing questionable SPEF files, the parser allows a number of forms which are strictly illegal. If the parser is in *strict* mode, you will receive this error when one of these strict-SPEF rules is violated.

WHAT NEXT

The first thing to try is to turn off strict mode. Or, you can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-107 (error) Expected %s but found '%s'
 at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a construct in the wrong place or out of order. Some examples include:

- The *D_NET section expects a certain series of optional sub sections. A SPEF keyword which is not a valid *D_NET sub section was found where a *D_NET sub section was expected.

- The *S connectivity attribute has some optional thresholds which must be positive fractions (between 0 and 1). The value found is not a positive fraction.

- Several sections of the SPEF file require a positive integer, and that was not found.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-108 (error) Invalid value '%s' at line %d in file '%s'.

DESCRIPTION

Many sections of the SPEF file use values, or triplets of values. You receive this message if the SPEF file has a syntax error in a value. Values are used in the *L and *S connectivity attributes, total capacitance of a D_NET or R_NET, capacitances, resistances, poles and residues, and so on.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-109 (error) Syntax error in complex number: '%s %s%s%s%s%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error in a complex number. Complex numbers are used in the specification of poles and residues. They can be specified as (r i), or as a triplet such as (r i):(r2 i2):(r3 i3). The message will

indicate the specific problem number.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-110 (error) Syntax error near '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax error not covered by any of
the other syntax error messages. The token in question, as well as the file name and
line number, will be given in the message.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-111 (error) Undefined name map index *%d referenced at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file finds a syntactically correct name map
reference, such as *2379, but no such entry was ever defined in the NAME_MAP
section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-112 (error) Non-terminated comment starting at line %d

of '%s'

DESCRIPTION

You receive this message if the SPEF file contains a multi-line comment, which begins with /*, but does not end. This message is intended to help you find the line where the non-terminated comment starts.

WHAT NEXT

You can try to correct this error manually by terminating or removing the comment. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-113 (error) Premature end-of-file reading '%s'.

DESCRIPTION

You receive this message if the SPEF file ends unexpectedly, for example, in the middle of parsing required header sections, or before any D_NET or R_NET sections were found. A missing double quote in the header section can cause this error.

WHAT NEXT

You might be able to correct this error manually if this is caused by missing header sub-sections, or by a missing closing quote in one of the header sub sections. But, generally, it will be difficult to isolate the problem in a large file.

SPFP-114 (information) Ignored unsupported %s section starting at line %d
 of '%s'

DESCRIPTION

You receive this informational message if the SPEF file contains a construct which is being ignored, such as D_PNET and R_PNET.

WHAT NEXT

No action is necessary.

SPFP-115 (error) BUS_DELIMITER cannot be the same as %s at line %d in '%s'.

DESCRIPTION

You receive this message if the BUS_DELIMITER is found to be the same as either the DIVIDER or the DELIMITER. SPEF does not allow this combination.

WHAT NEXT

The SPEF file will almost certainly need to be regenerated.

SPFP-116 (error) Semantic error near '%s': %s at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file reader has found a semantic error. The token in question, the specific problem, and the file name and line number will be given in the message.

WHAT NEXT

You can try to correct the error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the problem corrected.

SPFP-117 (error) SENSITIVITY syntax error at '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has a syntax or semantic error in an entry in the SENSITIVITY section of the file.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-118 (error) Sensitivity factor syntax error at '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid value for a sensitivity factor. A sensitivity factor is supposed to be a floating point number.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-119 (error) Invalid parameter ID '%d' value in sensitivity at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid value for a variation parameter ID in the sensitivity section. The variation parameters are defined in the *VARIATION_PARAMETERS section and are supposed to be within the values defined in this section. This error indicates that the current parameter ID is outside the valid range.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-120 (error) Invalid parameter types for process parameter '%s' at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has an invalid type of process variation parameter. The variation parameters are defined in the *VARIATION_PARAMETERS section and allowed values are 'D', 'N' or 'X' type of process variation parameters. This indication implies whether the parameter affects capacitance, resistance and inductance in numerator (for 'N'), denominator (for 'D') or does not affect resistance (for 'X').

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-121 (error) Syntax error at line %d in file '%s'. Cannot define process variations after temperature variations.

DESCRIPTION

You receive this message if the SPEF file has temperature variations followed by process variations. It is expected that the file contains process variation parameters followed by temperature variations. The variation parameters are defined in the *VARIATION_PARAMETERS section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-122 (warning) Invalid sensitivity for capacitance at line %d in file '%s'.

DESCRIPTION

You receive this message if the SPEF file has sensitivities for ground or coupling capacitances with respect to temperature variations or 'N' parameters to inform you that these sensitivities are illegal.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-123 (error) Syntax error at line %d in file '%s'. Expected

to see keyword CRT2.

DESCRIPTION

You receive this message if the SPEF file has syntax errors in the definition of
temperature variations. The variation parameters are defined in the
*VARIATION_PARAMETERS section.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-124 (error) Illegal name map index *%d referenced at line '%d' in file '%s'.

DESCRIPTION

You receive this message if the SPEF file finds a syntactically illegal name map
reference, such as *-1. Such lines will be ignored.

WHAT NEXT

You can try to correct the syntax error manually. However, since SPEF files are
usually machine generated and extremely large, you will most likely need to work
with the vendor of the application which wrote the file to get the syntax corrected.

SPICE-001 (error) The aggressor cell driver pin '%s' is not connected.

DESCRIPTION

The **write_spice_deck** command has found that the specified aggressor cell driver pin is not connected in the netlist.

WHAT NEXT

Examine the netlist file, and determine if this is the case. Send the test case to Synopsys to debug this problem.

SEE ALSO

write_spice_deck (2).

SPICE-002 (error) The aggressor cell clock pin '%s' is not connected.

DESCRIPTION

The **write_spice_deck** command has found that the specified aggressor cell clock pin is not connected in the netlist.

WHAT NEXT

Examine the netlist file, and determine if this is the case. Send the test case to Synopsys to debug this problem.

SEE ALSO

write_spice_deck (2).

SPICE-003 (warning) Unable to find the clock for pin '%s'.

DESCRIPTION

The **write_spice_deck** command cannot find the clock information related to the clock pin.

WHAT NEXT

Examine the netlist file, and determine whether the specified pin is connected. Check the script to determine whether clocks are defined for the design. Check the design to determine whether it is properly constrained. When this warning is issued, a default clock period of 10 is assumed.

SEE ALSO

write_spice_deck (2).

SPICE-004 (error) A conflict occurred in setting voltage level of pin '%s'. It is set to logic '%s'.

DESCRIPTION

The **write_spice_deck** command has tried to set the voltage level of the specified pin, whose level has been previously set.

WHAT NEXT

Examine the netlist file, and determine that the voltage source is correct for the timing path generated. Change it if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-005 (warning) Unable to find the arrival window for pin '%s'.

DESCRIPTION

The **write_spice_deck** command is not able to find the arrival window to write the

correct piecewise linear waveform (PWL) for the pin.

WHAT NEXT

Examine the netlist file, and verify that there is a timing path through the pin. If
this is the case, send the test case to Synopsys for debugging.

SEE ALSO

write_spice_deck (2).

SPICE-006 (warning) Forced initialization of the output of the cell '%s'
 might be necessary because the timing path's data input pin '%s' is
 connected to timing path nets '%s'.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is connected to a net
in the timing path so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to add the initialization option in the spice deck that is generated
to ensure the correctness of the timing path's initial state.

SEE ALSO

write_spice_deck (2).

SPICE-007 (warning) Forced initialization of the output of the cell
 '%s' might be necessary because the timing path's data input pin '%s'

is connected to a feedback net '%s' driven by the same cell.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is connected to a net driven by the same cell so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to add the initialization option in spice deck that is generated to ensure the correctness of the timing path's initial state.

SEE ALSO

write_spice_deck (2).

SPICE-008 (warning) The timing path data input pin '%s' is driven
 by a %s clock net '%s'.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is driven by a timing path clock net so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to increase all PWLs by a few clock periods.

SEE ALSO

write_spice_deck (2).

SPICE-009 (warning) The timing path data input pin '%s' is driven

by a %s clock cell '%s'.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is driven by a timing path clock cell so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to increase all PWLs by a few clock periods.

SEE ALSO

write_spice_deck (2).

SPICE-010 (warning) The timing path data pin '%s' is connected to an aggressor '%s'. Please check the PWL and voltage source of the aggressor's driver.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is driven by an aggressor so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to inspect the aggressor's driver PWL and voltage source or increase all PWLs for a few clock periods.

SEE ALSO

write_spice_deck (2).

SPICE-011 (warning) The timing path data pin '%s' is connected to an aggressor cell '%s'. Please check the PWL and voltage

source of
 the aggressor's driver.

DESCRIPTION

The **write_spice_deck** command has found that the data input pin is driven by an
aggressor cell so no piecewise linear waveform (PWL) is generated for this pin.

WHAT NEXT

You might have to inspect the aggressor's driver PWL and voltage source or increase
all PWLs for a few clock periods.

SEE ALSO

write_spice_deck (2).

SPICE-012 (error) The timing path sequential data input pin '%s' is
 not connected.

DESCRIPTION

The **write_spice_deck** command has found that the timing path sequential data input
pin is not connected in the netlist.

WHAT NEXT

Examine the netlist file and determine if this is the case. You might have to
inspect or generate it's piecewise linear waveform (PWL) or voltage source. If
timing path sequential data input pin is is connected, send the test case to
Synopsys to debug this problem.

SEE ALSO

write_spice_deck (2).

SPICE-013 (warning) A conflict occurred in setting the switching

direction of pin '%s'. It is set to '%s'.

DESCRIPTION

The **write_spice_deck** command has tried to set the switching direction of the
specified pin on which the direction was previously set. It usually indicates that
the aggressor is coupled with at least two nets in the timing path that are
switching in the opposite directions. There are conflicting requirements of the
switching direction (sense) of the aggressor input pin. In this case,
write_spice_deck choose the rising direction.

WHAT NEXT

Examine the netlist file, and verify that the switching is correct for the timing
path generated. Change the switching direction if it is better for the delay
analysis of the path.

SEE ALSO

write_spice_deck (2).

SPICE-014 (warning) The timing path cell side pin '%s' is driven by
 an aggressor '%s' that is set to %s.

DESCRIPTION

The **write_spice_deck** command has found that the side pin of a timing path cell is
driven by the specified aggressor.

WHAT NEXT

Examine the netlist file, and verify the connection and switching direction of the
aggressor. Change them if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-015 (warning) A conflict occurred in setting the voltage level

of the aggressor '%s'. It is set to '%s'.

DESCRIPTION

The **write_spice_deck** command has tried to set the voltage level of the specified
aggressor on which the voltage level was previously set.

WHAT NEXT

Examine the netlist file, and verify that the voltage level is correct for the
timing path generated. Change it if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-016 (information) The aggressor-driven latch '%s' is in transparent mode. The data pin is '%s'.

DESCRIPTION

The **write_spice_deck** command has found that the specified aggressor-driven latch in
the spice deck is in transparent mode.

WHAT NEXT

This is an informational message only. No action is required on your part. However,
you can examine the netlist file and verify that the piecewise linear waveform (PWL)
and voltage sources of the date pin and gate pin are correct for the timing path
generated. Change them if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-017 (information) The side pin '%s' is set to '%s'.

DESCRIPTION

The **write_spice_deck** command has set the specified side pin to the specified logic
level.

WHAT NEXT

This is an informational message only. No action is required on your part. However,
you can examine the netlist file and verify that the voltage source of the side pin
is correct for the timing path generated. Change it if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-018 (information) The cell '%s' could not be sensitized due to conflicting derived logic on pin(s) %s.

DESCRIPTION

The **write_spice_deck** command has found that cell could not be sensitized. The
specified side pins are not controllable and is driven by conflicting edge due to
tie-off or upstream logic. **write_spice_deck** attempts to duplicate this cell to
resolve this conflict.

WHAT NEXT

You can examine the netlist file and verify that the logic connected to side pins
will allow the signal to propagate through the cell. Disconnect and change the
voltage on conflicting side pins if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-019 (information) The setting of aggressor '%s' is changed
 from '%s' to '%s'.

DESCRIPTION

The **write_spice_deck** command has found that the aggressor logic needs to be changed
as specified to satisfy the sensitization of a side pin.

WHAT NEXT

This is an informational message only. No action is required on your part. However,

you can examine the netlist file and verify that the voltage of the aggressor has the correct effect on the side pin for the timing path generated. Change it if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-020 (information) The spice deck that is generated has PWLs
 for you to verify.

DESCRIPTION

The **write_spice_deck** command has generated piecewise linear waveforms (PWLs) to stimulate the timing path.

WHAT NEXT

This is an informational message only. No action is required on your part. However, you can examine the netlist file and verify the correctness of the PWLs for the timing path generated. Change them if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-021 (warning) Unable to propagate the side pin value '%s'
 backward through the aggressor arc %s -> %s
 due to a side pins sensitization problem.

DESCRIPTION

The **write_spice_deck** command is unable to sensitize the specified aggressor cell arc to generate the specified logic value.

WHAT NEXT

Examine the spice deck generated, and manually sensitize the arc to the specified

logic value.

SEE ALSO

write_spice_deck (2).

SPICE-022 (error) Unable to trace the clock tree from pin '%s' of cell '%s'.

DESCRIPTION

The **write_spice_deck** command is unable to trace the clock tree path from the specified pin due to a missing clock tree in PrimeTime's internal data structure.

WHAT NEXT

Examine the spice deck generated, and determine if the error will affect the spice run. Change the spice deck manually if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-023 (warning) A subckt declaration has no name in the file specified by the -sub_circuit_file option.

DESCRIPTION

The **write_spice_deck** command used with the **-sub_circuit_file** option has found a subcircuit declaration without a name in the SPICE pin order file.

WHAT NEXT

Examine the spice pin order file, and remove the subcircuit declaration. Correct the file if necessary.

SEE ALSO

write_spice_deck (2).

SPICE-024 (warning) The subckt '%s' declaration occurs without
 a pin in the file specified by the -sub_circuit_file option.

DESCRIPTION

The **write_spice_deck** command used with the **-sub_circuit_file** option has found a subcircuit declaration without a pin in the SPICE pin order file.

WHAT NEXT

Examine the spice pin order file, and remove the subcircuit declaration or add a subcircuit pin definition.

SEE ALSO

write_spice_deck (2).

SPICE-025 (warning) Unable to find the delay of port '%s'.

DESCRIPTION

The **write_spice_deck** command cannot find the delay of the specified input port.

WHAT NEXT

Use the **set_input_delay** command to define the delay for the port.

SEE ALSO

set_input_delay (2), **write_spice_deck** (2).

SPICE-026 (warning) Negative start time '%g' for PWL is generated.
 The initial_delay, %s delay and slew time are %g, %g and %g,

respectively.

DESCRIPTION

The **write_spice_deck** command generated a negative start time for a PWL.

WHAT NEXT

Use the **-initial_delay** option to define a larger initial delay to make the start time non-negative.

SEE ALSO

write_spice_deck (2).

SPICE-027 (warning) SPICE deck generation for non-delay timing arc (%s -> %s) is not supported.

DESCRIPTION

The **write_spice_deck** command can't generate the deck for non-delay arc.

WHAT NEXT

Check the arc specification for the get_timing_arcs is correct or not.

SEE ALSO

write_spice_deck (2).

SPICE-028 (error) -analysis_type cannot be specified for timing path.

DESCRIPTION

The option -analysis_type of **write_spice_deck** command is applicable only for crosstalk delay and noise analysis on a timing arc.

WHAT NEXT

Don't use this option when writing the spice deck for the timing path.

SEE ALSO

write_spice_deck (2).

SPICE-029 (information) -analysis_type is not set for timing arc. max_rise assumed.

DESCRIPTION

The **write_spice_deck** command didn't find the option -analysis_type for timing arc.

WHAT NEXT

Specify the option when writing the spice deck of a timing arc.

SEE ALSO

write_spice_deck (2).

SPICE-030 (error) Unable to find clock for the pin '%s' of the driving cell of the port '%s'.

DESCRIPTION

The **write_spice_deck** can't find the clock to the sequential driving cell of a port.

WHAT NEXT

Specify a valid clock or replace it with a combinatorial driving cell in the set_driving_cell command.

SEE ALSO

write_spice_deck (2). **set_driving_cell** (2).

SPICE-031 (error) Erroneous %s arrival window (min %g max %g)
 of the pin '%s'.

DESCRIPTION

The **write_spice_deck** found problem with the arrival window of the pin

WHAT NEXT

Check for related messages from update_timing about delay calculation and try to remove them.

SEE ALSO

write_spice_deck (2).

SPICE-032 (warning) Unable to find library cell '%s'.

DESCRIPTION

The **write_spice_deck** can't find the library cell in the library specified in the set_driving_cell command or the libraries used by the current design.

WHAT NEXT

Check the library name and library cell name of the set_driving_cell command.

SEE ALSO

write_spice_deck (2). **set_driving_cell** (2).

SPICE-033 (error) The cell arc in '%s' and the %s is not in one stage.

DESCRIPTION

The **write_spice_deck** find that the cell arc and the net arc specified don't for a single stage.

WHAT NEXT

Specified the correct cell arc that drives the net arc with this option.

SEE ALSO

write_spice_deck (2).

SPICE-034 (information) There are %d simulation sweeps from %d sweep points for %d active aggressors.

DESCRIPTION

The **write_spice_deck** generated the number of SPICE sweep described above.

WHAT NEXT

The SPICE run time may be large if the sweep is large.

SEE ALSO

write_spice_deck (2).

SPICE-035 (information) The plateau time (%g) of the clock pin '%s' is %s to %g%% of the period (%g) due to the skew of rise and fall delay.

DESCRIPTION

The **write_spice_deck** find that the delay skew between different edges of the clock pin might cause clock waveform problem.

WHAT NEXT

Examinate the clock network.

SEE ALSO

write_spice_deck (2).

SPICE-036 (error) The clock period on pin '%s' is too small for the rise and fall transitions to happen.

DESCRIPTION

The **write_spice_deck** found that the transition times of the clock pin are too large that the clock pulse will not reach logic one or logic zero state.

For example: The rise and fall slews are 0.1ns with 30-70 trip points and clock period is 0.3ns. When the slew values are converted to 0-100 points, the clock period is not large enough to hold the rising and falling edges completely inside the period.

WHAT NEXT

Increase the clock period or speed up the transition times of the pin.

SEE ALSO

write_spice_deck (2).

SPICE-037 (error) Can't specify both '%s' and '%s' options.

DESCRIPTION

The **write_spice_deck** find the two incompatible options.

WHAT NEXT

Specified the correct the options.

SEE ALSO

write_spice_deck (2).

SPICE-038 (warning) Can't align the aggressor '%s' (input pin '%s'.)

DESCRIPTION

The **write_spice_deck** wasn't able to align the aggressor.

WHAT NEXT

```
Sweep the input pin to find the worst case aggressor switching time.
```

SEE ALSO

write_spice_deck (2).

SPICE-039 (Information) The aggressor alignment for pin '%s' may not
 be the worst case because '%s'.

DESCRIPTION

```
The write_spice_deck wasn't able to align the aggressors of the victim net for its
worst case. Sweeping the aggresssors over a small window might be needed.
```

WHAT NEXT

```
Make sure you are using the above mentioned feature on this pin. If you cannot,
please use sweep option of write_spice_deck or manually sweep the generated spice
deck for input pins of all aggressors to find the wost case alignment.
```

SEE ALSO

write_spice_deck (2).

SPICE-040 (Error) The non-positive value (%g) specified by the option '%s'.

DESCRIPTION

```
The option value of the write_spice_deck must be a positive floating point number.
```

WHAT NEXT

```
Set a positive floating point number.
```

SEE ALSO

write_spice_deck (2).

SPICE-041 (information) The option '%s' is ignored for the %s.

DESCRIPTION

The option of the **write_spice_deck** is ignore. number.

WHAT NEXT

Remove the option from the write_spice_deck command.

SEE ALSO

write_spice_deck (2).

SPICE-042 (Error) Unable to write spice deck for the %s '%s' without appropiate annotated RC parasitic.

DESCRIPTION

The **write_spice_deck** cannot write out the spice deck. This may be because there is no annotated RC or no coupling in the noise analysis.

WHAT NEXT

Use another cell or net arc with the appropiate RC parasitics.

SEE ALSO

write_spice_deck (2).

SPICE-043 (Error) Unable to find the %s %s library pin '%s' of the set_driving_cell '%s' in the library '%s'.

DESCRIPTION

The **write_spice_deck** can't found the library pin specified in the set_driving_cell command.

WHAT NEXT

Specify the correct pin name on the set_driving_cell command.

SEE ALSO

write_spice_deck (2).

SPICE-044 (Error) Unable to find the library '%s' for the set_driving_cell '%s'.

DESCRIPTION

The **write_spice_deck** can't found the library specified in the set_driving_cell command.

WHAT NEXT

Specify the correct library name on the set_driving_cell command.

SEE ALSO

write_spice_deck (2).

SPICE-045 (Error) Unable to find any cell arc.

DESCRIPTION

You used a net timing_arc object to **write_spice_deck** which had no proper driver cell. The **write_spice_deck** cannot be performed on a stage that has no driver cell arc.

WHAT NEXT

Either use the correct net timing_arc object to **write_spice_deck**, or enable at least one of the cell timing arcs that drives the net.

SEE ALSO

write_spice_deck (2).

SPICE-046 (Error) Sequential driving cell '%s' of the clock port '%s' is not supported.

DESCRIPTION

You used a sequential library cell to drive a clock port. The **write_spice_deck** cannot write out correct voltage sources to generate the clock pulse required.

WHAT NEXT

Please use combinatorial library cells to drive clock port.

SEE ALSO

write_spice_deck (2).

SPICE-047 (Error) Unable to find the clock for clock pin '%s'.

DESCRIPTION

The **write_spice_deck** cannot find the (generated) clock for the clock pin. It can't write out the SPICE pulse statement related to the clock pin.

WHAT NEXT

Please properly define the clock related to the clock pin in PrimeTime.

SEE ALSO

write_spice_deck (2).

SPICE-048 (Warning) Unsupport timing path type.

DESCRIPTION

The **write_spice_deck** doesn't support the path type generated by the get_timing_paths.

WHAT NEXT

Please generate only the full path.

SPICE-049 (Error) Spice deck cannot be written because %s

DESCRIPTION

The **write_spice_deck** command cannot write the spice deck for one of the following reasons. The spice deck needs input stimulus to be applied on an internal pin of cell, which is not possible with spice models.

WHAT NEXT

Reconsider the inputs given to spice deck or try to eliminate the possibility of having cells with internal pins in spice deck.

SEE ALSO

write_spice_deck (2). **set_si_delay_analysis** (2).

SPICE-101 (Error) Not event pin.

DESCRIPTION

The **set_user_sensitization** cannot find any library or design pin corresponding to the name in the -event_pins options.

WHAT NEXT

Please check and correct the names.

SEE ALSO

set_user_sensitization (2).

SPICE-102 (Error) Number of states (%d) is less than number of

event pins (%d).

DESCRIPTION

The **set_user_sensitization** cannot find the number of state is less that the number of event pins.

WHAT NEXT

Please check and correct the consistency between states and event pins.

SEE ALSO

set_user_sensitization (2).

SPICE-103 (Error) '%s' is not a node name for initial transient condition.

DESCRIPTION

The **set_user_sensitization** find the name doesn't correspond to a output pin of the cell. Nor it has the format of a internal node which starts with a '.'.

WHAT NEXT

Please check and correct the node name.

SEE ALSO

set_user_sensitization (2).

SPICE-104 (Error) '%s' is not a floating point number for initial transient condition.

DESCRIPTION

The **set_user_sensitization** can't convert the string to a floating point number.

WHAT NEXT

Please check and correct the string.

SEE ALSO

set_user_sensitization (2).

SPICE-105 (Error) '%s' is not a pin of the library cell '%s'.

DESCRIPTION

The **set_user_sensitization** can't the pin on the library cell.

WHAT NEXT

Please check and correct the pin name.

SEE ALSO

set_user_sensitization (2).

SPICE-106 (Error) Pin '%s' appears more than once.

DESCRIPTION

The **set_user_sensitization** find the pin appears in more than one option.

WHAT NEXT

Please check and remove pin name from some pin related options.

SEE ALSO

set_user_sensitization (2).

SPICE-107 (Error) Can't find arc from pin '%s' in the event pins

list.

DESCRIPTION

The **set_user_sensitization** Can't find the from pin of the arc in the -event_pins list.

WHAT NEXT

Please check and add from pin name to the list.

SEE ALSO

set_user_sensitization (2).

SPICE-108 (Error) Find arc from pin '%s' in the tie high/low pins list.

DESCRIPTION

The **set_user_sensitization** finds the from pin of the arc in the -tie_high or -tie_low pins lists.

WHAT NEXT

Please check and remove the from pin name from the lists.

SEE ALSO

set_user_sensitization (2).

SPICE-109 (Error) No state found.

DESCRIPTION

The **set_user_sensitization** can't find and state transition for -event_pins.

WHAT NEXT

Please add correct states to -event_states option.

`set_user_sensitization` (2).

SPICE-110 (Error) Number of states (%d) isn't a multiple of number of
 event pins (%d).

DESCRIPTION

The **set_user_sensitization** found inconsistency between the number of states and the number of event pins.

WHAT NEXT

Please add correct states to -event_states option.

SEE ALSO

`set_user_sensitization` (2).

SPICE-111 (Error) Rise state followed by a rise or low states for pin '%s'.

DESCRIPTION

The **set_user_sensitization** found inconsistency consecutive states of a pin.

WHAT NEXT

Please give the correct states for the pin.

SEE ALSO

`set_user_sensitization` (2).

SPICE-112 (Error) High state followed by a rise or low states for

pin '%s'.

DESCRIPTION

The **set_user_sensitization** found inconsistency consecutive states of a pin.

WHAT NEXT

Please give the correct states for the pin.

SEE ALSO

set_user_sensitization (2).

SPICE-113 (Error) Fall state followed by a fall or high states for pin '%s'.

DESCRIPTION

The **set_user_sensitization** found inconsistency consecutive states of a pin.

WHAT NEXT

Please give the correct states for the pin.

SEE ALSO

set_user_sensitization (2).

SPICE-114 (Error) Low state followed by a fall or high states for pin '%s'.

DESCRIPTION

The **set_user_sensitization** found inconsistency consecutive states of a pin.

WHAT NEXT

Please give the correct states for the pin.

SPICE-115 (Error) The final state (%c) of the arc input pin '%s' doesn't satisfy the analysis type (%s) and the arc sense (%s).

DESCRIPTION

The **set_user_sensitization** found the final state of the input pin can't sensitize the arc according to the analysis type and the arc sense.

WHAT NEXT

Please give the correct final state for the arc input pin.

SEE ALSO

`set_user_sensitization` (2).

SPICE-116 (Error) When condition (%s) of the arc is not satisfied.

DESCRIPTION

The **set_user_sensitization** found the when condition is not satisfied by the final state of the input pin and the tie high/low pins.

WHAT NEXT

Please give the correct final state for the arc input pin.

SEE ALSO

`set_user_sensitization` (2).

SPICE-117 (Error) Unknown state symbol (%s), low state

assumed.

DESCRIPTION

The **set_user_sensitization** doesn't recognize the symbol used to represent the event pin state. It uses low state.

WHAT NEXT

Please replace it with the correct state symbol.

SEE ALSO

set_user_sensitization (2).

SPICE-118 (Information) %d user sensitization %s.

DESCRIPTION

The **report_user_sensitization** or the **remove_user_sensitization** how may user sensitiation they processed.

WHAT NEXT

Nothing.

SEE ALSO

set_user_sensitization (2).

SPICE-119 (Error) Must specify output directory name when using -sample_size.

DESCRIPTION

The **write_spice_deck** command is used with **-sample_size** option but without the **-output** option. The **-output** option is mandatory when you use **-sample_size** option.

WHAT NEXT

Specify a directory name via -output option and re-issue the command.

`write_spice_deck` (2).

SPICE-120 (Error) Did not find variation information.

DESCRIPTION

The **write_spice_deck** command is used with **-sample_size** option but there is no variation information available on the design. The **-sample_size** option should only be used in the context of Primetime VX when there are device or interconnect variations or both.

WHAT NEXT

Re-issue without the **-sample_size** option or set variation information and re-issue the command.

SEE ALSO

`write_spice_deck` (2).

SPICE-122 (warning) The timing path has duplicate occurrences of cell '%s'.

DESCRIPTION

The timing path given to **write_spice_deck** has multiple references to the listed cell instance.

This typically occurs when a timing path launches from and is captured by the same sequential cell, sometimes called 'loopback' paths. In these cases, there is a conflict between trying to capture a preload value in the cell (acting as the path startpoint) and trying to capture the value (acting as the path endpoint). These paths cannot be simulated reliably.

WHAT NEXT

The sensitization will be chosen for one instance of the cell. This sensitization may not be correct for all instances of the cell, or may not appear in the sensitization list at all.

`write_spice_deck` (2).

SPICE-123 (information) Detailed parasitics of the net '%s' are ignored due to '%s'.

DESCRIPTION

Detailed parasitics and lumped resistances of the net are ignored due to user set **set_load -wire_load** on the port connecting the net, **set_load** on the net or **set_resistance** on the net. SPICE results does not match with PT calculations.

WHAT NEXT

Please avoid using lumped parasitics on the nets. These lumped parasitics does not have a equivalent representation at transistor level.

SEE ALSO

`write_spice_deck(2), set_load(2), set_resistance(2).`

SPICE-124 (warning) Resistance set due to set_resistance on net '%s' is ignored due to '%s'.

DESCRIPTION

set_load and **set_resistance** cannot be used together on a net. Use only one of them. Also, if the net has multiple fanouts then resistance due to **set_resistance** will be ignored.

WHAT NEXT

Use only **set_load** or **set_resistance** on the net, but not both. Also, please avoid using **set_resistance** on a net with multiple fanouts.

SEE ALSO

`write_spice_deck(2), set_load(2), set_resistance(2).`

SPICE-125 (warning) -c_effective_load of write_spice_deck command is ignored.

DESCRIPTION

The ceff load capacitances are not stored and hence the option -c_effective_load of **write_spice_deck** command is ignored.

WHAT NEXT

set the variable **rc_cache_min_max_rise_fall_ceff** to true in order to enable the caching of ceff load capacitances.

SEE ALSO

write_spice_deck (2).

SPICE-126 (warning) No spice equivalence for composite aggressor. Turn off the composite aggressor for %s analysis

DESCRIPTION

Coupled analysis is performed by turning on the composite aggressor feature. There is no spice equivalence for composite aggressor. Hence the spice deck does not represent how the analysis is performed in PTSI engine.

WHAT NEXT

If you are doing correlation, please turn off the composite aggressor and run **update_timing**, **write_spice_deck** to regenerate the spice deck.

SEE ALSO

write_spice_deck (2).

SPICE-127 (Warning) The cell '%s' could not be sensitized

correctly because %s.

DESCRIPTION

The sensitization used for the above indicated cell does not match the worst case scenario it was characterized. This is mainly due to missing information in the library. **Write_spice_deck** tries to handle these situations by sensitizing the cell to behave closer to the condition it was characterized. Please verify this sensitization.

WHAT NEXT

Populate the library with the missing information and run write_spice_deck for correlation purposes.

SEE ALSO

write_spice_deck (2),

SPICE-130 (information) The cell '%s' is duplicated due to conflict in sensitization.

DESCRIPTION

The sensitization involves the input pin(net) or the output pin(net) of the cell to switch in specific direction at specific time. And for some cells there is conflict due to multiple of these requirements. **write_spice_deck** handles it by duplicating the cell and sensitizing them according to the requirement.

Sensitization conflict can happen due to many reasons some of them are,

o Crosstalk stage shares a common cell between the victim and aggressors. The above cell needs to be rising for victim and falling for aggressor at specific time. This conflict is resolved by dupliating the common cell and sensitizating one as victim and another one as aggressor. This could also happen between two aggressors.

o Timing false path or reconverging timing path, sometimes the timing path may not sensitizable or the reconverging paths is faster or conflicting with timing path of interest.

WHAT NEXT

Generally this is conservative and safe.

SPICE-200 (Warning) There is no library waveform set for the %s pin(%s). The default waveform (type : %s) is used.

DESCRIPTION

write_spice_deck needs the shape of the waveform that is used for the characterization of the timing library. Previously it was assumed to be ramp. Most of the current library characterization waveforms are type of smooth waveform called Synopsys pre-driver waveform. So to consider that the default waveform is changes to Synopsys pre-driver.

set_library_driver_waveform is the command used to set the library characterization wavefrom per library. This command allows to set multiple type of wavforms per libraray and library cell. The most appropriate approach is to find the waveform shape used for the library and apply it when the library is read to PrimeTime. However, to get the pre-2007.06 behaviour of ramp waveform as default waveform, apply "set_library_driver_waveform -type ramp" before update_timing.

WHAT NEXT

Apply appropriate waveform shape using **set_library_driver_waveform**.

SEE ALSO

write_spice_deck(2), set_library_driver_waveform(2).

STAT

STAT-001 (error) Invalid attribute %s.

DESCRIPTION

An element in the attribute name list does not match one of the valid names.

WHAT NEXT

Correct the command so that all attribute names are valid. See the command man page for a list of the valid commands.

STAT-002 (error) The "all" attribute was found but was not alone.

DESCRIPTION

If the "all" attribute is used it must be the only attribute name in the list.

WHAT NEXT

Remove all attribute names except the "all" name.

STAT-003 (error) Size of value list does not match name list.

DESCRIPTION

If the *-values* option is used then the number of elements in the list must match the number of elements in the name list.

WHAT NEXT

Fix the values or names list so that the number of elements match.

STAT-004 (error) Unrecognized variation names are given.

DESCRIPTION

Reference variation name list is given with the *reference_value* option of the *set_variation_library* command. Any other settings cannot provide names outside of this list.

WHAT NEXT

Remove extraneous names from the variation name list.

STAT-005 (error) Found reference value and value list options.

DESCRIPTION

The reference value option precludes the use of the value list option. They cannot be used together.

WHAT NEXT

Remove either the reference value or the value list from the command.

STAT-006 (error) More than one non-reference value is given.

DESCRIPTION

Reference variation value list is given with the *reference_value* option of the *set_variation_library* command. Any other settings can provide only one non-reference value.

WHAT NEXT

Ensure only one non-reference value.

STAT-007 (warning) Library %s, variation %s, value %f already

exists.

DESCRIPTION

The library, variation, and value already exists as a triplet. Only the first
setting is used; subsequent settings are ignored.

WHAT NEXT

Only set the library, variation, and value once.

STAT-008 (error) More than one distribution in distribution list.

DESCRIPTION

The *-distribution* option must reference exactly one distribution.

WHAT NEXT

Check that the variable used with the *-distribution* argument references exactly one
distribution.

STAT-009 (error) Missing a distribution in the distribution list.

DESCRIPTION

The *-distribution* option must reference exactly one distribution.

WHAT NEXT

Check that the variable used with the *-distribution* argument references a
distribution.

STAT-010 (warning) Cannot find variation.

DESCRIPTION

PrimeTime could not find the specified variable to delete it.

WHAT NEXT

Ensure that the variation has been created. Ensure that the variable has not already been deleted.

STAT-011 (error) Variation library %s does not exist.

DESCRIPTION

The given library does not exist in the search path.

WHAT NEXT

Ensure that the search path exists, and that the library exists in the search path.

STAT-012 (error) Cell %s may not have a timing arc or may not match across libraries.

DESCRIPTION

A cell in the library may not have a timing arc, or does not match across libraries. There could be cells in one library not in another, a different number of pins between cells of the same name, or pins having different directions.

WHAT NEXT

If the cell has no timing arc, check that it is not used. Check that the libraries all have the same cells, and that their pins match in name, number, and direction.

STAT-013 (error) %s quantile with value %lf is out of range.

DESCRIPTION

A quantile value falls outside the open interval zero to one. It must be strictly greater than zero and strictly smaller than one.

WHAT NEXT

Change the quantile to be a floating point number between zero and one.

STAT-014 (error) Cannot turn on variation analysis when power analysis is on.

DESCRIPTION

```
Power analysis and variation analysis are currently mutually exclusive. Variation
analysis cannot be enabled while power analysis is on.
```

WHAT NEXT

```
Turn off power analysis first then turn on variation analysis.
```

STAT-015 (error) Size of variation_name_list does not match size of variation_value_list.

DESCRIPTION

```
When the -reference_value option is used, the number of names in the
variation_name_list must match the number of values in the variation_value_list.
```

WHAT NEXT

```
Either remove the -reference_value option from the command, or make the number of
names equal the number of values.
```

STAT-016 (error) The %s distribution cannot be specified with %d values.

DESCRIPTION

```
The type of the distribution determines the number of elements needed in the value
list. See the create_distribution man page for a description of the types, the
number of values they need, and what the arguments mean.
```

WHAT NEXT

```
Make sure that the type on the command and the number of values match.
```

STAT-017 (error) The first and last function value of a pwl

distribution must be 0.0.

DESCRIPTION

```
The first and last function value in the value list of a pwl distribution must
always be 0.0.
```

WHAT NEXT

```
Change the distribution type to something other than pwl, or change the second value
and last value in the value list to 0.0.
```

STAT-018 (error) The -reference_value option is required on first call.

DESCRIPTION

```
The first time set_variation_library command is called it must have the -
reference_value option.
```

WHAT NEXT

```
Set a reference value the first time that set_variation_library is called. See the
set_variation_library command for more information.
```

STAT-019 (error) Variation library %s does not exist.

DESCRIPTION

```
The given library does not exist in the search path.
```

WHAT NEXT

```
Ensure that the search path exists, and that the library exists in the search path.
```

STAT-020 (error) Cannot have a variation called nom.

DESCRIPTION

```
The word 'nom' is a reserved variation name internal to PrimeTime.
```

WHAT NEXT

```
Select a different name for the variation.
```

STAT-021 (warning) %s %s is not supported yet.

DESCRIPTION

```
This feature is not supported in the current version of PrimeTime.
```

WHAT NEXT

```
Contact your PrimeTime representative if this feature is absolutely needed now.
```

STAT-022 (error) Library data for variation %s is needed in advance.

DESCRIPTION

```
PrimeTime requires that library data for each variation be entered before these
variations are defined using the set_variation command.
```

WHAT NEXT

```
Ensure that in your scripts, any set_variation_library commands occur before any
set_variation commands.
```

STAT-023 (error) Parameter names %s and %s do not match.

DESCRIPTION

```
The parameter name associated with a variation must match the name of the
corresponding variation parameter. PrimeTime has found a mismatch during the
```

execution of the command and produces this error.

WHAT NEXT

Ensure that the parameter name provided with the command matches the correct variation parmater.

STAT-024 (error) Value %s is unknown to class %s.

DESCRIPTION

The value is expected to be a valid value or a member of the class. This error shows that this expectation has failed.

WHAT NEXT

Check the allowed values for the class and ensure that the value belongs to this class.

STAT-025 (error) Cannot remove the variation from the arc.

DESCRIPTION

PrimeTime cannot remove a variation from an arc that does not have that variation.

WHAT NEXT

Provide those arcs that do have the given variation.

STAT-026 (error) The variation %s of the %s parameter is assigned to both the design and an arc.

DESCRIPTION

The same variation must not be used for both the design and any timing arcs.

WHAT NEXT

Uniquify the varition names or remove the shared variation from the design or the arcs.

STAT-027 (error) The number of variations to sub in the collection is %d.

DESCRIPTION

One can sub two and only two variations. The collection must contain two variations.
any timing arcs.

WHAT NEXT

Make the collection contain two variations and run again.

STAT-028 (error) A library is given for a second time.

DESCRIPTION

Variation libraries can only be given once.

WHAT NEXT

Remove from the script the redundant library and rerun.

STAT-029 (error) The lower bound %lf for the distribution is larger than the upper bound %lf.

DESCRIPTION

A distribution lower bound must be smaller than its upper bound.

WHAT NEXT

Fix the bounds and rerun.

STAT-030 (error) The area under the curve of this pwl

distribution is %lf and not 1.0.

DESCRIPTION

```
The area under the curve of a probability density function must be 1.0.
```

WHAT NEXT

```
Choose numbers such that the area under the curve of the pdf is 1.0, and rerun.
```

STAT-031 (warning) The variation %s of the %s parameter has a non-zero mean of %f.

DESCRIPTION

```
The variations are expected to have zero mean.
```

WHAT NEXT

```
Adjust the variation parameters to ensure zero mean.
```

STAT-032 (error) For a pwl probability distribution, the first and last weight values must be 0.0.

DESCRIPTION

```
Weight values at the ends of the distribution support must be 0.0.
```

WHAT NEXT

```
Fix the weight value(s) and run again.
```

STAT-033 (error) For a pwl probability distribution, the x-values must be increasing. Value %lf was smaller than its predecessor.

DESCRIPTION

```
x-values of a pwl distribution must be strictly increasing.
```

Fix the x value(s) and run again.

STAT-034 (error) For a pwl probability distribution, the weight values must be non-negative. Value %lf was found.

DESCRIPTION

Weight values of a pwl distribution must be nonnegative.

WHAT NEXT

Fix the w value(s) and run again.

STAT-035 (error) The lower or upper bound %lf must be smaller or larger than %lf.

DESCRIPTION

The lower or upper bound must be correct relative to the lowest or largest x-value.

WHAT NEXT

Fix the bounds or fix the x-values, and run again.

STAT-036 (error) This %s distribution must have its %s bound %s than %lf.

DESCRIPTION

The bounds or the parameters of this distribution are incorrect.

WHAT NEXT

Fix the bounds or the parameters of this distribution.

STAT-037 (error) The distribution attribute %s has parameter value %d.

DESCRIPTION

The parameter value for the distribution attribute of cdf_values (or pdf_values) must be two or larger.

WHAT NEXT

Increase the number of data points or use the distribution attribute cdf (or pdf).

STAT-038 (error) Invalid variable name %s.

DESCRIPTION

An element in the variable name list does not match one of the existing names. Each variable name in the variable name list must match one of the variable names defined with the **-reference_point** option.

WHAT NEXT

Either correct the command so that the variable name matches one of the reference point variable names, or correct the reference point definition to have the needed variable name.

STAT-039 (warning) Library %s contains a special cell %s with no timing arc. Variation-aware PrimeTime may not be able to handle this cell.

DESCRIPTION

A special cell in the library does not have timing arcs. If a design contains such a cell, Variation-aware PrimeTime may not be able to handle it.

WHAT NEXT

Check that these cells are not in the design.

STAT-040 (error) %s %s when variation-aware analysis is not enabled.

DESCRIPTION

```
Variable variation_enable_analysis must be TRUE to enable this feature.
```

WHAT NEXT

```
Set variable variation_enable_analysis to TRUE.
```

STAT-041 (error) For command %s, %s must be %s than %g.

DESCRIPTION

```
For certain commands, there are restrictions on the range of possible option values.
```

WHAT NEXT

```
Make sure that the values of the option are within the allowed range.
```

STAT-042 (error) Library specified in define_scaling_lib_group cannot be specified as a variation library.

DESCRIPTION

```
Any library specified as a scaling library using the command
define_scaling_lib_group cannot be specified as a variation library.
```

WHAT NEXT

```
If you want to specify the library as a variation library, re-define the
define_scaling_lib_group and re-link the design.
```

STAT-043 (error) For the %s distribution, the %s parameter

must be %s than %lf.

DESCRIPTION

```
The value entered for this parameter is incorrect.
```

WHAT NEXT

```
Fix the value of the parameter.
```

STAT-044 (error) For the %s distribution, the %s must be %s than %lf.

DESCRIPTION

```
The bound entered is incorrect.
```

WHAT NEXT

```
Fix the value or the bound of the distribution parameters.
```

STAT-045 (error) Command %s cannot be executed before linking the design.

DESCRIPTION

```
The design needs to be linked before using this command.
```

WHAT NEXT

```
Link the design and issue the command again.
```

STAT-046 (error) The support of this %s distribution has weight %lf. We require that the support of a truncated distribution be at

least %lf.

DESCRIPTION

Either the lower and upper bounds are too close, the lower bound is too large, or the upper bound is too small.

WHAT NEXT

Fix the bound(s) so the truncated distribution has heavier support or try another distribution.

STAT-047 (error) This %s probability distribution has a %s equal to %lf. This is invalid for this probability distribution.

DESCRIPTION

An invalid value(s) was entered for the relevant parameter(s) of this distribution.

WHAT NEXT

Fix the value of this parameter(s) for this distribution.

STAT-048 (error) Path-based analysis works with variation-aware analysis only when design is in on_chip_variation mode.

DESCRIPTION

Variation-aware analysis requires the *on_chip_variation* analysis type. Path-based analysis recomputes the paths only when analysis type is set to on_chip_variation. When analysis_type is set to *bc_wc* or *single*, no recomputed path will be returned.

WHAT NEXT

Use **set_operating_conditions** to set the design in *on_chip_variation* for variation-aware analysis; or disable variation-aware analysis when the design is in *bc_wc* or *single* analysis type.

SEE ALSO

set_operating_conditions(2), variation_enable_analysis(3).

STAT-050 (Error) Creation of variation library group failed %s.

DESCRIPTION

While creating a variation library, data for the same arcs and pins across the libraries for a variation library group are associated with each other; if this association fails, the variation library group cannot be completed and the STAT-050 error message is issued.

WHAT NEXT

Be sure that the set of arcs and pins is present across the members of the variation library groups and the linked libraries. This message is issued when some of the arcs or cells are missing across the members of the scaling library groups.

Note that it removes all the previous variation libraries that were set. So after making sure that the set of arcs and pins are present within all the libraries, set all the variation libraries again.

SEE ALSO

set_variation_library (2)

STAT-051 (warning) Cannot report library sensitivity. '%s'

DESCRIPTION

Sensitivity values cannot be computed due to different formats of delay and slew tables in variation libraries.

WHAT NEXT

Make sure all variation libraries have the same dimensions, sizes and breakpoints of delay and slew tables.

SEE ALSO

set_variation_library(2).

STAT-052 (Warning) Some of the timing arcs cannot be uniquely determined across the variation library group, it is

assumed that the timing arcs are defined in the same order across all the libraries.

DESCRIPTION

```
While creating a variation library, data for the same arcs and pins across libraries
are associated with each other; if the timing arcs cannot be associated across the
scaling libraries because the timing arcs cannot be identified uniquely within a
library, the STAT-052 warning message is issued. Since the timing arcs cannot be
uniquely identified, the arcs are assumed to be in the same order across the
libraries in a library group.

Note that this is only an informational warning, the association of pins and arcs
for the variation library group will still be created.
```

WHAT NEXT

```
Be sure that the set of arcs that cannot be uniquely identified are present in the
same order across the members of the scaling library groups.
```

SEE ALSO

set_variation_library (2)

STAT-053 (error) For command %s, the list for option %s contains an invalid number (%d) of elements.

DESCRIPTION

```
The number of elements in the list is invalid.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-054 (error) For command %s, the list for option %s must contain %d or more elements.

DESCRIPTION

```
The number of elements in the list is invalid.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-055 (error) For command set_variation_correlation %s, the number %d of variations in the list does not match the expected number %d derived from the size of the list of correlation values of correlation %s.

DESCRIPTION

```
For a set_variation_correlation command associated with a correlation that is cross,
the number of variations listed must equal the number of variations derived from the
size of the list of correlation values (listed in the corresponding
create_correlation command).
```

WHAT NEXT

```
Correct and rerun.
```

STAT-056 (error) For command set_variation_correlation %s, the corresponding covariance matrix is not positive definite.

DESCRIPTION

```
For a set_variation_correlation command associated with a correlation that is cross,
the covariance matrix formed by the correlation values listed in the corresponding
create_variation command along with the variances of the variations, must be
positive definite. Either there is a linear relationship between the variations, in
which case one should eliminate the redundant variation(s), or the correlation
values were not estimated precisely enough.
```

WHAT NEXT

```
Correct the correlation numbers or the standard deviations of the distributions.
```

STAT-057 (warning) The distribution of variation %s is %s. Variations with %s are assumed to have a %s normal distribution. This implies that the marginal distributions must be

normal.

DESCRIPTION

This type of correlation is supported under the condition that the variations have a
multidimensional normal distribution.

WHAT NEXT

Check whether the univariate distribution is modeled well enough by a normal. If
not, the results will not necessarily be mathematically correct.

STAT-058 (error) Variation %s has cross-correlation with another set of variations (associated with set_variation_correlation %s).

DESCRIPTION

A variation can have cross-correlation with one set of variations. Otherwise, it
should have a cross-correlation with the union of the sets.

WHAT NEXT

If there is no error, one should take a larger set of cross-correlated variations,
estimate the correlations for this larger set, and set a new create_correlation and
set_variation_correlation commands.

STAT-059 (error) %s cannot be set with option %s.

DESCRIPTION

Cross-correlations must be set on a specific set of variations. Further, the number
of variations in the set must be consistent with with the number of correlation
values entered in the corresponding create_correlation statement.

WHAT NEXT

Enter the list of variations this command applies to.

STAT-060 (error) Value %f of option %s of command

create_correlation is invalid.

DESCRIPTION

```
The value for this option is invalid or not yet supported.
```

WHAT NEXT

```
Fix the value for this option and rerun.
```

SEE ALSO

remove_correlation (2), **set_variation_correlation** (3).

STAT-061 (warning) Command %s with option -name %s has been reissued with possibly a different value(s). The current command will overwrite the previous one.

DESCRIPTION

```
The command has been reissued with possibly a different value(s).
```

WHAT NEXT

```
Make sure this was intended.
```

STAT-062 (error) For command %s, one and only one of the two options %s or %s must be given.

DESCRIPTION

```
Exactly one of the two options is required.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-063 (error) For option %s of command %s, the collection

of %s's is of size %d. It must be of size 1.

DESCRIPTION

```
The collection for the option must be exactly of size 1.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-064 (error) Cannot find a correlation with name '%s'.

DESCRIPTION

```
Each correlation object is identified with a unique string name. No correlation
object can be found with the given name.
```

WHAT NEXT

```
Make sure the correlation with the given name exists.
```

SEE ALSO

```
create_correlation(2). set_variation_correlation(2).
```

STAT-065 (error) %s quantile undefined.

DESCRIPTION

```
High and low quantiles must be defined together.
```

WHAT NEXT

```
Define both high and low quantiles with proper values.
```

STAT-066 (error) Parameter name required to set a variation on

timing objects

DESCRIPTION

The create_variation command has a list of timing objects but is missing the parameter name. It requires a parameter name when setting the variation on timing objects.

WHAT NEXT

Re-issue the command and add a parameter name.

STAT-067 (error) More than one design found in the timing object list

DESCRIPTION

The create_variation command only allows one design in the timing object list.

WHAT NEXT

Re-issue the command with only one design specified.

STAT-068 (error) If a design is specified it must be the current design

DESCRIPTION

The create_variation command requires that if a design is specified as a timing object then it must be the current design. If you leave out the timing object list and specify a parameter_name, create_variation defaults to using the current design.

WHAT NEXT

Re-issue the command with either the current design or an empty timing object list.

STAT-069 (error) The timing object list must be of a single object

type

DESCRIPTION

The create_variation command requires that all objects in the timing object list be the same time. The timing object list can be either timing arcs or a design.

WHAT NEXT

To put a variation on both timing arcs and a design, issue the command twice: once with timing arcs and once with the design.

STAT-070 (error) The name %s for command %s conflicts with another %s name

DESCRIPTION

This error message is generated if the command has already created an object with the same name.

WHAT NEXT

Re-issue the command with a different name for the -name option.

STAT-071 (error) Command %s cannot be executed with option

DESCRIPTION

The design needs to be linked before using this command with the given option.

WHAT NEXT

Link the design and issue the command again.

STAT-072 (error) Command %s requires at least two variations

in the object_list

DESCRIPTION

The command requires two or more variations in its object list in order to perform the operation. The object list is a collection of variations, and in this case there was less than two elements in the list.

WHAT NEXT

Include more variations in the collection. Either use **add_to_collection** to insert variations from other collections, or use pattern in **get_variations** to create a collection with more than one variation in it.

STAT-073 (error) Missing *-all* and *variation_list* arguments

DESCRIPTION

The command requires either the *-all* or the *variation_list* options on the command line, and it could not find either.

WHAT NEXT

Re-issue the command with either the *-all* or the *variation_list* option.

STAT-074 (error) Both *-all* and *varaition_list* specified

DESCRIPTION

The command requires one of either *-all* or *variation_list*, but it found both.

WHAT NEXT

Re-issue the command with only one of *-all* or *variation_list*.

STAT-075 (error) For spatial correlation %s, the list of pairs of values (distance, correlation) of option -physical_distance must

contain a positive even number of elements. It is %d.

DESCRIPTION

```
Elements must be missing from the list.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-076 (error) For spatial correlation %s, a %s has value %f. It is %s, and, so, is illegal.

DESCRIPTION

```
Elements of the list are out-of-order or are incorrect.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-077 (error) For spatial correlation, PrimeTime could not obtain a bounding box from the parasitics SBPF file(s). The physical locations of pins may not be available. Spatial correlation will be ignored. Full autocorrelation (i.e., correlation with constant 1.0) for the relevant variation(s) will be assumed.

DESCRIPTION

```
Physical location of pins must be available in the SBPF file(s).
```

WHAT NEXT

```
Verify that the SBPF file(s) contain(s) the pins physical locations.
```

STAT-080 (error) %s cannot be used when detailed variation-

aware clock analysis is disabled.

DESCRIPTION

Variable variation_enable_analysis must be TRUE and detailed clock analysis must be enabled to use this option.

WHAT NEXT

Ensure that the variation_enable_analysis variable is set to TRUE and that the variation_analysis_mode variable is set to detailed_clock_timing.

STAT-081 (warning) The %s physical distance %f is %s compared to the %s %f. Please verify that the units of distance of the correlation function are in nanometers.

DESCRIPTION

The warning is simply a recommendation to the user to double-check the units of distance (which must be in nanometers). PrimeTime checks whether the physical distances are very small or very large relative to the size of the bounding box (that is read in from the spef file).

WHAT NEXT

Verify that the values of the physical distance of this correlation were those intended. If they are indeed correct, please ignore this warning.

STAT-082 (warning) PrimeTime could not handle the spatial correlation %s. It will be assumed that the variations are not spatially dependent, and have a constant correlation with value 1.

DESCRIPTION

If the correlation function does not decay fast enough or varies wildly (i.e., it is not monotone at all), PrimeTime may have a problem handling this spatial correlation. Such correlation functions are atypical.

WHAT NEXT

Try a correlation function that decays to zero faster (with distance) or is more
monotone.

STAT-083 (error) set_variation is applied here on a non-variation.

DESCRIPTION

The command set_variation must be applied on a genuine variation, i.e., on a
construct declared via create_variation.

WHAT NEXT

Fix typo(s) if any, or precede the command by a create_variation if it is missing.

STAT-085 (error) %s is missing from command set_variation_library.

DESCRIPTION

The command set_variation_library is missing a list of variations, a list of values,
or a library name.

WHAT NEXT

See the **set_variation_library** command for more information.

STAT-086 (error) For command %s, options %s and %s are invalid together.

DESCRIPTION

The command does not take in these two options together.

WHAT NEXT

See the User Guide. Correct and rerun.

STAT-087 (error) For command set_variation_library with multi-libraries linked, library %s is out of order, or contains an incorrect variation name or value.

DESCRIPTION

```
When linking multi-libraries, the sets of set_variation_library commands must be in
step-lock.
```

WHAT NEXT

```
See the User Guide for a discussion.
```

STAT-088 (error) For command set_variation_library with multi-libraries linked, more than one library were linked.

DESCRIPTION

```
When linking multi-libraries in this context, there should be a single library
linked.
```

WHAT NEXT

```
See the User Guide for a description.
```

STAT-089 (error) For command %s, options %s and %s are incompatible without option %s.

DESCRIPTION

```
The command has either an incompatible option or is missing an option.
```

WHAT NEXT

```
See the man page for more information about this command.
```

STAT-090 (error) The command variation_correlation cannot

process the %s object.

DESCRIPTION

```
The command applies generally to variations queried from path-based analysis, such
as path variation_arrival and variation_slack.
```

WHAT NEXT

```
Apply this command to a variation queried via get_attribute on a timing path or
timing point obtained from a path-based analysis.
```

STAT-091 (error) %s variation report is not available %s.

DESCRIPTION

```
The cell and net variation report is only available when variation-aware analysis is
turned on in the default or detailed_clock_timing mode.
```

WHAT NEXT

```
Set variation_enable_analysis to TRUE and variation_analysis_mode to default or
detailed_clock_timing.
```

SEE ALSO

variation_enable_analysis(3), variation_analysis_mode(3).

STAT-092 (error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

DESCRIPTION

```
For a set_variation_correlation command with discrete parameter distributions,
associated with a correlation that is cross, all the weights of each discrete
parameter distribution should be identical. For a k-valued discrete parameter, the
corresponding weights (k in number) should each be equal to 1/k.
```

```
Correct and rerun.
```

STAT-093 (error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

DESCRIPTION

```
For a set_variation_correlation command with discrete parameter distributions,
associated with a correlation that is cross, all the weights of each discrete
parameter distribution should be identical. For a k-valued discrete parameter, the
corresponding weights (k in number) should each be equal to 1/k.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-094 (error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

DESCRIPTION

```
For a set_variation_correlation command with discrete parameter distributions,
associated with a correlation that is cross, all the weights of each discrete
parameter distribution should be identical. For a k-valued discrete parameter, the
corresponding weights (k in number) should each be equal to 1/k.
```

WHAT NEXT

```
Correct and rerun.
```

STAT-095 (error) An unknown variation %s.

DESCRIPTION

```
An unknown variation requires a name and cannot have a parameter name.
```

WHAT NEXT

Create an unknown variation with a unique name, without a parameter name.

SEE ALSO

create_variation(2).

STML

STML-1 (error) File %s: Error at line %d, token %s, %s

DESCRIPTION

```
Syntax error in the 'stamp' file.
```

WHAT NEXT

```
Correct the syntax error.
```

STML-2 (error) File %s: Line %d, lu_table_template '%s' already defined.

DESCRIPTION

```
The lu_table_template is already defined. You cannot define the same
lu_table_template more than once.
```

WHAT NEXT

```
Change the name of the lu_table_template so that it does not clash with the previous
one.
```

STML-3 (error) File %s: Line %d, in the lu_table_template %s definition,
 h variable 1 redefined.

DESCRIPTION

```
In the lu_table_template definition, the variable corresponding to variable_1 is
declared more than once.
```

WHAT NEXT

```
Perhaps variable_1 was mistakenly choosen instead of variable_2. Change it to
variable_2 or remove one of the lines which define variable_1.
```

STML-4 (error) File %s: Line %d, lu_table_template %s variable 2 redefined.

DESCRIPTION

In the lu_table_template definition, the variable corresponding to variable_2 is declared more than once.

WHAT NEXT

Perhaps you mistakenly chose variable_2 instead of variable_1. Change it to variable_1 or remove one of the lines which define variable_2.

STML-5 (error) File %s: Line %d, lu_table_template %s index 1 redefined.

DESCRIPTION

In the lu_table_template definition index_1 is redefined.

WHAT NEXT

Perhaps you mistakenly choose index_1 instead of index_2. Change it to index_2 or remove one of the lines which define index_1.

STML-6 (error) File %s: Line %d, lu_table_template %s index_2 redefined.

DESCRIPTION

In the lu_table_template definition index_2 is redefined.

WHAT NEXT

Perhaps you mistakenly choose index_2 instead of index_1. Change it to index_1 or remove one of the lines which define index_2.

STML-7 (error) File %s: Line %d, INTERNAL ERROR detected.

DESCRIPTION

```
Internal error detected.
```

WHAT NEXT

```
Check if the error was caused because of cumulative effect of previous errors. If
you cannot solve the error, contact Synopsys support.
```

STML-8 (error) File %s: In LU_TABLE_TEMPLATE %s variable_1
is not defined.

DESCRIPTION

```
For a lu_table_template, at least variable_1 must be defined. If variable_1 is not
defined, it is an error.
```

WHAT NEXT

```
Define variable_1.
```

STML-9 (error) File %s: In LU_TABLE_TEMPLATE %s variable_2
is defined but variable_1 is not defined.

DESCRIPTION

```
Variable_2 can be defined only if variable_1 is defined.
```

WHAT NEXT

```
Make the variable_2 definition to be the variable_1 definition and remember to
change index_2 to index_1.
```

STML-10 (error) File %s: In LU_TABLE_TEMPLATE of '%s'

index_2 is
 defined but variable_2 is not defined.

DESCRIPTION

```
Index_2 can be defined only if variable_2 is defined.
```

WHAT NEXT

```
Define variable_2, to which index_2 refers.
```

STML-11 (error) File %s: arc label '%s' at or before
 line %d redefined.

DESCRIPTION

```
The arc label has already been defined, so the same arc label cannot be defined
again.
```

WHAT NEXT

```
Perhaps the arc label is being redefined by mistake. If not, change the arc label
and proceed.
```

STML-12 (error) File %s: The values defined at or before line %d
 are not same for different rows.

DESCRIPTION

```
Each row of the value table must have the same size. This size must be equal to the
size of the index_2 table.
```

WHAT NEXT

```
Make sure that each row of the 'values' is same as each row of the index_2.
```

STML-13 (error) File %s: For the arc '%s' the
LU_TABLE_TEMPLATE name '%s'

used at or before line %d is not defined.

DESCRIPTION

```
The LU_TABLE_TEMPLATE used in the arc definition is not present. The
LU_TABLE_TEMPLATE must be defined before using the LU_TABLE_TEMPLATE name.
```

WHAT NEXT

```
Check that the LU_TABLE_TEMPLATE, which is referred to, is present. If the
lu_table_templateis not present, define it before use.
```

STML-14 (error) File %s: index_1 is not defined for the arc '%s' defined
  at or before line %d, which refers to LU_TABLE_TEMPLATE %s.

DESCRIPTION

```
In the arc label definition, the index_1 is not defined. Define it.
```

WHAT NEXT

```
index_1 is not defined, please give it a list of points. The index_1 definition is
not required for scalar tables.
```

STML-15 (error) File %s: index_2 is not defined, but var2 is defined
  for the arc '%s' defined at or before line %d, which refers to
  LU_TABLE_TEMPLATE %s.

DESCRIPTION

```
For the arc defined at or before the line specified, index_2 is not defined, but
variable_2 is defined.
```

WHAT NEXT

```
Define index_2 or remove the variable_2 definition.
```

STML-16 (error) File %s: In the arc '%s' defined at or before line %d,
  variable_1 and variable_2 defined refer to the same variable.

DESCRIPTION

```
variable_1 and variable_2 cannot refer to the same variable for a LU_TABLE_TEMPLATE
or an arc.
```

WHAT NEXT

```
Change the variable_1 or variable_2 to a different variable, or have a one
dimensional table.
```

STML-17 (error) File %s: In the arc '%s' defined at or before line %d,
  %d elements are expected in the one dimensional table but %d were found.

DESCRIPTION

```
In one dimensional table the number of elements expected in the value table is equal
to the number of elements in the index_1 list.
```

WHAT NEXT

```
Make the number of elements in the 'values' table equivalent to the number of
elements in the index_1 list.
```

STML-18 (error) File %s: For the arc '%s' before line %d, expected
  to find %d groups of values, but found %d groups of values.

DESCRIPTION

```
The number of rows in a 'values' table is equal to the number of values in index_1.
If this is not the case, an error occurs.
```

Check the index_1 values and the number of groups of values in the 'values' table
and make them equal.

STML-19 (error) File %s: For the arc '%s' defined before the line %d, expected to find %d group of values in a group, but found %d.

DESCRIPTION

The number of values in a group must be equal to the number of values in the defined
index_2 table.

WHAT NEXT

Verify that the number of values in a group (row) is equal to the number of elements
in the index_2 table.

STML-20 (error) File %s: %s table specified twice for the arc '%s' defined
at or before line %d.

DESCRIPTION

For an arc the same type of table (for example, RISE_TRANSITION) cannot be defined
more than once. If the table is defined more than once, it is an error.

WHAT NEXT

Delete one or more occurences of the repeated table types.

STML-21 (error) File %s: %s specified with one of %s/%s/%s for the arc '%s' defined at or before line %d.

DESCRIPTION

If propagation is specified for an arc, rise or fall propagation cannot be defined
for the same arc. The same holds true for transition and constraint.

Have either propagation or fall/rise propgation, transition or fall/rise transition,
and constraint or rise/fall constraint.

STML-22 (error) File %s: Specifed constraint tables and cell_delay
  transition tables for the arc '%s' defined at or before line %d.

DESCRIPTION

An arc can be a constraint arc or a delay arc; it cannot be both. Describe either
constraint or delay behavior for an arc.

WHAT NEXT

Do not mix constraint and delay behaviors for the same arc; separate them.

STML-23 (error) File %s: For the arc '%s' defined at or before line %d,
  transition table specified but corresponding cell delay table not specified.

DESCRIPTION

For an arc, if transition table is specified, corresponding cell delay table must be
specified. For example, if rise_transition is specified, cell_rise must also be
specified.

WHAT NEXT

Specify cell delay table if transition table is specified.

STML-24 (error) File %s: For the arc %s' defined at or before line %d,

the %s values are not monotonically increasing.

DESCRIPTION

```
The values defined in index_1 and index_2 are expected to be monotonically
increasing. If they are not monotonically increasing, it is an error.
```

WHAT NEXT

```
Change the specified table so that the values are monotonically increasing.
```

STML-25 (error) File %s: The arc_label %s referred to in line %d as

a drive table is not defined.

DESCRIPTION

```
The arc_label, as an argument to the DRIVE, is not defined.
```

WHAT NEXT

```
Define the arc referred in 'drive' and try again.
```

STML-26 (error) File %s: In the arc label (%s) referred by drive at or

before line %d, expected variable_1 to be OUTPUT_NET_CAPACITANCE, but found

it to be %s.

DESCRIPTION

```
The only variable (variable_1) that can be defined for the arc label referred to by
'drive' is output_net_capacitance. If the variable is anything else or is undefined,
it is an error.
```

WHAT NEXT

```
Make the variable_1 of the arc label definition to be output_net_capacitance.
```

STML-27 (warning) File %s: In the scalar table refered to by the arc
'%s' at or before line %d, %s defined, ignoring...

DESCRIPTION

```
For scalar tables, index_1, index_2, variable_1, and variable_2 cannot be specified.
If they are, they are ignored.
```

WHAT NEXT

```
If you have defined the table to be scalar by mistake, change it.
```

STML-28 (error) File %s: In the SCALAR table refered by the arc '%s'
at or before line %d, expected to see only one value but found %d.

DESCRIPTION

```
Scalar tables must have only one value. If more than one value is found, it is an
error.
```

WHAT NEXT

```
Change the scalar table in question to have only one value.
```

STML-29 (warning) File %s: at or before line %d, the value
of attribute '%s' is redefined for %s.
Replacing previous defined value...

DESCRIPTION

```
One of the attribute for the specified object is defined more then once. The new
redefined value will always replace the existing value, so the last defined value is
actually finally written in to the library.
```

If you do not want to keep the new value, delete the redefined values.

STML-30 (warning) File %s: Parameter defined for port %s in data
file but no such port is defined in the model file.

DESCRIPTION

The port parameter is defined for some port that is not defined in the model file.

WHAT NEXT

Define the port in the model file. If the port name in the port parameter definition is not correct, correct or delete it.

STML-31 (error) Timing arc '%s' is defined in file %s,
but thers is no data defined for it in file %s.

DESCRIPTION

The arc that is used in the model file is not defined in the data file.

WHAT NEXT

Arcs used in the model file must be defined in the data file. Define this arc in the data file and use it in the model file.

STML-32 (error) File %s: Line %d, the arc %s is already instanced in
the model file.

DESCRIPTION

An arc can be instanced in a model file only once.

Change the name of the arc label and define it in the data file, or remove the arc
label instance in the model file.

STML-33 (error) File %s: Line %d, The qualifier is already set to %s, but again it is being set to %s.

DESCRIPTION

The qualifiers for the delay arcs cannot be set to conflicting types. Check the
manual to see what qualifers conflict and cannot be used together.

WHAT NEXT

Change the qualifiers to remove the conflict.

STML-34 (error) File %s: Line %d, The tlatch edge arc '%s' has not been defined.

DESCRIPTION

The edge arc, which the 'tlatch' arc refers to (in the construct TLATCH = arc_name),
is not defined. The corressponding arc must be instantiated first in the model file
and then that arc can be referred by the tlatch arc.

WHAT NEXT

Instantiate the tlatch edge arc before using it in the 'tlatch' construct.

STML-35 (error) File %s: Line %d, The edge arc %s used along with the tlatch arc should be either POSEDGE or NEGEDGE arc, but arc %s is not.

DESCRIPTION

The arc refered by 'tlatch'arc ('tlatch'= edge_arc) has to be a 'posedge' or
'negedge' type. If the arc is not, it is an error.

Make the edge arc refered by the 'tlatch'arc to be 'posedge' or 'negedge'.

STML-36 (error) File %s: Line %d, Cannot use %s in conjuction with %s.

DESCRIPTION

Some types of arcs cannot be used in conjuction with others. Bitwise is used only in conjuction with 'nonunate', 'inverting', or 'noninverting'; it cannot be used with any other type of arc. Logic can be only in conjuction with 'enable_high' or 'enable_low.

WHAT NEXT

Remove the incompatible arc types from occuring together.

STML-37 (error) File %s: Line %d, The number of ports in start port list is > 1.

DESCRIPTION

The number of ports in the start port list that can be greater than 1 are only for 'inverting', 'noninverting', or 'nonunate' arcs. For any other type of arc the start port can only be a single port.

WHAT NEXT

If you have more than 1 port as start port, split the port up into different arcs and instantiate it separately.

STML-38 (error) File %s: Line %d, The number of ports in the start port
  (%d) does not equal the number of end ports (%d) for the

BITWISE qualifier.

DESCRIPTION

If the 'bitwise' qualifier is used, the number of ports in the start port must be
the same as the number of ports in the end port list.

WHAT NEXT

You might have missed out some ports; please check for missed ports and correct
them.

STML-39 (error) File %s: Line %d, Arc %s: %s can be only one of
 constrained_pin_transition or related_pin_transition.

DESCRIPTION

In the data file where the arcs are defined, the constraint arc label can have
variable_1 or variable_2 to be one of constrained_pin_transition or
related_pin_transition.

WHAT NEXT

Make sure that the constraint arcs have variables defined only as
constraint_pin_transition or related_pin_transition.

STML-40 (error) File %s: Line %d, Arc %s: found arc tables other than
 '%s', for this %s arc.

DESCRIPTION

For constraint arc the only tables allowed are 'constraint', 'rise_constraint' or
'fall_contstraint'. If any other table is specified, it is an error. For delay arc
the only tables allowed are 'cell', 'cell_rise' or 'cell_fall' and 'transition',
'fall_transition' or 'rise_transition'. If any other table is specified, it is an
error.

Make sure that the tables used to describe the arc are correct.

STML-41 (error) File %s: Line %d, Arc %s: Found tables other than
  CONSTRAINT.

DESCRIPTION

For width, period, recovery, or removal, only the constraint table can be specified.

WHAT NEXT

Change the table type to constraint for the previous type arcs.

STML-42 (error) File %s: Line %d, Arc %s: %s can be only one of
  input_net_transition or output_net_capacitance.

DESCRIPTION

In the data file where the arcs are defined, the delay arc label can have either
variable_1 or variable_2 to be as input_net_transition or output_net_capacitance.

WHAT NEXT

Make sure that the constraint arcs have variables defined as either
input_net_transition or output_net_capacitance.

STML-43 (error) File %s: Line %d, Arc %s, Both
  RISE_TRANSITION/CELL_RISE and FALL_TRANSITION/
CELL_FALL

must be specified for the arc.

DESCRIPTION

```
For 'inverting', 'noninverting', or 'nonunate' arcs, both rise and fall tables must
be specified.
```

WHAT NEXT

```
For 'inverting', 'noninverting', or 'nonunate' arcs specify both rise_transition and
fall_transition or cell_rise and cell_fall.
```

STML-44 (error) File %s: Line %d, Arc %s, Expected to find RISE_TRANSITION/CELL_RISE, but it was not found.

DESCRIPTION

```
For enable_high, set_high, clear_high, posedge, or disable_high arcs, cell_rise or
rise_transition must be present.
```

WHAT NEXT

```
Please specify the rise_transition or the cell_rise table.
```

STML-45 (warning) File %s: Line %d, Arc %s, Expected to see only the RISE tables but found FALL tables too; ignoring the fall tables...

DESCRIPTION

```
For enable_high, disable_high, set_high, clear_high, or posedge arcs, only rise
tables (rise_transition or cell_rise) are expected, but found fall tables too. The
compiler ignores fall tables
```

WHAT NEXT

```
This is just an information message. If you want to remove the warning message,
remove the fall table.
```

STML-46 (error) File %s: Line %d, Arc %s, Expected to find FALL_TRANSITION/CELL_FALL, but it was not found.

DESCRIPTION

For enable_low, set_low, clear_low, posedge, or disable_low arcs, fall_transition or cell_fall must be present.

WHAT NEXT

Specify fall tables.

STML-47 (warning) File %s: Line %d, Arc %s, Expected to see only the
FALL tables but found RISE tables too; ignoring the RISE tables.

DESCRIPTION

For enable_low, disable_low, set_low, clear_low, or posedge arcs, only fall tables (cell_fall or fall_transition) were expected, but found rise tables too. The compiler ignores rise tables.

WHAT NEXT

This is just an information message. If you want to remove the warning message, remove the fall table.

STML-48 (error) File %s: Line %d, Arc %s, Transition table not accompanied by corresponding cell delay tables.

DESCRIPTION

Transition tables must be accompanied by corresponding cell delay tables. For example, if RISE_TRANSITION is specified it must be accompnied by CELL_RISE table.

WHAT NEXT

Check to see that the transition table is accompanied by corresponding cell delay table.

STML-49 (error) File %s: Line %d, The mode %s is already defined.

DESCRIPTION

```
The mode you are trying to define is already defined.
```

WHAT NEXT

```
Change the mode name.
```

STML-50 (error) File %s: Line %d, The mode value %s is repeated
  for the mode %s.

DESCRIPTION

```
The value is repeated for the given mode.
```

WHAT NEXT

```
Remove the repetitive name. Either delete it or replace it with some other name.
```

STML-51 (error) File %s: Line %d, The mode used %s is not defined.

DESCRIPTION

```
The mode used in the arc definition is not defined.
```

WHAT NEXT

```
Define that mode (before the arc definition) and use it in the arc definition.
```

STML-52 (error) File %s: Line %d, Could not find mode_value %s in the

mode_definition of %s.

DESCRIPTION

The mode_value used in the arc_defintion is not found in the mode definition.

WHAT NEXT

Either add the mode_value in the mode_definition or use one of the defined mode_values.

STML-53 (error) File %s: Line %d, %s already defined as a %s.

DESCRIPTION

The name given for the port, pin, or bus declaration is already used for declaring either a port, a pin, or a bus. You cannot have more than 1 port, pin, or bus with the same name.

WHAT NEXT

Change the name of the port being declared so that there is no conflict.

STML-54 (error) File %s: Line %d, %d ports are declared to make
  the bus %s of width %d.

DESCRIPTION

The number of ports declared is different from the bus_width of the bus that contains the ports. They must be equal.

WHAT NEXT

Make the bus width equal to the the number of ports that make up the bus.

STML-55 (error) File %s: Line %d, %s is not defined as a PORT/

PIN/BUS.

DESCRIPTION

```
The port, pin, or bus used is not defined in the port_definitions. The ports must be
defined before they are used in the arcs.
```

WHAT NEXT

```
Define the port you are using in the arcs before using them.
```

STML-56 (error) File %s: Line %d, %s is a bussed pin, and cannot be
used as a start port for this arc.

DESCRIPTION

```
Bused pins or ports can be used as a start_port only for 'inverting',
'noninverting', or 'nonunate' arcs. No other arc can have start ports > 1.
```

WHAT NEXT

```
If the arc is not 'inverting', 'noninverting', or 'nonunate', do not have start_port
>1.
```

STML-57 (error) File %s: Line %d, ENABLE arc not of LOGIC type; must
end in a TRIOUT port. However, %s is not a TRIOUT port.

DESCRIPTION

```
enable_high or enable_low arcs without the 'logic' qualifier must end in a 'triout'
port. If the arc does not end with this, it is an error.
```

WHAT NEXT

```
Either make the 'enable' arc end in a 'triout' port or add the 'logic' qualifer if
there is a logic after the 'tristate' buffer.
```

STML-58 (error) File %s: Line %d, Port %s expected to be of INPUT/INOUT/OUTPUT but found to be %s.

DESCRIPTION

The start for delay_arcs is expected to be of input, inout, or output type. If the start is anything other than this, it is an error.

WHAT NEXT

Make the start port of the delay arcs either input, output, or inout type.

STML-59 (error) File %s: Line %d, Port %s expected to be of INOUT/OUTPUT/TRIOUT but found to be %s.

DESCRIPTION

The end_port for delay_arcs are expected to be either triout, inout, or output type. If the end_port is anything other than one of these, it is an error.

WHAT NEXT

Make the end port of the delay arcs either triout, output, or inout type.

STML-60 (error) File %s: Line %d, %s port indicated to be of BUSSED type but was found to be of NON BUSSED type.

DESCRIPTION

The port is infered to be a bus type because it is of port[start:end] type of usage. However, 'port' is not of bused type.

WHAT NEXT

If it was mistakenly declared to be a nonbused type, modify the port definition to be a bused type. If the usage in the arc definition was wrong, modify the usage.

STML-61 (error) File %s: Line %d, The bus limits %d:%d used

for the bus
 '%s' is not within the limits %d:%d of the port declaration.

DESCRIPTION

```
The bus limits used in the arc definition are not within the bus limits of the port
declaration.
```

WHAT NEXT

```
Either change the bus limits of the port declaration or change the bus limits in the
usage so that the bus limit usage is within the port declaration bus limits.
```

STML-62 (error) File %s: Line %d, The port name %s specified in the TLATCH
 arc output port does not exist in the corresponding edge delay arc.

DESCRIPTION

```
The output port specified in the 'tlatch' arc must be present as an output port in
the correponding edge delay arc. If the arc is not, it is an error.
```

WHAT NEXT

```
Make the output port of the 'tlatch' arc and the corresponding edge delay arc the
same
```

STML-63 (warning) File %s: Line %d, %s specified for %s, which is
 not an output port.

DESCRIPTION

```
'drive' cannot be specified for output ports only.
```

WHAT NEXT

```
Remove the 'drive' specification from the port parameter definitions in the data
```

```
file.
```

STML-64 (error) File %s: Line %d, the arc %s referred to by TLATCH
qualifier has not been instanced.

DESCRIPTION

```
The arc referred to by 'tlatch' = <arc_name> construct must be instanced before
referring to it.
```

WHAT NEXT

```
Instance the arc referred to by 'tlatch'before using it in 'tlatch' construct.
```

STML-65 (error) File %s: Line %d, The number of output ports in TLATCH
arc and the corresponding edge arc %s do not match.

DESCRIPTION

```
The ports used as output port in the 'tlatch' arc and the corresponding edge delay
arc must be the same.
```

WHAT NEXT

```
Use the same output ports for the 'tlatch' arc and the corresponding edge delay arc.
```

STML-66 (error) File %s: Line %d, Cannot create SHORTED ports before
defining the ports.

DESCRIPTION

```
The 'shorted' port section only comes after the ports used in the 'shorted' ports
are defined.
```

Define the ports that you are 'shorting' before using them.

STML-67 (error) File %s: Line %d, The port %s used in the SHORTED
ports is not defined.

DESCRIPTION

Ports must be defined before using the 'shorted' port construct on the ports that
you are shorting.

WHAT NEXT

Create the ports you want to short before 'shorting' them.

STML-68 (error) File %s: Line %d, Buses of different lengths shorted.

DESCRIPTION

Buses of different lengths cannot be shorted.

WHAT NEXT

Make sure that buses are of the same length while shorting.

STML-69 (error) File %s: Line %d, Port %s repeated twice in SHORTED
ports construct.

DESCRIPTION

Repeating the same port name twice in shorted ports is not allowed.

Remove the repetition.

STML-70 (error) File %s: Line %d, The bus limits declaration (%d:%d) is
  not consistent with its use (%d:%d) for the bus %s.

DESCRIPTION

The bus was declared with limits whose order (start and end limits) are inconsistent with the use.

WHAT NEXT

If the start and end index of a bus is in particular order, the usage of the bus must reflect the same order.

STML-71 (error) File %s: Line %d, The %s clock source pin %s is not defined.

DESCRIPTION

You used a pin as a source for either a master or generated clock, but it was not defined as a port or internal pin.

WHAT NEXT

Either define the generated or the master clock source as a port or internal pin; or if the pin name specified is an error, change the name to reflect the correct port or pin name.

STML-72 (error) File %s: Line %d, The master clock source pin %s is found to be of type %s.

DESCRIPTION

The master for a generated clock can only be an input or inout type. If it is of any other type it must be a generated clock.

Check the port or pin definition of the source pin of the master and change it to one of the allowed types.

STML-73 (error) File %s: Line %d, Generated Clock source pin %s
is of input type.

DESCRIPTION

A direction of the generated clock source pin cannot be input. If it is, an error occurs.

WHAT NEXT

Define generated clock only on output, inout, or internal pins.

STML-74 (error) File %s: Line %d, The %s factor used %d is not a power of two.

DESCRIPTION

The multiplication or division factor must be a power of two. If the factor is not, it is an error.

WHAT NEXT

If the multiplication or division factor is not a power of two, try to model the generated clock with 'edges' and 'edge_shift'.

STML-75 (error) File %s: Line %d, The duty_cycle specified (%f) is not within the limits (0 < duty_cycle <100).

DESCRIPTION

The duty cycle must be within 0 and 100.

Change the duty cycle to be within 0 and 100.

STML-76 (error) File %s: Line %d, The generated clock %s has already been defined.

DESCRIPTION

The generated_clock definition you are trying to define in the data file is already defined. There can be only one definition for a generated clock.

WHAT NEXT

Either change the name of the redefined clock, or remove the definition if it is really a repetition.

STML-77 (error) File %s: Line %d, In the generated clock specification,
  the number of edges (%d) does not equal the number of edge_shifts (%d).

DESCRIPTION

If 'edge_shift' has been specified using edge_shift(), the number of edge_shifts must equal the number of edges specified.

WHAT NEXT

If you want to use edge_shift, specify one edge shift for each edge specified.

STML-78 (error) File %s: Line %d, Expected to find a float value
  for the %s, but found something else.

DESCRIPTION

The value for the attribute was expected to be a float, but something else is found (for example, strings).

Make sure the attribute is a float.

STML-79 (error) File %s: Line %d, non-positive values found for %s.

DESCRIPTION

The argument was expected to be positive, but it is not.

WHAT NEXT

Make the necessary values positive.

STML-80 (error) File %s: Line %d, Expected to find an integer value
  for the %s, but found something else.

DESCRIPTION

The value for the attribute is expected to be an integer, but something else is found (for example, strings).

WHAT NEXT

Make sure that attribute is an integer.

STML-81 (warning) File %s: Line %d, The data defined for
  generated clock '%s' has not been defined in the model file.

DESCRIPTION

The generated clock defined in the data file should be defined in the model file first. Otherwise it is a potential error.

Please define the generated clock in the model file.

STML-82 (error) File %s: Line %d, The '%s' pin %s is not found in the design.

DESCRIPTION

The pin you are using has not been defined in the design.

WHAT NEXT

Define the pin before using it.

STML-83 (error) File %s: Line %d, The generated clock '%s' is being
   redefined.

DESCRIPTION

The generated clock is redefined in this model file. The generated clock is defined elsewhere in the model file with the same name. There can be only one generated clock defintion per generated clock name, per model file.

WHAT NEXT

Have only one generated clock definition per generated clock name, per model file.

STML-84 (error) Unable to open '%s' file - %s.

DESCRIPTION

Unable to open either the data file or model file.

WHAT NEXT

Check the path name of the data or model file in question and look at the search path if the file is present in the search path. If the file is not present in the

search path, update the search path. If the file is present in the search path, perhaps the access permission is not there.

STML-85 (error) File %s: Line %d Arc %s: expected to find '%s' table but it was not found.

DESCRIPTION

You receive this message if the **compile_stamp_model** command does not find the arc RISE_CONSTRAINT or FALL_CONSTRAINT in the Stamp data file. For the following arcs, the following tables are expected:

```
RECOVERY_RISE_CLK_RISE - RISE_CONSTRAINT;
RECOVERY_RISE_CLK_FALL - RISE_CONSTRAINT;
RECOVERY_FALL_CLK_RISE - FALL_CONSTRAINT;
RECOVERY_FALL_CLK_FALL - FALL_CONSTRAINT;
REMOVAL_RISE_CLK_RISE - RISE_CONSTRAINT;
REMOVAL_RISE_CLK_FALL - RISE_CONSTRAINT;
REMOVAL_FALL_CLK_RISE - FALL_CONSTRAINT;
REMOVAL_FALL_CLK_FALL - FALL_CONSTRAINT.
```

WHAT NEXT

Edit your Stamp file to add the required information, then reexecute **compile_stamp_model**. For information about creating Stamp files, see the *PrimeTime Modeling User's Guide*, Chapter 6.

SEE ALSO

compile_stamp_model (2).

STML-86 (warning) File %s, Line %d, Arc %s: expected to find only '%s' table, but also found '%s' table which will be ignored.

DESCRIPTION

For the type of arc that is being defined, found some other table types too.

WHAT NEXT

Other than the expected delay tables found, some other delay tables also presented in the file.

STML-87 (warning) File: %s, Line: %d, Arc: %s Found two edge specifications
  where only one was expected. Ignoring the second edge specification.

DESCRIPTION

For SETUP, HOLD, DELAY, NOCHANGE, PERIOD, and WIDTH only one edge needs to be
specified. If two edges are specified, only the first edge specified is considered.

WHAT NEXT

If the first edge being considered as the triggering edge is incorrect, please
change the file.

STML-88 (warning) File: %s, Design name not specified in the
 MODEL DATA file.

DESCRIPTION

Design name has not been specified in the MODEL DATA file.

WHAT NEXT

Please specify the design name in the MODEL DATA file.

STML-89 (warning) File %s, Line %d: Design name '%s' specified in the
  MODELDATA file (%s) does not match the one in MODEL file '%s'.

DESCRIPTION

There is a discrepancy in the design name between MODELDATA file and MODEL file.

WHAT NEXT

Make sure that the design name in the MODELDATA file and MODEL file match.

STML-90 (warning) File: %s, Design name not specified in the MODEL file.

DESCRIPTION

```
Design name has not been specified in the model file.
```

WHAT NEXT

```
Please specify the design name in the model file.
```

STML-91 (warning) Arc '%s' defined in the stamp data file '%s' has
  not been used in the model file '%s'.

DESCRIPTION

```
Data for an arc has been defined in the model data file, but the same arc has not
been defined in the model file.
```

WHAT NEXT

```
If you need that arc, define the arc in the model file. If the arc is not needed,
remove it from the modeldata file.
```

STML-92 (error) File %s, Line %d: Version %s for MODEL_VERSION illegal.

DESCRIPTION

```
For this release MODEL_VERSION can be only 1.0.
```

WHAT NEXT

```
Change the MODEL_VERSION string to 1.0.
```

STML-93 (error) File %s, Line %d: Version %s for

MODELDATA_VERSION illegal.

DESCRIPTION

For this release MODELDATA_VERSION can be only 1.0.

WHAT NEXT

Change the MODELDATA_VERSION string to 1.0.

STML-94 (information) No timing arcs are defined from or to pin '%s'.

DESCRIPTION

The pin or port does not have any arcs coming in or going out.

WHAT NEXT

If this is a real error please fix it.

STML-95 (Error) File %s, Line %d: The number of bits referred to
  by the two expressions %s, %s are different (%d, %d).

DESCRIPTION

The number of bits the operation performed for the binary operators (!, &, ^) must be equal.

WHAT NEXT

Check if the effective bus widths are the same.

STML-96 (Error) File %s, Line %d: Cannot specify more than one port

for clock in constraint arcs.

DESCRIPTION

The clock port in the constraint arc cannot consist of more than one port.

WHAT NEXT

If you want to constrain a port for different clocks, create separate arcs from each
clock port.

STML-97 (Error) File %s, Line %d: Different attribute types mixed in
the list.

DESCRIPTION

Different attribute types cannot be mixed in a list attribute. In a list, all the
attributes have to be of the same type.

WHAT NEXT

Make the attributes the same type in the list.

STML-98 (error) File %s, Line %d:
The STAMP language reserved %s attribute '%s'
has been defined as type '%s', but is used with a value
of type '%s'.

DESCRIPTION

You receive this message because the data type of the attribute value that you are
using in your STAMP model files is wrong. To use a reserved attribute in STAMP and
compile it, you need to define its value to be the same type as the application-
defined lib, lib_cell, or lib_pin attribute, or one of these attributes defined by
STAMP language:

```
    k_process_cell_rise
    k_temp_cell_rise
```

```
k_volt_cell_rise
k_process_cell_fall
k_temp_cell_fall
k_volt_cell_fall
k_process_rise_transition
k_temp_rise_transition
k_volt_rise_transition
k_process_fall_transition
k_temp_fall_transition
k_volt_fall_transition
original_pin
```

WHAT NEXT

Check and correct the attribute definitions in the STAMP files, then try compile the
STAMP again.

STML-99 (error) File %s, Line %d:
The user attribute '%s' for %s has already been defined as type '%s', but is used as '%s'.

DESCRIPTION

The data type for the attribute has already been defined to be of one type in the
STAMP files, but is used as a different type. For example, the attribute is defined
to be of type string, but is used as an integer.

WHAT NEXT

Check and correct the attribute definitions in the STAMP files, then try compile the
STAMP again.

STML-100 (warning) File %s, Line %d: The attribute '%s' is used as a list, but is not defined to be of list type.

DESCRIPTION

The attribute was not defined to be a list but is used as a list.

WHAT NEXT

Check the attribute definition and change the usage accordingly.

STML-101 (warning) File %s, Line %d: The attribute '%s' is defined to
  be of list type, but is not used as a list type.

DESCRIPTION

The atribute is defined to be of list type but is not used as a list type.

WHAT NEXT

Check the attribute definition and change either one of definition/usage to make
both of them consistent.

STML-102 (error) File %s: The gate_type %s referred to in line %d is
  not a valid type.

DESCRIPTION

Currently, supported gate types are DOMINO_N_FOOTED, DOMINO_N_FOOTLESS,
DOMINO_P_FOOTED, DOMINO_P_FOOTLESS, DOMINO_LATCH, DOMINO_RETAIN, DOMINO_FLOP.

WHAT NEXT

Correct the gate_type and try again.

STML-103 (error) File %s: Cannot use COND with SDF_COND for
  an arc, line %d.

DESCRIPTION

Conditions on a delay/constraint arc can be specified using either the COND
construct or by using the SDF_COND with WHEN construct, but not both.

WHAT NEXT

Choose one form of defining conditional arcs and delete the other.

STML-104 (error) File %s: Line %d, Arc %s
One of RISE_TRANSITION/FALL_TRANSITION/ TRANSITION
has to be specified for this arc.

DESCRIPTION

```
For 'posedge' and 'negedge' arcs, one of rise and fall delay tables must be
specified.
```

WHAT NEXT

```
For 'posedge' and 'negedge' arcs specify at least one of cell_rise and cell_fall.
```

STML-105 (warning) File %s: Line %d, Arc %s
One of RISE/FALL TRANSITION or RISE/FALL PROPAGATION not specified
for this arc. The missing data will be replaced by the data from the opposite TRANSITION/PROPAGATION.

DESCRIPTION

```
For 'posedge' and 'negedge' arcs, if one of rise/fall data is missing then the
missing data is copied from the existing data. For example, if a 'posedge' arc is
defined with only CELL_RISE, then the CELL_FALL data will be taken from the
CELL_RISE data. The same holds true in case of RISE/FALL_TRANSITION.
```

WHAT NEXT

```
Currently the PrimeTime timing engine cannot handle 'posedge' and 'negedge' arcs
that are single transition (rise only or fall only). Hence when compiling such arcs
from STAMP, they are forced to have data for both polarities by replicating the
values.
```

STML-106 (error) Option -remove_internal_arcs is no longer

supported.

DESCRIPTION

```
Option -remove_internal_arcs is no longer supported for the compile_stamp command.
```

WHAT NEXT

```
If the STAMP model is generated via the extract_model command and has internal arcs,
then use extract_model -remove_internal_arcs to remove the internal arcs from STAMP
model. Then compile with complie_stamp. If you are hand-creating STAMP model and you
do not want the compiled stamp model to have internal arcs, please remove all
internal arcs manually from the stamp model file.
```

STML-107 (error) File %s: Incorrectly specified a delay arc for the arc label '%s' on or before line %d that uses constraint arc data.

DESCRIPTION

```
You receive this message if compile_stamp_model, while reading a Stamp file, detects
an arc that is first defined as a delay arc and then used as a constraint arc. You
must define and use an arc either as a delay arc or as a constraint arc; it cannot
be both.
```

WHAT NEXT

```
Edit your Stamp file to correct the errors. For information about creating Stamp
files, see the PrimeTime Modeling User Guide, Chapters 5 and 6.
```

SEE ALSO

compile_stamp_model (2).

STML-108 (error) File %s: Line %d, Arc %s the expected %s table is not found in the data file.

DESCRIPTION

```
For 'POSEDGE' and 'NEGEDGE' specified for constraint arcs, the first edge
specification is for data and the second edge spec is for clock. For example, a
```

SETUP(POSEDGE, NEGEDGE) arc means the rising data is checked against falling clock, so a RISE_CONSTRAIN table is required in the data file. However, if you only specify one edge in the arc definition, it only means for the clock edge and both transitions for the data will be checked. For example, a hold arc HOLD(POSEDGE) means both the rising and the falling edge of the data will be checked against the falling edge of the clock, so both RISE_CONSTRAINT and FALL_CONSTRAINT tables are expected, or you can simply use CONSTRAINT if the timing numbers are the same for both edges.

WHAT NEXT

Please fix the problems identified for the arc and try compile again.

STML-109 (error) Generated clock '%s' is defined in file %s, but thers is no data defined for it in file %s.

DESCRIPTION

The generated clock that is defined in the model file is not defined in the data file.

WHAT NEXT

Generated clocks that are defined in the model file must be also be defined in the data file. Add the data definition for the generated clock in the data file before compile.

STML-110 (error) File %s:
Line %d, the conditions defined for mode %s are either not mutually exclusive or not complete.

DESCRIPTION

The conditions you defined for the mode values of the mode group must be mutually exclusive and must be complete as a set. In another words, there should be exactly one mode in the mode group that can be enabled under the specified conditions, given any combinations of variable values in the condition expressions. In addition, you should not include modes that have conditions with modes that do not have conditions in one mode group.

WHAT NEXT

Check the conditions defined for the modes.

STML-111 (error) File %s, Line %d: the table values are missing.

DESCRIPTION

A table must have values defined by VALUES.

WHAT NEXT

Please define the table values for the arc before compile.

STML-112 (error) File %s, Line %d: syntax error at or before token %s, '%s' is expected.

DESCRIPTION

A syntax error has been found during compile.The syntax error must be fixed for successful compile.

WHAT NEXT

Please fix the syntax error and try compile again.

STML-113 (error) File %s, Line %d: syntax error at or before token %s,
 one of the port direction specifiers '%s'
 is expected.

DESCRIPTION

A syntax error has been found during compile.The syntax error must be fixed for successful compile.

WHAT NEXT

Please fix the syntax error and try compile again.

STML-114 (warning) File %s, Line %d: skew check is not currently supported.

DESCRIPTION

```
The skew check is not supported.
```

WHAT NEXT

```
Please remove the arc for skew check and try compile again.
```

STML-115 (warning) File: %s, Line: %d, found unexpected "CLKGAT" attribute defined for arc %s. Ignoring the attribute...

DESCRIPTION

```
The CLKGAT attribute is to flag the constraint arcs as clock_gating checks. It is
valid only for SETUP, HOLD, and NOCHANGE arcs. It will be ignored if defined for any
other types of arcs.
```

WHAT NEXT

```
Please correct the arc in the STAMP file before using stamp compiler.
```

STML-116 (error) Found %s in the "when" expression '%s' defined for mode value '%s' in group '%s'.

DESCRIPTION

```
The conditional expression defined for the mode is incorrect. It does not comply
with the syntax definition for logical "when" expressions, or it refers to some
undefined objects.
```

WHAT NEXT

```
Please correct the specified error and try compile again.
```

STML-117 (error) File: %s, Line %d, found %s in the "when" expression '%s' defined for arc '%s'.

DESCRIPTION

```
There is either syntax error in the specified conditional expression, or the
expression refers to some undefined port/pins in the design.
```

WHAT NEXT

```
Please correct the specified error and try compile again.
```

STML-118 (error) Found mixed conditional expressions defined with both
 WHEN/SDF_COND and COND syntax for the modes of mode group '%s'.

DESCRIPTION

```
All the conditional expressions defined for a set of mode values within one mode
group should be either the old COND syntax or the new WHEN/SDF_COND syntax. You
cannot mix them in one mode group.
```

WHAT NEXT

```
Please choose one syntax for all the mode values. The new WHEN/SDF_COND syntax is
recommended.
```

STML-119 (warning) Found conditional expression in mode/arc defined by the old COND
 syntax. WHEN/SDF_COND syntax is recommended.

DESCRIPTION

```
To support the analysis of conditional modes/arcs more efficiently, it is
recommended to use the WHEN/SDF_COND syntax when defining the conditional mode and
timign arcs.
```

Please use the WHEN/SDF_COND syntax if possible.

STML-120 (warning) Port '%s' appears to be unbussed.

DESCRIPTION

You receive this message to warn you that **compile_stamp_model** has detected a port in your Stamp file that appears to be part of a bus, but has not been declared as a bus.

For example, the following declaration creates three ports, but no bus.

```
        INPUT A[2];
        INPUT A[1];
        INPUT A[0];
```

By contrast, the following declaration creates a port bus named A, and 3 ports, A[2], A[1], and A[0].

```
INPUT A[2:0];
```

This is a warning to help you identify places where you might have omitted bus declarations. Missing buses can cause problems later when you try to link the design.

WHAT NEXT

This is a warning message only; no action is required on your part. However, if the ports should be bussed, edit your Stamp file to add the correct syntax for a bus declaration, then reexecute **compile_stamp_model**. For information about creating Stamp files, see the *PrimeTime Modeling User Guide*, Chapters 5 and 6.

SEE ALSO

compile_stamp_model (2).

STML-121 (error) File %s, line %d: %s.

DESCRIPTION

There are some problems with the RELATED_OUTPUT defined for the timing arc as indicated.

Make sure that the RELATED_OUTPUT port: 1) is defined only once; 2) does not refer
to an INPUT port; 3) is not the same as either of the 2 end ports of the arc; 4) is
not defined for a WIDTH, or PERIOD arc.

STML-122 (warning) File %s, line %d: %s.

DESCRIPTION

A RELATED_OUTPUT port has been defined for the indicated timing arc in the STAMP
model file, but no delay tables defined for the timing arc in the STAMP data file
refers to the related output port, so it is not needed.

WHAT NEXT

Please make sure that the RELATED_OUTPUT port is really not needed.

STML-123 (error) File %s, line %d: DRIVE %s refers to related_ouput_load.

DESCRIPTION

The tables defined for the DRIVE arc refers to related_output_load. This is not
supported in timing analysis.

WHAT NEXT

Please make sure that the DRIVE arc does not depend on any related_output load.

STML-124 (error) File %s, line %d: %s has already been defined for arc %s.

DESCRIPTION

The indicated table field has been defined more than once for the timing arc.

WHAT NEXT

Please correct the error and compile again.

STML-125 (error) File %s, line %d: in the table for arc '%s', %s is defined without %s.

DESCRIPTION

You have to define the required table fields before defining the indicated one. For example, INDEX_2 and VARIABLE_2 have to be defined before you can define INDEX_3 and VARIABLE_3.

WHAT NEXT

Please correct the table definition and compile again.

STML-126 (error) File %s, Line %d: the VARIABLE_3 must be related_output_capacitance.

DESCRIPTION

The VARIABLE_3 can only be related_output_capacitance in a delay table.

WHAT NEXT

Please correct the definition of the table in the STAMP data file and try compile again.

STML-127 (warning) File %s: Line %d, Port %s expected to be of
   direction INOUT/OUTPUT/TRIOUT but found to be %s.

DESCRIPTION

The end_port for delay arcs are expected to be either triout, inout, or output type. If the end_port is anything other than one of these, it is suspectable and please verify.

WHAT NEXT

Make sure the end port of the delay arcs are of direction triout, output, or inout. If not, please verify that the directions and the arcs are really correct.

STML-200 (error) File %s: Line %d, the arc '%s' referred to by the DELAY
  qualifier is not defined.

DESCRIPTION

You receive this message if **compile_stamp_model**, while reading a Stamp file, detects an arc that is referred to by the DELAY = <arc_name> construct, but has not been defined. The arc must be defined before the definition of the RETAIN arc.

WHAT NEXT

Edit your Stamp file to correct the error. If the arc referred to by the DELAY qualifier is not defined, add the definition. If the definition of the missing arc DELAY arc is after the RETAIN arc, reverse the order of the two definitions. For information about creating Stamp files, see the *PrimeTime Modeling User Guide*, Chapters 5 and 6.

SEE ALSO

compile_stamp_model (2).

STML-201 (error) Cannot compile multiple data files in LIB format.

DESCRIPTION

You receive this message from **compile_stamp_model** if **-data-files** has more than one data file in its list and the **-formats** option has *lib*. The **compile_stamp_model** command cannot compile multiple stamp data files to a single library file.

WHAT NEXT

Either choose to output in DB format, or compile each data file separately.

SEE ALSO

compile_stamp_model (2).

STML-202 (error) Cannot expand busses for LIB format

DESCRIPTION

You receive this message from **compile_stamp_model** if you sepcify *-expand_buses* in conjunction with the *lib* output format. The **compile_stamp_model** command cannot expand busses when writing liberty format.

WHAT NEXT

Either choose to output in DB format, or do not expand the busses by removing *-expand_buses* from the command line.

SEE ALSO

compile_stamp_model (2).

STML-203 (error) The LIB format requires the -library_cell option

DESCRIPTION

You receive this message from **compile_stamp_model** if you do not sepcify *-library_cell* in conjunction with the *lib* output format. The **compile_stamp_model** requires the *-library_cell* option whenever writing liberty format.

WHAT NEXT

Either choose to output in DB format, or add the *-library_cell* option to the command line.

SEE ALSO

compile_stamp_model (2).

STML-204 (error) The -update option cannot be used when writing liberty format

DESCRIPTION

You receive this message from **compile_stamp_model** if you specify the *-update* option

in conjunction with writing liberty format. The **compile_stamp_model** cannot update a
liberty format file.

WHAT NEXT

Either choose to output in DB format, or remove the *-update* option from the command
line.

SEE ALSO

compile_stamp_model (2).

SVR-1 (error) Unable to open file '%s'.

DESCRIPTION

The Verilog file you tried to open does not exist or has incorrect permissions.

WHAT NEXT

Verify the file name and permissions.

SVR-2 (information) Verilog read failed.

DESCRIPTION

This is a summary informational message indicating that the Verilog file could not be read. Previous error messages will point you at the actual problem source. There are two types of syntax errors: a real violation of Verilog syntax, or reading a Verilog file that has non-structural or other unsupported constructs with this reader.

WHAT NEXT

Review previous error messages. Then, either correct the actual Verilog syntax errors in the file and reread the file, or use a Verilog reader that supports the constructs that are flagged as syntax errors.

SVR-3 (error) Unsupported construct '%s' at line %d in '%s'.

DESCRIPTION

The reader detected an unsupported construct. Not all unsupported constructs are trapped in this way. Many show up as more simple syntax errors.

WHAT NEXT

Either correct the error by removing the construct or use a Verilog reader that supports the construct.

SVR-4 (error) Expected %s but found '%s' at line %d in '%s'.

DESCRIPTION

This message covers a wide variety of syntax errors. A token was expected, but something else was found. For example, after a module formal list, a close paren is expected, but if it is omitted and a semicolon is found, this message appears.

This can be an indication of a real syntax error. It is also possible for this message to be used when Verilog constructs, which are not supported by this reader, are encountered.

WHAT NEXT

Review the line number reported in the message and determine if a real syntax error needs to be corrected or if the file contains unsupported constructs.

SVR-5 (error) Expected identifier after %s at line %d in '%s'.

DESCRIPTION

An identifier is expected after the token shown and something else was found.

WHAT NEXT

Review the line number reported in the message and determine if a real syntax error needs to be corrected or if the file contains unsupported constructs.

SVR-6 (error) Premature end-of-file reading '%s'.

DESCRIPTION

The reader detected end-of-file before it was expected. For example, an end-of-file within a module construct before the endmodule would cause this message to be raised.

WHAT NEXT

Correct the error and reread the file.

SVR-8 (error) Port '%s' is not defined in module terminal list
but is defined in an %s statement
at line %d in '%s'.

DESCRIPTION

```
While processing an input, output, or inout statement, a port was found which did
not exist anywhere in the module terminal list.
```

WHAT NEXT

```
Correct the module terminal list or remove the port wire from the appropriate input/
output/inout declaration.
```

SVR-9 (error) Duplicate wire/tri/wand/wor declaration for '%s'
at line %d in '%s'.

DESCRIPTION

```
The named wire was found in a wire, tri, wand, or wor statement. However, the wire
was already declared in a similar statement.
```

WHAT NEXT

```
Ensure that each wire is only declared once.
```

SVR-10 (error) Illegal assignment %s
at line %d in %s.

DESCRIPTION

```
An assign statement (or wire statement with inline assignment) has one of several
errors:
```

```
• Nothing is on the left side of the '='.
• The left side of the assignment contains an undeclared net or unexpected
characters.
• The right side of the assignment contains an undeclared net or unexpected
characters.
```

```
Note that the following syntax for assign is not supported:
```

```
assign z = ( a );
```

Use of parentheses is considered non-structural.

WHAT NEXT

Correct the syntax error and reread the file.

SVR-11 (error) Cannot assign to constant%s
 at line %d in %s.

DESCRIPTION

There is a constant on the left side of an assignment, which is not allowed.

WHAT NEXT

Correct the error, and reread the file.

SVR-13 (error) Number of ports of instance is inconsistent with other instances
 at line %d in %s.

DESCRIPTION

All ordered (non-name based) instances of a design must have the same number of
ports. The first such instance sets the number. The following example would raise
this error.

```
ND2 i1 (a, b, c);
ND2 i2 (d, e);
```

The first instance has 3 ports, whereas the second has only 2. It's possible that
the second instance is missing a comma. For example,

```
ND2 i1 (a, b, c);
ND2 i2 (d, , e);
```

WHAT NEXT

Examine the instances to determine which is correct. One might be missing a comma.

SVR-14 (error) Indexing into non-array '%s' is not allowed at line %d in %s.

DESCRIPTION

A connection has a wire or port with bus notation, and the wire or port was not declared as a bus. For example, the following would raise this error.

```
input A;

ND2 i1 (A[0], b, c);
```

WHAT NEXT

Determine if the wire or port declaration or usage is correct.

SVR-15 (error) Width of port %s (%d) is inconsistent with other instances (%d) at line %d in %s.

DESCRIPTION

The first instance of a design's port sets its width. The width is inferred from the connections to that port. This error indicates, and a subsequent instance has, a different width for a particular port. The following example would raise this error.

```
D1 i1 (A[15:0], b, c);
D1 i2 (A[17:16], e, f);
```

WHAT NEXT

Examine the various instances of the design to see which one is correct.

SVR-16 (error) Constant width overflow at line %d in %s.

DESCRIPTION

The constant is too large to be represented. Constants cannot exceed 32K bits.

Correct the error and reread the file.

SVR-17 (error) Decimal constant must have 32 bits or fewer at line %d in %s.

DESCRIPTION

Decimal constants are restricted to 32 bits. The number specified exceeds that limit.

WHAT NEXT

Correct the error and reread the file.

SVR-18 (error) Slice direction [%d:%d] does not match array direction at line %d in %s.

DESCRIPTION

An array (bus) was declared either ascending (like A[0:3]) or descending (like A[3:0]). The reference to this array is inconsistent with the way it was declared. For example, if the declaration is A[3:0], a reference like A[0:1] would raise this error.

WHAT NEXT

Correct the error and reread the file.

SVR-19 (error) Index range [%d:%d] is not within bounds [%d:%d] at line %d in %s.

DESCRIPTION

Some or all of the array (bus) indecies of the reference are out of range of the declaration. For example, if the bus was declared A[15:0], A[31:0] would raise this

error, because indecies 31 down to 16 are out of bounds.

WHAT NEXT

Correct the error and reread the file.

SVR-20 (error) Non-terminated comment starting at line %d of '%s'

DESCRIPTION

The reader detected end-of-file in the middle of a C-style comment.

WHAT NEXT

Go to the line number mentioned, and find where the comment should be terminated.

SVR-21 (information) %s converted to a wire with no special attributes
 at line %d in %s

DESCRIPTION

The verilog constructs wand, wor, and tri are converted to a simple wire with no special attributes. This is just an informational message.

WHAT NEXT

No action.

SVR-22 (error) Duplicate instantiation of '%s' (first instance at line %d)
 at line %d in %s

DESCRIPTION

A duplicate instance name was found. The line number of both the duplicate and the original are shown.

SVR-23 (error) Duplicate module '%s' (first occurrence at line %d)
 at line %d in %s

DESCRIPTION

A module is defined more than once in the file. The line number of both the
duplicate and the original are shown.

WHAT NEXT

Rename one of the duplicates.

SVR-24 (warning) Ignored '%s' construct
 at line %d in '%s'.

DESCRIPTION

This message covers a variety of constructs which are ignored by the native verilog
reader, including **specify**, **parameter**, and so on.

This can be an indication of a real problem, especially in the case of **parameter**.
The native verilog reader does not support parameters, so if the parameter is being
used, other syntax errors will follow. If the parameter is just defined but not
used, then ignoring it will be sufficient.

WHAT NEXT

In almost all cases, no action is necessary. If you have real parameters in your
netlist, you must use a different verilog reader which understands parameters.

SVR-25 (error) Global reference to '%s' not valid in this context

at line %d in '%s'.

DESCRIPTION

Global references are inter-module references, for example, a connection to a wire
in a different module like 'global.gnd'. Although this is part of the verilog
language, the native verilog reader has very limited support for global references.
They can only be used in connections - they cannot be used in assign statements,
tran statements, and so on.

This error is generated when a global reference is used in an unsupported context.

WHAT NEXT

For any usage of global references other than in a connection, you need to use a
different verilog reader.

SVR-26 (error) Port '%s' has no defined direction (input/output/ inout)
 in module %s at line %d in file %s.

DESCRIPTION

You received this message because the named port was defined in the module terminal
list, but did not appear in an input, output, or inout statement. The line number
reported is the line number in the module statement where the port is referenced.

WHAT NEXT

Add an appropriate input, output, or inout statement for the named port.

SVR-27 (error) Duplicate declaration of port '%s' in instance '%s'
 at line %d in '%s'.

DESCRIPTION

You received this message because the named port was defined twice in the terminal
list of the given instance, as in the following example:

```
AN2 i0 (.A(a), .A(b), .Z(z));
```

Remove or replace the duplicate port.

SVR-28 (warning) Number %s is too big. It will be truncated to 32 bits
 at line %d in '%s'.

DESCRIPTION

When reading a bus (array) declaration or instance, the msb or lsb was bigger than 32 bits, and was truncated. For example:

```
BOX u1 (.A(a[36'hF00000001:0]), .Z(z));
```

The range of a will be truncated to 1:0.

WHAT NEXT

Verify that the netlist is correct. This could be a typo.

SVR-31 (error) Expected %s '%s' to be declared as a range
 at line %d in '%s'.

DESCRIPTION

A port has been declared in an input/output/inout statement as a scalar, but was referenced in the module terminal list using a range. In this example:

```
module test (a, b[0], z);
input b;
```

port 'b' is either declared incorrectly in the input statement, or it is referenced incorrectly in the module statement.

WHAT NEXT

Correct one of the errors.

SVR-32 (error) Range of %s port '%s' (%d:%d) does not cover the range required by the module statement (%d:%d) at line %d in '%s'.

DESCRIPTION

A port has been declared in an input/output/inout statement as a range, but the range was inadequate to cover the range required by references to it from the module statement. In this example:

```
module test ({a, b[2:1]}, b[0], z);
input [1:0] b;
```

the module statement requires a range of 2:0, but the input statement declares 1:0. Either the module statement or the input statement is incorrect.

WHAT NEXT

Correct one of the errors.

SVR-33 (warning) Port '%s' (%s) has a different direction than other ports in module formal %d (declared line %d); %s statement at line %d in '%s'.

DESCRIPTION

A port has been declared in an input/output/inout statement, but its usage in the module statement creates a bus with mixed directions. For example:

```
module test ({a, b}, z);
output b, z;
input [1:0] a;
```

Port number 1 of the module statement has both inputs and outputs. The first **output** statement sets the direction as output. When the input statement is processed, this warning will be issued, since 'a' and 'b' are concatenated in the first module port, and they are different directions. The first port in the concatenation defines the direction for the entire bus (in this case, an input).

```
Verify that the ports are declared correctly, and consider that the netlist created
may not have the port directions that you expect.
```

SVR-34 (error) Slice direction for '%s' [%d:%d] in module port %d ('%s')
 does not match declared array direction
 at line %d in '%s'.

DESCRIPTION

```
A port has been declared in an input/output/inout statement as an array with a
particular order, like n:0 or 0:n. Its usage in the given port in the module
statement is inconsistent with that order. For example:
```

```
module test ({a[0:1], b}, z);
input [1:0] a;
input b;
output z;
```

```
Port number 1 of the module statement references a[0:1], but 'a' is declared 1:0.
Either the module statement or the input statement is incorrect.
```

WHAT NEXT

```
Correct one of the errors.
```

SVR-35 (error) Port wire '%s' was never declared in an input/ output/inout
 statement in module %s in file %s.

DESCRIPTION

```
A port in the module statement references a wire which was never declared in an
input/output/inout statement. For example:
```

```
module test ({a[0:1], b}, z);
input [1:0] a;
output z;
```

Port number 1 of the module statement references 'b', but 'b' was never declared.
Either the module statement or the input statement is incorrect.

WHAT NEXT

Correct one of the errors.

SVR-37 (warning) Port number %d of module '%s' was renamed to '%s'
 at line %d in '%s'.

DESCRIPTION

A port has been found in the module terminal list which needs to be renamed. Ports
will be renamed if they are explictly repeated, or if they are a single bit of a
bus. For example, in this module statement:

module test (a, b[0], a, {a,b});

The first port will be named 'a'. The second port will be renamed Port2. The third
port will be renamed Port3 because 'a' is already in use. Similarly, the fourth port
will be renamed Port4, again because 'a' is already in use. In case one of these
generated names is already in use, the Verilog reader will continue to append the
port number until a free port name is found.

WHAT NEXT

No action necessary.

SVR-40 (error) Could not open temp file in '%s'

DESCRIPTION

While reading Verilog, it was necessary to create a temporary file, and the file
could not be opened. This could be due to file permissions on the directory,
incorrect directory, and so on.

WHAT NEXT

Verify that you have access to the given directory. If necessary, change the

directory as directed by the application.

SVR-41 (error) while writing to temp directory '%s': %s

DESCRIPTION

An error occured while writing to a temporary file in the given directory. This could be due to insufficient space on the disk, or other disk errors.

WHAT NEXT

Use a different temporary directory.

SVR-50 (error) %s

DESCRIPTION

A syntax error occurred while parsing the Verilog file during the preprocessor phase. The message specifies where the error appeared and why it was issued.

WHAT NEXT

Action based on the text of the message.

SVR-51 (error) End of file seen before %s block begun at line %d was ended

DESCRIPTION

During preprocessing, a comment or directive was found which crossed the end of file boundry, indicating it wasn't terminated appropriately. This problem likely involves an unbalanced "/*", which will need a terminating "*/", or an ifdef without a terminating endif.

WHAT NEXT

For run-on comments, examine the lines immediately after the one specified in the error. Mark the boundry between code and comment with a terminating "*/".

For (preprocessor) directives, its very likely an `ifdef or `else was not completed
with an `endif. Determine what code should fit within the `ifdef, and end it with an
`endif.

SVR-52 (error) 'include' directive requires a filename enclosed in double quotes
 %s

DESCRIPTION

The Verilog preprocessor found a missing or misformed include filename. Here is an
example of the correct usage of `include:

`include "myfile.v"

WHAT NEXT

Provide the filename, if missing.

Preface the filename with a double-quote ("), and place another double-quote after
the last character in the filename.

SVR-53 (error) Recursive file inclusion detected for file "%s"

DESCRIPTION

While preprocessing the Verilog file, a circular dependency was found in the use of
an "`include" directive. This error is issued to prevent a file from including
itself in an endless loop. Breaking the need for an include loop will avoid
triggering this error.

A file that directly includes itself most likely meant to include another file with
a similiar name.

WHAT NEXT

Examine the need for the nested "`include". Most likely, several files all depend on
each other. The dependencies should be split up so that one file does not depend on
any of the others. This can be achieved by moving needed code or `defines to one
central file. When one file no longer depends on the others, the corresponding
`include(s) can be removed from that file. This should break the `include loop and
avoid this error.

SVR-54 (error) Unable to open file '%s' included by the 'include' directive %s

DESCRIPTION

The Verilog preprocessor was unable to open a file specified in an "`include"
directive. This is most likely caused by the file being outside of the search path.
This error is also triggered if the file permissions prohibit read access.

WHAT NEXT

If the file exists in the current directory, ensure that "." is present in the
search path.

For files in other directories, add the directory to your search path.

Permissions problems can be ruled out by trying to view the file in an editor.
Errors of this variety are not specific to Verilog.

SVR-55 (error) Mismatched directive %s

DESCRIPTION

The Verilog preprocessor found a compiler directive used with incorrect coupling.
For example, an "`endif" is used without a corresponding "`ifdef" before it.

WHAT NEXT

Delete the mismatched directive or add the missed one.

SVR-57 (warning) Macro %s is redefined %s

DESCRIPTION

The Verilog preprocess detected a macro redefinition. The same macro name is
provided two different definitions, leading to a single macro name having different
meanings in separate parts of the file. Although not an error, this is a potentially
hard to find and confusing problem.

WHAT NEXT

If the duplicate macro definition was accidental, provide a different name for one
of the usages.

If the duplicate usage is intentional, this warning can be avoided by performing an `undef of the macro name before each duplicate definition.

TIM

TIM-001 (Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

DESCRIPTION

```
No timing arcs exist between these pins of the cell. Therefore, we cannot time
between them. We will either report no paths or for unmapped logic, assume 0.
```

WHAT NEXT

```
Fix the library to create the proper timing arcs.
```

TIM-002 (information) Timing loop detected.

DESCRIPTION

```
The design contains at least one timing loop. This message is followed by a list of
pins on one loop, and then messages indicating which timing arcs are being
automatically disabled to break the loop.
```

WHAT NEXT

```
To view all timing loops in your design, use report_timing -loops. To manually break
loops, use disable_timing.
```

TIM-003 (warning) Disabling timing arc between pins '%s' and '%s' on cell '%s'%s

DESCRIPTION

```
This message is displayed when timing arcs are disabled by tool to break
combinational feedback loops. It is not displayed for arcs that are manually
disabled with the set_disable_timing command.
```

WHAT NEXT

```
If you want to manually break a timing loop, examine the design to see why there is
combinational feedback and then choose a different point at which to break the loop.
```

To do this, use the **set_disable_timing** command instead of letting the tool automatically break the loop.

EXAMPLE MESSAGE

Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'u10'to break a timing loop (TIM-003)

TIM-004 (error) The pin '%s' which is a derived clock pin is either in a loop or is in the fanout of two clock sources

DESCRIPTION

The derived clock pin is either in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network or can you have a derived clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the derived clock is in the fanout of two clock sources, try to isolate it or use internal clocks.

TIM-005 (information) Invalidating all auto-disabled timing arcs.

DESCRIPTION

Some arcs have been enabled, forcing the tool to do loop detection from scratch. Therefore, the tool enables all auto-disabled arcs.

WHAT NEXT

To view all timing loops in your design, use **check_timing -loops**. To manually break the loops, use **disable_timing**.

TIM-006 (error) report_delay_calculation is not enabled for library '%s'.

DESCRIPTION

The delay calculation report shows detailed performance information about library

cells. By default, cell delay reporting is disabled. The technology library vendor
can enable delay calculation for a library by specifying the following in the **.lib**
source:

```
library_features(report_delay_calculation);
```

WHAT NEXT

Contact your library vendor to request a library with this feature enabled.

TIM-007 (error) The master clock %s has %d edges in a period. Cannot
do frequency multiplication.

DESCRIPTION

If the master clock of a generated clock has more than 3 edges in a
 period, you cannot generate a frequency multiplied clock from that master
 clock.

WHAT NEXT

You can use -edges option to generate the clock.

TIM-008 (error) The generated clock '%s' is in the fanout of clock
source %s.

DESCRIPTION

A generated clock can only be in the fanout of a clock source from which it is
generated. Here the generated clock is found to be in the fanout of some other clock
source.

WHAT NEXT

Generate this clock from a clock in whose fanout it is in.

TIM-009 (error) Generated clock '%s' is not in the fanout of its

master clock.

DESCRIPTION

```
The generated clock is not in the fanout of the master clock with respect to which
it has been defined. A generated clock must be in the fanout of its master clock.
```

WHAT NEXT

```
Please check the design and redefine the generated clock to be in the fanout of its
master clock.
```

TIM-010 (warning) The generated clock '%s' has not been expanded,
 please create its master clock.

DESCRIPTION

```
A generated clock will not expand if the master clock from which it is generated has
not been created.
```

WHAT NEXT

```
Please create the master of the generated clock.
```

TIM-011 (error) The following generated clocks '%s' form a loop.

DESCRIPTION

```
The generated clock listed are defined in a loop. A loop of generated clocks is
formed in that there is a circular dependency of generated clock to master clock.
```

```
For example, if A and B are generated clocks, and A is generated from B, and B is
generated from A, there is a circular dependency.
```

WHAT NEXT

```
Remove cirular dependency in the generated clock sources.
```

TIM-012 (error) The master of the generated clock '%s' is not

connected to any clock source.

DESCRIPTION

```
The master clock of a generated clock must be either a clock source, or must be
connected to a clock source. If it is neither, it is an error.
```

WHAT NEXT

```
Make sure that the master source from which the clock is generated is a clock source
or is connected to a clock source.
```

TIM-013 (information) Found %d generated clock master pins that are not connected to clock sources.

DESCRIPTION

```
It gives a summary of the number of generated clock master pins that are not
connected to clock sources.
```

WHAT NEXT

```
For a more detailed description of which generated clock master pins are not
connected to any source, do check_timing -with -verbose option.
```

TIM-014 (information) Found %d loops in the generated clock network.

DESCRIPTION

```
This message gives a summary of the number of loops in the generated clock network.
If there is a circular dependency of generated clock sources and its master, there
will be a loop in the generated clock network.
```

WHAT NEXT

```
To get a more detailed description of where the generated clock loops are, use
check_timing -verbose.
```

TIM-015 (Error) The -edges spec of generated clock '%s' has

edge number
 less than 1, the edge number should be from 1 up.

DESCRIPTION

The -edge specification in creat_generated_clock command should use edge number of
the master clock which should be from 1 up. Zero or negative number are not allowed.

WHAT NEXT

Change your -edge spec in create_generated_clock coommand.

TIM-016 (Error) In the -edge specification of create_generated_clock
 '%s', the edge numbers must be in increasing order.

DESCRIPTION

In the -edge specification of a create_generated_clock command, the edge numbers
specified must be in increasing order.

WHAT NEXT

Check the -edge spec in create_generated_clock command and edge numbers increasing.

TIM-017 (warning) The master source of the generated clock '%s' is not known. Ignoring generated clock '%s'.

DESCRIPTION

You receive this warning because you did not specify the master clock source of the
named generated clock. The master clock of a generated clock must be a specified
clock source or be connected to a clock source. Otherwise, this error occurs.

WHAT NEXT

Make sure that the master source from which the clock is generated is a clock source
or is connected to a clock source. See the man page for the **create_generated_clock**
command.

TIM-018 (warning) The source of the generated clock '%s' is not known. Ignoring generated_clock '%s'.

DESCRIPTION

You receive this warning because you did not specify the source of a generated clock. The source of a generated clock can be a list of ports or pins.

WHAT NEXT

Make sure that the generated clock has a source object. See the man page for the `create_generated_clock` command.

SEE ALSO

`create_generated_clock` (2).

TIM-019 (warning) Ignoring incorrectly specified library generated_clock '%s' in library cell '%s/%s'.

DESCRIPTION

You receive this warning because the library generated clock description does not have complete specification for creating the derived waveform. A generated_clock must have a 'master_pin', source 'clock_pin', and specification for 'divide_by' or 'multiply_by' or 'edge_spec'.

WHAT NEXT

Fix the description in the library to completely specify the generated_clock.

SEE ALSO

`create_generated_clock` (2).

TIM-020 (Error) '%s' is not a legal value for '%s'. The value

defaults to '%s'.

DESCRIPTION

You have specified an invalid value for the variable. Therefore, the default value
described will be used.

WHAT NEXT

If you do not want the default value, please specify a valid value for this
variable.

TIM-021 (warning) The generated clock '%s' is being removed because the pin '%s' has been deleted and the clock no longer has a %s.

DESCRIPTION

Generated clocks require a master_pin and at least one clock source. If either of
these is deleted, then the generated clock is deleted as well.

WHAT NEXT

Create a new generated clock with the same name using remaining pins.

SEE ALSO

create_generated_clock (2) **remove_cell** (2).

TIM-052 (warning) A non-unate path in clock network for clock '%s'
 from pin '%s' is detected.

DESCRIPTION

The clock tree for the specified clock contains non-unate paths. Clock networks
normally do not contain cells such as exclusive-OR gates which have non-unate
behavior. This implies that both inverting and noninverting clock waveforms reach
the specified pin. The sense that is propagated from this pin is non-deterministic.

WHAT NEXT

Since there is ambiguity on which sense to choose to propagate, the tool picks one arbitrarily to propagate. If this is not acceptable, create a clock using the output of the non-unate gate as a source.

TIM-98 (Error) Minimum version must be a different library.

DESCRIPTION

The **set_min_library** command was used to set the minimum version of a library to be the same as the maximum version. This is not allowed.

WHAT NEXT

Enter the correct name of the minimum library, or use the '-none' option to revert to using the same library for both minimum and maximum analysis.

TIM-100 (error) Unable to obtain a DC-Expert license.

DESCRIPTION

Timing commands such as **report_timing** or **highlight_path** require that a DC-Expert key, other appropriate technology key, or both be checked out.

WHAT NEXT

To determine who is using the DC-Expert, use the **license_users** command. Should problems occur with the license server, contact your system administrator.

TIM-101 (error) The '%s' command is not supported in dt_shell.

DESCRIPTION

This error occurs when a valid Design Compiler command is used, but the command is not supported in **dt_shell**, the timing analysis user interface. Commands such as **compile** are supported only in **dc_shell**, and are ignored in **dt_shell**.

WHAT NEXT

If you need to use the command, use the **dc_shell** program instead of **dt_shell**.

TIM-102 (Error) Ultra license is required for true path reporting.

DESCRIPTION

The **-justify** and **-true** options of **report_timing** require an Ultra license.

WHAT NEXT

TIM-103 (Warning) Reference %s contains internal pins with clock attribute.

DESCRIPTION

The reference contains internal/generated clocks on some internal pins which are not accessible to user to create clocks.

WHAT NEXT

~

TIM-104 (Warning) Worst timing paths might not be returned.

DESCRIPTION

Design Compiler static timing verifier is optimized for finding the longest paths (max delay) and the shortest paths (min delay) in the design. The timing verifier cannot always efficiently compute the longest path in the design, which is shorter than a given amount or the shortest path in the design, which is longer than a given amount. This warning indicates that the current **report_timing** command has made such a request that cannot be satisfied efficiently.

In this case, **report_timing** uses the -nworst option to limit its search for paths meeting the -greater or -lesser criteria. There is no guarantee that the paths returned will be the worst ones in the design that meet the criteria specified in the **report_timing** command. In fact, it is possible that no paths will be returned even though a path meeting the report_timing criteria does exist in the design.

WHAT NEXT

Increasing the number of paths to return using the -nworst option of **report_timing** increases the likelihood that the worst paths will be found. However, increasing this value also increases the memory and runtime needed by **report_timing**.

TIM-105 (Information) Converting time units for library '%s' since those in library '%s' differ.

DESCRIPTION

The time units specified in the first library differ from those in the second
library. The second library is Design Compiler's "main" library and determines DC's
default time units. DC reports use these units and all time values annotated on the
design (using **create_clock**, **set_input_delay**, and so on.) are assumed to be in these
units.

The informational message notifies you that Design Compiler is handling conversion
of units so that delay calculation using cells in the first library use time values
in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main
library is the first library in the link path that contains a cell that is used in
the design. During optimization the main library is the first target library
specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

TIM-106 (Information) Converting capacitance units for library '%s' since those in library '%s' differ.

DESCRIPTION

The capacitance units specified in the first library differ from those in the second
library. The second library is Design Compiler's "main" library and determines DC's
default capacitance units. DC reports will use these units and all capacitance
values annotated on the design (using **set_load**) are assumed to be in these units.

The informational message notifies you that Design Compiler is handling conversion
of units so that delay calculation using cells in the first library will use
capacitance values in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main
library is the first library in the link path that contains a cell that is used in
the design. During optimization the main library is the first target library
specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

TIM-107 (Warning) Main library '%s' has no time units specified, but library '%s' does.

DESCRIPTION

Time units were not specified in the first (main) library, but time units were specified in the second library.

Design Compiler uses the main library to determine the default time units. The default time units are used in reports and all time values annotated on the design (using **create_clock**, **set_input_delay**, and so on.) are assumed to be in these units. However, this main library has no time units and as a result DC runs in a "unitless" mode. No time unit conversion is performed. This can result in incorrect analysis if different time units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

To change the main library to a different one with units specified, remove the local_link_library attribute on the current design if one is present and put the desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and the library must be read in using **read_lib**.

TIM-108 (Warning) Main library '%s' has no capacitance units specified, but library '%s' does.

DESCRIPTION

Capacitance units were not specified in the first (main) library, but capacitance units were specified in the second library.

Design Compiler uses the main library to determine the default capacitance units. The default capacitance units are used in reports and all capacitance values annotated on the design (using **set_load**) are assumed to be in these units. However this main library has no capacitance units and as a result DC runs in a "unitless" mode. No capacitance unit conversion is performed. This can result in incorrect analysis if different capacitance units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design.

During optimization the main library is the first target library specified.

WHAT NEXT

To see the units that are specified for a library, use the **report_lib** command.

To change the main library to a different one with units specified, remove the
local_link_library attribute on the current design if one is present and put the
desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and
the library must be read in using **read_lib**.

TIM-109 (Warning) Cell '%s' cannot be optimized because it has conflicting timing exceptions on pins '%s' and '%s'.

DESCRIPTION

The identified cell has multiple input pins with conflicting point-to-point timing
exceptions on them. During optimization this cell is dont_touch'ed to prevent the
point-to-point exceptions from being lost if the cell gets remapped to a
configuration with fewer input pins. An example of such an optimization is pulling a
multiplexer out of a mux'ed flip-flop. In this case, conflicts in timing exceptions
could not be accurately resolved in the new, single input configuration.

Commands which create timing exceptions are **set_max_delay**, **set_min_delay**,
set_false_path, **set_multicycle_path**, and **group_path**.

WHAT NEXT

To allow optimization to be performed on this cell, set timing exceptions on the
cell such that both of the indicated pins have matching timing constraints. To
analyze the timing exceptions that currently exist on the design, use the commands
report_timing_requirements and **report_path_group**.

TIM-110 (Warning) Cell '%s' is being dont_touch'ed because of timing constraints on pin '%s'.

DESCRIPTION

The identified cell has timing constraints which cannot always be transferred to
another cell during optimization. As a result, the cell is dont_touched to prevent
it from being replaced and to prevent the timing constraints from being lost.

WHAT NEXT

To view the timing constraints set on the pin, use **report_timing_requirements**. If the cell is sequential, verify that the library cell has the correct timing arcs.

TIM-111 (warning) Clock port '%s' is assigned input delay relative to clock '%s'.

DESCRIPTION

This issue will be issued when setting an input delay on clock port, and it is not specified relative to the same clock.

WHAT NEXT

Remove the unneeded input delay value using the **remove_input_delay** command.

SEE ALSO

remove_input_delay(2)

TIM-112 (Information) Input delay ('%s') on clock port '%s' will be added to the clock's propagated skew.

DESCRIPTION

An input delay set on a clock port is interpreted as clock tree delay between the ideal clock source and the input port.

WHAT NEXT

If you don't want to have the input delay on the clock added to the clock skew, unset the input delay using the **remove_input_delay** command.

TIM-113 (Information) set_input_delay values are added to the propagated clock skew.

DESCRIPTION

When setting input delay on a clock signal, this value is added to the clock network

delay when calculating the skew at the clock pins.

WHAT NEXT

If you don't want to have the input delay on the clock added to the clock skew, unset the input delay using the **remove_input_delay** command.

TIM-114 (Warning) File '%s' could not be opened.

DESCRIPTION

You receive this warning message because the log file specified by the **case_analysis_log_file** variable could not be opened. The case analysis information will not be output to a log file.

WHAT NEXT

Specify a valid file that can be opened by the **case_analysis_log_file** variable.

SEE ALSO

report_timing (2), **set_case_analysis** (2); **case_analysis_log_file** (3).

TIM-120 (Error) Cannot find library file named '%s'.

DESCRIPTION

The file specified cannot be found or is not readable.

WHAT NEXT

Check to make sure that the filename exists, permissions are set correctly, and the search_path variable contains the directories that should be searched.

TIM-121 (warning) The -locations option of the report_timing command is now obsolete. Use the -physical option instead.

DESCRIPTION

You receive this message if you have issued **report_timing -locations**. This message

informs you that the **-locations** option is now obsolete and has been replaced by the **-physical** option. **-locations** continues to be supported for backward compatibility.

WHAT NEXT

Unless you need to use the **-locations** option for backward compatibility, the next time you use **report_timing**, use **-physical** instead of **-locations**.

SEE ALSO

report_timing (2).

TIM-125 (error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

DESCRIPTION

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, or can you have a generated clock in the fanout of two clock sources.

WHAT NEXT

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

TIM-128 (warning) No controlling value could be found for the clock gating cell '%s' for the clock pin '%s'.

DESCRIPTION

You receive this warning message because you executed the **set_clock_gating_check** command but did not specify a controlling value for the pin of the clock gating cell driven by the clock. Normally, clock gating checks are performed for the interval where the clock does not have the controlling value. If no controlling value can be determined, no clock gating check will be performed.

WHAT NEXT

Use the **-high** or **-low** option with the **set_clock_gating_check** command to specify the noncontrolling interval for the clock pin.

set_clock_gating_check (2).

TIM-129 (warning) User specified controlling value is different.

DESCRIPTION

User defined controlling value for the clock gating cell '%s' for the clock pin '%s' conflicts with the one calculated by the tool. But the user specified value takes precedence over the calculated value.

WHAT NEXT

The clock gating check is performed for the interval of the clock pin depending on the controlling value. See the manual page for the command **set_clock_gating_check** for detailed instructions on using -high and -low options.

TIM-130 (warning) The attribute '%s' is not supported.

DESCRIPTION

You receive this message because the attribute specified in the ftiming_report_attributes variable is not supported by the **report_timing** command with the **-attributes** option. Currently, only the **dont_touch**, **dont_use**, **map_only**, **ideal_net** and **size_only** attributes are supported.

The **timing_report_attributes** variable is in the system .synopsys_dc.setup file.

WHAT NEXT

Modify the **timing_report_attributes** variable.

SEE ALSO

report_timing (2).

TIM-131 (warning) There are no specified attributes to report.

DESCRIPTION

You receive this message because you used the the **report_timing** command with the **-attributes** option; but, because there was no variable in the **timing_report_attributes** variable, no attributes are printed.

The **timing_report_attributes** variable specifies the attributes to be reported by the **report_timing** command with the **-attributes** option. Currently, only the **dont_touch**, **dont_use**, **map_only**, **ideal_net** and **size_only** attributes are supported.

The **timing_report_attributes** variable is in the system .synopsys_dc.setup file.

WHAT NEXT

Modify the **timing_report_attributes** variable.

SEE ALSO

report_timing (2).

TIM-133 (warning) Setting clock gating check on multiplexer '%s'.

DESCRIPTION

You receive this warning message because you have executed the
set_clock_gating_check command and specified a controlling value for a clock for a
multiplexer. Generally, clock gating checks ensure that the enable signal does not
change during the interval when the clock input has a noncontrolling value.

A multiplexer is a cell that has no controlling value. To perform a clock gating
check on a multiplexer, you must specify the noncontrolling interval for the clock.
Use the **-high** and **-low** options carefully, as the tool does not perform detailed
analysis to determine if the selected signal changes only in the safe intervals.

WHAT NEXT

Use the **-high** or **-low** option for performing clock gating checks carefully on cells
like multiplexers after understanding when it is safe to change the selected signal.
There can be situations when there is no interval when it is safe to change the
selected signal. Carefully analyze the consequences before using these options on
cells like multiplexers.

SEE ALSO

set_clock_gating_check (2).

TIM-134 (warning) Design '%s' contains %d high-fanout nets. A fanout number of %d will be used for delay calculations involving

these nets.

DESCRIPTION

The design contains high-fanout nets whose delays will be computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

WHAT NEXT

You can control the load pin threshold for high-fanout nets using the **high_fanout_net_threshold** variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the **high_fanout_net_pin_capacitance** variable times the high-fanout threshold.

EXAMPLE MESSAGE

Warning: Design 'reg_top' contains 3 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

SEE ALSO

high_fanout_net_threshold (3), **high_fanout_net_pin_capacitance** (3).

TIM-135 (Warning) Net '%s' exceeds the high-fanout threshold. Using a fanout number of %d to calculate net delay and load.

DESCRIPTION

The named net is classified as a high-fanout net because its fanout number exceeds the threshold specified by the **high_fanout_net_threshold** variable. Delays of high-fanout nets are computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained

should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

WHAT NEXT

You can control the load pin threshold for high-fanout nets using the **high_fanout_net_threshold** variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the **high_fanout_net_pin_capacitance** variable times the high-fanout threshold.

SEE ALSO

high_fanout_net_threshold (3), **high_fanout_net_pin_capacitance** (3).

TIM-140 (warning) Gated clock latch is not created for pin '%s' because pin has a connection to a clock.

DESCRIPTION

You receive this warning because the tool has detected that you set the **set_clock_gating_check** command on a pin that is driven by a clock. Clock-gating checks are normally performed on the enable pins of the clock-gating cell. Setting a clock-gating check on a pin driven by the clock in the clock-gating cell has no effect.

WHAT NEXT

If you are not sure which pin to set the clock-gating check on, consider setting the check on the clock-gating cell. The clock-gating cell performs clock-gating checks on all the enable pins of the cell. See the man page for the **set_clock_gating_check** command for more detailed information on this command.

set_clock_gating_check (2).

TIM-141 (warning) Gated clock latch is not created for cell '%s'

on pin '%s' in design '%s'.

DESCRIPTION

You receive this warning because the tool has detected that you set the
set_clock_gating_check command on a pin that is either a non-input pin or is driven
by a clock. Clock-gating checks should be performed on input enable pins of the
clock-gating cell. Setting clock-gating check on the pins driven by the clock in the
clock-gating cell has no effect. Similarly, setting clock-gating check on an output
pin has no effect.

WHAT NEXT

If you are not sure which pin to set the clock gating check on, consider setting the
check on the clock-gating cell, which will then perform clock-gating checks on all
the enable pins of the cell. See the man page for the **set_clock_gating_check** command
for detailed information on this command.

SEE ALSO

set_clock_gating_check (2).

TIM-142 (warning) No gated clock latch created for cell '%s'.

DESCRIPTION

You receive this warning because the tool has detected that you set the
set_clock_gating_check command on a pin that is a non-input pin or is driven by a
clock. Clock-gating checks should be performed on input enable pins of the clock-
gating cell. Setting a clock-gating check on the pins driven by the clock in the
clock-gating cell has no effect. Similarly, setting clock-gating check on an output
pin has no effect.

WHAT NEXT

If you are not sure which pin to set the clock-gating check on, consider setting the
check on the clock-gating cell, which will then perform clock-gating checks on all
the enable pins of the cell. See the man page for the **set_clock_gating_check** command
for more detailed information.

SEE ALSO

set_clock_gating_check (2).

TIM-143 (warning) Converting propagated clock at '%s' to ideal clock.

DESCRIPTION

You receive this warning to let you know that because you set the **set_clock_latency** command on a propagated clock object, that clock object will be changed to ideal.

WHAT NEXT

If you want the clock to be propagated, do *not* specify **set_clock_latency** on the propagated clock object.

TIM-144 (warning) Ideal timing is specified on the non-ideal pin '%s'.

DESCRIPTION

Ideal latency and ideal transition are ignored if they are set on a non-ideal network.

WHAT NEXT

If the user wants to use ideal latency or ideal transition on a pin object, it must marked as ideal.

TIM-149 (warning) Cannot preserve timing constraints on IO pin '%s' during ungroup.

DESCRIPTION

This warning message occurs when the **ungroup** command cannot move constraints from an IO pin that has more than one driver or more than one receiver. Timing constraints on that pin are not preserved after the ungrouping.

WHAT NEXT

This is only a warning message. No action is required.

TIM-150 (warning) Cannot preserve timing constraints on pin '%s' during ungroup.

DESCRIPTION

You receive this warning to let you know that the **ungroup** command could not find the named pin and therefore cannot move constraints to that pin.

This warning message reports the situation. The pin might not be connected.

WHAT NEXT

Verify that you set the constraint on the correct pin. Then invoke the **ungroup** command again.

SEE ALSO

ungroup (2).

TIM-151 (warning) Cannot preserve the clock at source pin '%s' during ungroup.

DESCRIPTION

This warning lets you know that a clock with a hierarchical source pin cannot be preserved because the source cannot be moved to another pin on the same net. The clock source might not be connected. Or possibly you have defined another clock on the same net.

WHAT NEXT

Check to see if the clock source is unconnected or if there is another clock defined on the same net. Make any necessary corrections, and invoke the command again.

SEE ALSO

ungroup (2).

TIM-152 (warning) Cannot preserve the generated clock source pin '%s' during ungroup.

DESCRIPTION

You receive this warning to let you know that the generated clock with a hierarchical source pin will not be preserved because it is not possible to move the source pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

SEE ALSO

ungroup (2).

TIM-154 (warning) Generated clock '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the tool is not preserving a generated clock with a hierarchical master pin or hierarchical source pin, because it is not possible to move the source pin or the master pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

SEE ALSO

ungroup (2).

TIM-155 (warning) The disable_timing constraint on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the disable_timing constraint that is

set on a hierarchical pin cannot be preserved because the **ungroup** command cannot find another pin on the same net where the constraint can be set.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-156 (warning) Case analysis on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the case-analysis value that you set on the named hierarchical pin cannot be preserved, because the **ungroup** command cannot find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-157 (warning) Generated clock '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning because the named generated clock that has a hierarchical master pin or hierarchical source pin will not be preserved, because it is not possible to move either the source pin or the master pin to another pin on the same net.

WHAT NEXT

The **ungroup** command will automatically remove the generated clock.

TIM-158 (warning) Input/output delay on pin '%s' will be lost after ungroup.

DESCRIPTION

You receive this warning to let you know that the input delay or output delay that you set on a hierarchical pin will not be preserved because the **ungroup** command could not find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-159 (warning) Exception through pin '%s' is lost after ungroup.

DESCRIPTION

You receive this warning to let you know that timing exception through a hierarchical pin will not be preserved after the ungroup process because the **ungroup** command cannot find another pin in the same net on which to set the constraint.

WHAT NEXT

This is a warning only and requires no action on your part.

SEE ALSO

ungroup (2).

TIM-160 (warning) The variable named %s is set to an illegal

value (%g) and will be ignored.

DESCRIPTION

This warning message occurs when a variable is set to a value that is not within the range of acceptable values. The variable setting is ignored.

The following shows an example of the warning message.
Warning: The variable named rc_input_threshold_pct_rise is set to an illegal value (150) and will be ignored. (TIM-160)

WHAT NEXT

This is only a warning message. No action is required.

However, if you do not want the variable value to be ignored, reset the variable to an acceptable value. Refer to the man page for the variable shown in the message to determine the acceptable values. After making your changes, run the command again.

TIM-161 (warning) The variable named %s is set to a very low value (%g).

DESCRIPTION

This warning message occurs when a variable is set to a legal value that is well below the range of values that are normally used. This message warns you to check the variable's value to make sure that it is correct.

The following shows an example of the warning message.
Warning: The variable named rc_input_threshold_pct_rise is set to a very low value (0.50). (TIM-161)

WHAT NEXT

This is a only a warning message. No action is required.

However, if the value of the variable is not the value you want, reset the variable to the correct value. Refer to the man page for the variable shown in the message to determine the range of values. After making your changes, run the command again.

TIM-162 (warning) The value of variable '%s' (%g) overrides the

original value (%g) in library '%s'.

DESCRIPTION

This warning message occurs when you set the named variable because you are
overriding a library parameter that is specified by the creator of the library. This
is not considered best practice because it can cause inaccurate or incorrect
results.

Consult the creator of the library before attempting to override a library
parameter.

The following shows an example of the warning message.
Warning: The value of variable 'rc_input_threshold_pct_rise' (80) overrides the
original value (50) in library 'cmos_013_comb'. (TIM-162)

WHAT NEXT

This is a warning message only. If you are sure you want to override the library
parameter value, no action is required.

However, to use the value defined in the library, unassign the variable and remove
the variable assignment from any scripts. After completing your changes, rerun the
command.

TIM-163 (warning) The library named %s specifies a very small trip-point value (%g).

DESCRIPTION

This warning message occurs when the library contains a trip-point value that is
legal, but is well below the range of values that are typically used.

The following shows an example of the warning message.
Warning: The library named cmos_013_comb specifies a very small trip-point value
(0.5). (TIM-163)

WHAT NEXT

This is a warning message only. No action is required.

However, it is best practice to ask the library creator to check the trip-point
values in the library. You can use the **report_lib** command to see the trip-point
values in the library.

TIM-164 (warning) The trip points for the library named %s differ from those in the library named %s.

DESCRIPTION

This warning message occurs when two libraries with different trip-point values are being used. This may result in a loss of timing accuracy when cells from one library are connected to cells of the other library.

The following shows an example of the warning message.
Warning: The trip points for the library named cmos_013_comb differ from those in the library named cmos_013_fflop. (TIM-164)

WHAT NEXT

This is a warning message only. No action is required.

However, you can check the trip points for a library using the **report_lib** command. It is best practice to use libraries that use the same trip-point values when cells from different libraries will be connected.

SEE ALSO

report_lib(2)

TIM-165 (warning) The library named %s contains an illegal trip-point value (%g) that will be ignored.

DESCRIPTION

This warning message occurs when a a library contains an illegal trip-point specification that is ignored.

The following shows an example of the warning message.
Warning: The library named cmos_013_comb contains an illegal trip-point value (150) that will be ignored. (TIM-165)

WHAT NEXT

This is only a warning message. No action is required.

However, you can check the trip points for a library using the **report_lib** command. Inform the library creator of the illegal trip-point value, because improper trip-point specifications may cause inaccurate timing results.

SEE ALSO

report_lib(2)

TIM-166 (error) For the library named %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

DESCRIPTION

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must always be larger than the lower trip point (even for falling transitions).

The following shows an example of the error message.
Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-166)

WHAT NEXT

Check the trip points for the library using the **report_lib** command.

• If the incorrect values are specified in the library, inform the library creator.

• If the trip-point values are not coming from the library, they were set using variables such as **rc_slew_lower_threshold_pct_rise**. In this case, reset the variables to the correct values.

SEE ALSO

report_lib(2)
rc_slew_lower_threshold_pct_rise(3)

TIM-167 (error) For the library named %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values

of %g and %g will be used.

DESCRIPTION

This error message occurs when a lower slew trip point is set to the corresponding upper trip point of the same value. This is not allowed because it makes all transition times zero.

The following shows an example of the error message.
Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-167)

WHAT NEXT

Check the trip points for the library using the **report_lib** command.

• If the incorrect values were specified in the library, inform the library creator.

• If the trip-point values are not coming from the library, they were set using variables such as **rc_slew_lower_threshold_pct_rise**. In this case reset the variables to the correct values.

SEE ALSO

report_lib(2)
rc_slew_lower_threshold_pct_rise(3)

TIM-168 (information) There are logic constants set for unused pins.

DESCRIPTION

This information message occurs when there are unused (hanging) pins in the design. The tool binds the unused pins to logic constants that may affect case analysis, arc disabling, and report_timing.

WHAT NEXT

This is only an information message. No action is required.

However, the tool ignores this setting if you set the **dont_bind_unused_pins_to_logic_constant** variable to true.

dont_bind_unused_pins_to_logic_constant(3)

TIM-169 (warning) Clock '%s' does not have edge values monotonically increasing, so waveform is adjusted.

DESCRIPTION

You receive this warning to let you know that the edge values of the clock is not in a monotonically increasing sequence. The reason that this is a TIM message instead of an UID message suggests that the waveform inferred from input delays could be violating the condition. In order to proceed with the analysis, the waveform edge values of the clock are adjusted.

WHAT NEXT

Clearly define the clock waveform to meet the conditions, or adjust external delays that could have led to this violation.

SEE ALSO

create_clock (2).

TIM-170 (warning) Restored the timing arcs disabled by loop breaking.

DESCRIPTION

When the timing graph is changed, the internally disabled timing arcs for loop breaking is restored.

WHAT NEXT

Exam the timing arcs to be sure they are correct for loop breaking.

SEE ALSO

set_disable_timing (2).

TIM-171 (warning) The hierarchical cell named %s that is being

ungrouped has derate. This derate will be set on the lower level leaf cells if the leaf cell does not have a derate itself. This may cause timing inconsistency before and after ungrouping.

DESCRIPTION

This warning message occurs when ungrouping a cell that has derate. The cell's derate factors are set on the lower level cells if the lower level cells do not have their own derate factors. Because the derate factor of library cells has has higher priority than hierarchical cells, this setting may cause the derate factors used in delay calculation to change after ungrouping.

WHAT NEXT

This is only a warning message. No action is required.

However, if this is not the result you intended, use the **set_timing_derate** command to change the derate factors.

SEE ALSO

set_timing_derate(2)

TIM-172 (error) For library pin %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

DESCRIPTION

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must be larger than the lower trip point (even for falling transitions).

The following shows an example error message:
error: For library pin clk, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-172)

WHAT NEXT

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-173 (error) For library pin %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values of %g and %g will be used.

DESCRIPTION

This error message occurs when a lower slew trip point is set to the same value corresponding upper trip point. This is not allowed, because it makes all transition times zero.

The following shows an example error message:
error: For library pin clk, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-173)

WHAT NEXT

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-175 (Warning) Breaking the timing path through pin '%s' due to user timing constraints.

DESCRIPTION

Some timing constraint commands can cause timing paths to be broken when placed on pins which are not normal timing startpoints or endpoints. Examples include **set_max_delay**, **set_min_delay**, **set_multicycle_path**, **set_false_path**, and **group_path**. Paths are broken by making the pin an endpoint for all timing paths leading to the pin. In addition, the pin becomes a startpoint for all timing paths going out of the pin.

WHAT NEXT

To avoid broken timing paths, try to set timing exceptions on ports and register clock or data input pins. For other types of pins, use -through pin exceptions rather than -from and -to pin exceptions. The major difference between the -from, -to, and -through options is that -from causes the path to be broken if the pin is not a normal timing startpoint, -to causes the path to be broken if the pin is not a normal timing endpoint, and -through does not break paths.

SEE ALSO

set_max_delay (2), **set_min_delay** (2), **set_multicyle_path** (2), **set_false_path** (2), **group_path** (2).

TIM-176 (information) Timer is not in zero interconnect delay mode.

DESCRIPTION

This information message advises you that the timer is no longer working in the zero interconnect delay mode. The timer is in normal mode so the net wire capacitance is restored from the back annotation or from the wire load model.

WHAT NEXT

This is an informational message only. No action is required.

However, if the result is not what you intended, you can enable zero interconnect delay mode by setting **set_zero_interconnect_delay_mode** to **true**.

SEE ALSO

get_zero_interconnect_delay_mode(2)
set_zero_interconnect_delay_mode(2)

TIM-177 (warning) Timer is in zero interconnect delay mode.

DESCRIPTION

This warning message occurs when the timer is working in the zero interconnect delay mode. The net wire capacitance is 0 when calculating the delay, for example, Cw = 0.

When you run the **set_zero_interconnect_delay_mode** command without specifying **true** or **false**, zero interconnect delay mode is enabled by default.

After you set the interconnect delay mode to zero, the **report_timing**, **report_constraint**, and all commands that use the wire delay reflect the zero Cw. This also affects optimization.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you intended, it is considered best practice to set **set_zero_interconnect_delay_mode** to **false** before the timing optimization. Otherwise, the optimization does not see the interconnect delay, even if the design has the wire load model specified, the design is back annotated, or the design is routed.

```
get_zero_interconnect_delay_mode(2)
set_zero_interconnect_delay_mode(2)
```

TIM-178 (warning) This '%s' constraint is no longer applicable to any path.

DESCRIPTION

This warning message occurs when pins or clocks have been removed from the timing path constraint to the extent that the constraint cannot be applied. For example, a false path from {A B} to {C D} is dropped if both C and D have been removed from the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the **ungroup** command from the top level using the **-all_instances** option, if needed.

SEE ALSO

ungroup(2)

TIM-179 (warning) '%s' constraint made a reference '%s %s' which no longer exists.

DESCRIPTION

This warning message occurs when the pin or object specified in the timing constraint has been removed as the result of an optimization or constraint propagation. This can cause the constraint to no longer apply to the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

WHAT NEXT

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the **ungroup** command from the top level using the **-all_instances** option, if needed.

SEE ALSO

ungroup(2)

TIM-180 (information) Total %d nets in the design, %d nets have timing window.

DESCRIPTION

This message gives a summary of the number of nets in the design and how many of them have timing windows. This message is issued during timing update when SI analysis is enabled and timing windows are considered in SI analysis.

WHAT NEXT

This is an informational message only. No action is required.

TIM-181 (Error) Relationship between clocks %s and %s is already defined to be %s by group %s

DESCRIPTION

The clock pair already has a relationship defined by a set_clock_groups command prior to the current set_clock_groups command.

WHAT NEXT

If you want to change the clock relationship, remove the exisiting relationship by using the **remove_clock_groups** command. You can use **report_clock** command with fb-groups option to see more details.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-182 (Warning) Clock group %s has all design clocks in one group.

DESCRIPTION

The current set_clock_groups command specifies all the clocks in the same group. This is a valid setting if you plan to add more clocks. This command serves no prupose otherwise.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-183 (Warning) False path got overridden by set_clock_groups.

DESCRIPTION

The current set_clock_groups command overrode an existing false path between the specified clocks. The clocks are from different groups of set_clock_groups command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_timing_requirements** (2), **report_clock** (2).

TIM-184 (Error) Clock group settings for %s and %s conflict with previously set clock group settings.

DESCRIPTION

This error message occurs when a set_clock_groups command conflicts with a previous set_clock_groups command. For example, if a previous command has specified a false path between a pair of asynchronous clocks, then a new command tries to allow paths between the pair of clocks, you will see this error message. Use report_clock - groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the clock pair.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-185 (Error) Clock group %s not found.

DESCRIPTION

The error occurs if the clock group of given name is not found by remove_clock_group command. Use report_clock with -groups option to list all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-186 (Error) Clock group %s already exists.

DESCRIPTION

The error occurs if the clock group of given name and given type already exists. Use report_clock with -groups option to list all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-187 (Error) Clock group setting clash with false path settings of group %s (%s).

DESCRIPTION

The current set_clock_groups command conflicts with an earlier set_clock_groups setting issued for the group of clocks. This message usually occurs when all clocks in the design have been specified in the same group and their false path settings clash with another set_clock_groups command. For example, a previous set_clock_groups command specifies false path but the current command allows timing paths. Use report_clock -groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the set of clocks.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-188 (Error) Clock group %s already defines the %s

relationship for given clocks.

DESCRIPTION

This error message occurs when a set_clock_groups command tries to redefine a
relationship for the set of clocks. Use remove_clock_groups remove the existing
clock group if you want to change the clock group settings. Use report_clock -groups
to report all clock groups.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

TIM-189 (warning) there are conflicting senses converging for clock '%s' from pin '%s' in the clock network.

DESCRIPTION

The clock tree for the specified clock contains paths that have conflicting senses
merging. This clock will not be propagated forward starting from this pin.

WHAT NEXT

Since there is ambiguity on which sense to choose to propagate, user could use
set_clock_sense to pick which sense to propagate for the clock.

TIM-190 (warning) sense defined on pin '%s' cannot be honored for clock '%s'.

DESCRIPTION

The sense defined on the pin is not available and cannot be honored. This happens
when the clock senses propagated to this pin doesn't contain the sense user has
chosen. The defined sense is ignored and the original senses are propagated forward.

WHAT NEXT

A feasible clock sense has to be set by set_clock_sense, otherwise the defined sense
is ignored.

TIM-193 (info) Generated Clock (%s) has non_unate sense on master source pin.

DESCRIPTION

For a generated clock if the master source pin has a non-unate sense, then by default the tool will only propagate the positive sense waveform from the generated clock source pin to the clock pins. This information will help the user understand which generated clock has non-unate sense on their master source pin.

WHAT NEXT

The user can create an additional generated clock with a -preinvert option to propagate the negative sense.

TIM-196 (error) Clock group %s already defines the relationship for the given set of clocks.

DESCRIPTION

This error message occurs when the clock group for the specified set of clocks and type already exists.

WHAT NEXT

Use the **report_clock** command with the **-groups** option to list all clock groups. Rerun the command with either a new clock group, or a new set of clocks.

SEE ALSO

remove_clock_groups(2)
report_clock(2)
set_clock_groups(2)

TIM-197 (error) Cannot find the definition of mode '%s'.

DESCRIPTION

This error message occurs when user tries to set an invalid mode value to cell, which is not defined in the reference library.

Use the **report_mode** command to list all modes to look for which mode is you wanted.

SEE ALSO

TIM-200 (warning) Data Checks from-pin (%s) and to-pin (%s) are the same pin. Ignoring

DESCRIPTION

Datacheck from pin and to pin cannot be the same pin. The tool will ingore the data-check constaint in that case.

WHAT NEXT

Tool will issue a warning message and skip the constaint.

TIM-201 (Error) Generated clock (%s) (%s) is not satisfiable; zero source latency will be used.

DESCRIPTION

This is an error message whenever the clock network traverse can not find a path which satisfies the sense relationship defined by create_generated_clock command.

WHAT NEXT

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with - divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, the warning message will be issued. In this case, generated clock source pin should be redefined to clock pin of divider.

TIM-202 (Error) The master of the following generated clock is

not connected to any clock source.

DESCRIPTION

This error message occurs when check_timing command finds generated clock in the design is not connect to any clock source.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-203 (Error) The following generated clocks form a loop.

DESCRIPTION

This error message occurs when check_timing command finds generated clocks in the design form a loop. For example, when the source pin of G_CLK1 is the definition point of G_CLK2, meanwhile the source pin of G_CLK2 is the definition point of G_CLK1, the tow generated clocks form a loop.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-204 (Warning) The following generated clock has no path to its master clock.

DESCRIPTION

This Warning message occurs when check_timing command finds the definition point of generated clock has no path to its master clock. For example, master clock CLK1 defines on point A, and its generated clock GCLK1 defines on B, if there's no path from A to B, the Warning message will be printed out.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-205 (Warning) cross clocks found.

DESCRIPTION

This Warning message occurs when check_timing command finds clock interactions. If a clock launches one or more paths, which are captured by other clocks, it will have an entry in clock crossing report. If all paths between two clocks are false paths or the are exclusive/asynchronous clocks, the path is marked by *. If only part of paths are set as false paths, the path is marked by #.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-206 (Warning) following data check register reference pins are not driven by clocked signal.

DESCRIPTION

This warning message occurs when check_timing command finds no clocked signal reaches a data check register reference pin.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-207 (Warning) following data check register reference pins are driven by multiple clocked signals.

DESCRIPTION

This warning message occurs when check_timing command finds multiple clocked signals reach a data check register reference pin.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-208 (Warning) the following input ports have no

clock_relative delay specified.Since the variable 'timing_input_port_default_clock' is 'true', a default input port clock will be assumed for these ports.

DESCRIPTION

This warning message occurs when check_timing command finds no clock related delay specified on an input port, where it propagates to a clocked latch or output port. Note that with timing_input_port_default_clock set to 'true', a default clock will be assumed for the input port. Otherwise it will no be clocked, and the paths are unconstrained. In this case, if there is no input delay specified, check_timing will not generate warnings.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-209 (Warning) timing loops detected.

DESCRIPTION

This warning message occurs when check_timing command finds combinational feedback loops.

SEE ALSO

check_timing (2), **timing_check_defaults** (3).

TIM-213 (warning) the specific arc is in clock path, report_delay_calculation result may not match with timing report or clock skew report for this arc.

DESCRIPTION

This warning message occurs when both from pin and to pin are in clock network. In clock skew/latency calculation, tool use the slew from clock propagation path to calculate delay result. While in report_delay_calculation command, tool use the worst slew to calculate delay. This may cause different delay results.

TIM-300 (Error) Could not %s timing data %s %s: %s.
Falling back to full update.

DESCRIPTION

The application sometimes saves timing data to a temporary file. Something went
wrong either saving or restoring this data. For example, if the target disk was
full, you would get this message. The program will continue as though the temporary
directory was unavailable, possibly with some performance penalty.

WHAT NEXT

Files are saved either to /tmp or the value of the TMPDIR environment variable. If
the message indicates that saving was in progress, most likely the temporary
directory does not exist, you don't have permissions to write to it, or it is full.
The message will indicate the cause. In most cases, the disk is full. Either delete
some files, or find a different temporary directory and set the TMPDIR environment
variable to point at it. A problem during restore is rare. It might be that someone
accidently deleted the file or the file became corrupt.

SEE ALSO

UIAT

UIAT-1 (error) Cannot specify %s for '%s' type.

DESCRIPTION

While defining a new user attribute, you specified (a) either or both of the options that define a range, but did not specify a data type that supports ranges, or (b) an option limiting a string type to a set of values without using a string data type.

WHAT NEXT

Ranges only work with integer and double data types. Limiting an attribute to a set of strings only works with the string data type.

UIAT-2 (error) Min of range (%s) cannot be greater than max (%s).

DESCRIPTION

While defining a new user attribute, you specified a numeric range, and the minimum value was greater than the maximum value.

WHAT NEXT

Complete ranges require that the max value is greater than min.

UIAT-4 (warning) Attribute '%s' is already defined in class '%s'

DESCRIPTION

While defining a new user attribute, you specified an attribute name that is already defined. There is no mechanism to change an attribute definition.

UIAT-5 (warning) Cannot get attribute for more than one object.

DESCRIPTION

While getting the value of an attribute, you specified more than one object. You can only get the attribute for a single object.

WHAT NEXT

Specify a single object.

UIAT-7 (warning) Cannot import user attributes for %ss.

DESCRIPTION

While defining a new user attribute, you specified that the attribute should be imported from db files. However, the class of objects for which you are defining the attribute does not allow attributes to be imported.

WHAT NEXT

UIAT-8 (warning) Attribute '%s' is already defined as %s for another class.

DESCRIPTION

While defining a new user attribute, you specified an attribute name which is in use for another object class, but the data type which you specified was not the same as for the other object class. An attribute must have the same data type for all object classes for which it is defined.

WHAT NEXT

Determine which is the correct data type, and re-define the attribute for each affected class.

UIMS

UIMS-001 (Warning) -setup, -hold and -op_cond are not supported in PrimeTime

DESCRIPTION

These options are not supported in PrimeTime, and used only in DC/PC/Astro.

UIMS-002 (error) Insufficient number of slaves for LSF,GRD, or GENERIC.

DESCRIPTION

LSF, GRD, and GENERIC require greater than 0 slaves to operate.

WHAT NEXT

Allocate at least one slave for LSF, GRD or GENERIC.

UIMS-003 (error) Insufficient number of licenses specified.

DESCRIPTION

Insufficient number of licenses have been specified. At least one PrimeTime license must be specified for slave usage before the analysis can begin.

WHAT NEXT

Allocate at least one PrimeTime license for slave use via the **set_multi_scenario_license_limit** command.

UIMS-004 (error) Cannot open the following %s type files %s.

DESCRIPTION

The file name provided cannot be opened.

WHAT NEXT

Validate that the file name is correct. Or, confirm that the file path is visible, by verifying that the search path with **list search_path**. Read the file once again after fixing.

UIMS-005 (error) Scenario '%s' already exists.

DESCRIPTION

The scenario has already been created. Each scenario must have a unique identifier.

WHAT NEXT

Use a different name for each scenario.

UIMS-006 (error) Invalid value for priority.

DESCRIPTION

The value specified for priority is incompatiable.

WHAT NEXT

The -priority option expects an integer value between 1 and 10.

UIMS-007 (error) No configuration exists.

DESCRIPTION

No configuration has been created or exists.

WHAT NEXT

Create a configuration using the create_configuration command.

SEE ALSO

create_configuration (2).

UIMS-008 (error) There is no current session.

DESCRIPTION

The current session has not been specified and does not exist.

WHAT NEXT

Use command *current_session* ***to create a current session.***

SEE ALSO

current_session (2). **report_session** (2).

UIMS-009 (error) The following scenario name '%s' does not exist.

DESCRIPTION

The specified scenario do not exist.

UIMS-010 (error) A configuration already exists.

DESCRIPTION

A configuration has already being created. It is not possible to have more than one configuration at any given time.

UIMS-011 (error) Must set session focus before setting command focus.

DESCRIPTION

The scenario must be set in the current session before **set_current_scenario** can be used.

WHAT NEXT

Put the scenarios in the current session using **set_current_session**, then execute

`set_current_scenario`.

UIMS-012 (error) It is illegal to source a file while in interactive mode.

DESCRIPTION

It is not possible to source a file while in interactive mode. This can only be done in batch mode.

WHAT NEXT

To source a file, exit from interactive mode with a "." and initiate batch mode.

UIMS-013 (error) The scenario '%s' is not defined in the current session.

DESCRIPTION

The specified scenario must be in the current session before using `set_current_scenario`.

WHAT NEXT

To bring the specified scenario into exclusive focus, use set_current_session **first.**

UIMS-014 (error) The options -num_of_hosts and -options must be used
 in conjuction with one a -farm_type of 'grd', 'lsf', or 'generic'.

DESCRIPTION

When using add_distributed_hosts, if the '-options' options is specified then the -farm_type must be one of 'grd', 'lsf', and 'generic'.

WHAT NEXT

See the man page for the **add_distributed_hosts** command

UIMS-015 (error) Could not set %s to be the error log .

DESCRIPTION

The multi scenario error log was set to an invalid file name. The file name given
was either a directory or the filename resolved to a file which could not be opened
or the file name contained a path which could not be resolved.

WHAT NEXT

Choose a valid file name for the error log.

UIMS-016 (Error) The host type has not been specified.

DESCRIPTION

PrimeTime cannot add a distributed host without host type being specified.

WHAT NEXT

Specify a host type when specifying a host.

UIMS-017 (Warning) The max number of hosts allowed to be added has been reached.

DESCRIPTION

The max number of hosts allowed to be added has been reached. The max allowable
number of hosts is %d.

UIMS-018 (Warning) Unable to read host '%s' . This host has not been added.

DESCRIPTION

There has been a problem reading the host '%s'. The host has not been added.

WHAT NEXT

Ensure that when adding a host, the format is correct, i.e. hostname.

UIMS-019 (Error) Cannot add a distributed host with an unknown host type.

DESCRIPTION

The host type specified is unknown, so the host has not been added.

WHAT NEXT

Ensure that when adding a host, the options are correct. Type help -v
add_distributed_processor.

UIMS-020 (Error) Cannot set the current session.

DESCRIPTION

The resources required to be able to set the current session are not available.

WHAT NEXT

See the **current_session** command for the resource requirements and how to query the
available resources.

UIMS-022 (Error) The command %s has exceeded the maximum number of allowable characters

DESCRIPTION

The remote execute command can not handle commands greater than 1000 characters
long.

WHAT NEXT

Use ';' to seperate the remote_execute command_string into a set of individual
commands. If a single command is greater than 1000 lines, place the command in a
script and issue remote_execute {source script}

UIMS-023 (error) No scenarios were found.

DESCRIPTION

```
While trying to create a multi-scenario session using all scenarios, no scenarios
were found to add to the current session.
```

UIMS-024 (error) The configuration must have at least one netlist file.

DESCRIPTION

```
When creating a configuration using the create_configuration command, at least one
file must be specified with the common_data option.
```

UIMS-025 (error) Cannot specify option %s with farm type %s.

DESCRIPTION

```
While trying to add a compute resource using the
```
add_distributed_hosts
```
command, an
option has been specified that is not compatible with the farm type.
```

WHAT NEXT

```
See the man page for the
```
add_distributed_hosts
```
command.
```

UIMS-026 (error) The option %s must be specified with a farm type of %s.

DESCRIPTION

```
While trying to add a compute resource using the
```
add_distributed_hosts
```
command, an
option farm type.
```

WHAT NEXT

```
See the man page for the
```
add_distributed_hosts
```
command.
```

UIMS-027 (Error) create_scenario does not support the usage of -common_variables or -common_data when the -image option is specified.

DESCRIPTION

The **create_scenario** command does not support the -common_variables or -common_data options when the -image option is passed to the command.

WHAT NEXT

Either use the -common_variables and -common_data options with the **create_scenario** command or user the -image option, but not both. If variables need to be set and/or data files sourced after loading the scenario image, the -specific_variables and -specific_data options can be used with the -image option.

SEE ALSO

create_scenario (2).

UIMS-028 (error) There are no scenarios in command focus.

DESCRIPTION

There are no scenarios in command focus on which the command can be run.

WHAT NEXT

Use the **current_scenario** command to specify the command focus.

UIMS-029 (error) The session saved at '%s' is not usable.

DESCRIPTION

The session saved in the location specified either cannot be accessed or is not a valid saved session.

WHAT NEXT

Ensure the directory specified is a network accessible directory so that both the master and remote processes can access the directory.

Ensure the user account has premssions to access the directory.

Ensure the directory contains a valid PrimeTime saved session compatible with the version of PrimeTime being run.

UIPWR

UIPWR-001 (error) Command '%s' is not enabled in UI backward compatibility mode. Set power_ui_backward_compatibility to FALSE to enable this command.

DESCRIPTION

You received this error message because variable **power_ui_backward_compatibility** has been set to **TRUE** while this command is not enabled in UI backward compatiblity mode.

WHAT NEXT

Set **power_ui_backward_compatibility** to **FALSE**.

SEE ALSO

power_ui_backward_compatibility (3).

UIPWR-002 (error) Command '%s' is not enabled as default. Set power_ui_backward_compatibility to TRUE to enable this command.

DESCRIPTION

You received this error message because variable **power_ui_backward_compatibility** has been set to **FALSE** while this command is not enabled if backward compatiblity is not ON.

WHAT NEXT

Set **power_ui_backward_compatibility** to **TRUE**.

SEE ALSO

power_ui_backward_compatibility (3).

UIPWR-003 (error) Command '%s' is not supported in '%s' power analysis mode. Set power_analysis_mode to '%s' in order to run this command.

DESCRIPTION

You received this error message because variable **power_analysis_mode** has been set to a mode which is not compatible with this command.

WHAT NEXT

Set **power_analysis_mode** to the recommended mode.

SEE ALSO

power_analysis_mode (3).

UIPWR-004 (warning) Command '%s' is not fully supported in '%s' power analysis mode. The annotated power value is only reflected in average power result but not in peak power result.

DESCRIPTION

Command 'set_annotated_power' is not fully supported in time_based power analysis mode yet. The annotated power value is only reflected in average power result but not in peak powers and power waveforms.

SEE ALSO

power_analysis_mode (3), **set_annotated_power** (2).

UIPWR-005 (error) Command '%s' is not supported in '%s' power analysis mode. Set power_analysis_mode to '%s' in order to run this command.

DESCRIPTION

You received this error message because variable **power_analysis_mode** has been set to a mode which is not compatible with this command.

WHAT NEXT

Set **power_analysis_mode** to the recommended mode.

SEE ALSO

power_analysis_mode (3).

UIPWR-006 (error) Command '%s' can not be run when power is not updated in '%s' power analysis mode. Please check the current power analysis mode and run update_power if necessary.

DESCRIPTION

In time_based power analysis mode, command 'write_saif' can only be issued after power analysis is done. Please make sure that the correct power analysis mode is set, and run update_power in case of time_based power analysis mode.

SEE ALSO

power_analysis_mode (3), **update_power** (2).

UIPWR-007 (error) Option '%s' in command '%s' has been moved to command **set_power_analysis_options**.

DESCRIPTION

The specified option has been moved to a new PrimeTime PX command **set_power_analysis_options**. Please use the new command for setting this specific option.

WHAT NEXT

Please check out the man page for command **set_power_analysis_options** for more information. Set the option by using command **set_power_analysis_options** instead. As a temporary work around, you can also set **power_ui_backward_compatibility** to true.

SEE ALSO

set_power_analysis_options (2), **power_ui_backward_compatibility** (3).

UIPWR-008 (error) Can not enable or disable UI backward compatibility after power analysis commands have been issued.

DESCRIPTION

Variable **power_ui_backward_compatibility** can only be set before the first power analysis command. It can not be changed after power analysis commands have been issued.

WHAT NEXT

Set variable **power_ui_backward_compatibility** before the first power analysis command.

SEE ALSO

power_ui_backward_compatibility (3).

UIPWR-009 (error) Can't switch to power analysis mode '%s'.

DESCRIPTION

Variable **power_analysis_mode** can be changed during run. However, error was incurred during mode switching.

WHAT NEXT

Please check the analysis mode setting and run power analysis again.

SEE ALSO

power_analysis_mode (3).

UIPWR-010 (error) '%s' option can only be specified in '%s' power analysis.

DESCRIPTION

The error message indicated that the option of **set_power_analysis_options** was not supposed to be used in the current power analysis mode.

WHAT NEXT

Check the value of **power_analysis_mode** and make sure the option can be used for the specified mode.

SEE ALSO

power_analysis_mode (3).

UIPWR-011 (error) Unknown power waveform format '%s'.

DESCRIPTION

You received this error message because the value specified by -waveform_format option in set_power_analysis_options was not supported. The supported values are 'fsdb', 'out' and 'none'.

WHAT NEXT

Check the -waveform_format option, correct the value and run the command again.

UIPWR-012 (error) Unknown value '%s' for -include option.

DESCRIPTION

You received this error message because the value specified by -include option in set_power_analysis_options was not supported. The supported values are 'top', 'all_without_leaf' and 'all_with_leaf'.

WHAT NEXT

Check the -include option, correct the value and run the command again.

UIPWR-013 (error) Current waveform in FSDB format is not supported. Please use .out format instead.

DESCRIPTION

You received this error message because the tool did not support current waveform in FSDB format. the value specified by -waveform_format option in set_power_analysis_options needs to be set to 'out' if -current option is also set

for the command.

WHAT NEXT

Correct the setting and run command again.

UIPWR-014 (error) Event file (VCD or its equivalent) is not properly read for the time based power analysis mode.

DESCRIPTION

You received this error message because the event file (VCD or its equivalent) was not properly read before the time based power analysis.

WHAT NEXT

Check whether read_vcd command was specified and worked correctly.

UIPWR-015 (error) Please set the variable power_analysis_mode instead of using the command set_power_analysis_mode.

DESCRIPTION

The power analysis mode is controlled by a variable, power_analysis_mode. Accidentally using the command set_power_analysis_mode is a mistake.

WHAT NEXT

The user should use .fBset power_analysis_mode.fP instead.

UIPWR-016 (warning) Previous VCD (or its equivalent) file '%s' exist, will be overriden in time based power analysis mode.

DESCRIPTION

You received this error message because time based power analysis mode only allow one VCD file (or its equivalent). If more than one read_vcd command is issued, the later one will override the previous one.

Check to see whether the latest file from read_vcd command is the expected file for event based power analysis.

UIPWR-017 (error) Unknown VCD format '%s'.

DESCRIPTION

You received this error message because the option -format of read_vcd is specified with the format unknown to PrimeTime PX. Only 'Verilog', 'VHDL' and 'SystemVerilog' are allowed for this option.

WHAT NEXT

Correct the option and run the command again.

UIPWR-018 (error) Negative start time or time interval (start_time >= end_time) in option "-activity_time {%g, %g}" of set_power_analysis_options commands.

DESCRIPTION

Incorrect time window. It is required that the start time be no less than 0 and the end time no less than the start time.

WHAT NEXT

Give correct time window and try again.

UIPWR-019 (error) Invalid value of "-activity_time

DESCRIPTION

Incorrect time window given.

WHAT NEXT

Refer to PrimeTime PX Manual or manpage of set_power_analysis_options for how to specify time window by -activity_time option.

UIPWR-020 (error) Command '%s' is not supported in '%s' power analysis mode.

DESCRIPTION

You received this error message because variable **power_analysis_mode** has been set to a mode which is not compatible with this command.

WHAT NEXT

Set **power_analysis_mode** to the mode which is compatible with this command.

SEE ALSO

power_analysis_mode (3).

UIPWR-109 (Warning) reset_switching_activity is not fully supported for objects when VCD files have been identified but not applied. The command will proceed, but since VCD activity is not applied yet, results may not be as expected.

DESCRIPTION

In the **averaged** or **leakage_variation** power analysis modes, VCD annotation may be deferred until later during **update_power**. Running **reset_switching_activity** prior to **update_power** will not invalidate the switching activity from the VCD if specific cells are selected.

WHAT NEXT

Either reset switching activity on the whole design, or run update_power first, then reset switching activity on specific instances.

UIPWR-110 (Error) Failed to properly annotate activity from activity file

DESCRIPTION

An unknown error resulted in the activity file not being properly read.

UIPWR-201 (Warning) cycle accurate options in set_power_analysis_options are ignored

DESCRIPTION

The **-cycle_accurate_clock** and **-cycle_accurate_cycle_count** options in **set_power_analysis_options** command can only take effect when RTL VCD or zero delay VCD is used. Otherwise, they are ignored.

WHAT NEXT

Check your VCD file. If it's RTL VCD, add -rtl to read_vcd. If it's zero-delay VCD, add -zero_delay to read_vcd. Otherwise, remove -cycle_accurate_clock and -cycle_accurate_cycle_count in set_power_analysis_options.

UIPWR-202 (Warning) name mappings are ignored in time_based mode

DESCRIPTION

The **set_rtl_to_gate_name** commands in the time_based power analysis mode are only for RTL VCD. It will be ignored for gate level VCD.

WHAT NEXT

Check your VCD file. If it's RTL VCD, add -rtl to read_vcd. Otherwise, don't use set_rtl_to_gate_name.

UIPWR-203 (Error) reset_switching_activity does not support reseting activity on individual objects in the time_based power analysis mode

DESCRIPTION

The **reset_switching_activity** command can only be used to clear the activity file indicated with **read_vcd** when **power_analysis_mode** has been set to **time_based**

In other modes, **reset_switching_activity** can be used to reset activity on individual objects. The **time_based** mode does not use toggle rates for power computation, but instead computes power for individual events in the activity file.

WHAT NEXT

Run **reset_switching_activity** without arguments to clear the VCD.

Or, switch to another mode if power analysis is desired with modified activity on individual design objects.

UIPWR-204 (Warning) -waveform_interval in set_power_analysis_options is ignored for RTL VCD and zero delay VCD

DESCRIPTION

For RTL VCD (read_vcd -rtl ...) and zero delay VCD (read_vcd -zero_delay ...), the waveform interval is determined by -cycle_accurate_cycle_count and -cycle_accurate_clock in set_power_analysis_options. The -waveform_interval in set_power_analysis_options is ignored for RTL VCD and zero delay VCD.

WHAT NEXT

Remove -waveform_interval in set_power_analysis_options.

SEE ALSO

read_vcd (2) set_power_analysis_options (2)

UIPWR-205 (Warning) When using -pipe_exec in time_based power analysis_mode, switching activity reports will not be available until after update_power has been run.

DESCRIPTION

In time_based mode, with the -pipe_exec option, the VCD is read during update power. Switching activity reports from **report_switching_activity** or **get_switching_activity** rely on the VCD. Before the VCD is read during update_power, such reports cannot display meaningful information.

WHAT NEXT

```
Run update_power
```

SEE ALSO

```
read_vcd (2) update_power (2)
```

UIPWR-206 (Error) In the **time_based** power analysis mode, activity reporting may not be available prior to **update_power**

DESCRIPTION

```
In time_based mode, activity annotation can be reported after read_vcd if the -
pipe_exec option is used. If the -pipe_exec option is used, annotation cannot be
reported until after update_power.
```

WHAT NEXT

```
Run read_vcd
```

SEE ALSO

```
read_vcd (2) update_power (2) power_analysis_mode (3)
```

UIPWR-301 (Error) variable power_enable_leakage_variation_analysis must be set to true to run leakage variation analysis

DESCRIPTION

```
In the leakage_variation power analysis mode, the variable
power_enable_leakage_variation_analysis must be set to true prior to reading the
library containing leakage varation data.
```

WHAT NEXT

```
Set the variable to true at the beginning of the script, and run the script again.
```

UIPWR-302 (Error) The variable **power_enable_leakage_variation_analysis** is turned on, but the power analysis mode is other than **leakage_variation**.

DESCRIPTION

Leakage variation analysis is performed when both the variable **power_enable_leakage_variation_analysis** is set to true, and the power analysis mode is set to **leakage_variation**. If leakage variation analysis is not desired, set the variable to false.

WHAT NEXT

Either set **power_enable_leakage_variation_analysis** to false, or change the power analysis mode to **leakage_variation**.

UIPWR-601 (error) Variable 'power_enable_transit_power_analysis' cannot be set after library power data has been loaded.

DESCRIPTION

Variable **power_enable_transit_power_analysis** can be used to enable transit power analysis and reporting capability. This variable needs to be set before library power data is loaded.

WHAT NEXT

Set variable **power_enable_transit_power_analysis** before library power data is loaded.

SEE ALSO

UIPWR-602 (error) Command '%s' is not enabled in Transit power analysis mode. Set power_enable_transit_power_analysis to FALSE to enable this

command.

DESCRIPTION

```
This command is not enabled in Transit power analysis mode.
```

WHAT NEXT

Set **power_enable_transit_power_analysis** to **FALSE**.

SEE ALSO

UIPWR-603 (error) Command '%s' is only enabled in Transit power analysis mode. Set power_enable_transit_power_analysis to TRUE to enable this command.

DESCRIPTION

```
This command is used for Transit power analysis. Variable
power_enable_transit_power_analysis must be set to TRUE in order to use this
command.
```

WHAT NEXT

Set **power_enable_transit_power_analysis** to **TRUE**.

SEE ALSO

UIPWR-604 (error) Command 'set_current_ground' is only supported in UPF or pre-UPF rail mapping modes.

DESCRIPTION

```
This command is used for Transit power analysis. Transit power analysis is support
in UPF or pre-UPF rail mapping modes.
```

Use UPF for pre-UPF rail mapping commands for this feature.

SEE ALSO

create_power_domain (2), **create_supply_net** (2), **power_domains_compatibility** (3), **create_power_rail_mapping** (2).

UIPWR-605 (error) Rail name is not specified for set_current_ground -rail.

DESCRIPTION

This command is used for Transit power analysis. Transit power analysis is support in UPF or pre-UPF rail mapping modes. In pre-UPF rail mapping mode, a valid design rail name must be specified for set_current_ground -rail.

WHAT NEXT

Make sure if a valid design rail name is provided for the command.

SEE ALSO

power_domains_compatibility (3), **create_power_rail_mapping** (2).

UIPWR-606 (error) There is no design rail defined in this design. This command is ignored. Use command create_power_rail_mapping to define design rails.

DESCRIPTION

Power or ground rails in the design can be defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_ground command to select the rail of interest. To list all the defined rails, use command report_power_rail_mapping.

WHAT NEXT

Type 'man create_power_rail_mapping' for more information

UIPWR-607 (error) There is only one design rail defined in this design. Command set_current_ground has no effect on single rail design. This command is ignored. Use command create_power_rail_mapping to define design rails.

DESCRIPTION

```
Power or ground rails in the design can be defined by command
create_power_rail_mapping. Then the defined design rail can be used in
set_current_ground command to select the rail of interest. To list all the defined
rails, use command report_power_rail_mapping.
```

WHAT NEXT

```
Type 'man create_power_rail_mapping' for more information
```

UIPWR-608 (error) Variable 'power_enable_transit_power_analysis' cannot be set to TRUE in -rail mode.

DESCRIPTION

```
Variable power_enable_transit_power_analysis can be used to enable transit power
analysis and reporting capability. This feature is not supported in pt_shell -rail
mode.
```

SEE ALSO

UIPWR-609 (error) Supply net is not specified for set_current_ground -supply_net.

DESCRIPTION

```
This command is used for Transit power analysis. Transit power analysis is support
in UPF or pre-UPF rail mapping modes. In UPF mode, valid supply net(s) must be
specified for set_current_ground -supply_net.
```

WHAT NEXT

Make sure if a valid supply net object is provided for the command.

SEE ALSO

create_supply_net (2).

UITE-100 (error) Design mode configuration '%s' is not defined.

DESCRIPTION

```
The given design mode configuration is not defined.
```

WHAT NEXT

```
Design mode might be misspelled. Try report_design_modes to find out. To make a new
design_mode_configuration, use create_design_mode.
```

UITE-101 (error) Design mode '%s' is not defined in mode configuration '%s'.

DESCRIPTION

```
The given design mode configuration does not contain the given mode. If no design
modes configuration is specified, the first one is assumed.
```

WHAT NEXT

```
The design mode might be misspelled. Try report_design_mode to find out. The wrong
design mode configuration might be assumed.
```

UITE-102 (error) No design modes have been defined.

DESCRIPTION

```
No design modes have been defined for the current design.
```

WHAT NEXT

```
To make a design_mode_configuration, use create_design_modes.
```

UITE-103 (error) Design mode group '%s' is already defined.

DESCRIPTION

There is already a design mode group of the specified name.

WHAT NEXT

To define a different design mode group, choose another name and enter the command
again. Once a design mode group is defined, you cannot change it. You must reset all
of the design modes and start again.

UITE-104 (error) Input port '%s' not found.

DESCRIPTION

Synchronize_inputs only works on top-level input or inout ports of the current
design.

WHAT NEXT

To find the names of the existing input ports, use report_port.

UITE-105 (error) Port '%s' must be an input or inout port.

DESCRIPTION

Synchronize_inputs only works on the top-level input or inout ports of the current
design.

WHAT NEXT

To find the names of the existing input and inout ports, use report_port.

UITE-106 (warning) The %s command will be discontinued in

future releases. This command has been replaced by %s

DESCRIPTION

A command has been renamed. The old command name is being supported temporarily but will cause syntax errors in future releases

WHAT NEXT

Use the new command instead of the discontinued command.

SEE ALSO

UITE-107 (error) Cannot set timing derates on a design that is not the current design.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with a design, which is not the current design, as an argument.

WHAT NEXT

If the user has intended to operate on the specified design, then set the current design using the current_design command.

SEE ALSO

set_timing_derate (2). **current_design** (2).

UITE-115 (error) Reference '%s' '%s' must be a leaf pin or port.

DESCRIPTION

-reference_pin should specify a leaf pin or port on some clock network, i.e. direct or transistive fanout of some clock source given by -clock.

UITE-116 (Error) Edge value of clock '%s' is greater than its subsequent edge values.

DESCRIPTION

The value of each edge must be less or equal than its subsequent edge values. There must be an even number of edges and they are assumed to be alternating rise and fall.

WHAT NEXT

Use `report_clock` to check for clock information.

UITE-119 (Warning) Clock does not have waveform values monotonically increasing, so waveform has been adjusted.

DESCRIPTION

There must be an even number of edges, which are interpreted as alternating rising and falling edges. The edges must be monotonically increasing, except for a special case with two edges specified. When only two edge values are specified and the first value is greater than the second value, it is interpreted as a return-to-one waveform instead of the normal return-to-zero waveform if the falling edge adding one period is still larger than rising edge.

WHAT NEXT

UITE-120 (error) Invalid waveform. Edges must be an even number of
  monotonically increasing values less than one period in duration.

DESCRIPTION

The specified clock waveform is not valid.

UITE-121 (warning) Creating virtual clock named '%s' with no sources.

DESCRIPTION

This warning occurs when a virtual clock is created. A virtual clock has a name but no sources. This means it is not applied to any ports or pins in the design. A virtual clock can be used to specify input or output delay.

WHAT NEXT

The command **create_clock -period 10 -name CLK** does not apply the clock to any sources. If you want to apply the clock to a pin or port, you must specify the pin or port as in **create_clock -period 10 CLK** or **create_clock -period 10 -name CLK ff1/ CP**.

UITE-122 (error) The 'create_clock' command cannot be used on output port '%s'.

DESCRIPTION

Clock sources must be input ports or internal pins. Inout ports can be used, but they are not recommended because of bus contention issues.

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** command.

UITE-123 (warning) Creating a clock source on inout port '%s'.

DESCRIPTION

A circuit, where a clock signal drives an inout port, can be unpredictable. If the port is functioning as an output while the clock is driving, bus contention occurs. If the clock is three-stated, any registers in the fanout of the clock can lose state.

Verify that the circuit is safe according to your design rules. The PrimeTime
product assumes that the clock is valid.

UITE-124 (error) Cannot remove internal path group '%s'.

DESCRIPTION

You cannot use **remove_path_group** to remove internal path groups (such as the default
group).

WHAT NEXT

Reenter the command without the internal path group name.

UITE-125 (warning) Invalid delay direction for port '%s'.

DESCRIPTION

The entered port direction does not match the specifier used. For example, an input
port is used with a -to specifier.

WHAT NEXT

Re-enter the command with valid port directions.

UITE-126 (error) Unable to %s on path from '%s' to '%s'.

DESCRIPTION

A timing exception command failed to apply or remove information on the specified
path.

WHAT NEXT

UITE-127 (information) Found a design with sdf backannotation: (design '%s', file '%s').

Performance will be better by reading the db with -netlist_only and
   then reading the sdf file with read_sdf.

DESCRIPTION

A design with sdf backannotation was read in from a db file. The performance of
PrimeTime will be improved if the design db is read in order to obtain only the
netlist (read_db -netlist_only), and the sdf data is read from an sdf file using
read_sdf.

WHAT NEXT

UITE-128 (error) Unable to set %s on '%s'.

DESCRIPTION

Failed to execute the given set operation on the specified clock.

WHAT NEXT

UITE-129 (error) Unable to remove %s on '%s'.

DESCRIPTION

Failed to execute the given remove operation on the specified clock.

WHAT NEXT

UITE-130 (warning) Creating a clock on internal pin '%s'.

DESCRIPTION

Clock sources must be input ports. Internal pins can be used, but they are not
recommended because they segment your path and prevent slew propagation. PrimeTime
restarts slew propagation from the internal clock source pins and reset its value to
zero as if the user issued a set_annotated_transition command with a value of zero
on the internal clock source pin. You can use the set_annotated_transition command
on the clock source pin to set a slew value different than zero.

Identify a valid set of sources and reapply the **create_clock** command.

create_clock (2), **set_annotated_transition** (2).

UITE-131 (error) Design mode '%s' is already defined.

DESCRIPTION

There is already a design mode of the specified name.

WHAT NEXT

Choose a different design mode name and enter the command again, or remove the old design mode with the remove_design_mode command.

UITE-132 (warning) Mode '%s' does not exist on cell '%s'.

DESCRIPTION

There is no mode of the specified name on the cell.

WHAT NEXT

Use report_mode to determine the valid modes for the cell.

UITE-133 (error) Pin '%s' is not a valid %s.

DESCRIPTION

The specified pin is not a valid timing startpoint or endpoint. Some commands such as set_mode require that the from objects be valid timing startpoints, and the to objects be valid endpoints.

WHAT NEXT

Use input ports or register clock pins for the from objects, and output ports or register data pins for the to objects.

UITE-134 (warning) Creating a %s on multi-driven net '%s', only driver
pin '%s' is used as the source.

DESCRIPTION

```
It is recommended that you use only ports/pins as clock or generated clock sources.
Net can be used as clock source, but the effective source used by PrimeTime is the
driver pin of the net. If the net is multi-driven, only one of the driver pins is
used as the source of the clock.
```

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** or
create_generated_clock command.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-135 (error) Creating a %s on net '%s' which does not have
a driver pin as real source.

DESCRIPTION

```
It is recommended that you use only ports/pins as clock or generated clock sources.
Net can be used as clock source, but the effective source used by PrimeTime is the
driver pin of the net. If the net is multi-driven, only one of the driver pins is
used as the source of the clock. If the net does not have a driver pin, the clock
will not be correctly created.
```

WHAT NEXT

Identify a valid set of sources and reapply the **create_clock** or
create_generated_clock command.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-136 (warning) Creating a generated clock on hierarchical

pin '%s'.

DESCRIPTION

It is recommended that you do not specify a generated clock on a hierarchical design pin. PrimeTime may support generated clocks on hierarchical pins in the future.

WHAT NEXT

Move the generated clock to a leaf driver or load pin on the same net.

SEE ALSO

create_clock (2), **create_generated_clock** (2).

UITE-137 (warning) Creating '%s' on a hierarchical pin '%s'.

DESCRIPTION

Defining a constraint at a hierarchical pin causes the timing arcs (net arcs) from leaf pins driving this pin to leaf pins driven by this pin to be broken. This gives rise to two distinct limitations. First, the hierarchical boundary is a virtual designation and, generally, does not map to a specific physical location. Hence, PrimeTime cannot make any assumptions as to distributing the interconnect delay to the left and right of the bidirectional boundary. Second, breaking the original timing arcs may introduce a loss of timing information. For example, if the hierarchical pin were driven by three leaf pins and drives three other leaf pins, then breaking at the hierarchical boundary would reduce nine timing arcs to six, or worse, three considering the first limitation.

WHAT NEXT

Move the constraint to a leaf driver or load pin on the same net.

SEE ALSO

create_clock (2), **set_clock_sense** (2), **set_input_delay** (2), **set_output_delay** (2).

UITE-150 (warning) Negative clock latency specified: %g

DESCRIPTION

You specified a negative value to **set_clock_latency**. Although this is legal, it is

not typical.

WHAT NEXT

Ensure that you really wanted a negative value.

UITE-200 (error) Must specify %s option along with %s option.

DESCRIPTION

The two options must be together; if one of them is not specified, it is an error.

WHAT NEXT

Specify both the options together.

UITE-201 (warning) Option '%s' is valid only with option '%s'.

DESCRIPTION

The option specified is valid only if specified along with the other option.

WHAT NEXT

This option will be ignored, so you can remove this option from the command.

UITE-202 (error) The factor for -MULTIPLY_BY/-DIVIDE_BY '%d' is
  not a power of two.

DESCRIPTION

The -MULTIPLY_BY or -DIVIDE_BY factor should be a power of two, if not, it is an error.

WHAT NEXT

If the multiplication factor or division factor is not a power of two, model the clock derivation with -EDGES option.

UITE-203 (error) The number of edges specified '%d' is not an odd number larger than or equal to 3.

DESCRIPTION

```
The number of edges to make one period of the generated clock waveform has to be an
odd number larger than or equal to 3.
```

WHAT NEXT

```
Carefully specify edges and ensure that you specify one full clock cycle using the
edges.
```

UITE-204 (error) The number of edge_shifts specified '%d' using '-EDGE_SHIFT' option is not equal to the number of edges specifed '%d' using '-EDGES' option.

DESCRIPTION

```
The number of edge_shifts specified using the '-EDGE_SHIFTS' option must be equal to
the number of edges specified using the '-EDGES' option.
```

WHAT NEXT

```
Make the number of edge_shifts equal to the number of edges.
```

UITE-205 (error) Expected to find, at most, two numbers along with the option '%s', but found %d.

DESCRIPTION

```
The options '-MAX_EDGE_DELAY/-MIN_EDGE_DELAY' can have, at the most, two numbers
along with each, one for rise and one for fall edge.
```

WHAT NEXT

```
Specify only the rise and fall edge delays.
```

UITE-206 (error) The clock %s is a generated clock.

DESCRIPTION

A generated clock cannot be removed using 'remove_clock' command.

WHAT NEXT

To remove the generated clocks, use the **remove_generated_clock** command.

UITE-207 (error) A generated clock has already been defined with the name %s.

DESCRIPTION

A generated clock has already been defined with the name you specified.

WHAT NEXT

Either delete the generated clock and change the name, or change the name of the clock you are defining.

UITE-208 (error) You can specify only a single object for master clock source.

DESCRIPTION

The -source option takes only a single object as an argument.

WHAT NEXT

You can have a generated clock derived from a single clock. You cannot generate a clock from more than one master clock.

UITE-209 (error) You cannot specify an output port '%s' to be a

generated clock master source.

DESCRIPTION

Generated clock master can be an input or inout port or a pin.

WHAT NEXT

An output port cannot be a generated clock master.

UITE-210 (warning) Creating a generated clock on input or inout port '%s'.

DESCRIPTION

When creating a generated clock on an input or inout port, please note that the
generated clock would only derive its waveform characteristics from the master
clock. Delay, on the other hand, is derived from delay information at the port
itself. Additionally, creating a generated clock to drive an inout port can cause
unpredictable circuit behavior. If the port is functioning as an output while the
clock is driving, bus contention occurs. If the clock is three-stated, any registers
in the fanout of the clock can lose state.

WHAT NEXT

Verify that the circuit is safe according to your design rules. The PrimeTime
product assumes the generated clock is valid.

UITE-211 (Error) The -edges spec of generated clock '%s' has edge number
 less than 1, the edge number should be from 1 up.

DESCRIPTION

The -edge specification in creat_generated_clock command should use edge number of
the master clock which should be from 1 up. Zero or negative number are not allowed.

WHAT NEXT

Change your -edge spec in create_generated_clock coommand.

UITE-212 (Error) In the -edge specification of create_generated_clock '%s', the edge numbers must be in increasing order.

DESCRIPTION

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order.

WHAT NEXT

Check the -edge spec in create_generated_clock command and edge numbers increasing.

UITE-213 (Warning) clock port '%s' cannot be assigned input delay relative to clock '%s'. Ignoring the value.

DESCRIPTION

When setting an input delay on clock port, it must be specified relative to the same clock. If a different clock is specified, this setting is ignored.

WHAT NEXT

Remove the unneeded input delay value using the **remove_input_delay** command.

UITE-214 (Information) Updating %-35s

DESCRIPTION

Shows the progress of update timing. The update timing can happen explicitly by calling update_timing or implicitly by calling one of the commands that need update timing.

UITE-215 (warning) Ignoring -significant_digits option with -

connections.

DESCRIPTION

Since the output of report_net with the -connections option formats the output according to the number of significant digits necessary, the -significant_digits option is ignored.

UITE-216 (warning) Object '%s' is not a valid %s.

DESCRIPTION

The specified object is neither a valid timing startpoint nor endpoint. Commands such as **set_false_path**, **set_multicycle_path**, and **group_path** require the **-from** option *from_list* objects to be valid timing startpoints and the **-to** option *to_list* objects to be valid timing endpoints.

One important limitation to note is that the call to **update_timing** command may cause the creation of path endpoints at combinational pins. One major example is clock gating checks if the pin connects to the signal gating the clock signal. In that case, entering an exception before an **update_timing** would emit this message, whereas doing so after an **update_timing** would not.

WHAT NEXT

Use input ports or register clock pins for the *from_list* objects. Use output ports or register data pins for the *to_list* objects.

SEE ALSO

group_path (2), **set_false_path** (2), **set_multicycle_path** (2), **update_timing** (2).

UITE-217 (warning) Forcing pin '%s' to be a timing %s.

DESCRIPTION

The specified pin is neither a valid timing startpoint nor endpoint. The **set_max_delay** and **set_min_delay** commands are point-to-point timing exception commands. In this case, these commands override the default single-cycle timing relationship for affected timing paths, so the matched component of each path has a new startpoint (if you specify the **-from** option) and a new endpoint (if you specify the **-to** option). The remaining portions of the path are left unconstrained at the specified pin.

WHAT NEXT

PrimeTime assumes the behavior described above is intended. If not, use input ports or register clock pins for the **from** *from_list* objects, and output ports or register data pins for the **-to** *to_list* objects.

SEE ALSO

set_max_delay (2), **set_min_delay** (2).

UITE-218 (Warning) set_clock_groups overwrote existing false paths.

DESCRIPTION

The **set_clock_groups** command won't analyze the paths between exclusive and asynchronous clocks. Previous manually defined false paths between these exclusive and asynchronous clocks will be removed by **set_clock_groups** command.

WHAT NEXT

Use the **report_exceptions** command to see the existing false paths. To undo the **set_clock_groups**, use the **remove_clock_groups** command.

SEE ALSO

set_false_path(2), set_clock_groups(2), remove_clock_groups (2), **report_exceptions(2).**

UITE-219 (warning) Exception overwrites a previous exception of the same type.

DESCRIPTION

The entered exception overwrites a previously entered exception that is of the same type: false path, multicycle path, min or max delay. The overwritten exception uses the same design objects in the specification. Part or all of the former exception will be discarded.

WHAT NEXT

Make sure that the appropriate exceptions are set to the desired design paths. Note that discarded exceptions will not appear as ignored in report_exceptions.

set_false_path (2), **set_multicycle_path** (2), **set_max_delay** (2), **set_min_delay** (2), **report_exceptions** (2).

UITE-220 (information) Design exceptions have been modified.

DESCRIPTION

Some user-entered false paths, multi-cycle paths, min or max delays, were cleaned up by the **transform_exceptions** command. While this clean up removed ignored path specifiers from the original specifications, the design paths utilization of the exceptions is unchanged.

WHAT NEXT

Refer to the man page for **transform_exceptions(2)** for more details.

UITE-221 (error) Transformation options %s are mutually exclusive.

DESCRIPTION

The **transform_exceptions** command options **-remove_ignored**, **-flatten**, **-use_to_for_endpoints** cannot be specified for the same command invocation. Since these are different transformations with different requirements that can be order dependent, the user cannot intermix these transformations.

WHAT NEXT

Separate the indicated transformation options into separate calls to the **transform_exceptions** command.

SEE ALSO

transform_exceptions (2).

UITE-222 (error) The feedback pin '%s' , and the output pin '%s'

do not belong to the same PLL.

DESCRIPTION

The feedback pin specified using the **-pll_feedback** and the output pin specified using the **-pll_output** option of **create_generated_clock** command do no belong to the same PLL. Since these pins belong to different cells, there is no valid feedback path for the PLL.

WHAT NEXT

Define a valid configuration for the PLL, where the feedback pin is connected to an output clock pin on the PLL.

UITE-223 (error) The source pin '%s' does not belong to the PLL cell '%s'.

DESCRIPTION

The master pin specified using the **-source** does not belong to the same PLL to which the feedback pin specified by the **-pll_feedback** belongs. During the defining of a PLL and its feedback path, the master pin specified using the **-source** option should be the reference clock pin of the PLL.

WHAT NEXT

Define a valid configuration for the PLL, where the master pin is the reference clock pin of the PLL.

UITE-300 (Error) %s '%s' in when expression: '%s' for libcell '%s'.

DESCRIPTION

There was an error while parsing the when expression for the specified library cell. Therefore, the when expression will be ignored.

WHAT NEXT

The library DB file has not been properly generated.

UITE-301 (Warning) Conflict in specifying '%s' with '%s'. Option '%s' will be used.

DESCRIPTION

```
The listed command options cause a conflict. The more specific option will be
chosen.
```

WHAT NEXT

```
Look at the manpage for this command for more information on command options.
```

UITE-302 (Warning) Negative clock uncertainty specified: %g

DESCRIPTION

```
You specified a negative value to set_clock_uncertainty.
```

```
Typically, clock uncertainty should be positive. Negative uncertainty values are
supported for constraining designs with complex clock relationships. Setting the
uncertainty value to a negative number may lead to optimistic timing analysis and
should be used with extreme care.
```

WHAT NEXT

```
Ensure that you really wanted a negative value.
```

UITE-303 (warning) Setting input delay on clock port '%s'. This will not be supported in future releases.

DESCRIPTION

```
The setting of an input delay on a clock port that does not fanout to a latch D pin
is interpreted as clock source latency. However, this feature will not be supported
in future releases.
```

WHAT NEXT

Use the **set_clock_latency** command with the **-source** option to specifically set clock source latency.

UITE-304 (warning) Setting input delay on clock port '%s', which also has a source latency. Input delay will be ignored.

DESCRIPTION

The setting of an input delay on a clock port that does not fanout to a latch D pin is interpreted as clock source latency. However, the clock also has a defined source latency, so the input delay is ignored.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-305 (warning) Converting a propagated clock '%s' to an ideal clock.

DESCRIPTION

The direct setting of a clock network latency on a propagated clock converts it to a ideal clock.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-306 (Error) The %s command requires all clocks are active.

DESCRIPTION

You receive this error message because there is inactive clocks in the design. The

characterize_context require all clocks in the design are active.

WHAT NEXT

To active all clocks in the design, use the **set_active_clocks [all_clocks]** command. To report clock status, use the **report_clock** command.

SEE ALSO

set_active_clocks (2), **report_clock** (2).

UITE-307 (error) Clock %s exists in more than one group.

DESCRIPTION

The **set_clock_groups** command allows each clock can be defined in only one clock group.

WHAT NEXT

To define multiple groups related to the same clock, use multiple **set_clock_groups** commands.

SEE ALSO

set_clock_groups(2).

UITE-308 (Error) Clock group %s does not exist.

DESCRIPTION

All names must be predefined by the **set_clock_groups**.

WHAT NEXT

Use the **set_clock_groups** command to define clock groups. Use the **report_clock** command with -groups option to see existing clock groups.

SEE ALSO

remove_clock_groups(2), set_clock_groups(2), report_clock(2).

UITE-309 (warning) Exclusive or asynchronous clock groups specification supercedes
  set_false_path between clocks.

DESCRIPTION

A preceding **set_clock_groups** command already dictates that paths between some or all of the clocks specified in the current **set_false_path** exception will not be analyzed. Therefore, the exception will not be entered into PrimeTime and would not show in the output of the **report_exceptions** command. Note that if the exception specifies more clocks than present in the asynchronous or exclusive groups, then a reduced exception is entered such that this reduced exception is a subset of the original that only specifies clock to clock pairs not in the asynchronous or exclusive groups.

WHAT NEXT

Use **report_clock -groups** to view the current asynchronous or exclusive clock groups. Use the **remove_clock_groups** command to remove existing clock groups, if desired.

SEE ALSO

report_clock(2), set_clock_groups(2), remove_clock_groups(2), set_false_path(2).

UITE-310 (warning) CRPR command options will be discontinued in future releases.

DESCRIPTION

The user interface to clock reconvergence pessimism removal (CRPR) has changed. The following discontinued options:

-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are replaced with the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

In future releases, use of the discontinued options will cause a syntax error.

WHAT NEXT

Use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the

discontinued options. For details on backward compatibility, see the
timing_remove_clock_reconvergence_pessimism man page.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2),
timing_remove_clock_reconvergence_pessimism. (3).

UITE-311 (error) CRPR command options cannot be used if the design is up to date.

DESCRIPTION

Until the following discontinued options:

-remove_clock_reconvergent_pessimism and
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are
completely removed, limited backward-compatibility support is provided: If the
design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to **TRUE**. If the design is up to date, then the command fails.

WHAT NEXT

Use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the
discontinued options. For more detail on backward compatibility, see the
timing_remove_clock_reconvergence_pessimism variable man page.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2), **update_timing** (2),
timing_remove_clock_reconvergence_pessimism. (3).

UITE-312 (information) Variable timing_remove_clock_reconvergence_pessimism was set to

TRUE.

DESCRIPTION

Until the following discontinued options:

-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism

of the **report_timing**, **report_constraint**, and **get_timing_paths** commands are completely removed, limited backward-compatibility support is provided. If the design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to **TRUE**. If the design is up to date, then the command fails.

WHAT NEXT

Update your scripts to use the new **timing_remove_clock_reconvergence_pessimism** variable instead of the discontinued command options.

SEE ALSO

get_timing_paths (2), **report_constraint** (2), **report_timing** (2), **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-313 (Information) '%s' has been renamed to '%s'.

DESCRIPTION

You receive this message because the -*exclusive* option has been renamed to -*logically_exclusive* since -*physically_exclusive* is added.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set. To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-314 (warning) Converting pin '%s' from propagated to ideal.

DESCRIPTION

Setting a clock network latency on a pin or port directly will convert all the latches in the transitive fanout to ideal if they were marked propagated before.

WHAT NEXT

Please verify that this is the intended behaviour.

UITE-315 (warning) Converting %s object '%s' from ideal to propagated.

DESCRIPTION

The direct setting of a propagated_clock attribute on a clock, pin, or port can convert all latches in the transitive fanout to propagated. This occurs if they were already marked ideal and had some network latencies set. The user-specified network latencies are removed and can not be recovered. This message is generated if you use the **set_propagated_clock** command on the objects (pin, port or clock) after setting network latencies by using the **set_clock_latency** command on the same objects.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2), **set_propagated_clock** (2).

UITE-316 (warning) Virtual clock '%s' cannot be made propagated.

DESCRIPTION

A virtual clock cannot be made propagated as it has no source and does not affect any register in the design.

WHAT NEXT

```
Remove the virtual clock from the clock list.
```

SEE ALSO

remove_clock (2).

UITE-317 (error) Exception is not set because no through objects could be found.

DESCRIPTION

```
The object list of the exception path is empty at the from, to, or through position.
This might happen if the specified object in the command line is a net that does not
have any global driver or is a cell with no output pins.
```

WHAT NEXT

```
Verify that this is the intended behavior.
```

UITE-318 (Warning) Clock groups with same clocks are already set.

DESCRIPTION

```
You receive this warning message because the clock groups you specified are already
set by previous command.
```

WHAT NEXT

```
Use the report_clock with -groups option to check what clock groups have been set.To
remove the existing clock groups, use the remove_clock_groups command.
```

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-319 (warning) Setting clock latency on a non-clock pin or

port.

DESCRIPTION

The direct setting of a clock network latency on a non-clock pin or a port converts all latches in the transitive fanout to an ideal clock.

WHAT NEXT

Verify that this is the intended behavior.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-400 (Error) No sequential clock pins in '%s' or its transitive fanout.

DESCRIPTION

You receive this message if you execute **report_clock_timing** with an input pin list (either *from_list* or *to_list*) that does not contain any sequential clock pins, nor any in the pins' transitive fanout. All pins in the *from_list* and *to_list* lists must be sequential clock pins, or must contain them in their transitive fanout.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins in the *from_list* or *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

SEE ALSO

report_clock_timing (2).

UITE-401 (Warning) Pins that are not sequential clock pins and contain no sequential clock pins in their transitive fanout have

been dropped from '%s'.

DESCRIPTION

You receive this message if the list of input pins submitted to **report_clock_timing** in the *to_list* or *from_list* contains pins that are not sequential clock pins, and do not have sequential clock pins in their transitive fanout. Such pins are not valid inputs to **report_clock_timing**. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

SEE ALSO

report_clock_timing (2).

UITE-402 (Error) No pins specified by the given '%s' belong to the

specified clock domains.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and none of the pins on the input pin list (either *from_list* or *to_list*) belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *clock_list*.

SEE ALSO

report_clock_timing (2).

UITE-403 (Warning) Pins specified by the given '%s' that do not belong to the specified clock domains have been dropped from the current %s report.

DESCRIPTION

You receive this message if you execute **report_clock_timing** with an input pin list (either *from_list* or *to_list*), and some of the pins do not belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are clocked by at least one of the clocks in *clock_list*.

SEE ALSO

report_clock_timing (2).

UITE-404 (Error) 'from_list' and 'to_list' contain no pins that are clocked by the same clock; therefore, the skew cannot be reported.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and specify a skew report, but the *from_list* and *to_list*) do not contain any pins clocked by the same clock. Skew reports are produced by **report_clock_timing** only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in the *from_list* is intersected with the set of clock domains clocking any pin in the *to_list*. If this intersection is null, the skew report cannot continue.

WHAT NEXT

Reexecute the **report_clock_timing** command, and ensure that the *from_list* and *to_list* contain pins clocked by the same clock. If you do not specify the *clock_list*, ensure

that pins on the *from_list* and *to_list* belong to the same clock domain or set of domains.

SEE ALSO

report_clock_timing (2).

UITE-405 (Warning) Pins have been dropped from '%s', because they are
 not contained in the clock intersection with '%s'.

DESCRIPTION

You receive this message if you execute **report_clock_timing** and specify a skew report, but the *from_list* and *to_list* contain some pins that are not clocked by the same clock. Skew reports are produced by **report_clock_timing** only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in *from_list* is intersected with the set of clock domains clocking any pin in *to_list*. This message warns you that pins in either input list that are not part of any of these derived domains are being removed from the list of pins to report.

WHAT NEXT

This is a warning message only; no action is required on your part. In general, you can ignore this warning, because the **report_clock_network** command makes it easy to specify a superset of the clock pins of interest; the pruning referred to in this message is helpful to narrow down the superset of clock pins. However, if you have specified pins that you believe are part of a shared clock domain or set of domains, you should investigate why a sink pin in *to_list* is not included in ANY domain implied by *from_list*, or vice versa.

SEE ALSO

report_clock_timing (2).

UITE-406 (Error) No clock pins of '%s' sequential devices found.

DESCRIPTION

A skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the **report_clock_timing** command failed to produce these two sets of pins.

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-407 (Error) No clock pins of launching or capturing sequential
 devices are found.

DESCRIPTION

A latency or transition time report requires a set of clock pins capable of either launching or capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the **report_clock_timing** command failed to produce these pins.

WHAT NEXT

If you specify the *from_list* or *to_list* value, ensure that they contain clock pins of launching or capturing sequential devices, either explicitly or in their transitive fanout. If you specify the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-408 (Error) No sequential clock pins in '%s' or its transitive
 fanout are clocked.

DESCRIPTION

The specified list contains sequential device clock pins, but none of them are clocked.

WHAT NEXT

The specified input pin list (either the *from_list* or *to_list* value) must be part of the clock network of a defined clock. Check the clock definitions and the scope of their networks and determine if this is true.

SEE ALSO

all_clocks (2), **create_clock** (2), **report_clock** (2), **report_clock_network** (2), **report_clock_timing** (2).

UITE-409 (Error) No pins specified by the given '%s' belong to the
specified '%s'.

DESCRIPTION

You receive this message if you execute an inter-clock skew report using **report_clock_timing** and none of the pins on the input pin list, either *from_list* or *to_list*, belong to the clock domains specified by *from_clock_list* or *to_clock_list* respectively. At least one pin in both *from_list* and *to_list* must be clocked by one of the specified clocks.

WHAT NEXT

Reexecute the **report_clock_timing** command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

SEE ALSO

report_clock_timing (2).

UITE-410 (Warning) Pins specified by the given '%s' that do not belong to the specified '%s' have been dropped from the current inter-clock skew report.

DESCRIPTION

You receive this message if you execute an inter-clock skew report using **report_clock_timing** and some of the pins on the input pin list, either *from_list* or *to_list*, do not belong to any of the clock domains specified by *from_clock_list* or

to_clock_list respectively. All pins in the *from_list* and *to_list* should be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

WHAT NEXT

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the **report_clock_timing** command, and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

SEE ALSO

report_clock_timing (2).

UITE-411 (Error) No clock pins of '%s' sequential devices found.

DESCRIPTION

An intre-clock skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, *from_clock_list* and *to_clock_list* values specified in the **report_clock_timing** command failed to produce these two sets of pins.

WHAT NEXT

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify *from_clock_list* or *to_clock_list*, ensure that the clocks have associated networks (that they are not virtual clocks).

SEE ALSO

report_clock (2), **report_clock_timing** (2).

UITE-412 (Error) Pin '%s' is not the clock pin of a sequential

device.

DESCRIPTION

You receive this message if you execute **report_crpr** with an input pin (either
from_pin or *to_pin*) that is not a sequential clock pin. Both the *from_pin* and *to_pin*
must be sequential clock pins.

WHAT NEXT

Reexecute the **report_crpr** command and ensure that the *from_pin* and *to_pin* are
sequential clock pins.

SEE ALSO

report_crpr (2). **timing_remove_clock_reconvergence_pessimism.** (3).

UITE-413 (Warning) Searching unconstrained paths will take longer run-time than expected.

DESCRIPTION

The tool will search for unconstrained paths when constrained paths can not be
found, which will involve partial update timing, and takes longer time than
searching constrained paths.

WHAT NEXT

It is suggested that all paths in the design get constrained. The potential
unconstrained paths may be caused by black boxes, no launching or capturing clocks,
empty hierarchy, cells from IP instead of from library, etc. To check constraints in
the design, please use the **check_timing** command. Specifing the to_pin_list can also
reduce the number of endpoints to search and speed up the report timing process.

SEE ALSO

check_timing (2), **timing_report_status_level** (3), **report_timing** (2),
report_constraint (2).

UITE-414 (Error) CRPR is currently switched off.

DESCRIPTION

This error message is being issued because the user has attempted to use some functionality related to Clock Reconvergence Pessimism Removal (CRPR) when it is not turned on (see the **report_crpr** man page).

WHAT NEXT

Set the variable, **timing_remove_clock_reconvergence_pessimism** to TRUE and carry out a full update_timing in order to have CRPR included in the timing analysis.

SEE ALSO

report_crpr (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-416 (Warning) There %s %d invalid %s.

DESCRIPTION

When report_timing is specified with "*" or a cell name, there is possibility that many invalid startpoints or endpoints are gotten, such as **-from [get_pins FF/*]** includes input, output and asynchronous pins. The current behavior for PrimeTime will consider these invalid startpoints or endpoints as through points and continues the path searching. Even though it is convenient to use, it is not suggested since it usually takes longer run time.

WHAT NEXT

You can use filter to filter redundant or invalid objects, such as **-from [get_pins "FF/* -filter "is_clock_pin == true"]**. You also can use variable **timing_report_always_use_valid_start_end_points** to report using valid startpoints and endpoints only.

SEE ALSO

report_timing (2), **timing_report_always_use_valid_start_end_points** (3).

UITE-418 (Error) Could not find latch for pin '%s'.

DESCRIPTION

You receive this error message because the input clock pin (either *from_pin* or *to_pin*) you specified with the **report_crpr** command does not correspond to a sequential device or constrained port. Both the *from_pin* and *to_pin* must be sequential clock pins or constrained ports.

WHAT NEXT

Reexecute **report_crpr** and ensure that the *from_pin* and *to_pin* are sequential clock pins or constrained ports.

SEE ALSO

report_crpr (2); **timing_remove_clock_reconvergence_pessimism** (3).

UITE-421 (warning) Using the %s option to specify both launching and capturing clocks has been discontinued and will not be supported in future releases.

DESCRIPTION

The command **report_crpr** has been enhanced to account for cases where multiple clocks fan out to the clock pins of sequential devices. In order to account for this new behavior optional command arguments have been added to allow the user to specify the clocks incident on both the launching and capturing devices. See the man page for report_crpr for more detiails.

WHAT NEXT

After examining the man page repeat the command with the relevant arguments.

SEE ALSO

UITE-422 (warning) -leaf cannot be specified for pins/ports.

Ignoring -leaf.

DESCRIPTION

The all_connected command allows -leaf option to be specified for net objects. You are seeing this message because you specified -leaf for pins/ports.

WHAT NEXT

The command will proceed by ignoring the -leaf. So, you need not do anything.

UITE-423 (error) path_collection cannot be used with any other path search option.

DESCRIPTION

The path_collection is intended to be directly printed according to formatting options specified. No option that need path search, like -nworst, -from, -to etc. can be used with this option.

WHAT NEXT

Try use only print formatting options with path_collection.

UITE-424 (error) Regular path-based analysis works only when design is in on_chip_variation mode.

DESCRIPTION

Regular path-based analysis only recomputes paths when the analysis type of the design is set to *on_chip_variation*. When the analysis type is set to *single*, no recomputed paths are returned.

WHAT NEXT

Use **set_operating_conditions** to set the design to the *on_chip_variation* analysis mode.

UITE-425 (error) Cannot activate modes %s and %s on cell %s

as they are in the same mode group %s, no mode has been activated.

DESCRIPTION

```
It is not possible to activate more than one cell mode in a cell mode group at any
one time.
```

WHAT NEXT

```
Select only one cell mode per cell mode group
```

UITE-426 (error) Cannot perform regular PBA on unconstrained paths.

DESCRIPTION

```
Regular PBA only recomputes constrained paths and ignores unconstrained paths,
regardless of the value of the variable timing_report_unconstrained_paths. Also, the
unconstrained paths will not be returned in the resulting collection.
```

WHAT NEXT

```
Only perform path-based analysis on constrained paths.
```

UITE-427 (warning) Setting a %s derate on hierarchical net '%s', all other portions of this net will also use this derate factor.

DESCRIPTION

```
This message is issued if the user has set a net-specific derate factor on a
hierarchical portion of a global net. A global net is a net that spans a number of
hierarchies.
```

```
Since PrimeTime will calculate only one delay for the entire global net the derate
factor will be set for every net segment (hierarchical portion) in this global net.
```

WHAT NEXT

```
No user action required.
```

`set_timing_derate` (2), `report_timing_derate` (2).

UITE-428 (warning) Maximum of %d paths can be recalculated together.

DESCRIPTION

Regular path-based analysis is intended to remove pessimism from critical paths. Recalculating a huge number of paths can lead to significant runtime. If path-based analysis is performed on more paths than the limit, then only the worst paths up to the path limit will be recomputed and returned. This path limit does not include unconstrained paths that are skipped by regular path-based analysis.

WHAT NEXT

Please perform path-based analysis on small paths sets below the path limit. Alternatively, the **pba_disable_path_recalculation_limit** variable can be used to disable the path limit; however, please note that the runtime can be significant when recalculating large numbers of paths.

UITE-429 (warning) The timing path due to a data check constraint at pin '%s' has not been recalculated.

DESCRIPTION

PrimeTime does not support the path-based recalculation of paths due to data check constraints. These paths are returned directly without recalculation.

SEE ALSO

`get_timing_paths` (2), `report_timing` (2), `set_data_check` (2).

UITE-430 (warning) Variable timing_report_maxpaths_nworst_reached is suggested to use

with timing_report_always_use_valid_start_end_points.

DESCRIPTION

```
Variable timing_report_maxpaths_nworst_reached message may count more endpoints and
less max paths if invalid start/through/end points are specified.
```

UITE-432 (warning) The %s variable is obsolete as of the %s release.
  Do not use this variable as it is no longer supported.

DESCRIPTION

```
You received this message because you have set the indicated variable to a value
other than the default value of the variable.
```

```
As of the indicated release of PrimeTime, this variable is obsolete and will no
longer be supported in this or subsequent releases. In the indicated release,
PrimeTime will honor the setting of this variable and issue this warning message. In
subsequent releases, the behavior with default value of this variable will be
supported only, and the variable will be removed from PrimeTime.
```

WHAT NEXT

```
Please remove the settings of this variable.
```

UITE-433 (warning) The %s option is obsolete as of the %s release.
  Do not use this option as it is no longer supported.

DESCRIPTION

```
You received this message because you have used the indicated option of the command
you are running.
```

```
As of the indicated release of PrimeTime, this option is obsolete and will no longer
be supported in this or subsequent releases. In the indicated release, PrimeTime
will honor the usage of this option and issue this warning message. In subsequent
releases, the option will be removed from the command that you are running and you
will receive an error message when you use the option.
```

Please do not use this obsolete option of the command that you are running.

UITE-434 (warning) The %s option is obsolete as of the %s release.
Do not use this option as it is no longer supported.

DESCRIPTION

You received this message because you have used the indicated option of the report_timing or get_timing_paths command.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

This variable is obsolete and replaced with the usage of the variable timing_enable_preset_clear_arcs. By setting the value of this variable to the non-default value, you can obtain the same effect as with this obsoleted option. You will, however, incur the CPU cost of a full update when the value of the variable is changed. In order to minimize the CPU cost, please do not change the value of the variable frequently.

WHAT NEXT

Please set timing_enable_preset_clear_arcs variable to true instead.

UITE-435 (Information) %s

DESCRIPTION

Display messages when variable **timing_report_maxpaths_nworst_reached** sets to TRUE.

WHAT NEXT

SEE ALSO

UITE-436 (warning) Resetting a %s derate on hierarchical net

'%s', all other portions of this net will also use this derate factor.

DESCRIPTION

This message is issued if the user has reset a net-specific derate factor on a
hierarchical portion of a global net. A global net is a net that spans a number of
hierarchies.

Since PrimeTime will calculate only one delay for the entire global net the derate
factor will be reset for every net segment (hierarchical portion) in this global
net.

WHAT NEXT

No user action required.

SEE ALSO

reset_timing_derate (2).

UITE-437 (warning) Implicitly setting the '%s' option for the set_timing_derate command.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with an
object_list and has not explicitly set one of the net_delay, cell_delay or
cell_check options.

WHAT NEXT

Explicitly specify one of the net_delay, cell_delay or cell_check options. The
net_delay and cell_delay options may be specified together.

SEE ALSO

set_timing_derate (2).

UITE-438 (error) Ambiguous command. One of the net_delay,

cell_delay or cell_check options must be specified.

DESCRIPTION

This message is issued if the user has called the set_timing_derate command with an object_list and has not explicity set one of the net_delay, cell_delay or cell_check options and the object_list contains hierarchical cells.

WHAT NEXT

Explicitly specify one of the net_delay, cell_delay or cell_check options. The net_delay and cell_delay options may be specified together.

SEE ALSO

set_timing_derate (2).

UITE-445 (Information) %s

DESCRIPTION

Display messages when variable **timing_report_maxpaths_nworst_reached** sets to TRUE.

WHAT NEXT

SEE ALSO

UITE-446 (Warning) Enabling Clock Reconvergence Pessimism Removal (CRPR).

DESCRIPTION

This message is being issued because the user has enabled the adaptive CRPR engine (turned on by setting **timing_crpr_enable_adaptive_engine** to TRUE) when CRPR is turned off. The adaptive engine will only function when CRPR is turned on, hence CRPR has been enabled automatically.

See the man page for **timing_crpr_enable_adaptive_engine** for more details.

Update scripts to set the variable **timing_remove_clock_reconvergence_pessimism** to TRUE.

SEE ALSO

timing_crpr_enable_adaptive_engine (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-447 (Warning) Derate summary report may not match the output of report_timing without timing derates applied.

DESCRIPTION

This warning message is issued when the **report_timing** command has been called with the '-derate' option when the design has derate and signal integrity data and signal integrity analysis is enabled.

The derate summary report may not match the output of report_timing when there are no timing derates applied. Application of derates to aggressor nets will widen arrival windows thus making crosstalk interaction more likely. These additional crosstalk effects appear in the output of report_timing with derates applied. A full analysis with no derating applied would be required to remove these additional crosstalk effects.

If CRPR is on, then the clock reconvergence pessimism (due to derating) in the derate summary report shows the amount of CRP removed due to the static effect of derating. It is not possible to remove the additional crosstalk effects arising from derating.

WHAT NEXT

Reset the timing derates using the **reset_timing_derate** command and use report_timing to determine the effect of removing timing derates.

SEE ALSO

report_timing (2), **reset_timing_derate** (2), **si_enable_analysis** (2), **timing_remove_clock_reconvergence_pessimism** (3).

UITE-448 (Warning) Unrealistically large derate value specified:

%g

DESCRIPTION

This warning message is issued when the **set_timing_derate** command has been called with a derate value greater than 2.

A derate factor greater than 2.0 is unrealistically large. As a consequence, the values shown in the Derate Summary Report in the **report_timing** output may not be accurate.

WHAT NEXT

It is likely that the specified derate value is incorrect, because of a user input error. Please specify a more realistic derate factor within the range [0 to 2].

SEE ALSO

report_timing (2), **set_timing_derate** (2).

UITE-450 (Warning) Transferring ideal net attribute onto driver pin '%s' of net '%s'.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it's driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

WHAT NEXT

No action is required.

SEE ALSO

set_ideal_network (2).

UITE-451 (Warning) Ignoring hierarchical pin '%s'. Object must

be a port, net or pin of a leaf cell.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with a
hierarchical pin in the object_list. You cannot specify a hierarchical pin as an
ideal network start point.

PrimeTime ignores the hierarchical pin specified in the warning message, but
continues to set ideal networks on any remaining valid objects in the object_list.

WHAT NEXT

Specify only ports, nets or pins of leaf cells in the object_list. A leaf cell is a
cell that does not contain other cells.

SEE ALSO

set_ideal_network (2).

UITE-452 (Warning) Ignoring net '%s' because the 'no_propagate' option is not specified.

DESCRIPTION

This warning message occurs when the set_ideal_network command is called with nets
specified in the object_list and the 'no_propagate' option has not been specified.

WHAT NEXT

To set a net ideal use the 'no_propagate' option.

SEE ALSO

set_ideal_network (2).

UITE-453 (Warning) Overwritting previous ideal network that

was set on pin '%s'.

DESCRIPTION

This warning message occurs when the user sets an ideal network on a pin, which already has an ideal network set on it. The previous ideal network that was set on the pin is overwritten with this ideal network set on the pin.

WHAT NEXT

No action is required.

SEE ALSO

set_ideal_network (2).

UITE-454 (Warning) Ignoring hierarchical pin '%s'. Object must be a port or pin of a leaf cell.

DESCRIPTION

This warning message occurs when the set_ideal_latency command or set_ideal_transition command is called with a hierarchical pin in the object_list. You cannot annotate ideal timing values on a hierarchical pin.

PrimeTime ignores the hierarchical pin specified in the warning message, but continues to set ideal values on any remaining valid objects in the object_list.

WHAT NEXT

Specify only ports or pins of leaf cells in the object_list. A leaf cell is a cell that does not contain other cells.

SEE ALSO

set_ideal_network (2), **set_ideal_latency** (2), **set_ideal_transition** (2).

UITE-455 (Warning) Removing ideal attribute from driver pin

'%s' of net '%s'.

DESCRIPTION

This warning message occurs when the remove_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it's driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

WHAT NEXT

No action is required.

SEE ALSO

remove_ideal_network (2).

UITE-456 (Warning) Ideal timing is specified on the non-ideal %s.

DESCRIPTION

This warning message occurs if the user has annotated ideal latency and/or ideal transition values on a pin or port that is not part of an ideal network. The annotated ideal timing values will only take effect if the object is part of an ideal network.

WHAT NEXT

If you intend to apply the annotated ideal timing values, then set an an network on the pin or port using the set_ideal_network command.

If you do not intend to apply annotated ideal timing values on the object, then remove the annotated ideal timing values using the remove_ideal_latency command and/or the remove_ideal_transition command.

SEE ALSO

set_ideal_network (2), **set_ideal_latency** (2), **set_ideal_transition** (2), **remove_ideal_latency** (2), **remove_ideal_transition** (2).

UITE-457 (Error) '%s' and '%s' are already defined as '%s' not allowing paths.

DESCRIPTION

You receive this error message because the *-allow_paths* defined by asynchronous clock groups is conflict with false path set by either the asynchronous, physically exclusive or logically exclusive clock groups for the same clock pair.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-458 (Error) '%s' and '%s' are already defined as -allow_paths in asynchronous clock groups.

DESCRIPTION

You receive this error message because the clock pair is already defined as asynchronous clock relationships which allow paths between these two clocks.

WHAT NEXT

Use the **report_clock** with -groups option to check what clock groups have been set.To remove the existing clock groups, use the **remove_clock_groups** command.

SEE ALSO

set_clock_groups (2), **remove_clock_groups** (2), **report_clock** (2).

UITE-459 (Error) Reference pin '%s' is not reached by any clock.

DESCRIPTION

You receive this error message because the input or output delay you defined on a pin or port with respect to a reference pin, which is not a fanout of any clock network. In case of no clock propagates to reference pin, the defined input/output delay will be ignored.

WHAT NEXT

It is suggested that reference pin for input/output delay constraints should be in the fanout of clock network. Please verify the connection of reference pin and modified the reference pin if needed.

SEE ALSO

set_input_delay (2), **remove_input_delay** (2), **set_output_delay** (2), **remove_output_delay** (2).

UITE-460 (Warning) Overwriting previously defined AOCVM value: %s.

DESCRIPTION

You received this warning message because the AOCVM value you have specified has overwritten a previously defined AOCVM value of the same type.

WHAT NEXT

No action is required. Use the **report_aocvm** command to show the AOCVM information that been defined.

SEE ALSO

set_aocvm_coefficient (2), **report_aocvm** (2).

UITE-461 (Error) Generated clock '%s' '%s' is not satisfiable%s

DESCRIPTION

This is an error message whenever the clock network traversal can not find a path

which satisfies the sense relationship defined by create_generated_clock command.

WHAT NEXT

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with -divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, PrimeTime will issue the warning message. In this case, generated clock source pin should be redefined to clock pin of divider.

UITE-462 (Error) No constant bounding derates have been defined.

DESCRIPTION

You have received this message because you have attempted to perform a path-based AOCVM analysis using either the **report_timing** command or the **get_timing_paths** command, but no constant timing derates have been defined.

Constant derates are required to pessimistically bound derates calculated during a path-based AOCVM analysis. PrimeTime aborted the AOCVM analysis, because there are no constant derates and so there is no OCV pessimism for AOCVM to remove.

WHAT NEXT

Define constant bounding derates using the **set_timing_derate** command. Alternatively, consider using the graph-based AOCVM analysis, which *automatically* determines tight non-optimistic bounding derates for the path-based AOCVM analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
set_timing_derate (2),
report_timing_derate (2),
timing_aocvm_enable_analysis (3).

UITE-463 (Error) No AOCVM derate factors have been defined.

PrimeTime cannot continue with AOCVM analysis.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis, but no AOCVM derate factors have been defined. An AOCVM analysis requires AOCVM derate factors.

AOCVM derate factors are specified using the **read_aocvm** command.

WHAT NEXT

Either define AOCVM derate factors using the **read_aocvm** command.

SEE ALSO

read_aocvm (2), **report_aocvm** (2).

UITE-464 (Warning) No coordinates locations have been defined; AOCVM analysis may be inaccurate.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis, but no coordinates locations have been defined.

Coordinates locations are used to calculate the systematic component of an AOCVM derate factor. The coordinates of various nodes of nets, pins, and ports are imported into PrimeTime from parasitic files using the **read_parasitics** command.

PrimeTime will continue with the AOCVM analysis and assume the most pessimistic coordinates locations possible.

WHAT NEXT

Set the **read_parasitics_load_locations** variable to **true** and read parasitics using the **read_parasitics** command.

SEE ALSO

report_timing (2), **get_timing_paths** (2), **read_parasitics** (2), **read_parasitics_load_locations** (3).

UITE-465 (Warning) No clock paths found. AOCVM requires a 'full_clock_expanded' path for an accurate analysis.

DESCRIPTION

You have received this message because you have attempted to perform an AOCVM analysis on a path, but the clock path has not been included.

PrimeTime will continue with the AOCVM analysis, however the analysis may be inaccurate due to the lack of information.

WHAT NEXT

Use the **get_timing_paths** command with the **-path_type** option to obtain a path with it's associated clock path.

SEE ALSO

get_timing_paths (2), **report_timing** (2).

UITE-466 (Warning) Ignoring hierarchical cell '%s'. Object must be a leaf cell or a library cell.

DESCRIPTION

This warning message occurs when the set_aocvm_coefficient command is called with a hierarchical cell in the object_list. You cannot annotate AOCVM coefficients on a hierarchical cell.

PrimeTime ignores the hierarchical cell specified in the warning message, but continues to set AOCVM coefficient values on any remaining valid objects in the *object_list*.

WHAT NEXT

Specify only leaf cells or library cells in the *object_list*. A leaf cell is a cell that does not contain other cells.

SEE ALSO

set_aocvm_coefficient (2), **report_aocvm** (2).

UITE-467 (Error) AOCVM and Variation-Aware analyses are mutually exclusive; PrimeTime will disable the AOCVM analysis.

DESCRIPTION

You have received this message because you have attemtped to perform an AOCVM analysis and a Variation-Aware analysis together. The analyses cannot be performed together.

WHAT NEXT

If you intend to perform a Variation-Aware analysis only, then no action is required.

If you intend to perform an AOCVM analysis, then you must disable Variation-Aware analysis, which is controlled using the PrimeTime variable **variation_enable_analysis**.

SEE ALSO

get_timing_paths (2), **report_timing** (2), **timing_aocvm_enable_analysis** (3), **variation_enable_analysis** (3).

UITE-468 (Information) The CRP value reported by report_timing and report_clock_timing will be %s.

DESCRIPTION

You are receiving this message because the report_crpr command has detected that its corresponding report_timing (or report_clock_timing) command is using a smaller CRP value. The report_crpr command reports the exact CRP value whereas report_timing (and report_clock_timing) use values calculated considering the CRPR threshold. This difference is a product of performance optimizations that are outlined in the next paragraph.

In order to prevent performance degradation during update_timing, CRPR groups sequential devices with similar CRP values (i.e. the difference between the CRP values is within the value of the crpr threshold). This can lead to some paths using a CRP value that will be smaller than the exact CRP. The difference between the two will be bounded by the value of the CRPR threshold.

WHAT NEXT

In order to align the CRP values used by report_timing, report_clock_timing and report_crpr the crpr threshold may be set to a smaller value. It should be noted that this can cause significant performance degradation during subsequent timing

updates.

SEE ALSO

timing_crpr_threshold_ps (3),

UITE-469 (error) Unable to set %s on '%s'.

DESCRIPTION

Failed to execute the given set operation on the specified object.

WHAT NEXT

UITE-472 (Error) You cannot specify the -aocvm_guardband option of set_timing_derate in the derate_list of the timing_aocvm_derate_list variable.

DESCRIPTION

You have received this message because you have attempted set guardband derate factors using the **-aocvm_guardband** option of the **set_timing_derate** command in the *derate_list* of the **timing_aocvm_derate_list** variable.

WHAT NEXT

Remove the **-aocvm_guardband** option.

SEE ALSO

set_timing_derate (2), **timing_aocvm_derate_list** (3).

UITE-473 (Error) You cannot specify the -aocvm_guardband option of set_timing_derate in the pba_derate_list variable.

DESCRIPTION

You have received this message because you have attempted set AOCVM guardband derate factors using the **-aocvm_guardband** option of the **set_timing_derate** command in the

`pba_derate_list` variable. This usage is not permitted.

WHAT NEXT

Remove the **-aocvm_guardband** option.

SEE ALSO

set_timing_derate (2), **pba_derate_list** (3).

UITE-474 (Warning) The option '%s' is now the default and will be removed from the UI in a later release. You can use '%s' to get the old default behavior.

DESCRIPTION

You have received this message because you have issued an option that is now the default option on the command and will be removed from the UI in a later release.

WHAT NEXT

Remove the option for future.

SEE ALSO

UITE-476 (Error) Graph-based AOCVM analysis must be performed in 'on_chip_variation' mode.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the 'single' or 'bc_wc' analysis mode, which is not supported.

WHAT NEXT

Use the **set_operating_conditions** command to set the design into 'on_chip_variation' mode.

UITE-477 (Error) Graph-based delay-weighted AOCVM analysis cannnot be performed in worst_arrival mode.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the design is in worst_arrival mode.

WHAT NEXT

Set the **timing_slew_propagation_mode** variable to "worst_slew" and set the **si_xtalk_delay_analysis_mode** variable to "all_paths" if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode.

SEE ALSO

si_xtalk_delay_analysis_mode (3), **timing_slew_propagation_mode** (3), **timing_aocvm_analysis_mode** (3), **timing_aocvm_enable_analysis** (3).

UITE-478 (Error) Graph-based delay-weighted AOCVM analysis cannnot be used when the si_use_driving_cell_derate_for_delta_delay variable is set to true.

DESCRIPTION

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the **si_use_driving_cell_derate_for_delta_delay** variable is set to *true*.

WHAT NEXT

Set the **si_use_driving_cell_derate_for_delta_delay** variable to *false* if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode. Otherwise, if you need to use the **si_use_driving_cell_derate_for_delta_delay** variable, turn off graph-based AOCVM using the **timing_aocvm_enable_analysis** variable.

`si_use_driving_cell_derate_for_delta_delay` (3), `timing_aocvm_analysis_mode` (3), `timing_aocvm_enable_analysis` (3).

UITE-479 (Warning) Exhaustive path-based analysis may take a long time using the current PrimeTime settings. Try using the following settings, which may reduce the runtime of the analysis:%s

DESCRIPTION

You have received this message because you have attempted to perform an exhaustive path-based analysis using settings that may considerably degrade the runtime of the analysis.

WHAT NEXT

The warning message suggests settings that should be changed to improve the runtime of the analysis.

SEE ALSO

`report_timing` (2),
`get_timing_paths` (2),
`pba_aocvm_only_mode` (3),
`timing_aocvm_analysis_mode` (3),
`timing_aocvm_enable_analysis` (3),
`timing_remove_clock_reconvergence_pessimism` (3),
`timing_report_use_worst_parallel_cell_arc` (3).

UITE-480 (Warning) The exhaustive path-based recalculation limit of %d has been exceeded at endpoint '%s' and group '%s'. The worst PBA slack found at this endpoint was %g. It is known that no PBA paths with slack worse than %g exist at this endpoint for this group.

DESCRIPTION

You have received this message because the user specified path-based endpoint recalculation limit has been met during an exhaustive search for worst paths at this

endpoint. This message gives details on the endpoint that has not been exhaustively searched.

WHAT NEXT

Exhaustive path recalculation is a last mile analysis technique and as a result it should only be used when the design is close to signoff. Try to recalculate the endpoint using conservative values for slack_lesser_than, nworst and max_paths.

Increasing the user specified path-based endpoint recalculation limit may allow the endpoint to be exhaustively searched, however this will increase the runtime of the analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_exhaustive_endpoint_path_limit (3),
timing_aocvm_analysis_mode (3).

UITE-482 (Error) Cannot specify a value for nworst (%d) greater than the exhaustive path-based recalculation limit (%d). Setting nworst to %d.

DESCRIPTION

You have received this message during a exhaustive path-based recalculation. An exhaustive path-based limit applies during this analysis and the user specified nworst value cannot exceed this limit.

WHAT NEXT

Set a conservative value for nworst. If necessary increase the path-based endpoint recalculation limit, however this will increase the runtime of the analysis.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_exhaustive_endpoint_path_limit (3),
timing_aocvm_analysis_mode (3).

UITE-485 (Error) Setting input delay on a clock port (%s) that

does not fanout to any data sink.

DESCRIPTION

A set_input_delay was set on this clock input port. However, this input port has no data sinks, so the input delay has no effect. To specify clock latency instead of data input delays, the set_clock_latency command should be used.

Note that simultaneous clock/data timing is not supported. A data input delay set on a clock port is ignored.

WHAT NEXT

Be sure to use set_clock_latency with the -source option to specifically set clock latency. If a data sink is expected in the fanout of this input port, check the design.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-486 (Error) Cannot specify a value for the pba_derate_list variable in an AOCVM context.

DESCRIPTION

You have received this message because you attempted to perform a path-based AOCVM analysis and you specified a value for the **pba_derate_list** variable.

WHAT NEXT

To perform a path-based AOCVM analysis, set the **pba_derate_list** variable to "". Otherwise, to use the derates specified in the **pba_derate_list** variable, you must remove all AOCVM information using the **remove_aocvm** command.

SEE ALSO

get_timing_paths (2), **report_timing** (2), **remove_aocvm** (2), **pba_derate_list** (3).

UITE-487 (Warning) AOCVM path-based analysis can take a

long time if path-specific slew propagation is also performed.

DESCRIPTION

The **-pba_mode** option on **report_timing** (and **get_timing_paths**) instructs PrimeTime to perform both AOCVM PBA and regular PBA (path-specific slew propagation). The analysis runtime is significantly improved if only AOCVM path-based analysis is performed.

This message is only displayed once per session.

WHAT NEXT

If you intended to perform AOCVM and regular path-based analyses, then no action is required.

If you intended to perform only AOCVM path-based analysis, then set the **pba_aocvm_only_mode** variable to true.

SEE ALSO

report_timing (2),
get_timing_paths (2),
pba_aocvm_only_mode (3),

UITE-488 (warning) Setting input delay on clock port ('%s') that has data sink(s). The behavior will change in future releases.

DESCRIPTION

The setting of an input delay on a clock port that has data sink(s) is also interpreted as clock source latency. However, this feature will not be supported in future releases.

WHAT NEXT

Use the **set_clock_latency** command with the **-source** option to specifically set clock source latency.

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UITE-489 (Error) Setting input delay on clock port ('%s') relative to a clock (%s) defined at the same port. Command is ignored.

DESCRIPTION

```
The setting of an input delay on a clock port relative to a clock defined at the
same port is ignored. The same signal at the port cannot be delayed relatif to
itself.
```

WHAT NEXT

```
Please make review the constrainst. Input delay can be set at the clock port, but
relative to a clock defined at another port.
```

SEE ALSO

remove_clock_latency (2), **set_clock_latency** (2).

UPF-001 (error) Cell '%s' is already in the extent of power domain '%s'

DESCRIPTION

```
A cell cannot belong to multiple power domains.
```

WHAT NEXT

```
Remove this cell from the list and re-run this command.
```

UPF-002 (warning) UPF version '%s' was requested but the tool supports '%s'

DESCRIPTION

```
The requested version of UPF syntax standard is different from the version supported
by the tool.
```

WHAT NEXT

```
Review which commands and options in your design scripts are not compliant with the
version supported by the tool. Replace the commands and options by supported syntax
if possible. Request the tool support team to add support for the other UPF version
of the standard.
```

UPF-003 (error) Power domain '%s' already contains primary power and ground supply nets.

DESCRIPTION

```
The primary power and ground supply nets have already been specified earlier. A
power domain can have only one set of primary and ground supply nets.
```

WHAT NEXT

```
The primary supply nets of a power domain cannot be changed once assigned. Do not
```

attempt to set them again.

UPF-004 (error) The '%s' option of %s command must specify exactly one %s.

DESCRIPTION

This option of the command takes exactly one of the specified object type.

WHAT NEXT

Check the command man page for more details and correct it accordingly.

UPF-005 (error) The -reuse option can only be used to reuse the supply net within another power domain in the same scope.

DESCRIPTION

The supply net object can only be resued in another power domain belonging to the same scope as the other power domains where the supply net object exists. Supply net objects cannot be reused across hierarchical scopes.

WHAT NEXT

Create a new supply_net and connect it through supply ports if you would like to extend this net across another power domain in another scope.

UPF-006 (error) The %s object cannot be created because %s of name %s already exists.

DESCRIPTION

The given object already exists. Names are expected to be unique in a given scope.

WHAT NEXT

Create a new object with a different name.

If you are using the create_supply_net command, please specify -reuse option to

reuse a supply net.

If you are using create_supply_net or create_supply_port command, the names cannot
be same as existing gnl nets and gnl ports.

UPF-007 (error) The given supply net already exists in this domain.

DESCRIPTION

The given object already exists in the given domain. Names are expected to be unique
in a given scope.

WHAT NEXT

Create a new object with a different name.

If you are using the create_supply_net command, please specify -reuse option to
reuse a supply net.

UPF-008 (Information) The option -vct will be ignored in PrimeTime.

DESCRIPTION

The value specified by option -vct refers to a value conversion table that is
created by command create_upf2hdl_vct which is not needed by PrimeTime for timing
analysis purposes. So this option will be ignored in PrimeTime.

UPF-009 (Error) The value specified by % can not be greater than the value specified by %s.

DESCRIPTION

You are receiving this error message because a set_voltage command has been
specified with dynamic component values that are greater than their associated
voltages. The dynamic component values must be less than the voltages (-min_voltage,
max_voltage) specified with the command.

Adjust the dynamic component values and re-issue the command.

UPF-010 (Error) Cannot open file '%s'.

DESCRIPTION

The file name provided to **load_upf** cannot be opened. Possible reasons for this are that the file does not exist in the search path specified or that it does not have read permissions.

WHAT NEXT

Verify the location of the file to be read on and its permissions. Once the file has been verified re-run **load_upf**.

UPF-011 (Error) Cannot set isolation on pin or port %s

DESCRIPTION

The pin or port must be in the same domain as the isolation strategy.

WHAT NEXT

Compare relevant set_isolation and create_power_domain -elements commands and correct.

UPF-012 (error) The '%s' option of create_power_switch command must specify exactly one pair of %s.

DESCRIPTION

This option of create_power_switch command takes exactly one port on the switch and the net where the port connects.

WHAT NEXT

Check the command man page for more details and correct it accordingly.

UPF-013 (error) Net '%s' specified for "create_power_switch -control_port

DESCRIPTION

```
Please check the signal net specified for option -control_port in command
create_power_switch. Please Make sure that it exists in the current scope.
```

WHAT NEXT

```
Check the command man page for more details and correct it accordingly.
```

UPF-014 (error) Supply net '%s' specified for command create_power_switch is not defined.

DESCRIPTION

```
Please check the supply net specified for options -input_supply_port and -
output_supply_port in command create_power_switch. Make sure that the supply nets
exist in the current_scope.
```

WHAT NEXT

```
Check the command man page for more details and correct it accordingly.
```

UPF-015 (warning) Cannot set retention on cell %s which is not of retention type.

DESCRIPTION

```
Retention can only be set of hierarchical blocks or leaf cells with retention
information in the Liberty model. The retention strategy is not applied for the
above mentioned cell (is ignored).
```

WHAT NEXT

```
Ensure that all retentions cells have necessary retention information in Liberty
(.lib). Refer to the Liberty standard on retention_cell attribute. If you cannot
correct the Liberty model for the above cell then you can explicitly connect power
and ground retention pins by connect_supply_net.
```

`set_retention` (2), **`connect_supply_net.`**

UPF-016 (error) The '%s' option of create_power_switch command is not specified.

DESCRIPTION

This option of create_power_switch command is a required option.

WHAT NEXT

Check the command man page for more details and correct it accordingly.

UPF-017 (error) The '%s' option of create_power_switch command must specify exactly one set of %s.

DESCRIPTION

This option of create_power_switch command takes exactly one set of a named state, the input_supply_port for which this is defined, and its corresponding Boolean function.

WHAT NEXT

Check the command man page for more details and correct it accordingly.

UPF-018 (error) The input_supply_port '%s' specified in '%s' option does not match the port_name of the input_supply_port defined for the power switch.

DESCRIPTION

This option of create_power_switch command takes exactly one set of a named state, the input_supply_port for which this is defined, and its corresponding Boolean function. The input_supply_port must match the port_name specified for -input_supply_port option in the same command.

Check the command man page for more details and correct it accordingly.

UPF-019 (error) The switch control port '%s' specified in boolean expression '%s' is not defined for the power switch.

DESCRIPTION

The control ports specified in the state boolean expression must be defined as the control ports of the power switch. Use option -control_port to create such control ports.

WHAT NEXT

Fix the syntax and check the command man page for more details.

UPF-020 (error) Invalid specification in boolean expression '%s' for option '%s' in command create_power_switch.

DESCRIPTION

The specification for the named option is not a valid boolean expression.

WHAT NEXT

Check the boolean expression for the named option in command create_power_switch.

UPF-021 (error) The boolean expression is too long for option '%s' in command create_power_switch. The maximum acceptable number of characters is %d.

DESCRIPTION

The length limit for the boolean expression is currently set to be 2048 characters.

Check the boolean expression for the named option in command create_power_switch.
Please contact Synopsys Customer Support Center if needed.

UPF-022 (error) Unknown function operator "%c '%s' for option '%s' in command create_power_switch.

DESCRIPTION

The operator used in boolean expression for the named option is not support. The supported operator list is: (,), ~, &, |, ^, !.

WHAT NEXT

Check the boolean expression for the named option in command create_power_switch.

UPF-023 (error) Missing close blacket in boolean expression '%s' for option '%s' in command create_power_switch.

DESCRIPTION

Missing close blacket in boolean expression for the named option in command create_power_switch.

WHAT NEXT

Check the boolean expression for the named option in command create_power_switch.

UPF-024 (warning) The state probability of net "%s the state boolean function for command create_power_switch is not set. Set to be 0.5.

DESCRIPTION

The state probability of nets should have been set at the beginning of power calculation in PrimeTime PX.

Contact Synopsys Customer Support Center if needed.

UPF-025 (warning) The state probability of net "%s the state boolean function for command create_power_switch is %.3f. This is not acceptable. Set to be 1.0.

DESCRIPTION

An internal rare error has occurred. The state probability of a net cann't exceed 1.0.

WHAT NEXT

Contact Synopsys Customer Support Center if needed.

UPF-026 (Information) Overwriting the voltage on nets "%s

DESCRIPTION

The specified nets already have a voltage set on them. This new set_voltage command will overwrite the voltage values on all the specified nets.

This could happen, if you have already set a voltage explicitly on the given nets or internally, we propagate the set_voltage on all net segments.

WHAT NEXT

If you think the voltages are propagated incorrectly in the tool, check the supply_net connections using report_power_network command.

UPF-027 (warning) Power domain '%s' instantiated cells from library '%s' that do not have PG pins.

DESCRIPTION

The cells in the extent of the power domain do not have PG pins. Any set_voltage on UPF supply net is ignored and design operating conditions, and library default voltages are used instead.

It is recommended to use libraries with PG pins for low-power flow. Contact Synopsys Customer Support Center if needed.

UPF-028 (error) '%s' is not supported in UPF mode.

DESCRIPTION

The set_rail_voltage command and -object_list option of set_operating_conditions command are not supported in UPF mode.

WHAT NEXT

Please use set_voltage to specify voltages and set_temperature to specify temperatures.

UPF-029 (warning) There are '%d' supply nets without set_voltage.

DESCRIPTION

Each supply net segment must have set_voltage defined. Supply net segment is a continuous metal connection through ports separated by switches.

The voltage needs to be set even on ground nets (typically 0.0) since UPF create_supply_net does not yet distinguish supply and ground nets.

If not specified, individual power and ground pins of cell instances connected to such nets are treated as unconnected during delay calculation (thus might default to library voltage map - see man set_voltage, effectively discarding any UPF power domains, isolation, retention, connectivity etc.).

WHAT NEXT

Use check_timing -verbose -include supply_net_voltage to list the nets without set_voltage and set_voltage on each listed net.

SEE ALSO

create_supply_net (2), **set_voltage** (2).

UPF-030 (warning) There are '%d' unconnected power and ground pins.

DESCRIPTION

Power and ground pins of each cell instance should be connected to supply nets. If
not connected, delay calculation thus might default to library voltage map - see man
set_voltage, effectively discarding any UPF power domains, isolation, retention,
connectivity etc.).

The connectivity of power supply nets is specified by UPF commands including
create_power_domain (use fhelp upf to list the commands).

WHAT NEXT

Use check_timing -verbose -include unconnected_pg_pins to list the pg pins. Then use
report_power_pin_info, report_power_domain and other UPF commands to find out why
the pg pin is not connected.

SEE ALSO

create_power_domain (2), **report_power_domain** (2), **report_power_pin_info** (2).

UPF-031 (error) The specified %s does not belong to the given power domain

DESCRIPTION

It is required that the supply nets should belong to the specified power domain for
the command to succeed.

WHAT NEXT

Check the supply nets and where they belong to. Rerun the command with the nets
belonging to this domain.

SEE ALSO

create_power_domain (2), **create_supply_net** (2), **report_power_domain** (2),
report_supply_net (2), **report_power_pin_info** (2).

UPF-032 (error) Inside/outside connection of supply port %s is

already established/cannot be established to supply net %s.

DESCRIPTION

A supply port can only be connected by one supply net at each side (inside/outside).

Also, the top-level ports cannot have a connection to any net from a different scope.

If you are making connections to a PG pin, please check if the supply net and the cell belong to the same power domain.

WHAT NEXT

Check the connections that have been already made.

SEE ALSO

create_supply_net (2), **connect_supply_net** (2).

UPF-033 (warning) PG pin "%s

DESCRIPTION

The PG pin of a cell should be connected to an appropriate supply net. Such connection can either be created through explicit connection or through auto-connection semantics. Missing PG connection can lead to incorrect power analysis results. This error could be caused by incorrect/incomplete UPF commands.

WHAT NEXT

Check the UPF commands for the design.

SEE ALSO

create_power_domain (2), **create_supply_net** (2), **connect_supply_net** (2), **report_power_domain** (2), **report_supply_net** (2), **report_power_pin_info** (2).

UPF-034 (error) The '%s' option must refer to signal and sense.

DESCRIPTION

This option must be specified in format {net high|low|posedge|negedge}.

Make sure the net exists in the current scope and that signal type is properly
defined.

UPF-035 (error) Cannot override supply net %s by %s on retention %s.

DESCRIPTION

The UPF standard does not allow overriding of supply nets. Supply nets can only be
layered (i.e., added to an existing retention that does not have the supply net
defined).

WHAT NEXT

Make sure that your previous set_retention command either does not have the supply
nets or it is same as this command.

SEE ALSO

set_retention (2).

UPF-036 (error) Cannot override save/restore net or objects of retention %s.

DESCRIPTION

The UPF standard does not allow overriding of save, restore signal or objects.

WHAT NEXT

Make sure that this is the first set_retention command for the strategy in this
domain.

SEE ALSO

set_retention (2).

UPF-037 (error) No retention strategy %s in domain %s.

DESCRIPTION

The set_retention_control can be only applied to existing retention strategy.

WHAT NEXT

Create the retention strategy by set_retention.

SEE ALSO

set_retention (2), **set_retention_control** (2).

UPF-045 (error) Cannot override supply net %s by %s on isolation %s.

DESCRIPTION

The UPF standard does not allow overriding of supply nets. Supply nets can only be layered (i.e., added to an existing isolation that does not have the supply net defined).

WHAT NEXT

Make sure that your previous set_isolation command either does not have the supply nets or it is same as this command.

SEE ALSO

set_isolation (2).

UPF-046 (error) Cannot override signal net or elements of isolation %s.

DESCRIPTION

The UPF standard does not allow overriding of isolation signal or elements.

WHAT NEXT

Make sure that this is the first set_isolation command for the strategy in this domain.

SEE ALSO

set_isolation (2).

UPF-047 (error) No isolation strategy %s in domain %s.

DESCRIPTION

The set_isolation_control can be only applied to existing isolation strategy.

WHAT NEXT

Create the isolation strategy by set_isolation.

SEE ALSO

set_isolation (2), **set_isolation_control** (2).

WMDB

WMDB-1 (error) Internal error in creating mdb object for design %s.

DESCRIPTION

WHAT NEXT

WMDB-2 (error) Layer information not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-3 (error) Via information not converted to mdb in design

'%s'.

DESCRIPTION

WHAT NEXT

WMDB-4 (error) Ports not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-5 (error) Cell rows not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-6 (error) Track information not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-7 (error) Obstructions not converted to mdb in design

'%s'.

DESCRIPTION

WHAT NEXT

WMDB-8 (error) Routing information not converted to mdb in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-9 (error) Movebounds not converted to mdb in design

'%s'.

DESCRIPTION

WHAT NEXT

WMDB-10 (error) No library information present for design.

DESCRIPTION

WHAT NEXT

WMDB-11 (error) No library information present for design .

DESCRIPTION

WHAT NEXT

WMDB-12 (error) Entry already in the hash table for site object%s.

DESCRIPTION

WHAT NEXT

WMDB-13 (error) Entry already in the hash table for wirecode object %s.

DESCRIPTION

```
This error message occurs when routes in the Milkyway database contain wires with
duplicate IDs.
```

WMDB-14 (error) Entry already in the hash table for via object '%s'.

DESCRIPTION

This error message occurs when the routes in the Milkyway database contain vias that have duplicate IDs.

WHAT NEXT

Check the routes by reviewing the PDEF file for duplicate layers. Remove the duplicate layers and rerun the command.

WMDB-15 (warning) Rectilinear shape for core area are not supported .

DESCRIPTION

The rectilinear core shapes on the floorplan are not supported by write_mdb. No floor plan data will be translated correctly by write_mdb.

WHAT NEXT

Dumpout PDEF and update the rectilinear shape to a rectangular shape until this feature is supported.

WMDB-16 (error) Die size of the chip not set correctly for design

'%s'.

DESCRIPTION

WHAT NEXT

WMDB-17 (information) The tool detected and pre-existing cell instance group "%s

DESCRIPTION

```
This message advises you that the cell group that existed in the CEL has been
deleted and updated with an instance group from the tool.
```

WHAT NEXT

```
This is only an informational message. No action is required.
```


WMDB-18 (warning) Creation of MDB to set the cell boundary failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-19 (information) The tool detected the pre-existing cell plan group "%s

DESCRIPTION

```
This message advises you that the plan group that existed in the CEL has been
deleted and updated with bounds from the tool.
```

WHAT NEXT

```
This is only an informational message. No action is required.
```

However, if the existing plangroup was a exclusive plangroup, you might have to re-apply the properties again, since the tool does not support the exclusive plangroup and the property might have been lost during a read or write operation.

WMDB-20 (error) creation of milkway DB for baseArray failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-21 (error) License expired, Please check the LM_LICENSE_FILE .

DESCRIPTION

WHAT NEXT

WMDB-22 (warning) Scheme generation for site failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-23 (warning) Creation of MDB site failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-24 (warning) Non default rule '%s' are incorrect, missing

via '%s'.

WMDB-25 (warning) Scheme generation for non default rule '%s' failed .

DESCRIPTION

WHAT NEXT

WMDB-26 (warning) Creation of MDB for non default rule '%s' failed .

DESCRIPTION

WHAT NEXT

WMDB-27 (warning) Failed to get the region coordinates..

DESCRIPTION

WHAT NEXT

WMDB-28 (warning) Scheme generation for cellgroups failed for

design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-29 (warning) creation of milkyway db for cellgroups failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-30 (warning) Scheme generation failed for routing obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-31 (warning) Creation of MDB failed for routing obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-32 (warning) Scheme generation failed for placement

obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-33 (warning) Creation of MDB failed for placement obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-34 (warning) Scheme generation failed for placement obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-35 (warning) Creation of MDB failed for placement

obstruction in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-36 (error) Internal Error for routing keepouts.

DESCRIPTION

WHAT NEXT

WMDB-37 (error) Failed to create obstruction '%s' .

DESCRIPTION

WHAT NEXT

WMDB-38 (warning) Rectilinear obstructions are not supported

'%s' .

DESCRIPTION

WHAT NEXT

WMDB-39 (error) Internal Error for routing obstructions '%s' .

DESCRIPTION

WHAT NEXT

WMDB-40 (error) Failed to create obstruction '%s' .

DESCRIPTION

WHAT NEXT

WMDB-41 (warning) Pin type COVER not supported.

DESCRIPTION

WHAT NEXT

WMDB-42 (warning) direction not set correctly for pin '%s'.

DESCRIPTION

WHAT NEXT

WMDB-43 (warning) Failed to create physical information for

Pin '%s'.

DESCRIPTION

WHAT NEXT

WMDB-44 (warning) Scheme generation for pins failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-45 (warning) Master cell '%s' not found in Milkyway, using pdb information.

DESCRIPTION

WHAT NEXT

WMDB-46 (error) Creation of physical only cell '%s' failed for reference '%s'.

DESCRIPTION

WHAT NEXT

WMDB-47 (warning) Scheme generation failed to create

placement for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-48 (warning) Creation of MDB Instance failed to create placement information for instance '%s' in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-49 (warning) scheme generation failed to create a cell instance '%s' in design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-50 (warning) scheme generation failed to create a cell instance '%s' in design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-51 (warning) link the design prior to running write_mdb

command .

DESCRIPTION

WHAT NEXT

WMDB-52 (error) Failed to get boundary info for '%s' .

DESCRIPTION

WHAT NEXT

WMDB-53 (warning) Route type not defined in milkyway db .

DESCRIPTION

WHAT NEXT

WMDB-54 (warning) Route type not defined in milkyway db .

DESCRIPTION

WHAT NEXT

WMDB-55 (warning) Assuming detail route type .

DESCRIPTION

WHAT NEXT

WMDB-56 (warning) Route type for Fill wire not supported.

DESCRIPTION

WHAT NEXT

WMDB-57 (error) Route attributes not mapped correctly.

DESCRIPTION

WHAT NEXT

WMDB-58 (warning) Ignoring net '%s',with length=0 for design .

DESCRIPTION

WHAT NEXT

WMDB-59 (warning) Internal (error) , layer_name not found for id %d .

DESCRIPTION

WHAT NEXT

WMDB-60 (warning) Internal (error) , ignoring route data for net '%s', with width 0 for layer name '%s'.

DESCRIPTION

WHAT NEXT

WMDB-61 (warning) Internal (error) , ignoring route data with

width 0 for layer name .

DESCRIPTION

WHAT NEXT

WMDB-62 (error) Cannot find via_name for '%d' .

DESCRIPTION

WHAT NEXT

WMDB-63 (warning) Route Via ignored '%s'.

DESCRIPTION

WHAT NEXT

WMDB-64 (warning) Marking Net type as Shield for net '%s' .

DESCRIPTION

WHAT NEXT

WMDB-65 (error) in accesing route data.

DESCRIPTION

WHAT NEXT

WMDB-66 (warning) This net '%s' does not have a pin

connection..

DESCRIPTION

WHAT NEXT

WMDB-67 (warning) Nondefault rule '%s' for net '%s' not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-68 (warning) Clock net '%s' not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-69 (warning) port '%s' not connected in scheme for cell instance '%s'.

DESCRIPTION

WHAT NEXT

WMDB-70 (warning) port '%s' not connected in milkyway db for

cell instance '%s'.

DESCRIPTION

WHAT NEXT

WMDB-71 (warning) creation of MDB for simple via failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-72 (warning) Scheme generation for simple via failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-73 (warning) Scheme generation for routing wires failed for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-74 (warning) Creation of MDB for routing wires failed for

design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-75 (warning) Tracks cannot be converted without outline of the chip.

DESCRIPTION

WHAT NEXT

WMDB-76 (warning) Track direction not set correctly .

DESCRIPTION

WHAT NEXT

WMDB-77 (warning) Scheme generation for wire tracks failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-78 (warning) Creation of MDB wire tracks failed for

design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-79 (warning) Scheme generation for wire direction failed for design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-80 (warning) Creation of MDB for wire direction failed for

design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-81 (warning) Creation of base array failed for site '%s'.

DESCRIPTION

WHAT NEXT

WMDB-82 (error) Layer Name not found for tracks '%s'.

DESCRIPTION

WHAT NEXT

WMDB-83 (error) Layer name '%s' not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-84 (warning) Net name '%s', not found in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-85 (error) Layer name '%s' not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-86 (error) Layer name '%s' not found in Milkway DB .

DESCRIPTION

WHAT NEXT

WMDB-87 (error) Failed to Create wire master for layer name '%s' in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-88 (error) Creation of Horizontal wire failed for net '%s' in design %s.

DESCRIPTION

WHAT NEXT

WMDB-89 (error) Setting of route_type failed for design %s.

DESCRIPTION

WHAT NEXT

WMDB-90 (error) Creation of Vertical wire failed for net '%s' in

design %s.

DESCRIPTION

WHAT NEXT

WMDB-91 (error) Setting of route_type failed for design %s.

DESCRIPTION

WHAT NEXT

WMDB-92 (error) Un connected routing data for net '%s' in design '%s'.

DESCRIPTION

WHAT NEXT

WMDB-93 (error) Creation of Wire Master failed for layer No '%d' with width '%d' .

DESCRIPTION

WHAT NEXT

WMDB-94 (error) Failed to create contact for via '%s' in design

'%s' .

DESCRIPTION

WHAT NEXT

WMDB-95 (error) Failed to create cell group for group name '%s' .

DESCRIPTION

WHAT NEXT

WMDB-96 (error) Failed to add cell instance '%s' to group '%s' .

DESCRIPTION

WHAT NEXT

WMDB-97 (error) Failed to create region for group name '%s' .

DESCRIPTION

WHAT NEXT

WMDB-98 (error) Failed to store hard/soft data as property for

group name '%s' .

DESCRIPTION

WHAT NEXT

WMDB-99 (error) Failed to open cell '%s'.

DESCRIPTION

WHAT NEXT

WMDB-100 (error) Failed to the cell boundary for cell '%s'.

DESCRIPTION

WHAT NEXT

WMDB-101 (error) Failed to map library via '%s' to contact/ contactarray .

DESCRIPTION

WHAT NEXT

WMDB-102 (warning) Failed to map the via '%s' to contact/ contactarray .

DESCRIPTION

This message indicates that the routing segment has a via, which violates the rules that are defined in the technology file.

The most common reasons, where a via violates the rule. 1. cut_min_spacing 2. Upper

and lower enclosure width.

WHAT NEXT

1. Check your technology file, to make that the design uses the right technology. 2. Rerun the routing for the nets, which violates this rule.

WMDB-103 (error) No library information present for design

'%s'.

DESCRIPTION

WHAT NEXT

WMDB-104 (error) Vias with no geometry not supported .

DESCRIPTION

WHAT NEXT

WMDB-105 (error) Routing via not translated .

DESCRIPTION

WHAT NEXT

WMDB-106 (error) Failed to Initialize MWX Api's code '%d' .

DESCRIPTION

WHAT NEXT

WMDB-107 (error) current design not linked .

DESCRIPTION

WHAT NEXT

WMDB-108 (error) File open error '%s'.

DESCRIPTION

WHAT NEXT

WMDB-109 (warning) Failed to get mdbout design context!.

DESCRIPTION

WHAT NEXT

WMDB-110 (warning) Failed to get cell (%s) hierarchy preservation data from hash table!.

DESCRIPTION

WHAT NEXT

WMDB-111 (warning) Failed to put design (%s) hierarchy preservation data into hash table!.

DESCRIPTION

WHAT NEXT

WMDB-112 (warning) Failed to query cell instance (%s) by name during hierarchy preservation.

DESCRIPTION

WHAT NEXT

WMDB-113 (warning) Failed to get hierarchy preservation data

for parent %s of cell %s.

DESCRIPTION

WHAT NEXT

WMDB-114 (warning) Failed to attach hierarchical port instance to hierarchical net!.

DESCRIPTION

WHAT NEXT

WMDB-115 (warning) Failed to attach hierarchical port instance to cell instance!.

DESCRIPTION

WHAT NEXT

WMDB-116 (warning) Could not to get cell hierarchy preservation data from hash table!.

DESCRIPTION

WHAT NEXT

WMDB-117 (warning) Failed to create hierarchical high-connect

net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-118 (warning) Failed to create hierarchical high-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-119 (warning) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-120 (warning) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-121 (warning) Failed to create hierarchical low-connect

net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-122 (error) Failed to create hierarchical low-connect net (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-123 (warning) Failed to create hierarchical port instance (%s)!.

DESCRIPTION

WHAT NEXT

WMDB-124 (warning) Failed to get port master data from hash table (%s)..

DESCRIPTION

WHAT NEXT

WMDB-125 (warning) Failed to attach hierarchical port instance

hi-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-126 (warning) Failed to attach hierarchical port instance hi-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-127 (warning) Failed to attach hierarchical port instance low-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-128 (warning) Failed to attach hierarchical port instance un-connect net!.

DESCRIPTION

WHAT NEXT

WMDB-129 (warning) Failed to attach hierarchical port instance

to cell instance!.

DESCRIPTION

WHAT NEXT

WMDB-130 (warning) Failed to query cell instance (%s) by name during hierarchy preservation.

DESCRIPTION

```
This warning message occurs when the Milkyway libraries are corrupted and the flat
instance does not match the database file.
```

WHAT NEXT

```
This is only a warning message.
```

```
However, you can eliminate this warning message by writing to a new cell.
```

WMDB-131 (error) Failed to attach the reference library '%s'.

DESCRIPTION

```
This error message occurs when the specified reference libraries cannot be set for
the design library.
```

WHAT NEXT

```
Check that the reference library path is valid. Check that the libraries have the
necessary permissions. Ensure that the reference libraries are relative to the
design library (and not the current directory).
```

WMDB-132 (warning) Failed to create instance '%s', for master '%s'.

DESCRIPTION

```
This warning message occurs when the FRAM libraries are missing. Some cells are
```

treated as a black box and are not recognized by the Astro router.

WHAT NEXT

Check the reference libraries added to the design libraries and verify that the master name exists in the corresponding reference library.

WMDB-133 (error) Failed to create net '%s'.

DESCRIPTION

This error message occurs when the creation of the specified net fails. This failure may be caused by corrupted Milkyway libraries.

WHAT NEXT

Rerun the design from a clean directory. Make sure that the permissions are correct and the is enough disk space.

WMDB-134 (error) Failed to bind the design with '%s'.

DESCRIPTION

This error message occurs when the FRAM libraries do not exist for all of the leaf cells.

WHAT NEXT

Check the reference libraries that are added for the design libraries and ensure that the necessary STD cells are present in the reference libraries.

WMDB-135 (error) Failed to create port '%s' for net '%s'.

DESCRIPTION

This error message occurs when the tool fails to create the specified port because of a mismatch in FRAM libraries and the hierarchy cells.

WHAT NEXT

Make sure that the library preparation is performed using the **gePrepLibs** command.

For the reported reference name, make sure that the FRAM libraries are consistent with the .lib file.

SEE ALSO

gePrepLibs(2)

WMDB-136 (error) Failed to connect port instance '%s' in cell '%s' with net '%s'.

DESCRIPTION

This error message occurs when the specified port instance is not connected with the specified net. This may be due to inconsistent FRAM libraries and .lib files.

WHAT NEXT

Make sure that your libraries are consistent and run the command again.

WMDB-137 (error) Top design is not set correctly.

DESCRIPTION

This error message occurs when the current design is not set correctly.

WHAT NEXT

Run the **current_design** command and set the top design for the **write_mdb** command to work correctly.

SEE ALSO

current_design(2)
write_mdb(2)

WMDB-138 (warning) Link the design prior to running the

write_mdb command.

DESCRIPTION

This warning message occurs to advise you to run the **link** and the **link_physical**
commands before running the **write_mdb** command.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following
the steps below.

Run the **link** command, and then run the **link_physical** command, making sure each
command completes successfully. Then run the **write_mdb** command.

SEE ALSO

link(2)
link_physical(2)
write_mdb(2)

WMDB-139 (warning) Failed to create port '%s', for ref_name '%s'.

DESCRIPTION

This warning message occurs when the specified port cannot be createed for the
specified reference name. The port is not created because of a mismatch in the FRAM
libraries and the hierarchy cells.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following
the steps below.

Make sure that the library preparation is done using the **gePrepLibs**. Also, make sure
that the FRAM libraries are consistent with the

SEE ALSO

gePrepLibs(2)

WMDB-140 (warning) Unable to save cell master '%s'.

DESCRIPTION

This warning message occurs when the specified cell cannot be stored to the Milkyway NETL view.

WHAT NEXT

This is only a warning message.

You can safely ignore this warning message if you are using Astro and you are not dependent on the NETL view.

If you want to use the NETL view, use the ASCII flow and the **auVerilogIn** Astro command.

SEE ALSO

The **auVerilogIn** Astro command in Physical Implementation Online Help.

WMDB-141 (warning) Unable to save cell master '%s'.

DESCRIPTION

This warning message occurs when the specified cell cannot be stored to the Milkyway NETL view.

WHAT NEXT

This is only a warning message.

You can safely ignore this message if you are using Astro and you are not dependent on the NETL view.

If you want to use the NETL view, use the ASCII flow and **auVerilogIn** Astro command.

SEE ALSO

The **auVerilogIn** Astro command in Physical Implementation Online Help.

WMDB-142 (warning) Instance doesn't exist '%s' .

DESCRIPTION

WHAT NEXT

WMDB-143 (error) Directory not writable '%s'.

DESCRIPTION

This error message occurs when the directory pointed by the **mw_design_library** variable is not writable.

WHAT NEXT

Verify that the directory pointed by **mw_design_library** is a valid directory and that you have the correct file permissions.

SEE ALSO

mw_design_library(3)

WMDB-144 (warning) Logical design data exists in '%s'.

DESCRIPTION

This warning message occurs when the LOGIC view design data already exists. This may be due to a previous **write_mdb** command. This may also be due to very low memory available on the system.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Run the command again on a new mw_design_library directory or use a machine with more swap space.

SEE ALSO

write_mdb(2)

WMDB-146 (error) Failed to create netlist view for design '%s'.

DESCRIPTION

This error message occurs when the netlist view is not created for the specified
design. This NETL view does not exist.

WHAT NEXT

Check that the permissions are correct for the value pointed to by the
mw_design_library variable and verify that the directory is writable.

Also, check that the values pointed to by the **mw_reference_library** variable exist.

If you are using Astro, you can use the CEL view to do routing without any issues
and the NETL view can be ignored.

SEE ALSO

mw_design_library(3)
mw_reference_library(3)

WMDB-147 (info) Starting to Expand the netlist for design '%s' .

DESCRIPTION

WHAT NEXT

WMDB-148 (error) Failed to create expand view for cell '%s'.

DESCRIPTION

WHAT NEXT

WMDB-149 (warning) Flat instance does not exist '%s'.

DESCRIPTION

This warning message occurs when the flat instances that are added for multi-voltage
do not exist in Milkyway. The region object in the tool may not be translated

correctly to Milkyway.

WHAT NEXT

This is only a warning message.

However, if the result is not what you intended, you can check the flat object where the multi-voltage property is set and determine if it exists in Milkyway.

Create the voltage area in Astro after performing the **write_mdb**. Also, make sure that the hierarchies are consistent in Milkway by running the **astRepairHierPreservation** Astro command.

SEE ALSO

write_mdb(2)
astRepairHierPreservation

WMDB-150 (error) Top design is not set correctly.

DESCRIPTION

This error message occurs when the current design is not set correctly.

WHAT NEXT

Run the **current_design** command and set the current design correctly.

SEE ALSO

current_design(2)

WMDB-151 (information) Applications of Milkyway do not accept a port name the same as the net name for design '%s', and are not connected.

DESCRIPTION

This error message occurs because the design has the same name on a net and on a port, but they are not connected in the specified design and are not accepted by the Milkyway database.

WHAT NEXT

Define the name rules and change the names on the design before running the
write_mdb command.

The following example shows one method you can use to change the names on the
design:

```
prompt> define_name_rules snps_milkyway -equal_ports_nets
prompt> define_name_rules snps_milkyway -check_internal_net_name
prompt> change_names -rule snps_milkyway -hier
```

The second way to change the names on the design is by running the following
command:

```
prompt> change_names -rule verilog -hier
```

SEE ALSO

change_names(2)
define_name_rules(2)

WMDB-152 (information) Cannot perform incremental operation; using non-incremental mode to save cell '%s'.

DESCRIPTION

This information message occurs when performing an incremental update using the
write_mdb command, if either of the following conditions exist:

• The cell with the same name already exists in the Milkyway design library.

• The **write_mdb** follows a **read_mdb** command, such as if the database is created or
updated using **read_mdb**.
The routing data and all of the floorplan data that exists in the LOGIC database is
saved in the Milkyway database.

In incremental mode, the route information that is changed in the tool is only
transferred to Milkyway. The change of route information is normally detected by
changes in nets or changes to cell locations in the design w.r.t to the Milkyway
database.

WHAT NEXT

This is an information message only. No action is required.

However, if you want the routing data to be transferred to Milkyway from the LOGIC database, make sure that there are no versions of cells with the same name in the Milkyway design library.

You can create a new design library using the **create_mw_design** command and use **write_mdb** to save the CEL from which to transfer the routes.

SEE ALSO

create_mw_design(2)
read_mdb(2)
write_mdb(2)

WMDB-153 (warning) Failed to get the master name for cell instance '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** command cannot get the master name for the given cell instance, possibly due to a corrupted Milkway database.

WHAT NEXT

Check that the **mw_reference_library** variable is set correctly and verify that the reference libraries are added to the design library.

SEE ALSO

create_mw_design(2)
set_mw_design(2)
mw_reference_library(3)

WMDB-154 (error) Failed to initiate a iterator.

DESCRIPTION

write_mdb can not initiate an iterator to iterate through mdb objects.

WHAT NEXT

Please verify your data and try again in need.

WMDB-155 (error) Failed to iterate through expanded cell instances.

DESCRIPTION

```
write_mdb failed to iterate through mdb expanded cell instances. The mdb may be
corrupted.
```

WHAT NEXT

```
Please verify your data and try again in need.
```

WMDB-156 (warning) Failed to delete cell instance '%s'.

DESCRIPTION

```
write_mdb failed to delete a mdb cell instances. This cell instance may not exist or
the mdb has been corrupted.
```

WHAT NEXT

```
Please verify your data and try again in need.
```

WMDB-157 (warning) Failed to get port type. (port id: %d)

DESCRIPTION

```
write_mdb can not get the port type attribute of a certain port. Port may not exist
or mdb has been corrupted.
```

WHAT NEXT

```
Please verify your data and try again in need.
```

WMDB-158 (error) Fail to create port '%s'.

DESCRIPTION

```
write_mdb can not create a port specified by name '%s' in mdb.
```

WHAT NEXT

```
Please verify your data and try again.
```

SEE ALSO

WMDB-159 (error) Failed to connect net '%s' to port '%s'.

DESCRIPTION

```
This error message occurs when the write_mdb command cannot connect the specified
net to the specified port. Refer to the log file for details.
```

WHAT NEXT

```
Check that the reference libraries are correct, and that the specified ports exist
in the reference libraries.
```

```
Also, you can try writing into a new design library by creating it with the
create_mw_design command.
```

SEE ALSO

```
create_mw_design(2)
write_mdb(2)
```

WMDB-160 (error) Failed to connect pin '%s/%s' to net '%s'.

DESCRIPTION

```
This error message occurs when the write_mdb command fails to connect the pin with
the specified net. This error indicates the Milkyway database may be corrupted.
```

WHAT NEXT

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-161 (error) Failed to delete the global route for net '%s'.

DESCRIPTION

write_mdb failed to delete the global route for a net. The global route data for the specified net does exist in the Milkyway database.

WHAT NEXT

Manually delete the global route data for the specified net.

SEE ALSO

Astro

WMDB-162 (warning) Failed to delete net '%s'.

DESCRIPTION

This warning message occurs the **write_mdb** command fails to delete a net. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following

the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.C

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-163 (warning) Failed to delete all pins for port '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** fails to delete all pins for specified port. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-164 (warning) Failed to delete a port '%s'.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to delete the specified port. The Milkyway database may be corrupted.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Create the design_library by changing the value of the **mw_design_library** variable in a new directory.

Make sure that the value of the **mw_reference_library** variable is set correctly and that all of the FRAM libraries exist.

Check that the reference libraries are correct and that the specified ports exist in the reference libraries.

You can try writing into a new design library by creating it using the **create_mw_design** command.

SEE ALSO

create_mw_design(2)
write_mdb(2)
mw_design_library(3)

WMDB-165 (warning) Failed to create port vector info object.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to create a vector info object for a hierarchical port. This could cause an inconsistent bus port for the design.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Verify your data and run the command again.

write_mdb(2)

WMDB-166 (warning) Failed to set port vector info object.

DESCRIPTION

This warning message occurs when the **write_mdb** command fails to build the relationship between a vector info object and a hierarchical port. This causes an inconsistent bus in the design. The bus information for ports may be lost during **read_mdb** or **write_mdb** command activity.

WHAT NEXT

This is only a warning message. You can eliminate this warning message by following the instructions below.

Check your design for RAMS, which may result from BUSES in the RAMS. If you are writing out a NETL view, there should not be any problems in the flow, since Astro can use the information from NETL. This is also true for **read_mdb**.

SEE ALSO

read_mdb(2)
write_mdb(2)

WMDB-167 (error) Failed to create hierarchical cell instance master '%s'.

DESCRIPTION

This error message occurs when the the hierarchical cell instance with the specified name for the design cannot be created in Milkyway. The result may cause inconsistent hierarchy data.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

WMDB-168 (error) Failed to create hierarchical port instance master '%s'.

DESCRIPTION

This error message occurs when the hierarchical port instance with the specified name for the design cannot be created in Milkyway. The result may be inconsistent hierarchy data. There is an internal error with the hierarchy preservation of Milkyway.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

See the **astRepairHierPreservation** Astro command in Physical Implementation Online Help.

SEE ALSO

write_mdb(2)

WMDB-169 (error) Hashing error during write_mdb.

DESCRIPTION

This error message occurs during **write_mdb** command activity and indicates an internal error with the hierarchy preservation of Milkyway.

WHAT NEXT

Run the **write_mdb** command on a new Milkyway design library and save it to a new CEL.

If the design is a flat design and if it is a one way flow, you may be able to ignore this message.

SEE ALSO

write_mdb(2)

WMDB-170 (error) Failed to attach hier port inst master '%s' to hier cell inst master '%s'.

DESCRIPTION

```
This indicates an internal error, during hierarchy preservation.
```

WHAT NEXT

```
File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.
```

SEE ALSO

WMDB-171 (error) Failed to create cell instance '%s'.

DESCRIPTION

```
This indicates an internal error, during hierarchy preservation.
```

WHAT NEXT

```
File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.
```

SEE ALSO

WMDB-172 (error) Failed to attach vcell instance '%s' to its parent '%s'.

DESCRIPTION

```
This indicates an internal error, during hierarchy preservation.
```

WHAT NEXT

```
File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.
```

WMDB-173 (warning) Failed to get cell instance data from hash table (%s)..

DESCRIPTION

```
This indicates an internal error, during hierarchy preservation.
```

WHAT NEXT

```
File a star, and if the design is FLAT, maybe you can ignore this warning message.
Try running change_names -rule verilog and save the design.
```

SEE ALSO

WMDB-174 (information) Initializing hierarchy preservation...

DESCRIPTION

```
This indicates the hierarchy perservation is getting initialized by write_mdb.
```

```
The old hierarchy data, if any will be deleted, and the new hierarchy preservation
data will be created in the CEL.
```

WHAT NEXT

SEE ALSO

WMDB-175 (warning) Failed to delete hierarchy preservation records.

DESCRIPTION

```
The hierarchy preservation data that exists in the CEL specified by mw_cell_name or
-cell option cannot be deleted. If you see this error, it is likely that the
hierarchy information is not correct, and needs to be fixed for hierarchy designs.
```

WHAT NEXT

The could indiciate the data is already corrupted. The user cannot delete the hierarchy preservation manually using Astro and do write_mdb again.

SEE ALSO

WMDB-176 (error) Failed to create new Milkyway library '%s'.

DESCRIPTION

This error message occurs when the Milkyway design library is not created as specified by the **mw_design_library** variable.

WHAT NEXT

Check that the technology file is correct and that there are no errors when parsing the technology file.

Verify that the value specified in **mw_design_library** is correct and the file has the necessary permissions.

Make sure there is enough disk space available to create a new design library.

SEE ALSO

mw_design_library(3)

WMDB-177 (error) Technology file is NULL or invalid.

DESCRIPTION

This error message occurs when the technology file is not provided or the file information is invalid.

WHAT NEXT

The technology file is required to run the **create_mw_design** command. The file provides the technology information for the Milkyway database library to be created.

Make sure that the information in the technology file does not contain any conflicts, since conflicts may cause the tf checker to fail.

Also, make sure that the required permissions specified in the **mw_design_library** variable are correct.

WMDB-178 (information) Please run 'change_names' command to make sure that the names are consistent across db.

DESCRIPTION

This message indicates that the port names and the net names does not have the same name and are not connected.

The flow may have some problems due to the above mentioned reasons, and it may be corrected by running change_name before saving the CEL.

WHAT NEXT

Run change_names -rules verilog -hier before running write_mdb.

SEE ALSO

change_names

WMDB-179 (error) Failed to load technology file '%s'.

DESCRIPTION

The technology file specified cannot be loaded to the memory.

WHAT NEXT

Please check if the technology file exists, and the permissions are set correctly.

SEE ALSO

mw_design_library variable

WMDB-180 (warning) Failed to set reference library '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-181 (error) Failed to open library '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-182 (warning) Failed to get milkyway library distance

unit converting factor.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-183 (information) Cell '%s' already exists in view '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-184 (error) Failed to create cell '%s' in view '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-185 (error) Failed to set layout view for cell '%s' in view

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-186 (error) Failed to close cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-187 (error) Failed to copy cell '%s' to '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-188 (error) Failed to open cell '%s', view '%s'.

DESCRIPTION

The specified leaf cell cannot be open during write_mdb. This error will affect translating the physical information for the design.

WHAT NEXT

Please if the reference libraries are specified correctly before write_mdb.

WMDB-189 (warning) Maximum var route rule crossed above limit.

DESCRIPTION

The number of default route rules has reached its limit of 256.

WHAT NEXT

Try deleting the number of var route rules available in the design, or merge the rules with the exisiting rules.

SEE ALSO

dbDefineVarRoute rule in Astro.

WMDB-190 (warning) Failed to get contact from technology file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-191 (error) Failed to create master cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-192 (error) Failed to set the port type for port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-193 (error) Failed to create pin '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-194 (warning) Failed to set var route rule '%s' for net

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-195 (error) Failed to get the net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-196 (error) Failed to get the cell instance '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-197 (error) Failed to get the port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-198 (error) Failed to connect port '%s' with net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-199 (error) Failed to connect a port with net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-200 (information) Failed to update capacitance mode to

TLU+.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-201 (error) Invalid number of Milkyway boundary points.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-202 (error) Failed to get Milkyway cell boundary.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-203 (error) Failed to convert Milkyway boundary.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-204 (error) Failed to calculate standard cell area in

current cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-205 (error) Failed to calculate standard cell area for cell

'%s.%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-206 (error) Failed to calculate area for current cell.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-207 (error) Failed to calculate area for cell '%s.%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-208 (error) Failed to create wire direction on layer '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-209 (information) Searching for any single pin nets.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-210 (warning) Failed to mark the db sync flag in milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-211 (warning) Failed to mark the SDC sync flag in milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-212 (warning) Failed to mark the Hierarchy preservation

flag in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-213 (warning) Failed to mark the write_mdb flag in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-214 (error) Failed to close cell '%s' view '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-215 (warning) Failed to get data for cell instance '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-216 (warning) Failed to set status for cell instance '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-217 (error) Failed to get tile(site) info, name '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-218 (error) Failed to create tile pattern for site '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-219 (warning) Failed to update base array Bbox, name

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-220 (error) Failed to create cell row, name '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-221 (error) Failed to set cell row tile.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-222 (error) Failed to set cell row pattern.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-223 (error) Failed to get tile pattern number, parttern

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-224 (error) Failed to set cell row tile pattern record to parttern '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-225 (error) Failed to set cell row starting tile, site '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-226 (error) Layer id '%d' exceeds Milkyway Layer id limit

'%d'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-227 (error) Failed to find layer '%s' in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-228 (error) Failed to create wire track.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-229 (error) Failed to compute wire track boundary BBox.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-230 (error) Failed to set wire track boundary BBox.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-231 (error) Failed to purge existing wire tracks in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-232 (error) Failed to purge existing wire directions in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-233 (error) Eeq class number exceeds Milkyway limit.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-234 (error) Failed to create a pin for port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-235 (error) Failed to create wire master for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-236 (error) Failed to create wire for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-237 (error) Failed to connect route segment with wire.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-238 (error) Failed to set net Max/Min layer.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-239 (error) Failed to create via '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-240 (error) Failed to read vias from design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-241 (warning) Via '%s' cut dimensions do not match.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-242 (warning) Via '%s' cut spacing do not match.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-243 (warning) Via '%s' enclosure dimensions are too short.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-244 (warning) Ignore via '%s' which violates the Min

Area rule in tech file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-245 (error) Internal error for via '%s' rule.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-246 (information) Stack vias not supported '%s:%d'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-247 (error) Failed to create global route for net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-248 (error) Failed to connect global route to net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-249 (error) Number of nets does not match number of

ports or cell masters or cell instances.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-250 (error) PGConnect failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-251 (error) Failed to create placement blockage.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-252 (error) Internal error for routing obstr in layer '%d'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-253 (error) Failed to create routing blockage.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-254 (information) Reassign group %s from region %d to

region %d.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-255 (error) Failed to get object type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-256 (error) Region '%d' is not a soft block.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-257 (error) Failed to find group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-258 (error) No any groups specified.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-259 (error) Failed to create cell region.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-260 (error) Failed to get group by name '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-261 (error) Failed to get group size.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-262 (error) No cell instance in group '%s'.

DESCRIPTION

WMDB-263 (warning) Group '%s' has been bounded to region '%d'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-264 (warning) Failed to set group parent, group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-265 (error) Failed to assign group to region.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-266 (error) Failed to update region group name

property.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-267 (error) Failed to delete group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-268 (error) Failed to create group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-269 (error) Failed to create property for group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-270 (error) Failed to get group property.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-271 (error) Failed to get expanded cell instance.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-272 (error) Cell boundary for cell instance '%s' is null.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-273 (error) Failed to update group 'groupLength' property, group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-274 (error) Failed to update group 'groupSize' property,

group '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-275 (error) Failed to purge existing tile patterns in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-276 (error) Failed to purge existing cell rows in Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-277 (error) Failed to purge existing base arrays in

Milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-278 (information) Update port shape ... port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-279 (error) Failed to get port data, port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-280 (error) Cell '%s' doesn't exist in view '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-281 (error) Version '%d" of cell '%s' doesn't exist in view

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-282 (error) Failed to get the place group '%s'.

DESCRIPTION

While creating a floor plan group, write_mdb detects that no place group with the given name existed. However, a plan group is usually based on a place group.

WHAT NEXT

Please create a place group using the given name first.

SEE ALSO

WMDB-283 (error) Failed to create plan group '%s".

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-284 (error) Failed to create/update '%s' property, value

’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-285 (warning) Bus information was not correctly set for port ’%s’.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-286 (warning) Bus information was not correctly set for

net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-287 (warning) Failed to set net name '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-288 (warning) Failed to set net type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-289 (error) Failed to createa ports for design '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-290 (error) Failed to createa connections for design

'%s'.

WHAT NEXT

SEE ALSO

WMDB-291 (error) Failed to lock library;

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-292 (error) Internal error, ignore non-default rule for

layer '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-293 (error) Internal error for via '%s' rule.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-294 (warning) Failed to set the boundary for design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-295 (warning) Physical information will not be translated. Set the chip boundary to translate physical

information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-296 (error) Internal error, failed to map layer '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-297 (error) Failed to create port instance for net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-298 (warning) Pin '%s' doesn't have complete physical

information, created in default location.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-299 (error) Failed to set port shape for pin '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-300 (error) Failed to set the Non default rule '%s' on net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-301 (error) Failed to get the Non default rule width for

net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-302 (warning) Wire extension doesn't comply with

milkyway.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-303 (error) Failed to create a route segment for net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-304 (warning) Placement blockage type not supported.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-305 (error) Failed to create a logical view for cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-306 (warning) Wire direction may be incorrect.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-307 (information) Design not uniquified, only logic view will be created.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-308 (error) Failed to create LOGIC view for library '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-309 (warning) Failed to preserve the Hierarchy

information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-310 (information) Updating SDC information...

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-311 (information) Done updating SDC information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-312 (error) Failed to get net name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-313 (error) Failed to get library id from cell id('%d').

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-314 (error) Failed to get cell instance master(id: '%d').

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-315 (error) Failed to get port instance master(id: '%d').

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-316 (error) Failed to set port net id.(port id: '%d')

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-317 (information) Connected %d ports to net '%s'

through pattern '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-318 (information) Disconnected %d ports from net '%s'

through pattern '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-319 (information) Connected %d ports to child net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-320 (information) Disconnected %d ports from child net.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-321 (error) Iteration error.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-322 (error) Failed to get cell name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-323 (information) On cell '%s':

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-324 (error) Failed to get cell instance count in cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-325 (information) Net '%s' does not exist, create it now …

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-326 (information) Can not find matched port for inputing

port pattern.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-327 (error) Failed to get net type for net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-328 (information) Net '%s' in cell '%s' has type '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-329 (information) Net '%s' in cell '%s' has different

subtype than that currently specified.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-330 (error) Failed to create port by net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-331 (error) Failed to create cell "PG connected port" property, net '%s', cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-332 (error) Failed to remove PGConnect created port,

by net '%s', in cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-333 (error) Must choose Disconnect mode when

deleting top cell port.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-334 (error) Failed to connect/disconnect PG.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-335 (error) Milkyway host initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-336 (error) Milkyway DB initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-337 (error) Milkyway ax initialization failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-338 (error) Library path is NULL.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-339 (error) Can not purge technology information.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-340 (error) Failed to initialize technology main table.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-341 (error) Failed to build technology main table.

DESCRIPTION

WMDB-342 (error) Failed to set port name for port '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-343 (warning) Cannot get tile table for tile '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-344 (error) Failed to update the property for tile '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-345 (error) Failed to create tile table '%s'.

DESCRIPTION

WHAT NEXT

WMDB-346 (error) Failed to create tile in paramset '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-347 (error) Tile pattern with name '%s' has existed in

DB, creation failed.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-348 (error) Failed to create tile pattern '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-349 (error) The tiles are not set correctly.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-350 (warning) Failed to get a Bounding box for the

design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-351 (error) Failed to get the default contact by layer '%d'

and '%d'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-352 (error) Failed to get library contact table.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-353 (error) Failed to attach the TLUPlus file.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-354 (error) No Milkyway design specified.

DESCRIPTION

WHAT NEXT

```
You need to specify a Milkyway library either from the command line or through
setting the 'mw_design_library' var previous to 'read_mdb/write_mdb' command. e.g.,
to set the var, please follow, set mw_design_library design_lib_name write_mdb

view man page to see how to specify from command line.
```

WMDB-355 (warning) No reference libraries set for Milkyway design.

DESCRIPTION

This warning message occurs when a reference library is not specified to the main Milkyway database library (the design library). Link errors may occur if the reference libraries are not specified for the design.

WHAT NEXT

This is only a warning message. A reference library is required for resolving cell instances.

You can specify a reference library by setting the **mw_reference_library** variable, as shown in the example below, before using the the **create_mw_design** command:

```
psyn_shell-t> set mw_reference_library "ref_lib_name1 ref_lib_name2"
```

You can also specify the reference library by running the **set_mw_design** command as shown in the following example:

```
psyn_shell-t> set_mw_design
```

SEE ALSO

create_mw_design(2)
set_mw_design(2)

WMDB-356 (error) Failed to save the milkyway db for design

'%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-357 (information) write_mdb done successfully.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-358 (error) Failed to set '%s' variable.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-359 (error) No Milkyway cell specified.

DESCRIPTION

WHAT NEXT

```
You need to specify a Milkyway cell either from the command line or through setting
the 'mw_cell_name' var previous to 'read_mdb' command. e.g., to set the var, please
follow, set mw_design_library mdb_design_name set mw_cell_name mdb_cell_name
read_mdb
```

```
Please view man page to see how to specify from command line.
```

WMDB-360 (error) Failed to link the design.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-361 (information) read_mdb will read only the logic db.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-362 (error) Failed to update the physical information for cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-363 (error) Failed to update the changed netlist

information for cell '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-364 (information) read_mdb done successfully.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-365 (error) Failed to open reference library '%s'.

DESCRIPTION

This error message occurs when the tool fails to open the specified reference library.

A reference library is required for resolving cell instances.

WHAT NEXT

Make sure you specified the correct reference libraries and that all of the libraries are accessible.

SEE ALSO

create_mw_design(2)
set_mw_design(2)

WMDB-366 (warning) No pdb library present for the reference

library '%s'.

DESCRIPTION

This warning message occurs when the **create_mw_design** command cannot find the physical library database for the specified reference library.

Physical library databases that provide physical information are required by the **link_physical_library** command. The **create_mw_design** command automatically adds the physical library databases from reference libraries to the **physical_library** variable.

WHAT NEXT

This is only a warning message. No action is required.

However, if you want the physical information from the reference Milkyway database library, make sure that sure that the physical database library exists for it.

SEE ALSO

create_mw_design(2)
link_physical_library(2)

WMDB-367 (information) Dumping plib from milkyway technology file...

DESCRIPTION

This information message occurs when the **create_mw_design** command is in the process of dumping the physical library from the Milkyway technology file.

WHAT NEXT

This is only an informational message. No action is required.

SEE ALSO

create_mw_design(2)

WMDB-368 (error) Failed to dump physical library from

Milkyway design library '%s'.

DESCRIPTION

This error message occurs when the `create_mw_design` command fails to dump the
physical library based on the specified technology file.

WHAT NEXT

Check that your technology file is correct and run the command again.

SEE ALSO

create_mw_design(2)

WMDB-369 (information) Replacing reference libary for design library '%s'.

DESCRIPTION

This information message occurs when the `set_mw_design` command is replacing the old
reference libraries in current `mw_design_library` with the new libraries.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

set_mw_design(2)
mw_design_library(3)
mw_reference_library(3)

WMDB-370 (error) Failed to get reference library for design library '%s'.

DESCRIPTION

This error message occurs when the tool cannot obtain the reference libraries for a
specific Milkyway design library.

WHAT NEXT

Make sure that the **mw_reference_library** is properly set for the current
mw_design_library variable.

SEE ALSO

```
create_mw_design(2)
set_mw_design(2)
mw_design_library(3)
mw_reference_library(3)
```

WMDB-371 (error) Failed to create Milkyway design library '%s'.

DESCRIPTION

This error message occurs when the tool fails to to create a Milkyway design
library.

WHAT NEXT

Make sure you run the flow correctly. For a detailed description of how to run the
flow, refer to the **create_mw_design** command man page.

SEE ALSO

```
create_mw_design(2)
```

WMDB-372 (error) Failed to import the physical library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to import the
specified physical library database.

WHAT NEXT

Verify that you provided the correct physical library database by checking the value
of the **physical_library** variable.

SEE ALSO

```
create_mw_design(2)
physical_library(3)
```

WMDB-373 (error) Failed to create TLUPlus model for Library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to create the TLUPlus model for the current **mw_design_library** variable.

WHAT NEXT

Verify that both the TLU table file and the layer map file are correct and then run the command again.

SEE ALSO

```
create_mw_design(2)
mw_design_library(3)
```


WMDB-374 (error) Failed to get TLUPlus attach file '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to get the TLUPlus attach file for the current **mw_design_library** variable.

WHAT NEXT

Verify that the TLUPlus file is created correctly.

SEE ALSO

```
create_mw_design(2)
mw_design_library(3)
```


WMDB-375 (error) Failed to remove reference libraries for design library '%s'.

DESCRIPTION

This error message occurs when the **create_mw_design** command fails to remove old reference libraries from the current design library while attempting to replace them with the new libraries.

Verify that you are using the correct design library and run the command again.

create_mw_design(2)

WMDB-376 (warning) Failed to add reference library '%s' for design library.

DESCRIPTION

This warning message occurs when the **create_mw_design** command fails to add the specified reference library to the design library.

WHAT NEXT

Verify that the reference libraries you specify meet the following criteria:
 1. The reference library does exist.
 2. The reference library is not the same as the design library.
 3. The reference library is accessible.
 4. The reference library is consistent with the main library in the technology file.
 5. The reference library does not exist in the main library reference list.

SEE ALSO

create_mw_design(2)

WMDB-377 (information) Unable to get direction for port,

assuming INPUT.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-378 (information) Unable to get direction for leaf port.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-379 (warning) Failed to get port type.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-380 (warning) Failed to get hierarchical net name.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-381 (warning) Failed to set routing segment width on a

layer for net '%s'.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-382 (warning) Failed to read the GCEL grid from milkway design library.

DESCRIPTION

WHAT NEXT

SEE ALSO

WMDB-383 (information) 'stop at any level' functionality is disabled by variable 'disable_mdb_stop_points'.

DESCRIPTION

This information message occurs when the **disable_mdb_stop_points** is set to **true**, which disables the "stop at any level" function for the current command.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

disable_mdb_stop_points(3)

WMDB-384 (information) Cell '%s' is a stop_point (module %s).

DESCRIPTION

This information message occurs when the current cell is a stop point module. The **write_mdb** command will not explore the submodules of the current cell. The **write_mdb** command will annotate the nonleaf macro modules as the stop points.

WHAT NEXT

This is only an information message. No action is required.

SEE ALSO

write_mdb(2)
disable_mdb_stop_points(3)

WMDB-385 (error) region %s is disjointed, which is not allowed in Milkyway.

DESCRIPTION

Current region contains disjointed areas, which is not supported by Milkyway. write_mdb will not save this region to Milkyway.

WHAT NEXT

Change the disjointed region into different regions and do write_mdb again.

SEE ALSO

create_region (3) remove_region (3)

WMDB-386 (error) Failed to create/update property %s for %s.

DESCRIPTION

write_mdb failed to create or update the property for the given object. This will lead to the property missing in the design.

Please make sure the disk space is enough for milkyway. Also verify your data and try again.

SEE ALSO

WMDB-387 (error) Failed to add hierarchical cell %s to the voltage area %s.

DESCRIPTION

write_mdb failed to add a hierarchical cell (and its sub-cells) into the voltage area. This is usually caused by a corrupted hierarchy on the db side.

WHAT NEXT

Verify your data and try again.

SEE ALSO

create_region (3)

WMDB-388 (Warning) Unit conversion needed, this could lead to precision loss.

DESCRIPTION

Current design has different "distance unit" value than the one in target mdb library (specified in the tf file). Therefore write_mdb needs to do the unit conversion.

WHAT NEXT

SEE ALSO

write_mdb (2)

WMDB-389 (error) Unit conversion could lead to precision loss

due to roundoff errors. To proceed regardless of precision loss, use the -enforce_scaling option.

DESCRIPTION

```
This error occurs because the tool defines the distance unit based on the unit
described in the first physical input (for example, in DEF). The error is caused
because the current design has a higher distance unit value than the one in the
target mdb library (specified in the tf file). Writing does not continue due to the
possible data loss caused by roundoff errors during unit conversion.
```

WHAT NEXT

```
Use the -enforce_scaling option to enforce this unit conversion regardless of
potential precision loss due to roundoff errors.
```

WMDB-390 (Info) Unit conversion between pdb and mdb. This could lead to precision loss.

DESCRIPTION

```
The specified pdb file(s) have different "distance unit" value as the one in target
mdb library (specified in the tf file). Therefore the unit conversion could have
precision loss. This usually happens when you specify your own pdb file instead of
the one generated by write_mdb.
```

WHAT NEXT

```
Adjust the unit per micro value in pdb files before write_mdb.
```

SEE ALSO

```
write_mdb (2)
```

WSCR

WSCR-001 (error) Cannot open the output file %s

DESCRIPTION

The output file for write_script cannot be opened.

WHAT NEXT

Verify that the path for the file name exists. If the path does exist, make sure you have access permission.

WSCR-002 (information) SDC supports a subset of the contraints supported by Primetime. Some constraints may not be preserved by write_sdc.

DESCRIPTION

The Synopsys Design Constraints (SDC) format is a subset of the constraints supported by PrimeTime. Some of the constraints which you applied to the design may not be written to SDC. Others may only be partially written.

The following is a complete list of the constraints which are written to SDC with limitations:

• For **set_driving_cell**, the -min and -max options are not supported.

• For **set_port_fanout_number**, the -min and -max options are not supported.

WHAT NEXT

WSCR-003 (information) The design has rise/fall qualified exceptions which will not be written out.

DESCRIPTION

Rise/Fall qualified exceptions are only supported by Primetime. So write_script will

not write out these exceptions for dcsh or dctcl mode. write_sdc also will not write these exceptions.

WHAT NEXT

WSCR-004 (warning) Your SDC output may contain ambiguous names because you have
set the variable sdc_write_unambiguous_names to FALSE.

DESCRIPTION

Beginning with version 1.2, the Synopsys Design Constraints (SDC) format has features ensuring that the cell, net, pin, lib_cell, and lib_pin names written to the file are unambiguous. Some third party applications do no understand these features.

You can set the **sdc_write_unambiguous_names** variable to **false** to suppress these features. This warning reminds you that the setting of this variable may cause your SDC output to be ambiguous.

WHAT NEXT

Verify that you really want to disable the writing of unambiguous names. Review the man pages for the **write_sdc** command and the **sdc_write_unambiguous_names** variable.

SEE ALSO

write_sdc (2), **sdc_write_unambiguous_names** (3).

WSCR-005 (warning) Clock '%s' created with -add option will not be written out.

DESCRIPTION

Multiple clock defination on same pin/port is only supported by PrimeTime. So write_script will not write out these clocks for dcsh or dctcl mode. write_sdc also will not write these clocks.

WSCR-006 (warning) Cannot disable %s objects from %s to %s.

DESCRIPTION

The write_script command has found multiple arcs between the pins noted in the message, such that a non-zero subset of the arcs is disabled and at least one arc is not disabled. Moreover, the write_script command is unable to generate a **filter expression** based on the attributes of the arc objects that can completely distinguish the subset of disabled arcs from the non-disabled ones. If it is the case that some, but not all, of the disabled arcs can be distinguished, then the write_script command will cause that subset only to be disabled.

WHAT NEXT

To match the set of disable arcs between the pins, you need to replicate the methodology by which the arcs were disable in the first place and append the necessary commands to the script file generated by the write_script command.

XTALK

XTALK-001 (information) Starting crosstalk aware timing iteration %d.

DESCRIPTION

The timing update is being performed in the crosstalk aware mode. In this mode multiple crosstalk aware timing iterations might be performed.

WHAT NEXT

For more information please refer to PrimeTime User Guide.

XTALK-002 (information) Setting timing_allow_short_path_borrowing to TRUE.

DESCRIPTION

You receive this informational message because in crosstalk aware timing mode, the **timing_allow_short_path_borrowing** variable must be set to TRUE for accurate crosstalk analysis.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

si_enable_analysis (3), **timing_allow_short_path_borrowing** (3).

XTALK-003 (information) Setting timing_save_pin_arrival_and_slack to TRUE.

DESCRIPTION

You receive this informational message because in crosstalk aware timing mode, the **timing_save_pin_arrival_and_slack** variable must be set to TRUE for accurate

crosstalk analysis.

WHAT NEXT

This is an informational message. No action is required on your part. For more
information, see the *PrimeTime User Guide*.

SEE ALSO

si_enable_analysis (3), **timing_save_pin_arrival_and_slack** (3).

XTALK-004 (information) Number of nets reselected for next iteration: %d.

DESCRIPTION

This message informs you of the number of crosstalk nets that are reselected for
detailed crosstalk aware timing calculation in the next iteration of timing
analysis.

The message is followed by a detailed table showing how many nets were reselected by
each reselection variable. In the following example there is 1 net reselected by
si_xtalk_reselect_min_mode_slack alone. Then 5 nets are reselected by
si_xtalk_reselect_min_mode_slack (and potentially other criteria), 4 by
si_xtalk_reselect_max_mode_slack (and potentially other criteria), and 1 by
si_xtalk_reselect_delta_delay_ratio (and potentially other criteria).

```
Information: Number of nets reselected for next iteration: 5.   (XTALK-004)
Number of reselected nets by criteria:all   exclusively
  si_xtalk_reselect_min_mode_slack5        1
  si_xtalk_reselect_max_mode_slack4        0
  si_xtalk_reselect_delta_delay0        0
  si_xtalk_reselect_delta_delay_ratio1        0
  set_si_delay_analysis -reselect                  0          0
  si_xtalk_reselect_time_borrowing_path           0          0
```

Note that the net counts are based on global nets. I.e., all hierarchical segments
of one global net are counted as one net. Unlike sizeof_collection [get_nets -hier
*] which returns the number of all individual hierarchical segments in the design.

Here 'all' means following number of nets got reselected due to the specific
reselection criteria. And 'exclusively' means out of 'all' these nets a subset of
nets were not covered by other criteria. For example in the above report 1 net got
reselected exclusively due to si_xtalk_reselect_min_mode_slack. Which means if we
disable si_xtalk_reselect_min_mode_slack by setting it to very lage negative number,
then one less net will be reselected, in total.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

si_enable_analysis (3),

XTALK-005 (information) Switching to on-chip-variation analysis type.

DESCRIPTION

Crosstalk analysis requires the on-chip-variation analysis type. The main reason is that minimum and maximum arrival times on aggressor nets are used to compute crosstalk effect on both minimum and maximum arrival times on the victim net. That means that the design can be in both minimum and maximum operating conditions at the same time.

WHAT NEXT

Once finished with crosstalk analysis use **set_operating_conditions** to return the design to the desired analysis type.

SEE ALSO

set_operating_conditions(2), si_enable_analysis(3).

XTALK-006 (information) Maximum number of crosstalk iterations %d was changed to %d.

DESCRIPTION

Variable **si_xtalk_exit_on_max_iteration_count** must be greater than or equal to 1.

WHAT NEXT

Use only valid range of maximum iteration count.

`si_xtalk_exit_on_max_iteration_count(3).`

XTALK-007 (error) Command read_parasitics -keep_capacitive_coupling requires si_enable_analysis set to TRUE.

DESCRIPTION

You receive this message if you execute **read_parasitics** with the **-keep_capacitive_coupling** option and crosstalk analysis is not enabled; that is, the variable **si_enable_analysis** is set to false. The option **-keep_capacitive_coupling** is a part of crosstalk analysis; to use it, you must enable crosstalk analysis.

WHAT NEXT

If you want to use the **-keep_capacitive_coupling** option, first set the **set si_enable_analysis** variable to true. Then reexecute **read_parasitics -keep_capacitive_coupling**. Otherwise, reexecute **read_parasitics** without the **-keep_capacitive_coupling** option.

SEE ALSO

`read_parasitics` (2); `si_enable_analysis(3).`

XTALK-008 (information) Crosstalk analysis was interrupted by user before iteration %d.

DESCRIPTION

You receive this message if PrimeTime receives an interrupt signal while inside the crosstalk iteration loop. The interrupt probably occurred because you pressed Control-C on the Unix workstation. As with other crosstalk exit criteria, PrimeTime completes the current iteration, then exits. The message informs you of the iteration number that was completed. For more information about exit criteria, see the manual page for any of the **si_xtalk_exit_on_*** variables.

WHAT NEXT

This is an informational message only; no action is required on your part. Be aware that fewer iterations of crosstalk analysis were performed; therefore, any report is more pessimistic.

`si_xtalk_exit_on_max_iteration_count` (3),

XTALK-009 (Error) For crosstalk analysis, timing_slew_propagation_mode can be set only to "worst_slew".

DESCRIPTION

You receive this error message because the **timing_slew_propagation_mode** variable can be set only to "worst_slew" in crosstalk aware timing mode.

WHAT NEXT

Set the **timing_slew_propagation_mode** variable to "worst_slew" if you want to set the **si_enable_analysis** variable. If you want to set **timing_slew_propagation_mode** to anything other than "worst_slew", you should set **si_enable_analysis** to false.

SEE ALSO

si_enable_analysis (3), **timing_slew_propagation_mode** (3).

XTALK-010 (information) Design has signal integrity data but signal integrity analysis is disabled.

DESCRIPTION

You received this error message because the **si_enable_analysis** variable has been set to **false** while the design still has signal integrity data, such as coupling capacitors. Signal integrity analysis will not be performed. Thus the signal integrity data is redundant and only increases memory usage.

WHAT NEXT

First, determine whether you want to perform signal integrity analysis. If you do, then set **si_enable_analysis** to **true**. If you do not and memory usage is not an issue, then no action is required on your part. However, if memory usage is important, do not use the **read_parasitics command** with the **-keep_capacitive_coupling** option to save memory.

XTALK-011 (information) Signal integrity analysis is enabled but the design has no signal integrity data.

DESCRIPTION

You received this error message because the **si_enable_analysis** variable has been set to **true** while the design has no signal integrity data, such as coupling capacitors.

WHAT NEXT

First determine whether you want to perform signal integrity analysis. If you do, then use the **read_parasitics command** with the **-keep_capacitive_coupling** option and analyze the output to verify that coupling parasitics data has been correctly read in. If you do not, then set **si_enable_analysis** to **false**.

SEE ALSO

`read_parasitics` (2), `si_enable_analysis` (3).

XTALK-012 (information) Signal integrity analysis is disabled. All
 SI-related global variables are no longer in use. Any coupling capacitors
 are reduced to ground by the reduction factor of one.

DESCRIPTION

You receive this message because the **si_enable_analysis** variable has been set to *false*.

WHAT NEXT

First, determine whether you want to perform regular PrimeTime analysis. If you do not, set **si_enable_analysis** to *true*. If you want to reduce the coupling capacitors with another factor, the annotated parasitics has to be removed and a new one read in by using the **read_parasitics** command with the appropriate factor.

read_parasitics (2), **remove_annotated_parasitics** (2), **si_enable_analysis** (3).

XTALK-014 (Warning) Crosstalk analysis with logically exclusive clocks could be conservative.

DESCRIPTION

You receive this warning message because **set_clock_groups** -logically_exclusive is applied when the signal integrity analysis is enabled (**si_enable_analysis** is true) or vice versa. This is to inform you that signal integrity analysis result could be pessimistic with exclusive clocks compared to analyzing each clock group separately. Even when the clocks are exclusive, they still might be active and physically coupled before the clock selection mux. Crosstalk correctly analyzes this. The crosstalk affect after the clock selection mux could be over estimated when the victim and aggressor arrival windows driven by clocks which are exclusive to each other.

WHAT NEXT

If this pessimism is not acceptable, one of the following approach could be adopted. (1) If the clocks are phsycially exclusive to each other use -physically_exclusive. (2) Only the clocks which could coexist in the chip at the same time should be created/derived for a single anlysis. (3) Only the clocks of one clock group will be activated at any time using **set_active_clock**. (4) The proper set of clocks propagated by setting **set_case_analysis** on the clock selection muxes.

When a proper set of clocks are analyzed together, it runs faster by analyzing only feasible crosstalk affect. The process of clock generation / activation / selection should be carefully done in the STA environment, to match the tool with the behaviour of the chip.

SEE ALSO

si_enable_analysis (3), **pba_enable_path_based_physical_exclusivity** (3), **remove_clock_groups** (2), **set_clock_groups** (2), **set_case_analysis** (2), **set_active_clocks** (2).

XTALK-015 (information) Setting rc_cache_min_max_rise_fall_ceff to TRUE.

DESCRIPTION

You receive this informational message because in crosstalk aware timing mode, the

rc_cache_min_max_rise_fall_ceff variable must be set to TRUE for accurate crosstalk analysis.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

si_enable_analysis (3), **rc_cache_min_max_rise_fall_ceff** (3).

XTALK-016 (information) Starting incremental signal integrity update.

DESCRIPTION

Update of timing and noise data is done incrementally (faster than full default update). The incremental updates are faster because only the affected parts of the design are updated. E.g., after size_cell the nets connected to the cell, their aggressors are reselected and their fanout cone are reevaluated. Due to iterative nature of signal integrity updates the incremental update may not perfectly match the full update if number of iterations is small. The difference should be marginal in most cases but if significant then please perform full update or increase number of iterations.

WHAT NEXT

This is an informational message. No action is required on your part. However, you can trade off accuracy for performance by forcing full update by e.g., **update_timing -full**

SEE ALSO

update_timing (2), **update_noise** (2), **si_xtalk_exit_on_max_iteration_count** (3), **si_xtalk_incr_iteration_count** (3).

XTALK-017 (information) Setting timing_update_effort to low.

DESCRIPTION

You received this informational message because incremental update of timing and noise has been enabled. Where possible, PrimeTimeSI automatically performs an incremental timing update when a change occurs that invalidates the timing of the

design.

Incremental signal integrity analysis generally requires more timing information to be updated. For example, nets coupled with a changed net need to be updated. PrimeTimeSI will revert to a full timing update depending on the number and severity of changes (see PTE-018).

The **timing_update_effort** variable must be set to low to ensure that the timing update will be incremental.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

update_timing (2), **update_noise** (2), **si_xtalk_exit_on_max_iteration_count** (3), **si_xtalk_incr_iteration_count** (3), **timing_update_effort** (3), **XTALK-016** (3), **PTE-018** (3).

XTALK-018 (information) Command '%s' requires signal integrity analysis enabled.

DESCRIPTION

You received this error message because the **si_enable_analysis** variable has been set to **false** while the commend requires signal integrity analysis.

WHAT NEXT

Determine whether you want to perform signal integrity analysis. If you do, then set **si_enable_analysis** to **true**. to save memory.

SEE ALSO

report_si_bottleneck (2), **si_enable_analysis** (3).

XTALK-019 (information) report_si_bottleneck found zero net to

report.

DESCRIPTION

You received this error message because the report_si_bottleneck command has filter out all the candidate nets.

WHAT NEXT

Relax the filtering criteria of this command. For example, include clock nets, lower the number of active aggressors, include both min and max analysis, or increase the slack (by make it more positive.)

SEE ALSO

report_si_bottleneck (2),

XTALK-020 (information) Setting rc_driver_model_mode to basic.

DESCRIPTION

You receive this informational message because in crosstalk aware timing mode, the **rc_driver_model_mode** variable must be set to basic. Advanced driver model is not supported in crosstalk analysis.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

si_enable_analysis (3), **rc_driver_model_mode** (3).

XTALK-021 (Warning) Usage of the -slack_lesser_than option in report_si_bottleneck requires that

timing_save_pin_arrival_and_slack be set to true.

DESCRIPTION

You received this error message because the **timing_save_pin_arrival_and_slack** variable is set to **false**, while the command option requires that it be set to **true**. The default value of the **timing_save_pin_arrival_and_slack** variable is **false** to save memory.

WHAT NEXT

No explicit action is required on your part - PrimeTime sets the value of **timing_save_pin_arrival_and_slack** to **true** when a command requiring it is issued.

SEE ALSO

report_si_bottleneck (2).

XTALK-101 (information) Crosstalk net re-selection: Pin Slack Thresholds - Min-mode %.2f, Max-mode %.2f

DESCRIPTION

These are the crosstalk nets that are re-selected for detailed crosstalk aware timing calculation in the next iteration of timing analysis.

WHAT NEXT

For more information please refer to PrimeTime Modeling User Guide.

XTALK-102 (information) Net Re-selection criteria was : Critical Path Only.

DESCRIPTION

These are the crosstalk nets that are re-selected for detailed crosstalk aware timing calculation in the next iteration of timing analysis.

WHAT NEXT

For more information please refer to PrimeTime Modeling User Guide.

XTALK-103 (information) Crosstalk net re-selection: Delta Delay Thresholds - Abs %.2f, Ratio %.2f

DESCRIPTION

These are the crosstalk nets that are re-selected for detailed crosstalk aware timing calculation in the next iteration of timing analysis. Abs shows the value of the variable **si_xtalk_reselect_delta_delay** and Ratio shows the value of the variable **si_xtalk_reselect_delta_delay_ratio**.

WHAT NEXT

For more information please refer to PrimeTime Modeling User Guide.

XTALK-104 (information) Removing crosstalk between nets %s and %s.

DESCRIPTION

You receive this informational message because the annotation on a net is being removed. Because of this, all coupling capacitances between the net being removed and aggressor nets are put to ground on the aggressor nets.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

SEE ALSO

remove_annotated_parasitics (2).

XTALK-105 (information) Number of nets evaluated in the previous iteration: %d.

DESCRIPTION

This message specifies the number of nets that were evaluated during each crosstalk-aware timing update iteration. This number includes the number of selected nets in that iteration plus any other net in its fanout cone of logic that needed a timing update.

For more information, see the *PrimeTime User Guide.*

remove_annotated_parasitics (2).

XTALK-106 (information) Following net is not reselected for next iteration %s.

DESCRIPTION

You receive this informational message because the net was not reselected for the next iteration, though you wanted to reselect it by applying the command set_si_delay_analysis -reselect. This net is removed from crosstalk analysis either by filtering or screening in first iteration.

WHAT NEXT

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide.*

SEE ALSO

set_si_delay_analysis (2)

XTALK-107 (Warning) Cannot remove %s that was not set on net(s) %s %s.

DESCRIPTION

You receive this warning message because the behaviour that you are trying to reset was not set on the net. This may also be due to the following reasons.

a) You have set the net to be globally excluded or separated from all the nets and are trying to remove an individual pairwise behavior.

b) You have set the net to be pairwise excluded or separated from some nets and you are trying to remove the exclusion or separation globally.

c) The exclusive group that you have specified was not set.

WHAT NEXT

You can use the report_si_delay_analysis, report_si_noise_analysis or report_si_aggressor_exclusion commands to view the exclusions, separations or aggressor exclusive groups applied on the specified nets respectively.

For more information, see the *PrimeTime User Guide*.

SEE ALSO

report_si_delay_analysis(2), report_si_noise_analysis (2), **report_si_aggressor_exclusion(2), remove_si_delay_analysis(2), remove_si_noise_analysis** (2), **remove_coupling_separation(2), remove_si_aggressor_exclusion** (2)

XTALK-201 (Error) For clock OCV pessimism reduction, timing_remove_clock_reconvergence_pessimism should be enabled.

DESCRIPTION

You receive this error message because the **timing_remove_clock_reconvergence_pessimism** variable can be set only to "true" when the clock OCV pessimism reduction is anabled.

WHAT NEXT

Set the **timing_remove_clock_reconvergence_pessimism** variable to "true".

SEE ALSO

pba_enable_xtalk_delay_ocv_pessimism_reduction (3).

XTALK-302 (Information) The higher iteration is less likley to improve the result, so exiting from the iteration loop.

DESCRIPTION

You receive this message because the adaptive reselection found that higher iteration recalculation has lower potential for quality of result (slack, path arrival) improvement. It is exiting from the iteration loop.

WHAT NEXT

If the timing violation shows even from the uncoupled analysis, the constraint and the design should be fixed.

SEE ALSO

set_si_delay_analysis(2).

>TH messages n "Oct 2007"

This message informs about the composite aggressor settings.

In normal mode, PrimeTime SI combines the effect of some small aggressors (possibly including filtered ones) into a single composite aggressor, thereby accounting for their worst-case effects in an efficient manner.

In the statistical mode, all of the small aggressors below the threshold are still included as part of the composite aggressor. However, some statistical analysis is applied to adjust the composite bump height to a lower level. This analysis considers the finite probability that all the small aggressors will switch simultaneously to adversely affect the victim. This adjustment results in a more realistic, less pessimistic analysis than the normal composite aggressor mode.

An aggressor is treated as part of the composite aggressor if the bump height is below the threshold (Noise Peak Ratio). The variable "si_xtalk_composite_aggr_noise_peak_ratio" controls this threshold. In statistical mode PrimeTime SI statistically combines the individual aggressors below the threshold. It determines largest composite aggressor bump height having a probability of occurrence no greater than a certain value (Percentile). The variable "si_xtalk_composite_aggr_quantile_high_pct" controls this percentile value.

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

si_xtalk_composite_aggr_mode (3), **si_xtalk_composite_aggr_noise_peak_ratio** (3), **si_xtalk_composite_aggr_quantile_high_pct** (3).

ZDPP-001 (error) Cannot specify option %s with farm type %s.

DESCRIPTION

While trying to add a compute resource using the **add_distributed_hosts** command, an option has been specified that is not compatible with the farm type.

WHAT NEXT

See the man page for the **add_distributed_hosts** command.

ZDPP-002 (error) The option %s must be specified with a farm type of %s.

DESCRIPTION

While trying to add a compute resource using the **add_distributed_hosts** command, an option with the specified farm type.

WHAT NEXT

See the man page for the **add_distributed_hosts** command.

ZDPP-003 (Warning) Unable to add '%d' more hosts. The maximum number of supported hosts is '%d' and '%d' hosts have already been added.

DESCRIPTION

The number of hosts added cannot go above the maximum number of hosts supported.

ZDPP-004 (Error) Cannot add a distributed host with an

unknown host type.

DESCRIPTION

The host type specified is unknown, so the host has not been added.

WHAT NEXT

Ensure that when adding a host, the options are correct. Type help -v
add_distributed_hosts.

ZDPP-005 (error) Failed to create directory '%s'.

DESCRIPTION

The specified directory could not be created by Primetime. You may not have access
to the directory.

WHAT NEXT

Verify the permissions and reissue the command

ZDPP-006 (error) Failed to launch remote processes.

DESCRIPTION

After attempting to launch remote processes, the create_distributed_farm command
waits for the remote processes to notify the master that they are alive. This error
is issued when the master does not receive any notification from a slave. This error
may occur because, the shell script cannot be found at the slave, or there is a
problem with the script or there is a problem with rsh.

WHAT NEXT

Examine the Stdout and Stderr fields for clues as to what has gone wrong. Make sure
that the script is stored in a location that can be accessed by the slave.

ZDPP-007 (Error) The command %s has exceeded the

maximum number of allowable characters

DESCRIPTION

```
The remote execute command can not handle commands greater than 1000 characters
long.
```

WHAT NEXT

```
Use ';' to seperate the remote_execute command_string into a set of individual
commands. If a single command is greater than 1000 lines, place the command in a
script and issue remote_execute {source script}
```

ZDPP-008 (Warning) The variable '%s' contains a directory '%s' that could not be resolved to an absolute path.

DESCRIPTION

```
The master was unable to find the absolute directory location of an entry in a
resolved variable. The erroneous entry will not be sent to the slave.
```

WHAT NEXT

```
Remove or correct the erroneous resolved variable entry.
```

ZDPP-009 (error) The slave was unable to resolve the working directory %s.

DESCRIPTION

```
The working directory is specified during the setup phase of the master. At that
stage a check is done to verify that the working directory is understood by the
master. This error occurred because the slave could not understand the location of
the working directory.
```

WHAT NEXT

```
Change the working_directory to point to a location which can be resolved by the
slave.
```

ZDPP-010 (error) Could not set %s to be the error log .

DESCRIPTION

The error log was set to an invalid file name. The file name given was either a
directory or the filename resolved to a file which could not be opened or the file
name contained a path which could not be resolved.

WHAT NEXT

Choose a valid file name for the error log.

ZDPP-011 (warning) The type of the specified object is not supported .

DESCRIPTION

The object is not of type list,variable,array or collection

WHAT NEXT

Specify an object which is a list,variable,array or collection

ZDPP-012 (warning) The object %s does not exist .

DESCRIPTION

The specified object does not exist. No object will be returned.

WHAT NEXT

Specify an object that does exist

ZDPP-013 (warning) The collection type for object %s is not supported .

DESCRIPTION

The collection type for the specified object is not supported by the distributed

objects functionality.

WHAT NEXT

Only query supported collections.

ZDPP-014 (error) The specified object is not an array .

DESCRIPTION

The specified object must be an array indexed by scenario name

WHAT NEXT

Specify an array of the correct type. An array can be created using the array set command.

ZDPP-015 (error) The specified object %s already exists .

DESCRIPTION

The specified object can not be returned to the master because a variable of that name already exists at the master.

WHAT NEXT

Use unset to remove the variable at the master.

ZDPP-016 (error) Cannot send collection %s to the slave.

DESCRIPTION

The specified collection can not be sent from the master to the slave because the collection type is not supported for set_distributed_variable.

WHAT NEXT

Trasnfer information from the collection into a list or array. Send information to the slave in list or array format.

ZDPP-017 (error) Master/Slave version misalignment detected.
Master : Version => %s
Slave : Version => %s

DESCRIPTION

```
The master launched slaves processes that are not the same version as the master.
The master and slave process will be incompatible in this situation and processing
cannot proceed. This is an unrecoverable error in the PrimeTime master which will
cause the master and all slave processes to exit.
```

WHAT NEXT

```
Ensure the pt_shell wrapper used to launch the master process is the same wrapper
used to launch the slave processes. This should typically be the wrapper in
$synopsys_root/bin/pt_shell.
```

```
If the set_distributed_parameter command has been used to select a specific pt_shell
wrapper script for the slave processes, ensure this script launches the same version
of PrimeTime as the script used to launch the master process.
```

```
See the set_distributed_parameters command for more details.
```

ZDPP-018 (error) Exiting master prcess due to a critical distribution error.

DESCRIPTION

```
The master process has detected a critical distribution error which has caused it to
exit.
```

WHAT NEXT

```
Examine the prior errors to determine and correct the problems encountered giving
rise to the problem.
```

```
A problem such as master/slave version misalignment can cause this such a critical
error, see ZDPP-017.
```

ZDPP-019 (error) Could not set variable %s because the variable already exists and cannot be overwritten due to

incompatible type.

DESCRIPTION

This error has occurred because get/set_distributed_variables has been issued and a
variable cannot be overwritten at the master/slave as a variable of that name
already exists at the master/slave of incompatible type. The following variable type
transitions are allowed variable -> collection variable -> list collection ->
variable collection -> list list -> variable list -> collection The following
variable type transitions are not allowed array -> collection array -> list array ->
variable collection -> array list -> array variable -> array

WHAT NEXT

Remove the existing variable using the unset command

ZDPP-020 (error) The farm submission script '%s' could not be accessed.

DESCRIPTION

While trying to add compute resources of type lsf/grd/generic, the script specified
to launch jobs on the farm could not be accessed. This script is specified using the
-setup_path and -submission_script options to the **add_distributed_hosts** command.

WHAT NEXT

Ensure that the script specified by the -submission_script option can be found at
the location specified by the -setup_path option.

See the man page for the **add_distributed_hosts** command.

ZDPP-021 (error) Exiting master process due to a critical communication error.

DESCRIPTION

The master process has detected a critical communication error from which it cannot
recover and needs to terminate.

The likely cause is that a slave process has terminated while communicating with the master. Examine the slave logs to determine why the slave process(s) may have terminated pre-maturely.

ZDPP-022 (error) Found null value in merged_object when -null_merging_method was set to error.

DESCRIPTION

When merging variables at the master, this error is issued because the -null_merging_method is set to error and a null value has been found

WHAT NEXT

Find the source of the null value.