EE214a Project

Amy Yen

Matthew Feldman

Table : Summary of Specs

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Gain** | **Bandwidth** | **Power** | **G\*BW/Power** | **CM Output Voltage** |
| **Required** | 30.000 kΩ | 90.0000 MHz | 2.0000 mW |  | [-150 mV, 150 mV] |
| **Achieved** | 30.019 kΩ | 96.6133 MHz | 1.9444 mW |  | -114.45 mV |

Table : Summary of Areas

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Core Circuit** | **Bias Circuit** | **VPMOS-bias** | **VNMOS-bias** |
| **Area** | 134.236 µm | 493.4545 µm | 46 µm | 54 µm |
| **% of Core Circuit** | 100% | 367.6% | 34.3% | 42.5% |





Figure 2: Inside of “COMPUTE CIRCUIT PARAMETERS” Block

**COMPUTE CIRCUIT PARAMETERS**

Figure 1: Overview of Optimization Process



Figure 3: Schematic of Final Circuit

|  |  |  |
| --- | --- | --- |
| Node | Time Constant | Assumptions |
| 1 - Input | ~ | Cin >> Cgs2 |
| 2 - Vx |  |  |
| 3 - Vy |  |  |
| 4 - Vz |  |  |
| 5 - Vout |  | Cgs10 <<  >> 1 |

|  |  |
| --- | --- |
| Stage | Gain |
| 1 - CG |  |
| 2 – Cascode |  |
| 3 – CS |  |
| 4 – CD |  |

Table : Time Constant Approximations Table : Gain Approximations

When working out the design by hand, we started by figuring out properties of the circuit at the output node. We took into account the gm/Id methodology to aim for the most efficient trans-conductance (i.e. gain) vs power

1. Find sweeping range for Vz to be between 1.15V and 1.85V
   1. We know that Vout = 0V because of the common-mode output requirement
   2. We know that the overdrive voltage on any transistor must be bigger than 0.15V, but we also know that a bigger overdrive voltage will result in worse power consumption
   3. Since Mn10’s source is not connected to its bulk, we know that there will be body effect, resulting in a larger Vth, which we assumed to be ~1V
   4. To keep Mn10’s Vov > 0.15V, this means Vz must be greater than 1.15V
   5. To keep Mp8’s Vov > 0.15V, this means Vz must be less than 1.85V
2. Find sweeping range for Vy to be between 0V and -1.85V.
   1. We know that Vy cannot be less than -1.85V, or else Mn7 will not have big enough overdrive. (A stricter bound on Vy may be later computed based on how Vbias\_n is set, such that Mn6 stays in saturation)
   2. We know that Vy cannot be bigger than 0V, because this is the highest voltage of the R3-R4 voltage divider
3. Determine relationship between W7/W8 and Vy:
   1. Assuming minimum L7 and L8, then
4. Determine relationship between R3/R4 and Vy
   1. Treating R3 and R4 as a voltage divider,
5. Find sweeping range for Vin to be between -1.15V and -2.35V. This range will help us figure out the overdrive voltage on Mn2
   1. We know that the lower bound for Vin must not go 0.5V below Vbias\_n or else Mn1 will go into linear. Assuming Vbias\_n was set to it’s minimum of -1.85V, then the absolute minimum for Vin is -2.35V
   2. We know that Mn2 has body effect, so if we estimate the overdrive to be about 1V, then Vin must be below -1.15V to keep Mn2 in saturation with enough overdrive voltage
6. Find sweeping range for Vx to be between 0V and 1.85V
   1. Vx cannot go below 0V, because this is the lowest voltage on the voltage divider. Since the gate on Mn2 is ground, Mn2 will never go into linear with this range.
   2. We know that Vx cannot go above 1.85V, or else Mp4 will not have enough overdrive voltage and will not stay in saturation. (A stricter bound on V\_x may be found later, depending on how Vbias\_p is set, in order to prevent Mp3 from going into linear)
7. Find relationship between R1/R2 and Vx
   1. Treating R1 and R2 as a voltage divider,
8. Once we were able to get relationships and ranges for the properties above, we had to take into account gain to figure out how to size the first resistor stack relative to the second resistor stack.
   1. Assuming the Common Drain stage will have gain slightly less than 1, and that the gain of the Common Source stage should be close to -1 in order to minimize the Miller Effect on Cgd7, this means that the parallel combination of R1-R2 and R3-R4, times gm4, must be bigger than 30,000Ω. (See Table 4)
   2. Let be “known” values
9. Finally, now that we have a rough estimate of the resistor sizes, we took into account the Zero-Valued Time-Constant (ZVTC) with the estimates shown in Table 3 to figure out how to design the rest of the circuit. We first found the relationship between W10 and how much bandwidth was allocated to the output node:
   1. We know that the output node will be very slow because of the large load capacitance, so we allocated a large percentage, (possibly over 100% if we build in a margin of safety for our target BW) of the ZVTC of to this node.
   2. Using Vov10 as calculated previously, and L10 to be 1um, we find can find W10 with:
10. Find relationship between W9 and Vbias\_n
    1. MN9 has same Id as MN10 (because they are in the same stack).
    2. In order to minimize the capacitors that Mn9 contributes, we want to keep W9 as small as possible.
    4. Since Mn9 is a bias current generator, we want Vbias\_n to be as big as possible so that in does not affect the speed of the circuit and since we do not need to worry about it generating gain. However, a larger Vbias\_n has consequences on the rest of the circuit. Specifically, it pushes the lower bound on Vin higher, which lowers the overdrive on Mn2, which makes the input node slower.
11. Determine relationship between W2 and
    1. Choose small gm/id (i.e. big overdrive) for this stage because this is a CG with close to unity current gain).
    2. Allocate some percentage of the time constant to this node, of ZVTC.
    3. , according to Table 4
    4. , and let L be minimum value of 1um
12. Determine relationship between W1, W3, Vbias\_n, and Vbias\_p
    1. Ideally, Mn1, Mn2, and Mp3 have the same current
    2. Vov1 = Vov9, which has already been set.
    4. Similarly,
    5. For MP3, since it’s a bias xtor, pick small W=2u and small L=1u. From Id3, W3, and L3, we can solve for Vov3, which determines the voltage pmos biasing generator circuit needs to generate.
13. Determine relationship between W4, W5, W6, and Vbias\_n
    1. We want W4 = W5 so there is a gain of -1 from the input to the inner node of the cascade. This minimizes Miller Effect on Cgd4
    2. As usual, we choose minimum lengths for all devices
    3. We know Mp4, Mp5, and Mn6 have the same current
    4. , we have a relationship between W4 and Id4, and therefore also between W4, W5, and W6 (equations omitted for brevity)
14. Determine W7 and W8
    1. We know W7/W8 from previously.
    2. Given our power budget and knowing the amount of current in every other stack (three transistor stacks and two resistor stacks), we allocated whatever remaining current there was to this stack. Knowing the overdrive of both devices, we could calculate the sizes.
    3. Total power = 2mW, Power in resistor stacks = , Power in transistor stacks = 5 \* Id

Using the previous steps, it is easy to separate our independent variables from our dependent variables. We optimized the circuit by playing with time constants, gain values for various stages, power constraints, and DC operating voltage constraints. We used knowledge about the different kinds of tradeoffs to help us choose how to select parameters, such as gm/Id methodology and transit frequency estimates. See Figure 1 on Page 1 for a summary. We eventually converged on a working circuit, shown in Figure 3 on Page 2.

The last step was to design the bias circuitry. We opted to use a current mirror with a resistor current source on the original current and a diode-connected transistor to “compute” the voltage in the mirrored current stack.

Table 6 below shows a summary of a few select properties and how they varied between what we expected them to be based on computation, and what they ultimately were in our final design after we did educated tweaking of our best candidates.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **M1** | **M2** | **M3** | **M4** | **M5** | **M6** | **M7** | **M8** | **M9** | **M10** |
| **SPICE Vov (V)** | 0.90 | 0.54 | 0.89 | 0.79 | 0.73 | 0.90 | 0.74 | 0.94 | 0.90 | 0.14 |
| **Computed Vov (V)** | 0.93 | 0.67 | 4.64 | 0.40 | 0.40 | 0.93 | 0.40 | 1.25 | 0.93 | 0.25 |
| **% error** | 3.7% | 24.3% | 418.9% | 49.3% | 45.4% | 3.6% | 46.3% | 33.5% | 3.6% | 73.6% |
| **SPICE Id (uA)** | 180.80 | 180.80 | 122.40 | 68.40 | 68.40 | 64.10 | 37.60 | 37.60 | 45.00 | 39.30 |
| **Computed Id (uA)** | 125.11 | 87.13 | 19.99 | 25.19 | 21.72 | 60.31 | 205.03 | 33.19 | 20.10 | 7.15 |
| **% error** | 30.8% | 51.8% | 83.7% | 63.2% | 68.2% | 5.9% | 445.3% | 11.7% | 55.3% | 81.8% |
| **Final W (um)** | 17 | 20 | 23 | 8 | 8 | 6 | 2 | 3 | 4 | 60 |
| **Computed W (um)** | 19 | 12 | 2 | 3 | 3 | 6 | 15 | 3 | 2 | 14 |
| **Final L (um)** | 2 | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 2 | 1 |
| **Computed L (um)** | 3 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 2 | 1 |

Table : Comparison between SPICE results and expected results

**Source of errors**

1. Over-simplification of time constants, ignoring extrinsic capacitances, Cds, and considering intrinsic capacitances negligible to input and output capacitances.
2. Current leaked between transistor stack and resistor stacks, hence changing the gate voltages on Mp4 and Mn7, as well as the operating points of all transistors
3. Neglecting channel length modulation, so DC currents were not exactly what we calculated
4. gm/Id and transit frequency methodology only provided rough estimates for performance
5. Did not consider bias circuit power or feedback effects

**Optimization Process Notes**

1. Manually resized transistors to lower current leakage between stacks and ensure saturation
2. Occasionally used gain and bandwidth outputs by SPICE at each node to target which nodes are significantly hurting our performance

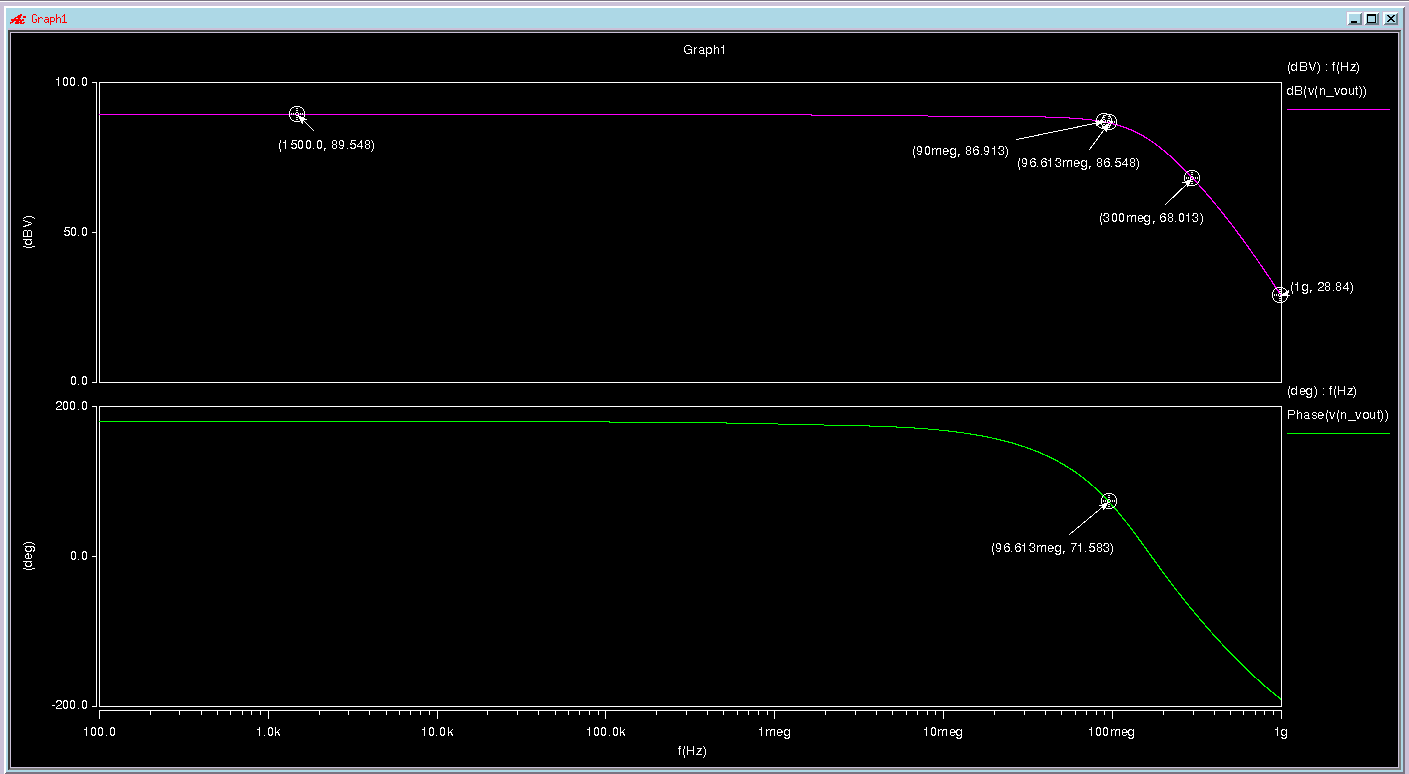


Figure 3: Annotated Bode Plot with 1A input source

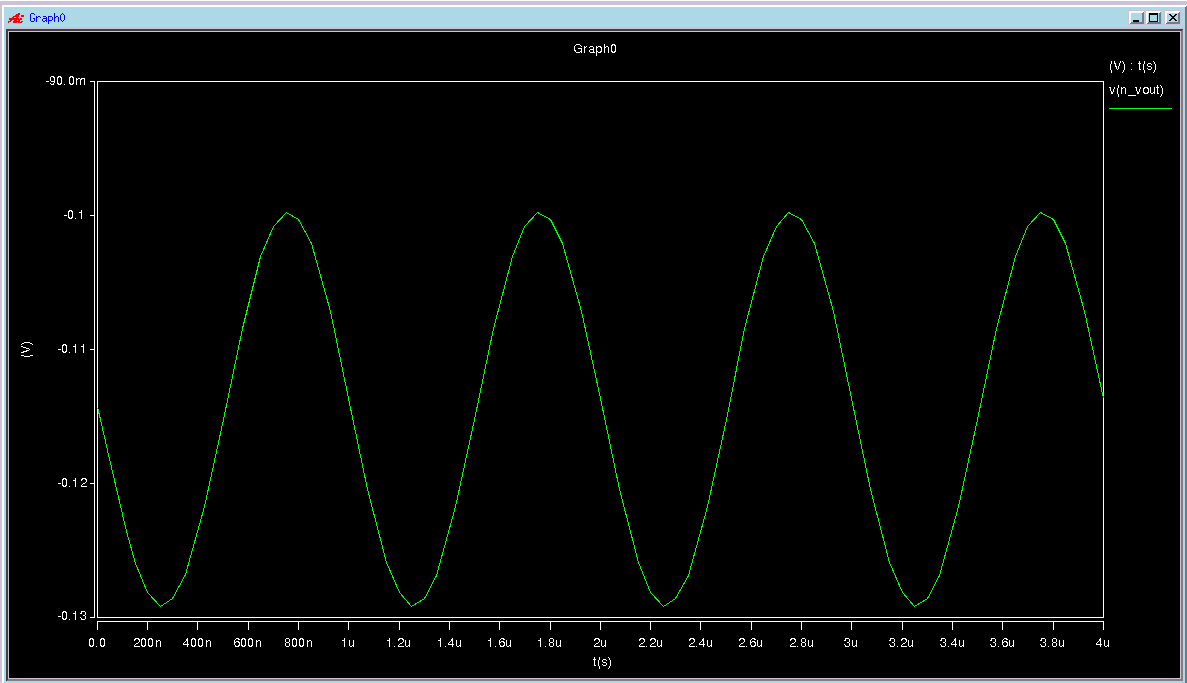


Figure 5: Transient with 1MHz, 1uA input current source showing no distortion

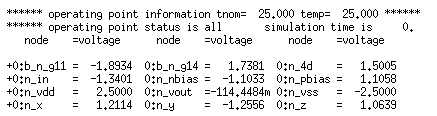
This project proved to be a challenging, many-hour task. In order to find a working design for the circuit, we went through numerous stages that flowed from analysis to confusion to discovery to frustration and repeat.

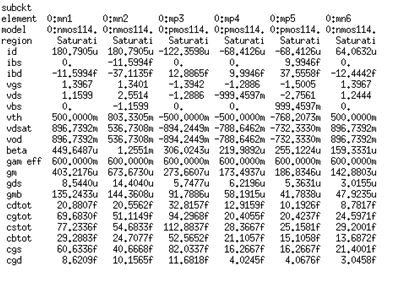
One of the valuable take-aways from this project was what circuit design is actually like. Up to this point in our academic career, we have only taken circuits classes that focus on analysis rather than design. This was our first experience that required us to use analysis as a tool in the feedback loop of the design process. We now have a deeper appreciation of how analysis simplifications and assumptions can turn a vastly complex circuit into fundamental components that can be managed by hand. Furthermore, while these assumptions help to get us a first order design, we also learned to appreciate their limitations and the more nuanced effects that cause the hand-calculated design to differ from what happens in the actual circuit when all effects are taken into account.

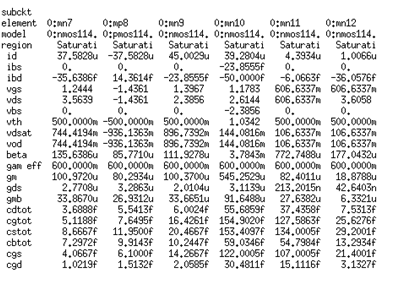
However, one of the drawbacks of the project was that, at times, it felt like the techniques that were taught in class did not really help too much with design, except for having some intuition on which knobs control what in a circuit. There seemed to be a lot of “educated” tweaking that we used to fix the circuit, but could not replicate the exact numbers on paper because of channel length modulation, body effect, loading effect, and other non-ideal factors. While the homework throughout the course broke parts of this design process into fundamental components, there still seemed to be a huge gap between those problems and this design project.

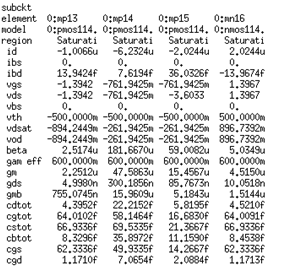
**APPENDIX I**

**.op Output (Only MOSFET and Node Voltage listings)**









.**sp File**

\* Design Problem, ee114/214A-2015

\* Team Member 1 Name: Matthew Feldman

\* Team Member 2 Name: Amy Yen

\* Please fill in the specification achieved by your circuit

\* before you submit the netlist.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\* sunetids of team members = mattfel, htyen

\* The specifications that this script achieves are:

\* Power <= 2.00 mW

\* Gain >= 30.0 kOhm

\* BandWidth >= 90.0 MHz

\* FOM >= 1350

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.param W1\_val = 17u

.param L1\_val = 2u

.param W2\_val = 20u

.param L2\_val = 1u

.param W3\_val = 23u

.param L3\_val = 2u

.param W4\_val = 8u

.param L4\_val = 1u

.param W5\_val = 8u

.param L5\_val = 1u

.param W6\_val = 6u

.param L6\_val = 2u

.param W7\_val = 2u

.param L7\_val = 1u

.param W8\_val = 3u

.param L8\_val = 1u

.param W9\_val = 4u

.param L9\_val = 2u

.param W10\_val = 60u

.param L10\_val = 1u

.param R1\_val = 9.400000k

.param R2\_val = 15.400000k

.param R3\_val = 90.000000k

.param R4\_val = 68.000000k

.param Vbias\_p\_val = 1.100000

.param Vbias\_n\_val = -1.100000

\*\* Including the model file

.include /usr/class/ee114/hspice/ee114\_hspice.sp

\* Defining Top level circuit parameters

.param p\_Cin = 220f

.param p\_CL = 250f

.param p\_RL = 20k

\* defining the supply voltages

vdd n\_vdd 0 2.5

vss n\_vss 0 -2.5

\* Defining the input current source

\*\* For ac simulation uncomment the following 2 lines\*\*

Iin n\_in 0 ac 1

\*\* For transient simulation uncomment the following 2 lines\*\*

\*Iin n\_in 0 sin(0 0.5u 1e6)

\* Defining Input capacitance

Cin n\_in 0 'p\_Cin'

\* Defining the load

RL n\_vout 0 'p\_RL'

CL n\_vout 0 'p\_CL'

\*\*\* Your Trans-impedance Amplifier here \*\*\*

\*\*\* d g s b n/pmos114 w l

\* nmos b tied to lowest voltage

\* pmos b tied to highest voltage (or s)

\* xtor stack 1

MN1 n\_in n\_nbias n\_vss n\_vss nmos114 w='W1\_val' l='L1\_val'

MN2 n\_x 0 n\_in n\_vss nmos114 w='W2\_val' l='L2\_val'

MP3 n\_x n\_pbias n\_vdd n\_vdd pmos114 w='W3\_val' l='L3\_val'

R1 n\_x n\_vdd 'R1\_val'

R2 n\_x 0 'R2\_val'

\* xtor stack 2

MP4 n\_4d n\_x n\_vdd n\_vdd pmos114 w='W4\_val' l='L4\_val'

MP5 n\_y 0 n\_4d n\_vdd pmos114 w='W5\_val' l='L5\_val'

MN6 n\_y n\_nbias n\_vss n\_vss nmos114 w='W6\_val' l='L6\_val'

R3 n\_y 0 'R3\_val'

R4 n\_y n\_vss 'R4\_val'

\* xtor stack 3

MN7 n\_z n\_y n\_vss n\_vss nmos114 w='W7\_val' l='L7\_val'

MP8 n\_z n\_z n\_vdd n\_vdd pmos114 w='W8\_val' l='L8\_val'

\* xtor stack 4

MN9 n\_vout n\_nbias n\_vss n\_vss nmos114 w='W9\_val' l='L9\_val'

MN10 n\_vdd n\_z n\_vout n\_vss nmos114 w='W10\_val' l='L10\_val'

\*\*\* Your Bias Circuitry goes here \*\*\*

\* Bias Circuitry - Vb\_p (Vbias-Gen pmos)

\* a current mirror + a diode connected pmos to compute 1.1V

.param W11\_val = 30u

.param L11\_val = 2u

.param W12\_val = 6u

.param L12\_val = 2u

.param W13\_val = 2u

.param L13\_val = 20u

.param R11\_val = 1000000

MN11 b\_n\_g11 b\_n\_g11 n\_vss n\_vss nmos114 w='W11\_val' l='L11\_val'

MN12 n\_pbias b\_n\_g11 n\_vss n\_vss nmos114 w='W12\_val' l='L12\_val'

MP13 n\_pbias n\_pbias n\_vdd n\_vdd pmos114 w='W13\_val' l='L13\_val'

R11 n\_vdd b\_n\_g11 'R11\_val'

\* Bias Circuitry - Vb\_n (Vbias-Gen nmos)

\* a current mirror + a diode connected nmos to compute -1.1V

.param W14\_val = 14u

.param L14\_val = 2u

.param W15\_val = 4u

.param L15\_val = 2u

.param W16\_val = 2u

.param L16\_val = 20u

.param R13\_val = 680000

MP14 b\_n\_g14 b\_n\_g14 n\_vdd n\_vdd pmos114 w='W14\_val' l='L14\_val'

MP15 n\_nbias b\_n\_g14 n\_vdd n\_vdd pmos114 w='W15\_val' l='L15\_val'

MN16 n\_nbias n\_nbias n\_vss n\_vss nmos114 w='W16\_val' l='L16\_val'

R13 b\_n\_g14 n\_vss 'R13\_val'

\*\*\* defining the analysis \*\*\*

.op

.option post brief nomod

\*\* For ac simulation uncomment the following line\*\*

.ac dec 1k 100 1g

.measure ac gainmax\_vout max vdb(n\_vout)

.measure ac f3db\_vout when vdb(n\_vout)='gainmax\_vout-3'

.measure ac gainmax\_vx max vdb(n\_x)

.measure ac f3db\_vx when vdb(n\_x)='gainmax\_vx-3'

.measure ac gainmax\_vy max vdb(n\_y)

.measure ac f3db\_vy when vdb(n\_y)='gainmax\_vy-3'

.measure ac gainmax\_vz max vdb(n\_z)

.measure ac f3db\_vz when vdb(n\_z)='gainmax\_vz-3'

\*\* For transient simulation uncomment the following line \*\*

\*.tran 0.01u 4u

.end