First pass design strategy

1. Find gain equation at each of the 4 stages
   1. Ignore ro, assume ro >> R1-4
2. Find RC time constaint at each node
   1. Ignore Cgd b/c Cgd = Cov << Cgs = 2/3WLCox + Cov
   2. Ignore bulk terminal caps b/c hard to estimate
3. Product of the 4 gains >= 30k. Allocate a percentage of 30k for each stage
4. 1/(sum of all nodes’ time constants) >= 90MHz. Allocate a percentage of 1/90Mhz for each node.
5. At this point, we have each stage’s gain in function of gm, R; each node’s time constant as a function of gm, R, C. We can correlate the 2 equations to assign values to gm, C, R variables.
6. From gm, we can find W.
7. After all xtors are sized, we will calculate Ids of the xtors connected to Vbias-Gen to determine the biasing voltage.

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| Node | Time Constant | Assumptions/Simplifications | Simplified Time Constant |
| 1 - Input |  | * Cin >> Cgs2 |  |
| 2 - Vx |  | * R2/R1 < 4 |  |
| 3 - Vy |  | * R3/R4 < 4 |  |
| 4 - Vz |  |  |  |
| 5 - Vout |  |  |  |

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| Stage | Gain | Equals | Simplified Time Constant |
| 1 - CG |  | 5000 |  |
| 2 – Cascode |  | 5 |  |
| 3 – CS |  | 1.2 |  |
| 4 – CD |  | 1 |  |
|  |  |  |  |