EE214a Project

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Table 1: Summary of Specs

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Gain** | **Bandwidth** | **Power** | **G\*BW/Power** | **CM Output Voltage** |
| **Required** | 30.000 kΩ | 90.0000 MHz | 2.0000 mW |  | [-150 mV, 150 mV] |
| **Achieved** | 30.019 kΩ | 96.6133 MHz | 1.9444 mW |  | -114.45 mV |

Table 2: Summary of Areas

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Core Circuit** | **Bias Circuit** | **VPMOS-bias** | **VNMOS-bias** |
| **Area** | 134.236 µm | 493.4545 µm | 46 µm | 54 µm |
| **% of Core Circuit** | 100% | 367.6% | 34.3% | 42.5% |

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1. Estimated equations for gain and time constant in each stage

|  |  |  |
| --- | --- | --- |
| Node | Time Constant | Assumptions/Simplifications |
| 1 - Input | ~ | * Cin >> Cgs2 |
| 2 - Vx |  | * R2/R1 < 4 |
| 3 - Vy |  | * R3/R4 < 4 |
| 4 - Vz |  |  |
| 5 - Vout |  | * Cgs10 << * >> 1   => tau = |

|  |  |  |
| --- | --- | --- |
| Stage | Gain | R in terms of gain |
| 1 - CG |  | R2 = 4R1  = gain  => = = gain  => R1 = 5/4\* gain |
| 2 – Cascode |  | R3 = 4R4  = 5  => = 5  => = 5  => R4 = |
| 3 – CS |  |  |
| 4 – CD |  |  |

1. Estimate R1,R2,R3,R4

* To find R3, R4 ratio:

n\_out = 0V and Vov > 0.15 from spec. Vth10 ~ 1V from experimenting with spice

=> Vg10 = Vov + Vth10 = 0.15 + 1 = 1.15; assume 1.2V for some margin

Ids7 = Ids8 => 1/2\*kn\*(W7/L7)(Vy-Vss-Vt)^2 = 1/2\*kp\*(W8/L8)(Vdd - Vz - Vt)^2

=> 2W7(Vy-(-2.5)-0.5)2 = W8(2.5-1.2-0.5)2 => 2W7(Vy+2)2 = W8\*0.82

=> Vy =sqrt( \* ) – 2 = -1.43; to mitigate Miller effect

Vy = Vss \* (R3/(R3+R4)); Vy = voltage divider of Vss assuming no current through R

=> -1.43 = -2.5 \* (R3/(R3+R4))

=> R3/(R3+R4) = 0.572

=> R3/R4 = 1.34

Through iterations, found R3/R4 = 90k/68k yielded the best result

* To find R1 and R2:

Vg2 = 0, Vov2 = -Vs2 – Vth2 > 0.15 => Vs2 < -0.15 - 0.5 = -0.65

Sweep 0 < Vx < 1.8:

Vx < 1.8 or else M4 will not have enough overdrive:

Vov4 = Vdd - Vx - Vt4 > 0.15 => Vx < 2.5 - 0.5 - 0.15 = 1.85

Vx > -0.5 or else M2 goes into triode region: Vds2 > Vov2 => Vx – Vs2 > 0.15

=> Vx > 0.15 + Vs2 = 0.15 - 0.65 = -0.5

Vx can’t be lower than 0 b/c the voltage divider cannot go lower than ground

=> 0 < Vx < 1.8

Through iterations, found Vx = 0.9V yielded best result

=> Vx = Vdd \* (R1/(R1+R2))

=> 0.9 = 2.5 \* (R1/(R1+R2)) => (R1/(R1+R2) = 0.36

=> R1 = 0.36R1 + 0.36R2 => 0.64\*R1 = 0.36\*R2 => R1/R2 ~ 0.6

Through iterations, found R1/R2 = 9.4k/15.4k = 0.6 is the best choice.

1. Use gm/id design methodology to size the xtors:
2. Start with output stage. Pick gm/id of 8 (8-10 is valid range, 8 is the best one from iterations) for MN10 based on the gm/id v.s. ft and v.s. gain graphs presented in discussion section. Time constant ~ gm10/Cl = allocated 110% of target 90MHz. Solve for gm10. From gm10 and gm/id of 8, solve for id10. From gm and Id, solve for Vov10. Pick min L of 1u for MN10 (CD gain stage). From L, Vov, and id, get W10.
3. MN9 has same Id as MN10 (b/c within same branch). Since MN9 is a bias xtor, pick small L (2u) and min W (2u). Calculate Vov9 = sqrt((2\*Ids9)/(kp\*(W9/L9))).
4. Next tackle input stage. Pick gm/id of 3 for MN2 (small gm/id for this stage b/c this is a CG with close to unity current gain). Time constant on the input node ~ Cin/gm2 = allocated 6% of total 110Mhz. Solve for gm2 = Cin \* 110Mhz/0.06. From gm2 and gm/id of 3, solve for id2. From id and gm, solve for Vov2. Pick min L of 1 us for MN2 (CG gain stage). From L, Vov, and id, get W2.
5. Id2 = Id1 = Id3 (b/c within same branch).
   1. Vov1 = Vov9 per schematic. Find W1 from Id1 and Vov1
   2. For MP3, since it’s a bias xtor, pick small W=2u and small L=1u. From Id3, W3, and L3, we can solve for Vov3, which determines the voltage pmos biasing generator circuit needs to generate.
6. 2nd stack, MN6 is a bias xtor. Pick L6=2u, W6=6u (big enough to match our allocated Ids %). Vov6 = Vov9. From Vov, l, and W6, solve for Id6.
7. Id4 = Id5 = Id6 (b/c within same branch)
   1. For MP4, pick Gm/id=5 (we assigned same gm/id for 2nd and 3rd stack; both smaller compared to last stage; 5 is the best pick through iterations). Find gm4 from Id4 and gm/id. From Id and gm, find Vov4. Pick L4=1u. From L, Vov, and Id, solve for W4.
   2. For MP5, we want gm5 ~ gm4 (both in cascade). From gm and Id, solve for Vov5. Pick L5=1u. From L, Vov, and Id, solve for W5.
8. Third stack Id = remaining Id after what the other 3 xtor branches + 4 R’s have already used up = Id8 = id 7
   1. For MP8, we know its Vg8 = Vov10. So Vov8 = Vs8 – Vg8 – Vt = Vov10 – Vdd – Vt. Pick L8=1u. From L, Id and Vov, solve for W8.
   2. For MN7, pick gm/id = 5 (same as 2nd stack). With Id know, solve for gm7. From gm and Id, solve for Vov7. Pick L=1u. From L, Vov, and Id, solve for W7.

Total power budget = 0.002V. Power dissipated by resistor stacks = Vdd2/(R1+R2) + Vss2/(R3+R4). Power to be dissipated by xtors = 0.002 – power dissipated by R’s = 1.71mV.So, Ids to be distributed among 4 stacks = 1.71mV/(vdd-vss) = 0.342mA. Table1 shows how total power is consumed by resistors and xtors. Table 2 shows each xtor stack’s Ids. Table 3 shows the discrepancy in power result from spice sim v.s. the budget our calculation assumed.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| power target | R power | xtor power | total xtor Ids |  |
| 2.00E-03 | 2.92E-04 | 1.71E-03 | 3.42E-04 |  |
| Table1 |  |  |  |  |
|  | stack1 | stack2 | stack3 | stack4 |
| spice Ids | 1.80E-04 | 6.80E-05 | 3.75E-05 | 4.50E-05 |
| Our Ids % | 0.55 | 0.2 | 0.1 | 0.15 |
| calc Ids | 1.34E-04 | 6.48E-05 | 5.92E-05 | 2.16E-05 |
| % error | -2.56E-01 | -4.17E-02 | 5.79E-01 | -5.20E-01 |

Table2

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | RL | R1 | R2 | R3 | R4 | R11 | R13 | total R | total power  dissipated |
| spice power | 6.55E-07 | 1.77E-04 | 9.50E-05 | 1.75E-05 | 2.28E-05 | 1.93E-05 | 2.64E-05 | 3.59E-04 | 1.94E-03 |
| calc R power |  |  |  |  |  |  |  | 2.92E-04 | 2.00E-03 |
| % error |  |  |  |  |  |  |  | -1.86E-01 | 2.86E-02 |

Table3

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | M10 |
| spice Vov | 8.96E-01 | 5.37E-01 | -8.94E-01 | -7.89E-01 | -7.32E-01 | 8.97E-01 | 7.44E-01 | -9.36E-01 | 8.97E-01 | 1.44E-01 |
| calc Vov | 9.29E-01 | 6.67E-01 | 4.64 | 4.00E-01 | 4.00E-01 | 9.29E-01 | 4.00E-01 | 1.25E+00 | 9.29E-01 | 2.50E-01 |
| % error | 3.68E-02 | 2.43E-01 | 4.19E+00 | -4.93E-01 | -4.54E-01 | 3.60E-02 | -4.63E-01 | 3.35E-01 | 3.60E-02 | 7.36E-01 |
| spice gm | 4.03E-04 | 6.73E-04 | 2.73E-04 | 1.73E-04 | 1.86E-04 | 1.42E-04 | 1.00E-04 | 8.00E-05 | 1.00E-04 | 5.45E-04 |
| calc gm |  | 4.03E-04 |  | 3.24E-04 | 3.24E-04 |  | 2.96E-04 |  |  | 1.73E-04 |
| % error |  | -4.01E-01 |  | 8.73E-01 | 7.42E-01 |  | 1.96E+00 |  |  |  |
| spice W | 1.70E-05 | 2.00E-05 | 2.30E-05 | 8.00E-06 | 8.00E-06 | 6.00E-06 | 2.00E-06 | 3.00E-06 | 4.00E-06 | 6.00E-05 |
| calc W | 1.87E-05 | 1.21E-05 | 2.00E-06 | 3.24E-06 | 3.24E-06 | 6.00E-06 | 1.48E-05 | 3.03E-06 | 2.00E-06 | 1.38E-05 |
| spice L | 2.00E-06 | 1.00E-06 | 2.00E-06 | 1.00E-06 | 1.00E-06 | 2.00E-06 | 1.00E-06 | 1.00E-06 | 2.00E-06 | 1.00E-06 |
| calc L | 3.00E-06 | 1.00E-06 | 1.00E-06 | 1.00E-06 | 1.00E-06 | 2.00E-06 | 1.00E-06 | 1.00E-06 | 2.00E-06 | 1.00E-06 |

Table4

**Source of error on Ids stack**

1) Stack4 % error is due to over simplification of tau = Cl/gm equation.

2) Spice sim showed that stack1 and stack2 both had some current leaked to R1-R4; so not all xtor’s Ids within the same stack are the same, violating our assumption. We assumed that no current could leak into the 2 resistor stacks; so bias voltage for MP4 and MN7 are just the voltage divider set by Vx and Vy respectively. With the assumption violated, MP4 and MN7 biasing becomes off.

3) Stack3 Ids is the left over current from other 3 xtor stacks and from the 2 resistor stacks. So the prior % error is carried over here.

**Source of error on mosfet’s Vov**

1. MP3: initially picked of 2u for speed but resulted in a lot of current leaking to R stack. Had to enlarged W3 until minimum leakage.
2. Usage of equations such as: Vov = (2\*Ids)/gm and Vov = (sqrt(2\*Ids)/(kp\*(W/L)) in gm/id methodology assume xtor is in saturation already. The initial hand calculation plugged directly into spice showed a few xtors in linear state. Had to make manual adjustment to put all xtors in saturation state.

**Source of error on mosfet’s gm**: gm/id selection based on nmos’ gm/id v.s. ft and gm/id v.s. gain graphs is rough estimate. Error can result from either the graph itself or our selection point.

**Source of error on mosfet’s W**: usage of this equation, W = (2\*Ids\*L)/(kp\*Vov^2) assumes xtor is in saturation already. Some turned out to be in linear region; need to make adjustment to put into saturation.

**Source of error on power:** Did not account for R’s in bias generation circuit and RL.

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This project proved to be a challenging, many-hour task. In order to find a working design for the circuit, we went through numerous stages that flowed from analysis to confusion to discovery to frustration and repeat.

One of the valuable take-aways from this project was what circuit design is actually like. Up to this point in our academic career, we have only taken circuits classes that focus on analysis rather than design. This was our first experience that required us to use analysis as a tool in the feedback loop of the design process. We now have a deeper appreciation of how analysis simplifications and assumptions can turn a vastly complex circuit into fundamental components that can be managed by hand. Furthermore, while these assumptions help to get us a first order design, we also learned to appreciate their limitations and the more nuanced effects that cause the hand-calculated design to differ from what happens in the actual circuit when all effects are taken into account.

However, one of the drawbacks of the project was that, at times, it felt like the techniques that were taught in class did not really help too much with design, except for having some intuition on which knobs control what in a circuit. There seemed to be a lot of “educated” tweaking that we used to fix the circuit, but could not replicate the exact numbers on paper because of channel length modulation, body effect, loading effect, and other non-ideal factors. While the homework throughout the course broke parts of this design process into fundamental components, there still seemed to be a huge gap between those problems and this design project.

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Appendix I

Appendix I