

As per National Education Policy (NEP-2020 Scheme) from Academic Year 2024 - 2025

Semiconductor Physics

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TechKnowledgeTM
Publications

SYLLABUS

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
BSC2022	Semiconductor Physics	2	--	-	2	-	-	2

Course Code	Course Name	Theory						Term work	Pract / Oral	Total			
		Internal Assessment Test (IAT)			End Sem Exam	Exam Duration (in Hrs)							
		IAT- I	IAT- II	IAT-I + IAT-II (Total)									
BSC2022	Semiconductor Physics	15	15	30	45	2	--	--	--	75			

Course Objectives :

1. To provide students with a basic understanding of Semiconductors in the field of Basic Engineering.
2. To explain basic importance of p-n junction diodes.
3. To learn about few special diode important for semiconductor industry.
4. To understand the basics of transistors and their applications in the field of electronics.
5. To build foundation of Field effect transistors and their applications.
6. To give exposure to the upcoming field of Nano technology in the field of solid state physics.

Course Outcomes :

1. Learners will be able to USE and DEMONSTRATE his/ her ability earned here to apply it to calculate Hall voltage
2. Learners will be able to CALCULATE barrier potential and PLOT I-V characteristics of p-n junction diode.
3. Learners will be able to PLOT I - V characteristics and understand their applications of some special diodes
4. Learners will be able to CALCULATE current gain and PLOT I-V characteristics for CB-CE configurations.
5. Learner will be able to PLOT I-V characteristics and understand applications of FETs
6. Learner will be able to APPLY the knowledge of Nano Technology to certain emerging areas of technology.

Detailed Syllabus :

Sr. No.	Name of Module	Detailed Content	Hours	CO Mapping
	Prerequisite	Band theory of solids Fermi Dirac Distribution function Density of states and	-	-
1	Basics of Semiconductors	Types of semiconductors, Carrier Concentration in Intrinsic Semiconductors, Fermi level of Intrinsic Semiconductors, Variation of Fermi level of Intrinsic Semiconductors, wrt temperature. Extrinsic Semiconductors, Fermi level of Extrinsic Semiconductors, Variation of Fermi level of Extrinsic Semiconductors, wrt temperature and Impurity Concentration, Equation of conductivity with current flow, Hall Effect, Calculation of Hall Voltage. (Refer Chapter 2)	4	CO 1
2	Junction diode	Formation of p-n junction, calculation of barrier potential Diode equation, p-n junction in forward Bias, p-n junction in Reverse bias, Current- voltage curve for p-n junction diode, LED and its working (Refer Chapter 3)	4	CO 2
3	Important Diodes	Working of: Photo diode, solar cell, Zener diode ,Varactor diode ,Gunn diode and their applications. (Refer Chapter 4)	4	CO 3

Sr. No.	Name of Module	Detailed Content	Hours	CO Mapping
4	Bipolar Junction Transistors	BJT Structure and Operation - BJT structure, Modes of operation, CB, CE I-V characteristics BJT Amplification and Switching - Current gain, BJT as a switch, (Refer Chapter 5)	4	C04
5	Field Effect Transistors	Field-Effect Transistors (FETs) - FET types: JFET, MOSFET, Structure and operation MOSFETs in Detail - MOSFET structure, Enhancement and depletion modes, Threshold voltage MOSFET Applications - MOSFET as a switch, (Refer Chapter 6)	6	C05
6	Nano Technology	Introduction to Nanotechnology , Properties (optical, Electrical, Structural, Mechanical) Importance of surface to Volume ratio, Bonding in solids (Vander walls interactions) , Application: Lithography, Single Electron Transfer (SET), Spin Valves.	4	C06

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Unit - I**Chapter 1 : Basics of Semiconductors**

1-1 to 1-23

1.1	Introduction to Semiconductors.....	1-1
1.1.1	Types of Semiconductors.....	1-1
1.1.2	Carrier Concentration in Intrinsic Semiconductor.....	1-2
1.1.3	Fermi Level in Intrinsic Semiconductors.....	1-3
1.1.4	Variation of Fermi level in intrinsic Semiconductor (With Respect to Temperature).....	1-4
1.1.4(A)	Fermi Level in Conductor	1-5
1.1.4(B)	Fermi Level in Semiconductor.....	1-6
1.2	Extrinsic Semiconductor.....	1-8
1.2.1(A)	n-Type Semiconductors.....	1-9
1.2.2(B)	p-Type Semiconductors.....	1-10
1.3	Variation of Fermilevel Extrinsic Semiconductors with respect to Temperature and Impurity Concentration	1-13
1.3.1	Effect of Temperature on n-type Material.....	1-13
1.3.2	Effect of Temperature on p – type Material	1-14
1.3.3	Effect of Impurity on Fermi Level	1-15
1.4	Equation of Continuity.....	1-16
1.5	Hall Effect and Calculation of Hall Voltage.....	1-17
1.5.1	Experimental Determination of Mobility.....	1-18
1.5.2	Applications	1-20
1.6	Solved Problems	1-20

Unit - II**Chapter 2 : Junction Diode**

2-1 to 2-14

2.1	Introduction.....	2-1
2.2	p-n Junction.....	2-1
2.3	Depletion Layer and Potential Barrier.....	2-2
2.3.1	Calculation of Potential Barrier.....	2-3
2.4	Biassing of p-n Junction	2-4

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2.5	Light Emitting Diode (LED) and its Working	2-8
2.6	Solved Problems	2-11

Unit - IIIChapter 3 : Important Diodes

3-1 to 3-15

3.1	Introduction.....	3-1
3.2	Photodiode.....	3-2
3.3	Photovoltaic Cell.....	3-4
3.3.1	Applications of Solar Cell	3-8
3.4	Zener Diode.....	3-9
3.4.1	Physics of Zener Break Down.....	3-10
3.4.2	Application.....	3-10
3.5	Varactor Diode.....	3-12
3.5.1	Symbol of Varactor Diode.....	3-12
3.5.2	Function of Varactor Diode.....	3-12
3.5.3	Important Highlights	3-12
3.6	Gunn Diode.....	3-13
3.6.1	Gunn Effect.....	3-13
3.6.2	Gunn Diode Basics.....	3-13
3.6.3	Function of Gunn Diode	3-14
3.6.4	Applications	3-14

Unit - IVChapter 4 : Bipolar Junction Transistors

4-1 to 4-14

4.1	BJT Structure and Operation	4-1
4.2	Configurations of BJT.....	4-2
4.2.1	Common Base (CB) Configuration	4-2
4.2.1(A)	Current Relations in CB Configuration	4-3
4.2.1(B)	Current Amplification Factor or Current Gain (α or α_{dc})	4-4
4.2.2	Common Emitter (CE) Configuration	4-4
4.2.2(A)	Current Gain β of CE Configuration	4-5
4.2.2(B)	Relation between α_{dc} and β_{dc}	4-5
4.2.3	Input Characteristics of CE configuration.....	4-7

4.2.4	Circuit used for CE configuration and DC load line	4-8
4.3	Various Regions of Operations on Output Characteristics.....	4-10
4.4	BJT Acts as Switch.....	4-11
4.5	Problems.....	4-12

Unit - V

Chapter 5 : Field Effect Transistor		5-1 to 5-15
5.1	Introduction.....	5-1
5.2	Basic Operating Principle of JFET.....	5-2
5.2.1	Structure of JFET.....	5-3
5.2.2	Physics of JFET Operation	5-3
5.2.3	Operation Modes	5-5
5.3	Application of JFET	5-7
5.4	MOSFET or IGFET	5-8
5.4.1	Depletion-type MOSFET (D-MOSFET)	5-8
5.4.2	Enhancement-Type MOSFET	5-11

Unit - VI

Chapter 6 : Nanotechnology		6-1 to 6-11
6.1	Introduction to Nanotechnology	6-1
6.2	Properties of Nanotechnology.....	6-2
6.2.1	Optical Properties	6-2
6.2.2	Electrical Properties	6-2
6.2.3	Magnetic Properties	6-2
6.2.4	Structural Properties	6-3
6.2.5	Mechanical Properties.....	6-3
6.3	Importance of Surface to Volume Ratio	6-3
6.4	Bonding in Solids (Vander waals Interaction).....	6-4
6.5	Applications of Nanotechnology.....	6-7
6.5.1	Optical Properties	6-7
6.5.2	Single Electron Transfer.....	6-9
6.5.3	Spin Valves	6-10



CO PO Mapping

Dear Learner...

As you are aware that the syllabus revised for FE semester- I and II is under National Education Policy (NEP) that is emphasizing a lot on Out Come based Education (OBE). Outcome based education is targeted at achieving desirable outcomes (in terms of knowledge, skills, attitudes and behaviour) at the end of a program. Teaching with this awareness and making the associated effort constitutes outcome based education. This entails a regular methodology for ascertaining the attainment of outcomes, and benchmarking these against the program outcomes consistent with the objectives of the program.

For the present syllabus Objectives and Course outcome are given below:

Course Objectives

1. To provide students with a basic understanding of Semiconductors in the field of Basic Engineering.
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6. Learner will be able to APPLY the knowledge of Nano Technology to certain emerging areas of technology

Suggestive CO PO mapping based on Performance Indicators (PIs) on AICTE website .

(this description is suggestive , A faculty member may use his/her own justification)

Here for every Course outcome, the corresponding Performance Indicator (PI) checked for alignment or correlation. If more than 80% correlation is observed than level of that CO PO is "High" (denoted by : 3) , If 50% to 80% PIs are mapping than suggestively the correlation level is "Moderate" (denoted by :2) and below 50% we consider as "Low" (denoted by :1)

		CO1	CO2	CO3	CO4	CO5	CO6
Competency	Performance Indicators (PI)						
1.1 Demonstrate competence in mathematical modeling	1.1.1 Apply mathematical techniques such as calculus, linear algebra, and statistics to solve problems 1.1.2 Apply advanced mathematical techniques to model and solve engineering problems	✓	✓		✓		
1.2 Demonstrate competence in basic sciences	1.2.1 Apply laws of natural science to an engineering problem	✓	✓	✓	✓	✓	✓
1.3 Demonstrate competence in engineering fundamentals	1.3.1 Apply fundamental engineering concepts to solve engineering problems	✓	✓		✓		
1.4 Demonstrate competence in specialized engineering knowledge to the program	1.4.1 Apply engineering concepts to solve related problems.	✓	✓		✓		
CO PO MAPPING		3	3	1	3	1	1

		CO1	CO2	CO3	CO4	CO5	CO6
Competency	Performance Indicators						
2.1 Demonstrate an ability to identify and formulate complex engineering problem	2.1.1 Articulate problem statements and identify objectives 2.1.2 Identify engineering systems, variables, and parameters to solve the problems 2.1.3 Identify the mathematical, engineering and other relevant knowledge that applies to a given problem	✓	✓	✓			
2.2 Demonstrate an ability to formulate a solution plan and methodology for an engineering problem	2.2.1 Reframe complex problems into interconnected sub-problems 2.2.2 Identify, assemble and evaluate information and resources. 2.2.3 Identify existing processes/solution methods for solving the problem, including forming justified approximations and assumptions 2.2.4 Compare and contrast alternative solution processes to select the best process.	✓	✓	✓			
2.3 Demonstrate an ability to formulate and interpret a model	2.3.1 Combine scientific principles and engineering concepts to formulate model/s (mathematical or otherwise) of a system or process that is appropriate in terms of applicability and required accuracy. 2.3.2 Identify assumptions (mathematical and physical) necessary to allow modeling of a system at the level of accuracy required.	✓		✓			

CO PO Mapping

Semiconductor Physics

C-4

CO PO Mapping

h	CO1	CO2	CO3	CO4	CO5	CO6					
g											
s,											
ts	✓	✓		✓							
s,											
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al,											
nt											
en											
to	✓	✓		✓							
ite											
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nd	✓		✓								
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CO PO MAPPING											
							2	3	2		
PO: 3 Design and development of solutions : Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.											
							CO1	CO2	CO3	CO4	CO3
											CO6
Competency		Performance Indicators									
3.1 Demonstrate an ability to define a complex/ open-ended problem in engineering terms		3.1.1 Able to define a precise problem statement with objectives and scope. 3.1.2 Able to identify and document system requirements from stakeholders. 3.1.3 Able to review state-of-the-art literature to synthesize system requirements. 3.1.4 Able to choose appropriate quality attributes as defined by ISO/IEC/IEEE standard. 3.1.5 Explore and synthesize system requirements from larger social and professional concerns. 3.1.6 Able to develop software requirement specifications									

3.2 Demonstrate an ability to generate a diverse set of alternative design solutions	<p>3.2.1 Able to explore design alternatives.</p> <p>3.2.2 Able to produce a variety of potential design solutions suited to meet functional requirements.</p> <p>3.2.3 Identify suitable non-functional requirements for evaluation of alternate design solutions</p>								
3.3 Demonstrate an ability to select optimal design scheme for further development	<p>3.3.1 Able to perform systematic evaluation of the degree to which several design concepts meet the criteria.</p> <p>3.3.2 Consult with domain experts and stakeholders to select candidate engineering design solution for further development</p>								
3.4 Demonstrate an ability to advance an engineering design to defined end state	<p>3.4.1 Able to refine architecture design into a detailed design within the existing constraints.</p> <p>3.4.2 Able to implement and integrate the modules.</p> <p>3.4.3 Able to verify the functionalities and validate the design</p>								
CO PO MAPPING									

PO: 4 Conduct investigations of complex problems : Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions for complex problems

Competency	Performance Indicators							
4.1 Demonstrate an ability to conduct investigations of technical issues consistent with their level of knowledge and understanding	4.1.1 Define a problem for purposes of investigation, its scope and importance 4.1.2 Able to choose appropriate procedure/algorithm, dataset and test cases. 4.1.3 Able to choose appropriate hardware/software tools to conduct the experiment.							
4.2 Demonstrate an ability to design experiments to solve open-ended problems	4.2.1 Design and develop appropriate procedures/methodologies based on the study objectives							
4.3 Demonstrate an ability to analyze data and reach a valid conclusion	4.3.1 Use appropriate procedures, tools and techniques to collect and analyze data 4.3.2 Critically analyze data for trends and correlations, stating possible errors and limitations 4.3.3 Represent data (in tabular and/or graphical forms) so as to facilitate analysis and explanation of the data, and drawing of conclusions 4.3.4 Synthesize information and knowledge about the problem from the raw data to reach appropriate conclusions							
CO PO MAPPING		0						
PO : 5 Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations								

		CO PO Mapping				
Competency	Performance Indicators					
5.1 Demonstrate an ability to identify/create modern engineering techniques and resources	5.1.1 Identify modern engineering tools such as computer-aided drafting, modeling and analysis; techniques and resources for engineering activities 5.1.2 Create/adapt/modify/extend tools and techniques to solve engineering problems			✓	✓	✓
5.2 Demonstrate an ability to select and apply discipline specific tools, techniques and resources	5.2.1 Identify the strengths and limitations of tools for (i) acquiring information, (ii) modeling and simulating, (iii) monitoring system performance, and (iv) creating engineering designs. 5.2.2 Demonstrate proficiency in using discipline-specific tools					✓
5.3 Demonstrate an ability to evaluate the suitability and limitations of tools used to solve an engineering problem	5.3.1 Discuss limitations and validate tools, techniques and resources 5.3.2 Verify the credibility of results from tool use with reference to the accuracy and limitations, and the assumptions inherent in their use.					
CO PO MAPPING				1	1	1
PO: 6 The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice						

Competency	Performance Indicators
6.1 Demonstrate an ability to describe engineering roles in a broader context, e.g. pertaining to the environment, health, safety, legal and public welfare	6.1.1 Identify and describe engineering roles; pertains to protection of public interest at the local level
6.2 Demonstrate an understanding of professional engineering regulations, legislation and standards	6.2.1 Interpret legislation, codes, and standards related to the discipline and explain the protection of public interest
CO PO MAPPING	
PO: 7 Environment and Sustainability: Understand the professional engineering solutions in environmental contexts, and demonstrate the need for sustainable development	
Competency	Performance Indicators
7.1 Demonstrate an understanding of the impact of engineering and industrial practices on social, environmental and economic contexts	7.1.1 Identify risks and opportunities in the cycle of an engineering activity 7.1.2 Understand the relationship between the technology and environment, and its impact on sustainability

Competency	Performance Indicators						
6.1 Demonstrate an ability to describe engineering roles in a broader context, e.g. pertaining to the environment, health, safety, legal and public welfare	6.1.1 Identify and describe various engineering roles; particularly as pertains to protection of the public and public interest at the global, regional and local level						✓
6.2 Demonstrate an understanding of professional engineering regulations, legislation and standards	6.2. 1 Interpret legislation, regulations, codes, and standards relevant to your discipline and explain its contribution to the protection of the public						
CO PO MAPPING		0					1

PO: 7 Environment and Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development

Competency	Performance Indicators						
7.1 Demonstrate an understanding of the impact of engineering and industrial practices on social, environmental and in economic contexts	7.1.1 Identify risks/impacts in the life-cycle of an engineering product or activity 7.1.2 Understand the relationship between the technical, socio-economic and environmental dimensions of sustainability	✓	✓	✓	✓	✓	✓

		CO PO Mapping				
		7.2.1	7.2.2	√	√	
7.2 Demonstrate an ability to apply principles of sustainable design and development	7.2.1 Describe management techniques for sustainable development 7.2.2 Apply principles of preventive engineering and sustainable development to an engineering activity or product relevant to the discipline					
CO PO MAPPING		1	1	2	2	1
PO: 8 Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice						
Competency	Performance Indicators					
8.1 Demonstrate an ability to recognize ethical dilemmas	8.1.1 Identify situations of unethical professional conduct and propose ethical alternatives					
8.2 Demonstrate an ability to apply the Code of Ethics	8.2.1 Identify tenets of the code of ethics 8.2.2 Examine and apply moral & ethical principles to known case studies					
CO PO MAPPING						
PO: 9 Individual and Team Work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.						
Competency	Performance Indicators					
9.1 Demonstrate an ability to form a team and define a role for each member	9.1.1 Recognize a variety of working and learning preferences; appreciate the value of diversity on a team 9.1.2 Implement the norms of practice (e.g. rules, roles, charters, agendas, etc.) of effective team work, to accomplish a goal.					

9.2 Demonstrate effective individual and team operations--communication, problemsolving, conflict resolution and leadership skills	9.2.1 Demonstrate communication, conflict resolution and leadership skills 9.2.2 Treat other respectfully 9.2.3 Listen to other 9.2.4 Maintain compa
9.3 Demonstrate success in a team-based project	9.3.1 Present results smooth integration from all individual effi
CO PO MAPPING	
PO: 10 Communication: Communicate effective engineering activities with the engineering community at large, such as, being able to communicate effective reports and design documentation presentations, and give and receive clear instructions	
Competency	Performance
10.1 Demonstrate an ability to comprehend technical literature and document project work	10.1.1 Read, understand and interpret technical information 10.1.2 Produce clear and well-supported engineering documents 10.1.3 Create flowcharts, presentation - a ideas so that the n

9.2 Demonstrate effective individual and team operations-- communication, problemsolving, conflict resolution and leadership skills	9.2.1 Demonstrate effective communication, problem-solving, conflict resolution and leadership skills						
	9.2.2 Treat other team members respectfully						
	9.2.3 Listen to other members						
	9.2.4 Maintain composure in difficult situations						
9.3 Demonstrate success in a team-based project	9.3.1 Present results as a team, with smooth integration of contributions from all individual efforts						

CO PO MAPPING

0

PO: 10 Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	C01	C02	C03	C04	C05	C06
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Competency	Performance Indicators						
10.1 Demonstrate an ability to comprehend technical literature and document project work	10.1.1 Read, understand and interpret technical and non-technical information 10.1.2 Produce clear, well-constructed, and well-supported written engineering documents 10.1.3 Create flow in a document or presentation - a logical progression of ideas so that the main point is clear						

10.2 Demonstrate competence in listening, speaking, and presentation	10.2.1 Listen to and comprehend information, instructions, and viewpoints of others					
	10.2.2 Deliver effective oral presentations to technical and non-technical audiences					
10.3 Demonstrate the ability to integrate different modes of communication	10.3.1 Create engineering-standard figures, reports and drawings to complement writing and presentations					
	10.3.2 Use a variety of media effectively to convey a message in a document or a presentation					
CO PO MAPPING		0				

PO: 11 Project Management and Finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

CO1 CO2 CO3 CO4 CO5 CO6

Competency	Performance Indicators					
11.1 Demonstrate an ability to evaluate the economic and financial performance of an engineering activity	11.1.1 Describe various economic and financial costs/benefits of an engineering activity 11.1.2 Analyze different forms of financial statements to evaluate the financial status of an engineering project					
11.2 Demonstrate an ability to compare and contrast the costs/benefits of alternate proposals for an engineering activity	11.2.1 Analyze and select the most appropriate proposal based on economic and financial considerations					

11.3 Demonstrate an ability to plan/manage an engineering activity within time and budget constraints	11.3.1 Identify the tasks required to complete an engineering task. 11.3.2 Use project management techniques to schedule an engineering task to be completed on time and within budget.
CO PO MAPPING	

PO: 12 Life-long Learning: Recognize the need for continuous preparation and ability to engage in independent learning in the broadest context of technological development.

Competency	Performance Indicators
12.1 Demonstrate an ability to identify gaps in knowledge and a strategy to close these gaps	12.1.1 Describe the requirements for professional development 12.1.2 Identify deficiencies in knowledge and demonstrate how to source information to address them
12.2 Demonstrate an ability to identify changing trends in engineering knowledge and practice	12.2.1 Identify technological advances that required professional development in order to keep up with new developments 12.2.2 Recognize the importance of clearly explaining important knowledge to keep up with new developments
12.3 Demonstrate an ability to identify and access sources for new information	12.3.1 Source technical literature and other sources of information 12.3.2 Analyze the popularity and viability of new information

CO PO MAPPING

11.3 Demonstrate an ability to plan/manage an engineering activity within time and budget constraints	11.3.1 Identify the tasks required to complete an engineering activity, and the resources required to complete the tasks.								✓
	11.6.2 Use project management tools to schedule an engineering project, so it is completed on time and on budget								
CO PO MAPPING		0							1

PO: 12 Life-long Learning: Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.	CO1	CO2	CO3	CO4	CO5	CO6
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Competency	Performance Indicators							
12.1 Demonstrate an ability to identify gaps in knowledge and a strategy to close these gaps	12.1.1 Describe the rationale for the requirement for continuing professional development 12.1.2 Identify deficiencies or gaps in knowledge and demonstrate an ability to source information to close this gap				✓	✓		
12.2 Demonstrate an ability to identify changing trends in engineering knowledge and practice	12.2.1 Identify historic points of technological advance in engineering that required practitioners to seek education in order to stay current 12.2.2 Recognize the need and be able to clearly explain why it is vitally important to keep current regarding new developments in your field		✓					✓
12.3 Demonstrate an ability to identify and access sources for new information	12.3.1 Source and comprehend technical literature and other credible sources of information 12.6.2 Analyze sourced technical and popular information for feasibility, viability, sustainability, etc	✓						
CO PO MAPPING		1	1					1

CO PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
2.1	3	2					1					
2.2	3	2										1
2.3	1						1					1
2.4	3	2			1		2					
2.5	1				1		2					
2.6	1				1	1	1					1

□□

1

Basics of Semiconductors

Syllabus

Types of semiconductors, Carrier Concentration in Intrinsic Semiconductors, Fermi level of Intrinsic Semiconductors, Variation of Fermi level of Intrinsic Semiconductors, w.r.t. temperature. Extrinsic Semiconductors, Fermi level of Extrinsic Semiconductors, Variation of Fermi level of Extrinsic Semiconductors, w.r.t. temperature and Impurity Concentration, Equation of conductivity with current flow, Hall Effect, Calculation of Hall Voltage.

1.1 Introduction to Semiconductors

The reader has already covered introductory part of this module in applied physics of semester - I, where in concept of holes, Fermi-Dirac Statistics, position of Fermi level in Intrinsic and Extrinsic semiconductors were covered.

1.1.1 Types of Semiconductors

Semiconductors are materials that have electrical conductivity between conductors and insulators. The conductivity of semiconductors can be controlled by the introduction of impurities or the application of external energy.

Intrinsic Semiconductors

- Intrinsic semiconductors are pure materials, typically silicon (Si) or germanium (Ge), without any added impurities.
- In their pure form, they have an equal number of charge carriers: electrons and holes. At absolute zero, the electrons fill the valence band, and there are no free electrons in the conduction band, making the material an insulator.

- When energy is supplied (such as heat or light), electrons gain enough energy to jump from the valence band to the conduction band, creating free electrons and holes (the absence of an electron in the valence band). These free carriers allow the semiconductor to conduct electricity.
- The conductivity of intrinsic semiconductors is relatively low and increases with temperature.

Extrinsic Semiconductors

- Extrinsic semiconductors are created by adding impurities, a process known as doping, to an intrinsic semiconductor. Doping introduces additional charge carriers, which greatly enhances the material's conductivity.
- N-type Semiconductor:** In N-type doping, elements with more valence electrons than the semiconductor material (like phosphorus in silicon) are added. These extra electrons become free carriers, increasing the negative charge (electron) concentration in the conduction band.
- P-type Semiconductor:** P-type doping introduces elements with fewer valence electrons (like boron in silicon). This creates "holes" (positive charge carriers) in the valence band, enhancing conductivity by allowing the movement of these holes in the material.
- Extrinsic semiconductors have significantly higher conductivity compared to intrinsic semiconductors, and their electrical properties can be tailored by adjusting the type and amount of dopant added.

1.1.2 Carrier Concentration in Intrinsic Semiconductor

- As discussed in Section 1.1.1 for intrinsic semiconductor, the concentration of holes and that of electrons is the same

$$\therefore n_i = p_i$$

- For an intrinsic semiconductor, the equilibrium electron and hole concentrations are represented by

$$n_i = N_C e^{-(E_C - E_F)/kT}$$

$$p_i = N_V e^{-(E_F - E_V)/kT}$$

Where

E_F = Position of the Fermi level for an intrinsic semiconductor that lies between at the middle of the bandgap

$$\therefore n_i p_i = N_C N_V e^{-E_g/kT}$$

gain enough energy to jump from electrons and holes (the absence of an

low the semiconductor to conduct

atively low and increases with

, a process known as doping, to an charge carriers, which greatly

more valence electrons than the ded. These extra electrons become entration in the conduction band. with fewer valence electrons (like e carriers) in the valence band, holes in the material.

ductivity compared to intrinsic ilored by adjusting the type and

tor

ne concentration of holes and that

on and hole concentrations are

miconductor that lies between

Where E_g = bandgap

The equilibrium concentrations n_0 and p_0 are given by

$$\begin{aligned} n_0 p_0 &= [N_C e^{-(E_C - E_F)/kT}] [N_V e^{-(E_F - E_V)/kT}] \\ &= N_C N_V e^{-E_g/kT} \end{aligned}$$

Where n_0 = Conduction band electron concentration

p_0 = Valance band hole concentration

∴ For intrinsic semiconductors

$n_i = p_i$ implies that

$$n_0 p_0 = n_i^2$$

1.1.3 Fermi Level in Intrinsic Semiconductors

- It can be shown for intrinsic semiconductors, Fermi energy level E_F lies midway between conduction and valence band. The proof is given below.
- At any temperature $T > 0^\circ K$,

$$n_e = \text{Number of electrons in conduction band}$$

$$n_v = \text{Number of holes in valence band}$$

$$\text{We have } n_e = N_C e^{-(E_C - E_F)/kT} \quad \dots(1.1.1)$$

Where N_C = Effective density of states in conduction band

$$\text{And } n_v = N_V e^{-(E_F - E_V)/kT} \quad \dots(1.1.2)$$

Where N_V = effective density of states in valance band

$$\text{For best approximation } N_C = N_V \quad \dots(1.1.3)$$

For intrinsic semiconductor

$$n_C = n_v$$

$$\therefore N_C e^{-(E_C - E_F)/kT} = N_V e^{-(E_F - E_V)/kT}$$

$$\therefore \frac{e^{-(E_C - E_F)/kT}}{e^{-(E_F - E_V)/kT}} = \frac{N_V}{N_C}$$

$$\therefore e^{-(E_C - E_F - E_F + E_V)/kT} = \frac{N_V}{N_C}$$

$$\therefore e^{-(E_C + E_V - 2E_F)/kT} = \frac{N_V}{N_C}$$

$$\text{as } N_V = N_C = 1$$

$$e^{-(E_C + E_V - 2E_F)/KT} = 1$$

\therefore Taking ln on both sides

$$\frac{-(E_C + E_V - 2E_F)}{KT} = 0$$

$$\therefore (E_C + E_V) = 2E_F$$

$$\therefore E_F = \frac{E_C + E_V}{2} \quad \dots(1.1.4)$$

Thus, the Fermi level in an intrinsic semiconductor lies at the center of forbidden energy gap.

1.1.4 Variation of Fermi level in intrinsic Semiconductor (With Respect to Temperature)

- | | |
|--|--------------------------|
| Q. What is Fermi level in semiconductor? | May 12, Dec. 13, 5 Marks |
| Q. What is Fermi level? Write Fermi-Dirac distribution function. | May 14, 3 Marks |
| Q. Draw and explain Fermi level diagram of p-n junction diode. | May 23 |

- When the filling up of electrons is undertaken, the universal rule is that the lowest energy level gets filled first.
- However, there will be many more allowed energy levels left vacant as shown in Fig. 1.1.1.

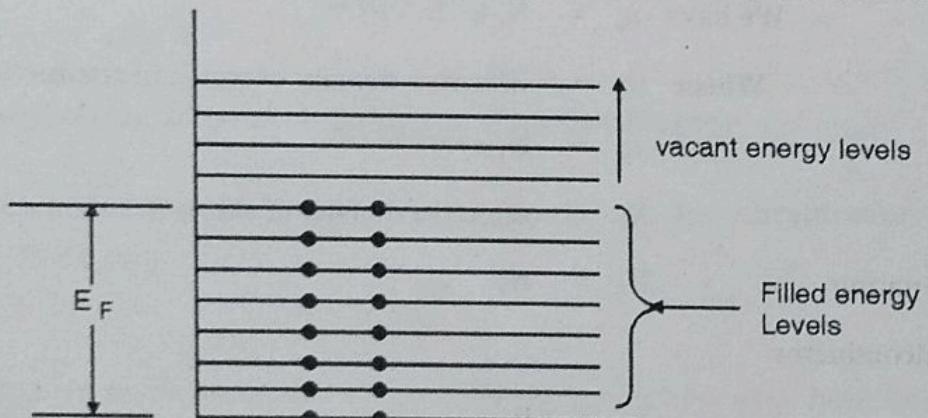


Fig. 1.1.1 : Fermi energy

Here we define Fermi energy or Fermi level as -

- The energy of the highest occupied level at zero degree absolute is called the Fermi energy, and the level is referred to as the Fermi level E_F .
- All the energy levels above the Fermi level at $T = 0^\circ K$ are empty and those lying below are completely filled. E_F may or may not be an allowed state. It provides a reference with which other energy levels can be compared.

1.1.4(A) Fermi Level in Conductor

Q. What is Fermi level in semiconductor?

Dec. 13, Dec. 15, 5 Marks

Q. Define Fermi level and explain it in detail for conductors.

May 23

As mentioned in classification the conductors have many free electrons. Let us see how Fermi function helps us understand their distribution.

(a) At $T = 0^\circ K$

- At $0^\circ K$ electrons occupy the lower energy levels in the conduction band leaving upper energy levels vacant.
- The band is filled up to a certain energy level E_F , therefore Fermi level may be regarded as the uppermost filled energy level in conductor at $0^\circ K$.
- At $T = 0^\circ K$, levels below E_F have $E < E_F$

$$\therefore f(E) = \frac{1}{1 + e^{(E - E_F)/KT}}$$

$$= \frac{1}{1 + e^{-\infty}} = 1$$

$f(E) = 1$ means all the levels below E_F
are occupied by electrons.

At $T = 0^\circ K$, levels above E_F have $E > E_F$

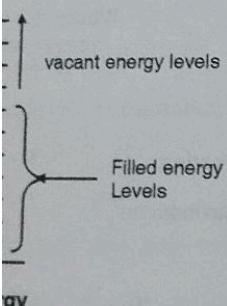
$$\therefore f(E) = \frac{1}{1 + e^{(E - E_F)/KT}}$$

$$= \frac{1}{1 + e^{\infty}} = 0$$

$$= \frac{1}{1 + \infty} = 0$$

 $\therefore f(E) = 0$ means all the levels above E_F are vacant.At $T = 0^\circ K$, for $E = E_F$

$$f(E) = \frac{1}{1 + e^{(E - E_F)/KT}} = \frac{1}{1 + e^0}$$

 $\therefore f(E)$ is indeterminable.

The absolute is called the Fermi energy,

are empty and those lying below are
filled. It provides a reference with which

This is summarized in Fig. 1.1.2.

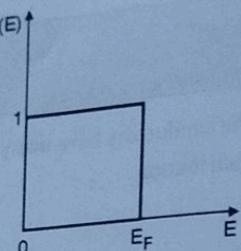


Fig. 1.1.2 : Fermi-Dirac distribution at $T = 0^\circ\text{K}$

(b) At $T > 0^\circ\text{K}$

- At temperature above 0°K , few electrons are excited to vacant levels above E_F . This happens to those electrons which are close to E_F hence probability to find an electron at $E > E_F$ will become greater than unity which was zero at $T = 0^\circ\text{K}$.
- Similarly, due to excitation of electrons, few levels just below E_F will become vacant and $f(E)$ will be slightly reduced which was unity at $T = 0^\circ\text{K}$.
- In a simple way one can understand that, what increase in $f(E)$ at $T > 0^\circ\text{K}$ above $E = E_F$ we get is equal to reduction in $f(E)$ below $E = E_F$. This is shown as below in Fig. 1.1.3.

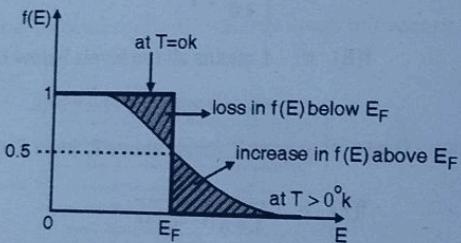


Fig. 1.1.3 : Electron occupancy at $T > 0^\circ\text{K}$

$$\text{At } E = E_F \text{ for } T > 0^\circ\text{K}$$

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}} = \frac{1}{1 + 1} = \frac{1}{2} = 0.5$$

1.1.4(B) Fermi Level in Semiconductor

- Once the concept of Fermi level is understood properly by considering conductors, it is proper to go to semiconductors.
- A semiconductor has conduction band and valence band separated by a small energy gap.

- At normal temperature, a significant number of electrons from Valence band (VB) leaving behind same number of holes.
- Therefore $f(E)$ has non-zero probability above Fermi level and below E_F as shown in Fig. 1.1.4.

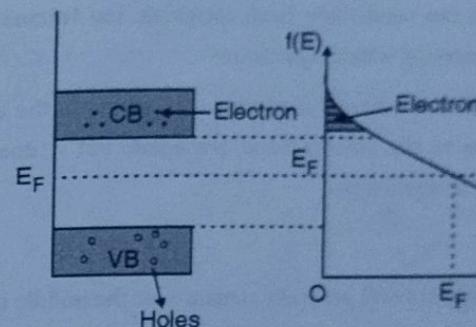


Fig. 1.1.4 : Fermi-Dirac distribution of semiconductors

Fermi level is halfway between CB and VB if it is intrinsic.

- In an **intrinsic semiconductor**, the Fermi level is halfway between the conduction band and the valence band. It is the probability of an electron occupying a given energy state which is essentially the energy level that separates filled states from unfilled states.
- As temperature increases in an intrinsic semiconductor, the Fermi level shifts towards the valence band.

1. At absolute zero (0°K)

- The Fermi level lies at the midpoint of the energy gap between the valence band and the conduction band.
- All the electrons fill up the valence band, and there are no electrons in the conduction band.
- At this temperature, there is no electrical conductivity because no electrons have enough energy to jump into the conduction band.

2. As temperature increases

- With the rise in temperature, some electrons in the valence band gain enough energy to jump into the conduction band, leaving behind holes.
- These free electrons in the conduction band and the holes in the valence band give rise to electrical conductivity.

- At normal temperature, a significant number of electrons are excited to conduction band (CB) and from Valence band (VB) leaving behind same number of holes.
- Therefore $f(E)$ has non-zero probability above Fermi level and $f(E)$ reduces by same amount below E_F as shown in Fig. 1.1.4.

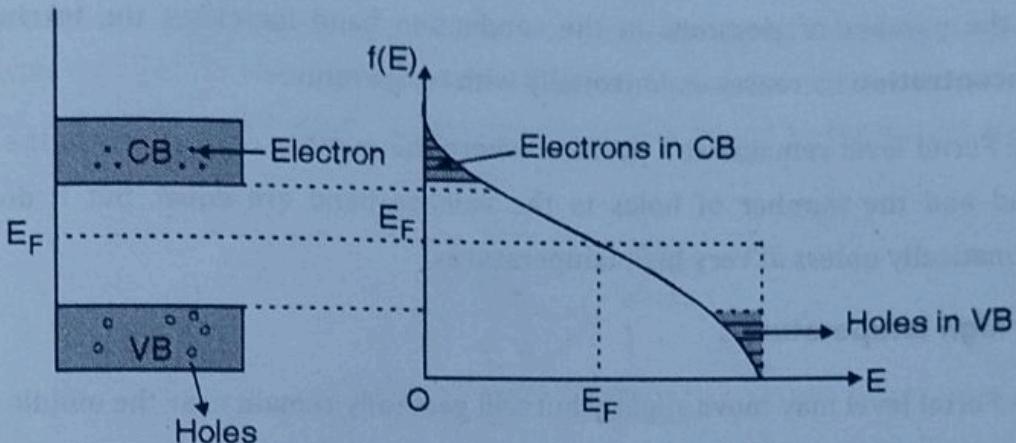


Fig. 1.1.4 : Fermi-Dirac distribution of semi conductor at $T > 0^\circ \text{ K}$

Fermi level is halfway between CB and VB if it is intrinsic.

- In an **intrinsic semiconductor**, the Fermi level is the energy level that represents the probability of an electron occupying a given energy state at absolute zero temperature. It is essentially the energy level that separates filled states from empty states in a material.
- As temperature increases in an intrinsic semiconductor, the Fermi level behaves as follows:

1. At absolute zero (0° K)

- The Fermi level lies at the midpoint of the energy gap (band gap) between the **valence band** and the **conduction band**.
- All the electrons fill up the valence band, and there are no electrons in the conduction band.
- At this temperature, there is no electrical conductivity since no electrons have enough energy to jump into the conduction band.

2. As temperature increases

- With the rise in temperature, some electrons in the valence band gain enough thermal energy to jump into the conduction band, leaving behind **holes** in the valence band.
- These free electrons in the conduction band and the holes in the valence band contribute to electrical conductivity.

3. Variation of Fermi level with temperature

- At higher temperatures (but still within the intrinsic region), the Fermi level slightly shifts towards the **mid-gap** position but remains relatively close to it.
- As the number of electrons in the conduction band increases, the **intrinsic carrier concentration** increases exponentially with temperature.
- The Fermi level remains at a position where the number of electrons in the conduction band and the number of holes in the valence band are equal, but it doesn't move dramatically unless at very high temperatures.

5. At very high temperatures:

- The Fermi level may move slightly but will generally remain near the middle of the band gap in intrinsic semiconductors. However, in some high-temperature cases, the intrinsic carrier concentration becomes so high that the semiconductor starts behaving more like a conductor.

1.2 Extrinsic Semiconductor

- Intrinsic semiconductors have low conductivity** and serve only in limited applications. It is necessary to modify and control conductivity of intrinsic semiconductors to employ them in manufacturing useful devices.
- The conductivity of intrinsic semiconductor can be increased by adding impurities. A deliberate introduction of controlled quantities of impurities into pure semiconductor is called **doping**.
- The impurity added is called **dopant**. The doped semiconductor is called **extrinsic semiconductor**.
- The impurities to be used as dopants are selected from group III or group V elements because of the following reasons.
- These atoms are nearly of the same size as Si or Ge and substitute themselves easily into the host lattice by going into the place of some of the host atoms.
- The impurity is of substitutional type and the original crystal structure does not get distorted.
- Extrinsic semiconductors are of two types depending upon the impurity element introduced.

1.2.1(A) n-Type Semiconductors

- If a pentavalent impurity is added to a semiconductor. The impurity added is called **donor atom**.
- As shown in Fig. 1.2.1 antimony (Sb) added atom forms covalent bonds with the surrounding four valence electrons and the fifth valence electron remains which becomes available as current carrier.

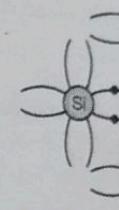


Fig. 1.2.1 : n-type semiconductor

- The energy required to remove the fifth electron from a donor atom is small in comparison to 1.12 eV, which is the energy required to break a covalent bond.
- So at modest temperatures the fifth electron is easily liberated. This liberated electron is called **free electron** and enters the conduction band.
- Unlike the intrinsic semiconductors, by adding impurities. Therefore at ordinary temperatures, there are holes in the valence band (holes are produced).
- It means here electrons in conduction band are:
 - (i) By the donor atom.
 - (ii) By intrinsic process
- Therefore, the majority current carriers in n-type semiconductors are holes.
- The addition of an impurity adds an allow electrons in the conduction band as shown in Fig. 1.2.2.

1.2.1(A) n-Type Semiconductors

- If a pentavalent impurity is added to a pure semiconductor it becomes n-type extrinsic semiconductor. The impurity added is called donor impurity.
- As shown in Fig. 1.2.1 antimony (Sb) added as an impurity has five valence electrons. Each Sb atom forms covalent bonds with the surrounding four Si atoms with the help of four of its five electrons and the fifth valence electron remains loosely bound to the parent impurity atom which becomes available as current carrier.

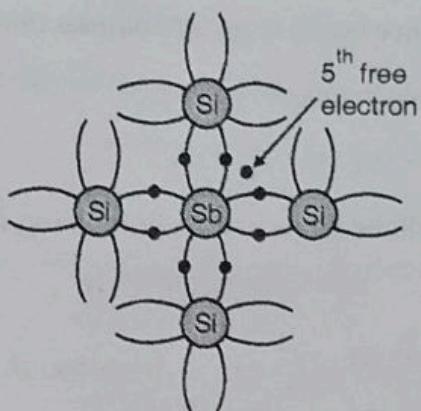


Fig. 1.2.1 : n-type semiconductor

- The energy required to remove the fifth electron is very small (0.05 eV). This energy is very small in comparison to 1.12 eV, which is the energy gap for Si, and it also represents the energy to break a covalent bond.
- So at modest temperatures the fifth electron can be detached from the impurity atom. The liberated electron is called **free electron** and it can take part in conduction by entering into conduction band.
- Unlike the intrinsic semiconductors, by leaving fifth electron there is no hole created. Therefore at ordinary temperatures, there will be more electrons in the conduction band than holes in the valence band (holes are produced by intrinsic process).
- It means here electrons in conduction band come from two different ways.

- By the donor atom.
- By intrinsic process

- Therefore, the majority current carriers in n-type semiconductors are electrons and minority current carriers are holes.
- The addition of an impurity adds an allowed energy level E_D at a very small distance below the conduction band as shown in Fig. 1.2.2.

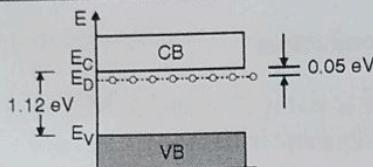


Fig. 1.2.2 : Donor level in n-type semiconductor

- This additional level lies in forbidden energy gap. An electron located at the donor level will have to acquire an energy equal to ($E_C - E_D$) only, as against the energy ($E_C - E_V = E_g$) required by an electron located in valence band, to go into conduction band at moderate temperatures. As the conductivity is due to electrons, it is given by

$$\sigma_e = n \cdot e \cdot \mu_e \quad \dots(1.2.1)$$

The electron concentration will be governed by Boltzmann factor as

$$n \propto e^{-(E_C - E_D)/KT} \quad \dots(1.2.2)$$

and conductivity can be written as

$$\sigma_e = \sigma_0 e^{-(E_C - E_D)/KT} \quad \dots(1.2.3)$$

Position of Fermi level

In n-type semiconductors, as there are many free electrons in conduction band, the Fermi level gets shifted towards the conduction band. At 0°K it is between the bottom of conduction band and the level E_D.

1.2.2(B) p-Type Semiconductors

- If a trivalent impurity (Group III) is added to a pure semi-conductor, it becomes p-type extrinsic semiconductor. The impurity added is called as **acceptor impurity**.
- As shown in Fig. 1.2.3 boron (B) has been added as impurity which has three electrons. Each B atom tries to form covalent bonds with surrounding four Si atoms and falls short of one electron for completing four covalent bonds.

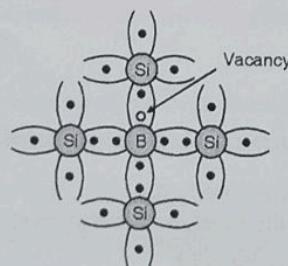


Fig. 1.2.3 : p-type semiconductor

- As a result a vacancy is left in the bonding. This vacancy environment in the crystal lattice is electrically neutral.
- The introduction of impurity atom does not disturb the envir due to the non-formation of bond is not a hole.
- However, when an electron from a neighbouring bond acqu vacany, it leaves behind a positively charged environment i hole is generated there.
- The addition of an impurity adds an allowed level E_A at a very the valence band as shown in Fig. 1.2.4

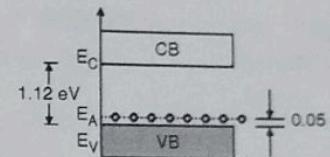


Fig. 1.2.4 : Acceptor level in p-type semic

- At T = 0°K all acceptor levels at E_A are vacant as shown in Fig. 1.2.4, but the conduction band is empty.
- When the temperature increases, electrons from the valence band move to the acceptor level and leave holes behind. At moderate temperature all acceptor levels are filled and correspondingly for each acceptor atom one hole is created in the valence band.
- The generation of holes is not followed by the simultaneous annihilation of electrons. Therefore p-type semiconductor has holes as majority carriers, which results because of intrinsic process.
- The conductivity of a p-type semiconductor at ordinary temperature is given by

$$\sigma_p = p \cdot e \cdot \mu_h$$

The hole concentration is governed by Boltzmann law as

$$\sigma_p = e^{(E_V - E_A)/KT}$$

The conductivity of a p-type semiconductor is given by

$$= \sigma_0 e^{(E_V - E_A)/KT}$$

Position of Fermi level

In n-type semiconductor, as there are many free holes in valence band, the Fermi level is shifted towards the valence band. At 0°K it is between top of valence band and the level E_A.

- As a result a vacancy is left in the bonding. This vacancy is not a hole. Originally, the environment in the crystal lattice is electrically neutral.
- The introduction of impurity atom does not disturb the environment, and the vacancy arising due to the non-formation of bond is not a hole.
- However, when an electron from a neighbouring bond acquires energy and jumps into this vacancy, it leaves behind a positively charged environment in the broken bond. Therefore, a hole is generated there.
- The addition of an impurity adds an allowed level E_A at a very small distance above the top of the valence band as shown in Fig. 1.2.4

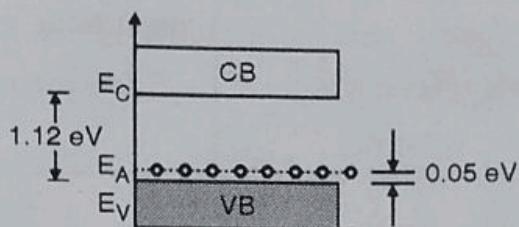


Fig. 1.2.4 : Acceptor level in p-type semiconductor

- At $T = 0^\circ\text{K}$ all acceptor levels at E_A are vacant as shown in Fig. 6.7.4 and valence band is full but the conduction band is empty.
- When the temperature increases, electrons from the valence band jump into acceptor level and leave holes behind. At moderate temperature all acceptor levels are filled and correspondingly for each acceptor atom one hole is created in the valence band.
- The generation of holes is not followed by the simultaneous generation of electrons. Therefore p-type semiconductor has holes as majority carriers and electrons as minority carriers, which results because of intrinsic process.
- The conductivity of a p-type semiconductor at ordinary temperature is given by

$$\sigma_p = p \cdot e \cdot \mu_h \quad \dots(1.2.4)$$

The hole concentration is governed by Boltzmann law as

$$\sigma_p = e^{(E_V - E_A) / KT} \quad \dots(1.2.5)$$

The conductivity of a p-type semiconductor is given by

$$= \sigma_0 e^{(E_V - E_A) / KT} \quad \dots(1.2.6)$$

Position of Fermi level

In n-type semiconductor, as there are many free holes in valence band, the Fermi level gets shifted towards the valence band. At 0°K it is between top of valence band and the level E_A .

Table 1.2.1 : Difference between conduction for conductors and semiconductors

Sr. No.	Conduction	Semi-conduction
1.	Resistance depends upon temperature, impurity, type of material and ageing factor.	Semi-conduction depends upon temperature (for intrinsic) and on impurity atoms (for extrinsic type).
2.	(a) single crystal (b) poly crystalline (c) alloys or (d) amorphous material can be used for conductor.	Only single crystal is used for semi-conduction.
3.	Resistance increases with temperature.	Resistance decreases with temperature.
4.	Charge carriers are only electrons.	Charge carriers are both electrons and holes.
5.	Resistivity and hence conductivity cannot be altered to a desired value.	Conductivity (for extrinsic) can be altered by addition of impurity atoms.
6.	Active components cannot be made out of conductor.	Active components like diodes and transistors can be made of semiconductors.
7.	Conductivity is due to loosely bound electrons (metallic bonds).	Conductivity is due to covalently bonded electrons.

Table 1.2.2 : Comparison between intrinsic and extrinsic semiconductors

Sr. No.	Intrinsic semiconductors	Extrinsic semiconductors
1.	This is a pure element crystal.	This is a single crystal with impurity.
2.	The charge carriers are electrons of the parent atom of crystal and holes formed in absence of that electron.	The charge carriers are electrons or holes of the impurity atoms fitted into the crystal of parent atoms.

Sr. No.	Intrinsic semiconductors	Extrinsic semiconductors
3.	The charge carriers, electrons and holes are equal in numbers i.e. $n_e = n_p$	In n-type majority charge carriers are electrons and in p-type majority carriers are holes.
4.	The charge carriers, say electrons, can be increased only by increase in temperature.	The majority charge carriers can be increased by slightly increasing the percentage of impurity atoms.
5.	More energy is needed for the electrons to cross E_g (compared to extrinsic).	Less energy is needed for the electrons (impurity atoms) to cross E_g (compared to intrinsic).

1.3 Variation of Fermilevel Extrinsic Semiconductors with respect to Temperature and Impurity Concentration

1.3.1 Effect of Temperature on n-type Material

- Q. With the help of diagram, explain the variation of Fermi level with temperature in n-type semiconductor. May 17, 5 Marks
- Q. With energy band diagram explain the variation of Fermi energy level with temperature in extrinsic semiconductor. Dec. 17, May 18, 5 Marks
- Q. Draw the energy band diagram of p-n junction diode in forward and reverse bias condition. Dec. 17, May 18, 3 Marks
- Q. Discuss the effect of variation in temperature on the fermi energy level of n-type Semiconductor with the help of labelled diagram. May 22

(i) **At low temperature :** When the temperature in the semiconductor is low, only few donor atoms get ionized and electrons move from the donor level to the conduction band.

Hence, Fermi level for n-type semiconductor at low temperature lies midway between the bottom of the conduction band and donor level.

(ii) **At moderate temperature :** At moderate temperature all donor atoms are ionized. So, the concentration of electrons in conduction band is equal to the concentration of donor atoms.

When the temperature increases upto moderate value, Fermi level slowly shifts away from the conduction band and moves towards the center of the forbidden gap.

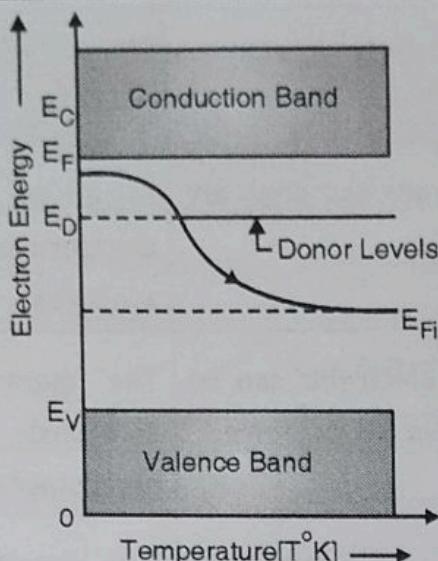


Fig. 1.3.1 : Variation of E_F with temperature in n-type material

- (iii) **At higher temperature :** At high temperature, the concentration of transfer of electrons from valence band to conduction band is more compared to concentration of electrons from donor atoms and Fermi level is shifted to middle of the forbidden gap.

The variation of Fermi level with temperature for n-type of material is shown in Fig. 1.3.1.

1.3.2 Effect of Temperature on p – type Material

Q. Draw the energy band diagram of p-n junction diode in forward and reverse bias condition.

Dec. 17, 3 Marks

Q. With energy band diagram explain the variation of Fermi energy level with temperature in extrinsic semiconductor.

Dec. 17, 5 Marks

Q. Draw the energy band diagram of p-n junction diode in forward and reverse bias condition.

May 18, 3 Marks

- (i) **At low temperature :** At low temperature only few acceptor levels are occupied, and simultaneously holes are produced in valence band.

So, Fermi level lies in the middle of the top of the valence band and the acceptor level.

- (ii) **At moderate temperature :** At moderate temperature, all acceptor levels are filled.

So, at moderate temperature, Fermi level gradually moves up i.e. moves towards the middle of the forbidden gap.

- (iii) **At higher temperature :** At very high temperature, the contribution of conduction band for the formation of holes in the valence band is more compared to acceptor impurity.

Hence, at very higher temperature, Fermilevel approaches the middle of the energy gap i.e. the position of E_F for intrinsic semiconductor. The variation of E_F with temperature in p-type material is shown in Fig. 1.3.2.

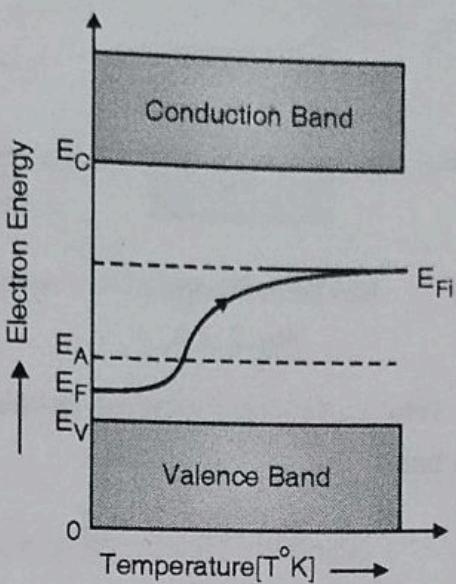


Fig. 1.3.2 : Variation of E_F with temperature in p-type material

1.3.3 Effect of Impurity on Fermi Level

Q. Draw a neat labelled energy band diagram to show the variation of Fermi level with doping concentration in n-type semiconductors. Dec. 15, 3 Marks

Q. How does the position of Fermi energy level change with increasing doping concentration in p-type semiconductors? Sketch the diagram. Dec. 16, 5 Marks

- We have seen the effect of temperature on Fermi level. The position of Fermi level is also affected by addition of impurity and by variation in the concentration of impurity.
- If a donor impurity is added to an intrinsic semiconductor, it results in n-type of semiconductor and a donor level comes into existence below the bottom of conduction band.
- At impurity concentrations, the impurity atoms are so spaced that they do not interact with each other. Once the concentrations are increased, interaction among them starts.
- The donor levels starts splitting and forms an energy band below the conduction band. The width of this band increases with increase in the impurity concentration. At one stage it overlaps with the conduction band.
- Due to broadening of the donor levels into band the width of forbidden energy gap reduces and the Fermi level is found moved upwards.
- With increase in concentration of donor impurity, the Fermi level continues shifting towards conduction band and enters into conduction band.

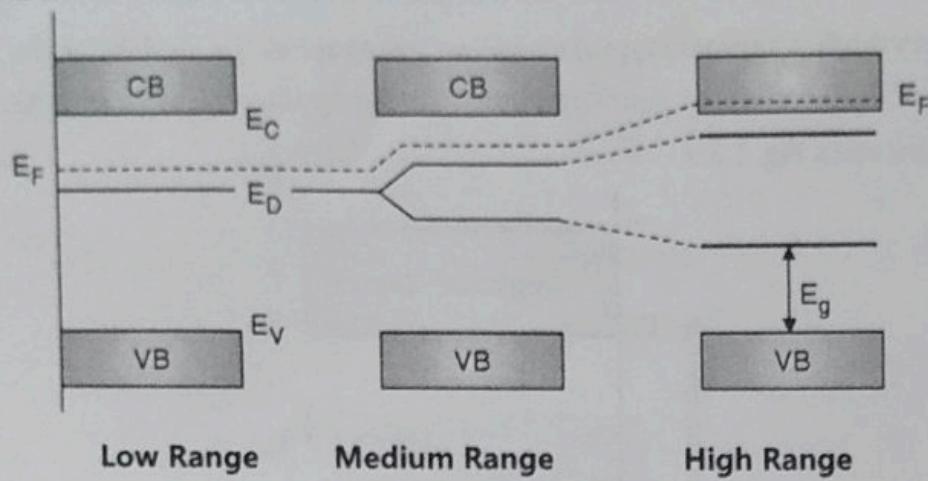


Fig. 1.3.3

- In the same way, for p-type semi conductors increase in the impurity concentration makes Fermi level shift into valence band.

$$\sigma = q(\eta \mu_n + p \cdot \mu_p)$$

$$\sigma = q \cdot \eta \cdot \mu_n$$

$$\sigma = q \cdot p \cdot \mu_p$$

$$\sigma_{\text{intrinsic}} = q \cdot \eta_i (\mu_p + \mu_n)$$

1.4 Equation of Continuity

In an **extrinsic semiconductor**, the conductivity (σ) depends on the concentration of charge carriers, the charge of the carriers, and the mobility of the carriers. The general equation for electrical conductivity in an extrinsic semiconductor can be written as:

$$\sigma = q(n \cdot \mu_n + p \cdot \mu_p)$$

Where :

- Σ is the electrical conductivity of the semiconductor.
- q is the charge of the carriers (for electrons, $q = -1.6 \times 10^{-19}$ C n is the concentration of electrons in the conduction band (for an N-type semiconductor).
- p is the concentration of holes in the valence band (for a P-type semiconductor).
- μ_n is the mobility of electrons.
- μ_p is the mobility of holes.

In N-type semiconductors :

- The majority carriers are electrons, and the conductivity mainly depends on the electron concentration n

- The hole concentration p is relatively low and can be treated as negligible compared to n
- Thus, for N-type semiconductors :

$$\sigma = q \cdot n \cdot \mu_n$$

In P-type semiconductors :

- The majority carriers are holes, and the conductivity mainly depends on the hole concentration p

- The electron concentration n is relatively low and can be treated as negligible compared to n

Thus, for P-type semiconductors :

$$\sigma = q \cdot p \mu_p$$

For Intrinsic Semiconductors (special case of extrinsic) :

In intrinsic semiconductors, the concentration of electrons n is equal to the concentration of holes p , and the conductivity is given by :

$$\text{Where } \sigma_{\text{intrinsic}} = q \cdot n_i (\mu_p + \mu_n)$$

Temperature Dependence :

- In extrinsic semiconductors, the carrier concentration n or p is temperature-dependent and increases exponentially with temperature.
- For N-type semiconductors, the carrier concentration of electrons n increases with temperature as the donor levels become ionized.
- For P-type semiconductors, the carrier concentration of holes p increases with temperature as the acceptor levels become ionized.
- Thus, the conductivity of an extrinsic semiconductor increases with temperature due to an increase in the number of charge carriers.

1.5 Hall Effect and Calculation of Hall Voltage

- If a metal or semiconductor, carrying a current I is placed in a transverse magnetic field B , an electric field E is induced in the direction perpendicular to both I and B . This phenomenon is known as **Hall effect** and the electric field or voltage induced is called **Hall voltage (V_H)**. The physical process of Hall effect is as follows. Consider a specimen along positive x -direction (Fig. 1.5.1).

- The current flowing through the specimen is in the positive x-direction and the magnetic field is in the positive z-direction. The force exerted on charge carriers, that is, on electrons is downward. The electrons move downward and thus voltage V_H (Hall voltage) is developed along upper surface as positive and lower as negative

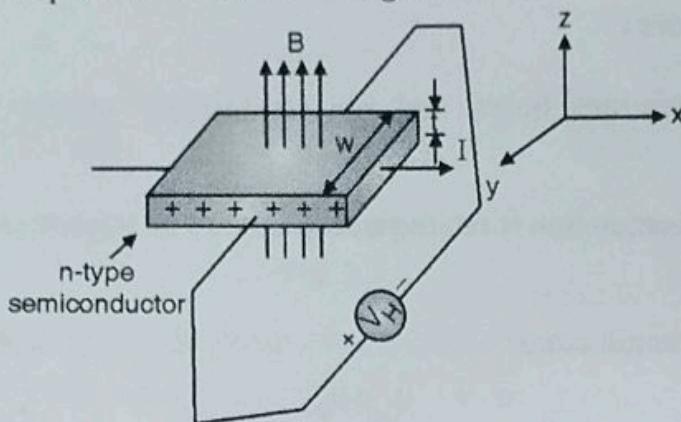


Fig. 1.5.1: Hall effect

1.5.1 Experimental Determination of Mobility

- If the specimen in Fig. 1.5.1 is assumed to be of n-type, then magnetic force experienced by electrons will be towards -Y direction as it is applied transversely.
 \therefore Magnetic force $F = e v B$
- Holes present in specimen will experience the same force but in positive Y direction. Hence, electrons and holes will be separated.

This develops potential difference between both the surfaces, denoted by V_H , called Hall voltage.

$$\therefore E_H = \frac{V_H}{w} \quad \dots(1.5.1)$$

- The current in this case is given by

$$= n A e v \quad \dots(1.5.2)$$

(Where, v = drift velocity)

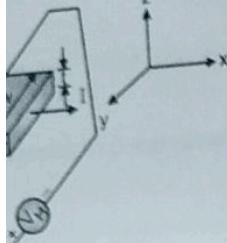
- In equilibrium condition, the force due to magnetic field B and the force due to electric field E_H acting on the charge are balanced.

$$\therefore e E_H = evB \quad \dots(1.5.3)$$

or

$$E_H = vB$$

In the positive x-direction and the magnetic field acted on charge carriers, that is, on electrons is developed and thus voltage V_H (Hall voltage) is developed negative.



Hall effect

Mobility

If the carrier is of n-type, then magnetic force experienced by the carrier is directed towards the positive Y direction. If the carrier is of p-type, then magnetic force experienced by the carrier is directed towards the negative Y direction. Hence, the same force but in positive Y direction. Hence,

the Hall voltage is developed on both the surfaces, denoted by V_H , called Hall voltage.

$$\dots(1.5.1)$$

For p-type semiconductor, the Hall voltage is given as

$$\dots(1.5.2)$$

For n-type semiconductor, the Hall voltage is given as

$$\dots(1.5.3)$$

Using equation (1.5.3) and (1.5.1)

$$V_H = Bvw$$

Using equations (1.5.1) and (1.5.2),

$$v = \frac{I}{enA} = \frac{J}{en}$$

$$\text{where } J = \frac{I}{A}$$

Hence, Hall voltage can be written as

$$V_H = \frac{IBw}{enA} = \frac{Bw}{en} \cdot J$$

It can be also modified by using, $A = w \times t$

$$V_H = \frac{IB}{en t} \quad \dots(1.5.4)$$

By measuring V_H , I , B , and t , the charge density ($n_h e$ or $n_e e$) can be calculated.

Another important parameter is Hall coefficient R_H it is defined as,

$$R_H = \frac{1}{pe} \quad (\text{for p-type semiconductor})$$

$$= \frac{1}{ne} \quad (\text{for n-type semiconductor})$$

From equation (1.5.4),

$$R_H = \frac{V_H t}{BI} \quad \dots(1.5.5)$$

$$\text{As } \sigma = \mu ne, \mu = \sigma R_H$$

\therefore If the conductivity and Hall coefficient are measured then the mobility and density of charge carriers can be determined.

- With increase in temperature of the semiconductor, the carrier concentration is increased and R_H decreases.
- The net electric field E acting on the charge carrier is constant of the applied electric field E_x and Hall electric field E_H . The angle made by E with x-axis is called Hall angle, given by

$$\theta_H = \tan^{-1} \left(\frac{E_H}{E_x} \right)$$

Which can also be proved as,

$$\theta_H = \tan^{-1} (R_H \sigma B)$$

1.5.2 Applications

1. The Hall voltage V_H is proportional to magnetic field B , for the given current I , therefore Hall effect is used in magnetic field meter.
2. The charge carrier concentration can be determined.
3. The mobility of charge carriers can be determined.
4. The nature of semiconductor (p-type or n-type) can be determined.

1.6 Solved Problems

Ex. 1.6.1 : The single carrier holes in a shaped silicon sample is $2.05 \times 10^{22} \text{ m}^{-3}$. Calculate its Hall coefficient. Electronic charge = $1.602 \times 10^{-19} \text{ C}$.

Soln. :

$$\begin{aligned} R_H &= \frac{1}{ne} = \frac{1}{\text{charge carrier density} \times \text{electronic charge}} \\ &= \frac{1}{(2.05 \times 10^{22}) \times (1.602 \times 10^{-19})} \\ &= 3.045 \times 10^{-4} \text{ m}^3/\text{C} \end{aligned}$$

Ex. 1.6.2 : Assuming there are 5×10^{28} atoms/m³ in copper, find the Hall coefficient.

Soln. :

$$\begin{aligned} R_H &= \frac{1}{ne} \\ \therefore R_H &= \frac{1}{(5 \times 10^{28}) \times (1.6 \times 10^{-19})} \\ &= -0.1255 \times 10^{-9} \text{ m}^3/\text{C} \end{aligned}$$

Ex. 1.6.3 : Using free electron model, find the Hall coefficient of sodium assuming BCC structure of Na of cell side 4.28 Å.

Soln. :

Unit cell of sodium atom (Na) of volume a^3 has 2 atoms. Therefore,

$$\begin{aligned} n &= 2 \times \left(\frac{1}{a^3} \right) = 2 \times \left[\frac{1}{(4.28 \times 10^{-10})^3} \right] \\ &= 2.55 \times 10^{28} \text{ m}^{-3} \end{aligned}$$

Now, Hall coefficient,

$$R_H = -\frac{1}{ne}$$

$$\therefore R_H = \frac{1}{(2.55 \times 10^{28}) \times (1.6 \times 10^{-19})}$$

$$= -0.245 \times 10^{-9} \text{ m}^3/\text{C}$$

Ex. 1.6.4 : The resistivity of a sample semiconductor is 9 milli-ohm-metre. IT holes have mobility of 0.03 m²/V-s. Calculate hall coefficient.

Soln. :

We know that

Conductivity,

$$\sigma = \frac{1}{\text{resistivity}} = \frac{1}{9 \times 10^{-3}}$$

Now, Hall coefficient,

$$R_H = \frac{\mu}{\sigma} = \frac{0.03}{111.11}$$

$$= 2.7 \times 10^{-4} \text{ m}^3/\text{C}$$

Ex. 1.6.5 : The resistivity of doped silicon material is $9 \times 10^{-3} \Omega\text{-m}$. The Hall coefficient is $3.6 \times 10^{-4} \text{ m}^3/\text{C}$. Assuming single carrier concentration, find mobility and the density of charge carrier.

Soln. :

Here,

$$\sigma = \frac{1}{9 \times 10^{-3}} = 111.11/\Omega\text{-m}$$

$$\rho = \frac{1}{R_H} = \frac{1}{3.6 \times 10^{-4}} = 2778 \text{ C/m}^3$$

$$\therefore n = \frac{\rho}{e} = \frac{2778}{1.6 \times 10^{-19}}$$

$$= 1.73625 \times 10^{22}/\text{m}^3$$

The mobility is given by,

$$\mu = \sigma R_H = 111.11 \times (3.6 \times 10^{-4})$$

$$= 0.04 \text{ m}^2/\text{V}\text{-s}$$

Ex. 1.6.6 : The resistivity of Cu is 1.72×10^{-8} ohm-m. Calculate the mobility of electrons in Cu given that number of electrons per unit volume is $10.41 \times 10^{28} \text{ m}^{-3}$.

Soln. :

Given :

$$\rho = 1.72 \times 10^{-8} \Omega\text{-m},$$

$$\sigma = \frac{1}{\rho} = 58.1 \times 10^6 \text{ mho/m}$$

$$n = 10.41 \times 10^{28} \text{ m}^{-3}$$

Formula :

$$\mu = \frac{\sigma}{ne} = \frac{58.1 \times 10^6}{10.42 \times 10^{28} \times 1.6 \times 10^{-19}}$$

$$\therefore \mu = 3.488 \times 10^{-3} \frac{\text{m}^2}{\text{volt sec.}}$$

...Ans.

Ex. 1.6.7 : Find the resistivity for Cu assuming that each atom contributes one free electron for conduction.

Soln. :

Given : Density = 8.96 g/cm^3 , Atomic weight = 63.5

Avogadro's number = $6.02 \times 10^{23} / \text{g-mole}$

Mobility of electron = $43.3 \text{ cm}^2 / \text{V-sec.}$

Formula :

$$\sigma = n\mu e$$

$$\text{And } \rho = \frac{1}{\sigma}$$

$$\therefore \rho = \frac{1}{n\mu e}$$

\therefore Calculation of n

$$\text{Atomic density} = \frac{6.023 \times 10^{23} \times 8.96}{63.5}$$

$$= 8.4985 \times 10^{22} / \text{cm}^3$$

$$\therefore n = 1 \times \text{Atomic density}$$

$$= 1 \times 8.5 \times 10^{22} / \text{cm}^3$$

$$\therefore \rho = \frac{1}{8.5 \times 10^{22} \times 1.6 \times 10^{-19} \times 43.3}$$

$$\therefore \rho = 1.698 \times 10^{-6} \text{ ohm-cm}$$

...Ans.

Ex. 1.6.8 : Find the resistivity of intrinsic Ge at 300°K given the density of carriers as $2.5 \times 10^{19} \text{ m}^{-3}$.

Soln. :

Formula :

$$\sigma_{in} = n_e \cdot e \cdot \mu_e + n_h \cdot e \cdot \mu_h$$

For intrinsic semiconductor

$$n_e = n_h = n_i$$

$$\therefore \sigma = n_i \cdot e (\mu_e + \mu_h)$$

Using standard values of μ_e and μ_h

$$\therefore \sigma_{in} = 2.5 \times 10^{19} \times 1.6 \times 10^{-19} [0.39 + 0.19] = 2.32 \text{ (ohm.m)}^{-1}$$

$$\therefore \rho_i = \frac{1}{\sigma} = 0.43 \text{ ohm.m} \quad \dots \text{Ans.}$$

Ex. 1.6.9 : In an intrinsic semiconductor the energy gap E_g of an intrinsic semiconductor is 1.2 eV. Its hole mobility is much smaller than electron mobility and is independent of temperature. What is the ratio between conductivity at 600°K and that at 300°K? Comment on the result.

Soln. :

Since $\mu_e \gg \mu_h$, for intrinsic semiconductor equation (3.6.3) can be rewritten as,

$$\sigma_i = n_i \cdot e \cdot \mu_e \text{ (as } n_i = n_e = n_h\text{)}$$

$$\therefore n_e = N \exp [-E_g / 2KT]$$

$$\therefore \sigma_i = e \cdot \mu_e \cdot N \exp [-E_g / 2KT]$$

All the pre-exponential terms are independent of temperature. We can put a constant

$$\sigma_o = \mu_e \cdot e \cdot N$$

$$\therefore \sigma_i = \sigma_o \exp \left[\frac{-E_g}{2KT} \right]$$

$$\text{Now, } \sigma(600^\circ\text{K}) = \sigma_o \exp \left[\frac{-1.2}{2 \times K \times 600} \right]$$

$$\sigma(300^\circ\text{K}) = \sigma_o \exp \left[\frac{-1.2}{2 \times K \times 300} \right]$$

Taking K, the Boltzmann constant in eV as $K = 8.62 \times 10^{-5} \text{ eV/K}$ and solving we get

$$\frac{\sigma(600^\circ\text{K})}{\sigma(300^\circ\text{K})} = 1 \times 10^5 \quad \dots \text{Ans.}$$

Comment: The conductivity of an intrinsic semiconductor is greatly influenced by temperature.

Ex. 1.6.10 : Predict the effect on the electrical properties of a silicon at room temperature if every millionth silicon atom is replaced by an atom of indium. Comment on results.

Given :

$$\text{Concentration of Si atoms} = 5 \times 10^{28} \text{ m}^{-3}$$

$$\text{Intrinsic conductivity of Si} = 4.4 \times 10^{-4} \text{ mho.m}^{-1}$$

$$\text{Mobility of holes } \mu_h = 0.048$$

Soln. :

As indium belongs to group III, holes will remain as majority carrier. Concentration of Si atoms = $5 \times 10^{28} \text{ m}^{-3}$

Concentration of impurity atoms

$$n = 5 \times 10^{28} \times 1 \times 10^{-6} = 5 \times 10^{22} \text{ m}^{-3}$$

$$\therefore \sigma_p = \mu_h \cdot e \cdot n = 0.048 \times 1.6 \times 10^{-19} \times 5 \times 10^{22}$$

$$\therefore \sigma_p = 384 \text{ mho.m}^{-1}$$

...Ans.

Comment : Intrinsic conductivity for Si at room temperature is $4.4 \times 10^{-4} \text{ mho.m}^{-1}$ and when trivalent impurity of indium at one part per million is added, the conductivity becomes 384 mho.m^{-1} which is increased by almost six orders of magnitude.

Ex. 1.6.11 : An impurity of 0.01 ppm (particles per milion) is added into Si. The semiconductor has a resistivity of 0.25 ohm.m^{-1} at 300°K . Calculate the hole concentration and its mobility. Also comment on result.

Given : Atomic weight of Si = 28.1 and density of Si = $2.4 \times 10^3 \text{ kg/m}^3$.

Soln. :

$$\begin{aligned} \therefore \text{Number of Si atoms / m}^3 &= \frac{\text{Avogadro number} \times \text{Density}}{\text{Atomic weight}} \\ &= \frac{6.024 \times 10^{26} \times 2.4 \times 10^3}{28.1} \\ &= 5.14 \times 10^{28} \text{ atoms / m}^3 \end{aligned}$$

Impurity level is 0.01 ppm i.e. 1 atom at every 10^8 atoms of Si

$$\therefore \text{Number of impurity atoms} = \frac{5.14 \times 10^{28}}{10^8} = 5.14 \times 10^{20}$$

Each impurity introduces one hole

$$\text{i.e. holes/m}^3 = 5.14 \times 10^{20} = n_h$$

$$\therefore \mu_p = \frac{1}{e.p.n_h}$$

$$= \frac{1}{1.6 \times 10^{-19} \times 0.25 \times 5.14 \times 10^{20}}$$

$$\therefore \mu_p = 0.0486 \text{ m}^2/\text{volt.sec}$$
...Ans.

Comment: On addition of trivalent impurity the mobility of Si remains the same but the concentration of holes increases.

Ex. 1.6.12 : The resistivity of intrinsic InSb at room temperature is $2 \times 10^{-4} \Omega \text{ cm}$. If the mobility of electron is $6 \text{ m}^2/\text{V-sec}$ and mobility of hole is $0.2 \text{ m}^2/\text{V-sec}$. Calculate its intrinsic carrier density.

Soln. :

Given

$$\rho_i = 2 \times 10^{-4} \Omega \text{ cm} = 2 \times 10^{-6} \Omega \text{ m}$$

$$\mu_n = 0.2 \text{ m}^2/\text{V-sec},$$

$$\mu_e = 6 \text{ m}^2/\text{V-sec.}$$

$$\sigma_{in} = n_e e \mu_e + n_h e \mu_n$$

Formula:

For intrinsic semiconductor

$$n_e = n_h = n_i$$

$$\therefore \sigma_{in} = n_i e (\mu_e + \mu_n)$$

$$\rho_{in} = \frac{1}{\sigma_{in}} = \frac{1}{n_i e (\mu_e + \mu_n)}$$

$$\therefore n_i = \frac{1}{\rho_{in} e (\mu_e + \mu_n)}$$

$$= \frac{1}{2 \times 10^{-6} \times 1.6 \times 10^{-19} (6 + 0.2)}$$

$$\therefore n_i = 5.04 \times 10^{23}$$

...Ans.

Ex. 1.6.13 : Calculate electron and hole concentration in intrinsic silicon at room temperature if its electrical conductivity is $4 \times 10^{-4} \text{ mho/m}$. Given that mobility of electron = $0.14 \text{ m}^2/\text{V-sec}$ and mobility of holes = $0.04 \text{ m}^2/\text{V-sec}$.

May 14, May 17, Dec. 18, 3/5 Marks

Soln. :

For intrinsic semiconductor $n_e = n_h = n_i$.

and

$$\sigma_{in} = n_i e (\mu_n + \mu_e)$$

$$n_i = \frac{\sigma_{in}}{e(\mu_n + \mu_e)} = \frac{4 \times 10^{-4}}{1.6 \times 10^{-19} (0.14 + 0.4)}$$

$$n_i = 1.388 \times 10^{16}$$

...Ans.

Ex. 1.6.14 : Determine the concentration of conduction electron in a sample of silicon if one in every million silicon atoms is replaced by a phosphorous atom. Assume every phosphorous atom to be singly ionized. Si has a molar mass of 0.028 kg/mole and density of 2300 kg/m³

Dec. 14, 5 Marks

Soln. :

Given :

$$\text{Molar mass} = 0.028 \text{ kg/mole}$$

$$\text{Density} = 2300 \text{ kg/m}^3$$

As the molar mass is given, number of silicon per m³ is given by

$$\begin{aligned} &= \frac{\text{Density}}{\text{Molar mass}} \times \text{Avogadro number} \\ &= \frac{2300}{0.028} \times 6.023 \times 10^{26} = 4.947 \times 10^{31} \end{aligned}$$

As every millionth atom is replaced by phosphorous hence number of phosphorous atoms per m³ is 4.947×10^{25}

Also, phosphorous is singly ionized, each atom contributes i.e.

$$\therefore \text{Concentration of electron} = 4.947 \times 10^{25} / \text{m}^3$$

... Ans.

Ex. 1.6.15 : Calculate conductivity of a germanium sample if donor impurity atoms are added to the extent of one part in 10^6 germanium atoms at room temperature.

Assume that only one electron of each atom takes part in conduction process.

Given : Avogadro's number ; 6.023×10^{23} atoms / g-mole

Atomic weight of Ge = 72.6

Mobility of electrons = $3800 \text{ cm}^2 / \text{volt-sec}$. Density of Ge = 5.32 g/cm^3

Dec. 16, 3 Marks

Soln. :

$$\text{Atomic weight} = 72.6$$

$$\text{Density} = 5.32 \text{ g/cm}^3$$

$$\frac{5.32}{72.6} \times 6.023 \times 10^{23} = \frac{\text{Number of atoms}}{\text{cm}^3} = 4.413 \times 10^{22}$$

Since Ge is doped with a donor impurity, it will become n-type. For impurity added one part in Ge

$$\frac{\text{Number of donor atoms}}{\text{cm}^3} = 4.413 \times 10^{16}$$

Every atom provides one electron.

$$\therefore \text{Concentration of electron} = 4.413 \times 10^{16} = n$$

$$\begin{aligned}\text{Conductivity } \sigma &= n e \mu_e \\ &= 4.413 \times 10^{16} \times 1.6 \times 10^{-19} \times 3800 \\ &= 26.831 \text{ mho.cm}^{-1}\end{aligned}$$

...Ans.

Ex. 1.6.16 :

Calculate the current produced in a Ge sample of cross section 1 cm^2 and thickness of 0.01 m when potential difference of $2V$ is applied across it. The concentration of free electrons in Ge is $2 \times 10^{19}/\text{m}^3$ and mobilities of electron and holes are $0.36 \text{ m}^2/\text{V}\cdot\text{sec}$ and $0.17 \text{ m}^2/\text{volt}\cdot\text{sec}$, respectively.

Dec. 16, 3 Marks

Soln.:

Ge is an intrinsic semiconductor.

$$\begin{aligned}\therefore \text{Conductivity } \sigma &= ne(\mu_n + \mu_e) \\ &= 2 \times 10^{19} \times 1.6 \times 10^{-19} \\ &\quad (0.36 + 0.17) \\ &= 1.696 \text{ mho m}^{-1}\end{aligned}$$

∴ Resistivity

$$\rho = \frac{1}{\sigma} = \frac{1}{1.696} = 0.5896 \text{ ohm-m}$$

Now

$$R = \frac{\rho l}{A} = \frac{0.5896 \times 0.01}{1 \times 10^{-4}} = 58.96 \text{ ohm.}$$

$$\therefore I = \frac{V}{R} = \frac{2}{58.96} = 0.034 \text{ Amp.}$$

Ex. 1.6.17 : Calculate the intrinsic carrier concentration in GaAs at $T = 300^\circ\text{K}$ and 400°K . Assume N_C and N_V at 300°K to be 4.7×10^{17} and $7.0 \times 10^{18}/\text{cm}^3$ respectively. Assume that the gap energy of GaAs is 1.42 eV and it is independent of temperature for this temperature range.

Soln.:

The intrinsic carrier concentration η_i is given by,

$$\eta_i = \sqrt{N_C N_V} \cdot e^{-E_g/kT} \quad \dots(1)$$

Substituting values of N_C and N_V

$$\text{At } T = 300^\circ\text{K}$$

$$\eta_i = \sqrt{4.7 \times 10^{17} \times 7 \times 10^{18}} \cdot e^{-1.42/0.026 \times 2}$$

(here kT when converted to eV it becomes 0.026)

$$\therefore \eta_i = 2.5 \times 10^6 / \text{cm}^3 \quad \dots(2)$$

$$\therefore \text{At } T = 400^\circ\text{K}$$

$$kT = 0.026 \times \left(\frac{400}{300}\right) = 0.035 \text{ eV}$$

\therefore Using Equation 2 and 3 in Equation 1

$$\begin{aligned} \eta_i &= \sqrt{(4.7 \times 10^{17}) \times (7 \times 10^{18}) \times \left(\frac{400}{300}\right)^2} \times e^{-1.42/0.035 \times 2} \\ &= 3.746 \times 10^9 / \text{cm}^3 \end{aligned} \quad \dots\text{Ans.}$$

Ex. 1.6.18 : An n-type of Ge sample has a $N_D = 10^{21} / \text{m}^3$ and width 5 mm. It is arranged in a Hall effect experimental set up. If $B = 0.6 \text{ T}$, $J = 500 \text{ A/m}^2$, find Hall voltage.

Soln. :

$$\text{We know } V_H = \frac{BIw}{neA}$$

$$\text{Here } wd = A$$

$$\text{and taking } \frac{I}{A} = J$$

$$V_H = \frac{Bw}{ne} \cdot J \quad \text{take } n = N_D = \frac{BwJ}{N_D e}$$

$$\therefore V_H = \frac{0.6 \times 5 \times 10^{-3} \times 500}{10^{21} \times 1.6 \times 10^{-19}}$$

$$= 9.3 \text{ mV} \quad \dots\text{Ans.}$$

Ex. 1.6.19 : A copper strip 2cm wide and 1mm thick is placed in a magnetic field $B = 1.5 \text{ wb/m}^2$. If current of 200A is set up in the strip, calculate Hall voltage that appears across the strip. (Given $R_H = 6 \times 10^{-7} \text{ m}^3/\text{C}$)

May 10, 5 Marks

Soln. : Using equation (3.10.5)

$$R_H = \frac{V_H t}{BI}$$

$$V_H = R_H \frac{BI}{t} = 6 \times 10^{-7} \times \frac{200 \times 1.5}{1 \times 10^{-3}}$$

$$V_H = 0.18 \text{ Volt}$$

...Ans.

Ex. 1.6.20 :

The mobility of holes is $0.025 \text{ m}^2/\text{V}\cdot\text{sec}$. What would be the resistivity of p-type silicon if the Hall coefficient of the sample is $2.25 \times 10^{-5} \text{ m}^3/\text{C}$.

Dec. 10, Dec. 12, May 17, May 19, 3 Marks

Soln. :

Formula :

$$\text{We know, } \sigma = ne\mu \text{ or, } \mu = \frac{1}{ne} \cdot \sigma = R_H \sigma$$

$$\text{or, } \sigma = \frac{\mu}{R_H} \text{ or, Resistivity } \rho = \frac{R_H}{\mu}$$

Data given :

$$R_H = 2.25 \times 10^{-5} \text{ m}^3/\text{C},$$

$$\mu = 0.025 \text{ m}^2/\text{V}\cdot\text{s}$$

$$\text{So, } \rho = \frac{2.25 \times 10^{-5}}{0.025}$$

$$= 9 \times 10^{-4} \text{ ohm-m}$$

...Ans.

Ex. 1.6.21 :

A sample of a n-type silicon has a donor density of $10^{20}/\text{m}^3$. It is used in the Hall effect experiment. If the sample of width 4.5 mm is kept in a magnetic field of (0.55T) with current density of 500 A/m^2 . Find

- (i) Hall voltage developed in it
- (ii) Hall coefficient (iii) Hall angle if mobility of electron is $0.17 \text{ m}^2/\text{V sec}$.

Dec. 11, 5 Marks

Soln. :

Hall voltage developed

$$V_H = \frac{BJw}{ne} = R_H B J w$$

$$\text{Hall coefficient } R_H = \frac{1}{ne}$$

Data given :

$$n = 10^{20}/\text{m}^3, e = 1.6 \times 10^{-19} \text{ C}$$

So,

$$R_H = \frac{1}{10^{20} \times 1.6 \times 10^{-19}}$$

$$= 0.0625 \text{ m}^3/\text{C}$$

(i) Hall voltage

$$V_H = R_H B J w$$

Data given :

$$B = 0.55, J = 500 \text{ A/m}^2, w = 4.5 \times 10^{-3} \text{ m}$$

$$V_H = 0.0625 \times 0.55 \times 500 \times 4.5 \times 10^{-3}$$

$$= 77.3 \times 10^{-3} \text{ V}$$

$$= 77.3 \text{ mV}$$

...Ans

(ii) Hall coefficient

$$R_H = 0.0625 \text{ m}^3/\text{C}$$

...Ans

(iii) Hall angle

$$\theta_H = \tan^{-1}(\mu B)$$

$$= \tan^{-1}(0.17 \times 0.55)$$

$$= 5.3^\circ$$

...Ans

Ex. 1.6.22 : The Hall coefficient of a specimen is $3.66 \times 10^{-4} \text{ m}^3/\text{C}$. Its resistivity is $8.93 \times 10^{-3} \Omega \text{ m}$. Find μ and n .

Soln. :**Formula :**

$$\text{Hall coefficient } R_H = \frac{1}{n e}$$

$$n = \frac{1}{R_H \cdot e}$$

Data given :

$$R_H = 3.66 \times 10^{-4} \text{ m}^3/\text{C}$$

So,

$$n = \frac{1}{3.66 \times 10^{-4} \times 1.6 \times 10^{-19}}$$

$$= 1.7 \times 10^{22} / \text{m}^3$$

...Ans.

Also, we know

$$\sigma = n e \mu$$

$$\mu = \frac{\sigma}{n e} = \sigma \times R_H = 1/\rho \times R_H = \frac{R_H}{\rho}$$

$$= \frac{3.66 \times 10^{-4}}{8.93 \times 10^{-3}}$$

$$\mu = 0.040 \text{ m}^2/\text{v} \cdot \text{s}$$

...Ans.

Ex. 1.6.23 : A bar of n-type Ge of size $0.010 \text{ m} \times 0.001 \text{ m} \times 0.001 \text{ m}$ is mounted in a magnetic field of $2 \times 10^{-3} \text{ T}$. The electron density in the bar is $7 \times 10^{21}/\text{m}^3$. If one millivolt is applied across the long ends of the bar, determine the current through the bar and the voltage between Hall electrodes placed across the short dimensions of the bar. Assume $\mu_e = 0.39 \text{ m}^2/\text{vs}$.

May 13, 5 Marks

Soln. :

$$\text{As } \rho = \frac{1}{\mu_n e} = \frac{1}{0.39 \times 7 \times 10^{21} \times 1.6 \times 10^{-19}} \\ = 2.29 \times 10^{-3} \text{ ohm/m}$$

$$\text{Now } R = \frac{\rho l}{A} = \frac{2.29 \times 10^{-3} \times 0.01}{(0.001 \times 0.001)} = 22.9 \Omega$$

(Here long side is used as length as instructed and other two sides are forming width and height which in turn gives cross-sectional area)

Using Ohm's law

$$I = \frac{V}{R} = \frac{1 \times 10^{-3}}{22.9} = 43.66 \mu\text{A}$$

Using formula for Hall voltage

$$V_H = R_H B j w$$

$$\text{As, } R_H = \rho \times \mu$$

$$\text{And, } J = \frac{I}{A} = \frac{I}{w \times t}$$

$$V_H = \rho \times \mu \times B \times \frac{I}{w t} \times t = \frac{\rho \mu B I}{w} \\ = \frac{2.29 \times 10^{-3} \times 0.39 \times 0.2 \times 43.66 \times 10^{-6}}{0.001} \\ = 7.798 \mu\text{V}$$

...Ans.

Ex. 1.6.24 : In a semiconductor with Hall coefficient 145 cc/C having width 2 cm and thickness 0.2 cm with a magnetic field induction of 2T along the smaller dimension, a current of 150 mA is calculate the current density and Hall voltage.

Dec. 14, 5 Marks

Soln. :

Given : Hall coefficient $R_H = 145 \text{ cc/C}$, Width $w = 2 \text{ cm}$
 thickness $t = 0.2 \text{ cm}$, magnetic field $B = 2 \text{ T}$

Current density

$$J = \frac{I}{A} = \frac{I}{W \times d} \\ = \frac{150 \times 10^{-3}}{2 \times 10^{-2} \times 0.2 \times 10^{-2}} \\ = 3750 \text{ A/m}^2$$

Now

Hall co-efficient

$$R_H = \frac{V_H/d}{JB}$$

$$V_H = R_H JB$$

$$\text{Now, } w = 145 \times 10^{-6} \times 3750 \times 2 \times 0.2 \times 10^{-2}$$

$$= 21.75 \text{ mV}$$

...Ans.

Ex. 1.6.25 : In an n-type semiconductor the Fermi level lies 0.4 eV below the conduction band. If the concentration of donor atom is doubled, find the new position of the Fermi level w.r.t. the conduction band.

May 13, 5 Marks

Note : This problem needs assumption of temperature to arrive at the answer

Soln. : Given :

$$E_C - E_F = 0.4 \text{ eV}$$

Now concentration of donor atom is doubled, hence number of electrons will be doubled.

∴ At any temperature $T > 0^\circ \text{K}$

$$n_e = N e^{-(E_C - E_F) / KT} \quad \dots(1)$$

where n_e = Number of electrons in conduction band

When donor concentration is doubled, $n'_e = 2 n_e$, and Fermi level must have been shifted to a new location say E'_F ,

$$2 n_e = N e^{-(E_C - E'_F) / KT} \quad \dots(2)$$

Divide equation (2) by (1)

$$\frac{2 n_e}{n_e} = \frac{N e^{-(E_C - E'_F) / KT}}{N e^{-(E_C - E_F) / KT}}$$

$$\alpha = e^{[(E'_F - E_C) + (E_C - E_F)] / 4KT}$$

For Boltzmann constant $K = 1.38 \times 10^{-23} \text{ J/K}$ and with an assumption $T = 300^\circ \text{K}$

$$\begin{aligned} KT &= \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} \\ &= 0.026 \text{ eV} \end{aligned}$$

∴ Equation (3) becomes,

$$2 = e^{[(E'_F - E_C) + (E_F - E_C)] / 0.026}$$

Taking ln on both sides

$$\ln 2 = \frac{[(E'_F - E_C) + (E_F - E_C)]}{0.026}$$

$$0.026 \times \ln 2 = (E'_F - E_C) + (E_F - E_C)$$

$$\text{But } E_F - E_C = 0.4 \text{ eV given}$$

$$0.01802 = (E'_F - E_C) + 0.4$$

$$E_C - E'_F = 0.4 - 0.01802 = 0.38198$$

...Ans.

\therefore Fermi level will be shifted towards conduction band.

- Ex. 1.6.26 : In a Hall effect experiment a potential difference of $4.5 \mu\text{V}$ is developed across a foil of zinc of thickness 0.02 mm. When a current of 1.5 A is in a direction perpendicular to applied magnetic field of 2T , calculate
- Hall coefficient of zinc
 - Concentration of electrons

Dec. 16, 7 Marks

Soln. :

Using formula

$$1. R_H = \frac{V_H t}{BI} = \frac{4.5 \times 10^{-6} \times 0.02 \times 10^{-3}}{2 \times 10^5} = 3 \times 10^{-11}$$

$$2. \text{ As } R_H = \frac{1}{n_e}$$

$$\therefore n_e = \frac{1}{R_H \cdot e} = \frac{1}{3 \times 10^{-11} \times 1.6 \times 10^{-19}}$$

$$= 2.083 \times 10^{29} / \text{m}^3$$

... Ans.

Review Questions

- Differentiate between intrinsic and extrinsic semiconductors.
- How is Fermi level changing with respect to (a) variation in temperature (b) Variation in concentration.
- What is Hall effect ? Derive the expression of Hall voltage.
- Write few applications of hall effect.



2

Junction Diode

Syllabus

Formation of p-n junction, calculation of barrier potential Diode equation, p-n junction in forward Bias, p-n junction in Reverse bias, Current- voltage curve for p-n junction diode, LED and its working

2.1 Introduction

Most semiconductor devices contain at least one junction between p-type and n-type material. These p-n junctions are fundamental to the performance of functions such as :

- (a) Rectification
- (b) Amplification
- (c) Switching etc.

In this module, we shall discuss

- (a) Formation of pn junction
- (b) Potential Barrier
- (c) Diode equation
- (d) Biasing of pn junction
- (e) LED

2.2 p-n Junction

A pn junction is formed when a p-type doped semiconductor is made to join an n-type doped semiconductor. The variation in the impurity concentration occurs over a short distance (few microns) as a result a potential gradient is developed due to which there is a flow of carriers even through no voltage is applied. In case of majority carrier current, the majority holes diffuse out of

the p-region, leaving behind negatively charged acceptor atoms bound to lattice. A space charge is generated in a region that was neutral earlier. Similarly electrons diffusing from the n-region leave behind positively charged donor atoms bound to the lattice. Thus a double space charged layer is formed which is of opposite sign to the majority carriers diffusing into them. The space charged layer gradually starts to build up resistance for the flow of majority diffusing carriers across the boundary. The majority current gradually starts to decrease, as an electric field builds up due to the space charge and finally inhibits the flow of current.

The space charge layer is referred to as the depletion layer or the barrier layer

2.3

Depletion Layer and Potential Barrier

- In p-type of semiconductor, holes are majority carriers and its Fermi level is just above the top of acceptor level at room temperature (300°K). For n-type of semiconductor, electrons are majority carriers and its Fermi level is just below the donor level at 300°K .
- When p-n junction is being formed, both materials will find their Fermi levels non-aligned as shown in Fig. 2.3.1 and they must be aligned.

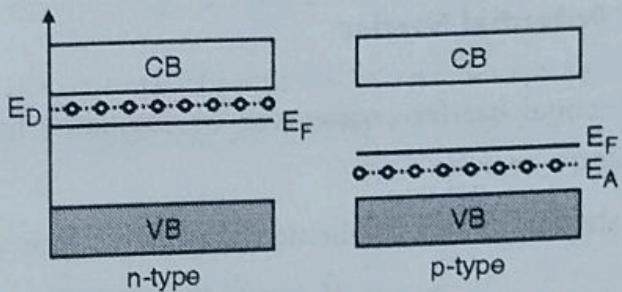


Fig. 2.3.1 : Position of Fermi-level in n-type and p-type semiconductor

- In order to obtain alignment, holes from p-type (majority carriers for a p-type) move n-type and at the same time electrons from n-type (majority carriers from n-type) towards p-type. This is called **diffusion**.
- As the diffusion takes place across the junction the holes and the electrons combine to neutralise each other at the junction and produce a free space called **depletion layer** as shown in Fig. 2.3.2.
- At the junction due to the migration of a few holes from p-type to n-type region, the negative immobile ions are produced in p-region and in the same way positive immobile ions are produced in n-region as shown in Fig. 2.3.2.
- As the name suggest these ions are immobile in nature (fixed in lattice). Under equilibrium condition it can be assumed similar to a charged parallel plate capacitor and creates an

electronic potential called potential barrier or junction potential which prevents further diffusion of majority charge carriers.

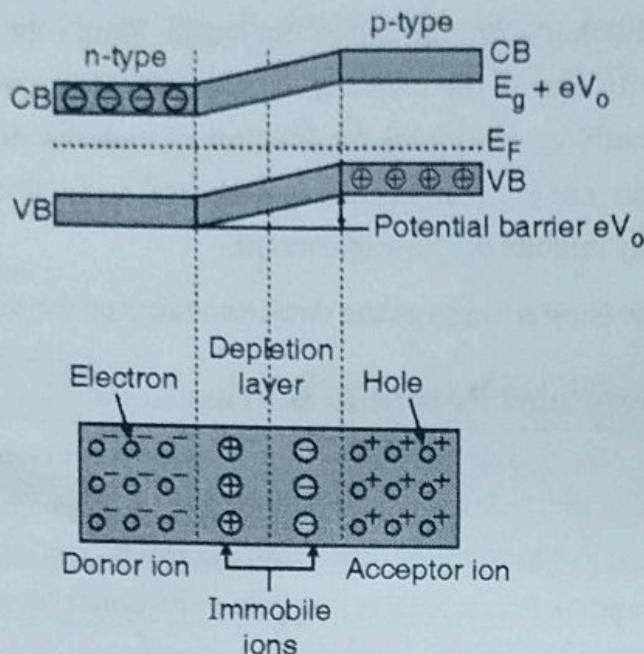


Fig. 2.3.2 : Unbiased p-n junction

2.3.1 Calculation of Potential Barrier

- The magnitude of potential barrier created can be estimated from the knowledge of the carrier densities in p and n-regions.
- The concentration of electrons in the conduction band on n-side is written as

$$n_n = N_c \exp [- (E_g - E_F) / KT] \quad \dots(2.3.1)$$

Similarly the concentration on p-side is written as

$$n_p = N_c \exp [- \{ (E_g + eV_0) - E_F \} / KT] \quad \dots(2.3.2)$$

Dividing Equations (2.3.1) by equation (2.3.2),

$$\frac{n_n}{n_p} = \exp [eV_0 / KT] \quad \dots(2.3.3)$$

Taking natural logarithm on both sides of Equation (2.3.3) we get

$$V_0 = \frac{KT}{e} \ln \left(\frac{n_n}{n_p} \right) \quad \dots(2.3.4)$$

By rewriting Equation (2.3.4) as

$$V_0 = \frac{KT}{e} \ln \left(\frac{n_n}{n_p} \cdot \frac{p_p}{p_n} \right) \quad \dots(2.3.5)$$

Where p_p is hole concentration on p-side.

At room temperature, all impurities are ionised therefore

$$n_n = N_D$$

= Donor impurity concentration

$$p_n = N_A$$

= Acceptor impurity concentration using relation,

$$n_p p_p = n_i^2$$

Equation (2.3.5) can be modified as

$$V_o = \frac{KT}{e} \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad \dots(2.3.6)$$

$$\frac{KT}{e} = \text{Constant} = V_T$$

$$V_o = V_T \ln \left(\frac{N_D N_A}{n_i^2} \right) \quad \dots(2.3.7)$$

Taking

2.4 Biasing of p-n Junction

In preceding sections, the concept of potential barrier is established. This potential barrier can be overcome and a current element can be created. We are going to discuss in detail two types of biasing :

- (a) Forward bias
- (b) Reverse bias

Forward biasing and Divide equation

When battery connections to the p-junctions are such that it reduces the potential barrier height, then it is called forward biasing.

Here we will derive the expression for the total current as a function of the applied voltage (The V-I graph)

In this discussion we will use terms like :

(1) Current density $J = \frac{I}{A}$

(2) Diffusion current : A current density that comes into existence due to difference in density.

Lets starts with an unbiased pn junction where Fermi-level is at the same level for p and n side both.

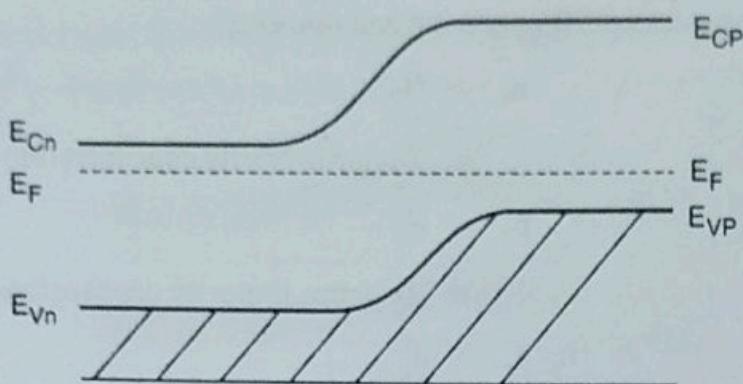


Fig. 2.4.1 : Energy level diagram for unbiased pn junction

Here

E_{CN} = Energy of conduction band for n-type

E_{Cn} = Energy of valance band for n-type

E_{CP} = Energy of conduction bond for p-type

E_{Vn} = Energy of valance band for p-type

E_F = Fermi level

Number of holes carrier concentrations in valance band of p-side is given by

$$P_n = N_v e \frac{(E_{VP} - E_F)}{kT}$$

Number of electrons carrier concentrations in valance band for p-type is given by

$$P_n = N_v e \frac{(E_{VN} - E_F)}{kT}$$

Number of holes in conduction band on n-side

$$n_p = N_c e \frac{(E_F - E_{cp})}{kT}$$

Similarly, $n_n = N_c e \frac{(E_F - E_{CN})}{kT}$

Where k = Boltzmann constant

T = Temperature in °K

$$\therefore \frac{P_p}{P_n} = \frac{N_v \exp\left(\frac{E_{VP} - E_F}{kT}\right)}{N_v \exp\left(\frac{E_{VN} - E_F}{kT}\right)}$$

$$P_n = P_p \exp\left(-\frac{(E_{VP} - E_{VN})}{kT}\right) \quad \dots(2.4.1)$$

Now, let's apply a forward voltage V to this junction. The effect is reported as
Difference between E_{VP} and E_{VN} is reduced by a margin V .

1. Barrier height is reduced
2. The holes will be injected towards the n-region.
3. The holes will be injected towards the n-region.

$$P'_n = P_p \exp \left[-\frac{(E_{VP} - E_{VN} - V)}{kT} \right] \quad \dots(2.4.2)$$

The injected holes are given by.

$$\therefore \Delta P = P'_n - P_n \quad \dots(2.4.3)$$

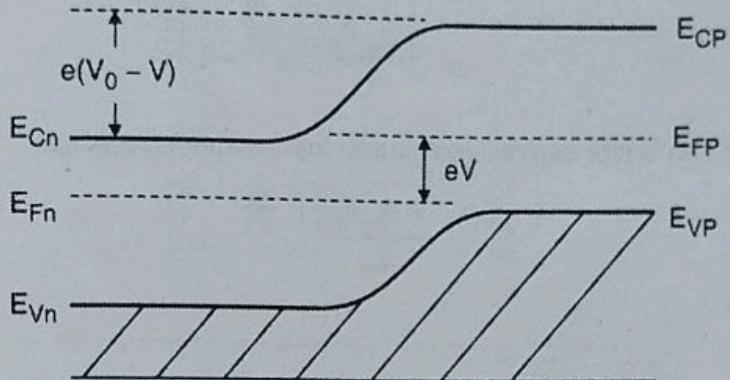


Fig. 2.4.2 : Energy level diagram of p-n junction with forward biased voltage V

Equation (2.4.3) becomes (using Equations (2.4.1) and (2.4.2))

$$\therefore \Delta P = P_p e^{\frac{-e(\Delta\phi - V)}{KT}} - P_p e^{\frac{-e\Delta\phi}{KT}}$$

Where $e\Delta\phi = (E_{VP} - E_{VN})$

$$\therefore \Delta P = P_p \left[e^{\frac{-e\Delta\phi}{KT}} \cdot e^{\frac{eV}{KT}} \right] - P_p e^{\frac{-e\Delta\phi}{KT}}$$

$$\Delta P = P_p e^{\frac{-e\Delta\phi}{KT}} \left[e^{\frac{eV}{KT}} - 1 \right]$$

Using Equation (2.4.1)

$$\Delta P = P_n \left(e^{\frac{eV}{KT}} - 1 \right) \quad \dots(2.4.4)$$

Now correct density due to injected holes

$$J_n = -e D_p \frac{\partial(\Delta P)}{\partial x}$$

Where D_p = Diffusion coefficient of minority carriers holes in region

Let us introduce L_p = Diffusion length for holes

$$\begin{aligned}\therefore J_n &= -e D_p \frac{\partial}{\partial x} \left\{ \Delta P_0 e^{\frac{-x}{L_p}} \right\} \\ &= \frac{-e D_p \Delta P_0}{L_p} \cdot e^{\frac{-x}{L_p}} \\ &= \frac{-e D_p \Delta P}{L_p} \left[\Delta P_0 e^{\frac{-x}{L_p}} = \Delta P \right]\end{aligned}$$

Using Equation (2.4.4)

$$\begin{aligned}J_n &= \frac{e D_p}{L_p} \left[P_n \left(e^{\frac{eV}{KT}} - 1 \right) \right] \\ &= \frac{e D_p P_n}{4} \left[\left(e^{\frac{eV}{KT}} - 1 \right) \right] \quad \dots(2.4.5)\end{aligned}$$

On the same line we can write expression due to injected electrons as

$$\therefore J_e = \frac{e D_n n_p}{L_n} \left[\left(e^{\frac{eV}{KT}} - 1 \right) \right] \quad \dots(2.4.6)$$

Where

D_n = Diffusion coefficient of minority carrier electron in p-region

L_n = Diffusion length for electrons

$$\therefore \text{Total current density } J = J_n + J_e$$

using Equations (2.4.5) and (2.4.6)

$$\begin{aligned}J &= \left(\frac{e D_n P_p}{L_p} + \frac{e D_p L_n}{L_p} \right) \left(e^{\frac{eV}{KT}} - 1 \right) \\ J &= J_0 \left(e^{\frac{eV}{KT}} - 1 \right) \quad \dots(2.4.7) \\ \text{Where } J_0 &= \left(\frac{e D_n P_p}{L_p} + \frac{e D_p L_n}{L_p} \right) \\ &= \text{Saturation current density}\end{aligned}$$

Where converted to current

$$J = \frac{I}{A}$$

We get

$$I = I_0 \left(e^{\frac{eV}{KT}} - 1 \right) \quad \dots(2.4.8)$$

$$\begin{aligned}
 &= -e D_p \frac{\partial}{\partial x} \left[\Delta P_0 e^{\frac{-x}{L_p}} \right] \\
 &= \frac{-e D_p \Delta P_0}{L_p} \cdot e^{\frac{-x}{L_p}} \\
 &= \frac{-e D_p \Delta P}{L_p} \left[\Delta P_0 e^{\frac{-x}{L_p}} = \Delta P \right] \\
 \\
 &= \frac{e D_p}{L_p} \left[P_n \left(e^{\frac{eV}{kT}} - 1 \right) \right] \\
 &= \frac{e D_p P_n}{4} \left[\left(e^{\frac{eV}{kT}} - 1 \right) \right]
 \end{aligned} \quad \dots(2.4.5)$$

ssion due to injected electrons as

$$= \frac{e D_n n_p}{L_n} \left[\left(e^{\frac{eV}{kT}} - 1 \right) \right] \quad \dots(2.4.6)$$

ient of minority carrier electron in p-region

for electrons

$$\begin{aligned}
 &= \left(\frac{e D_n P_p}{L_p} + \frac{e D_p L_n}{L_p} \right) \left(e^{\frac{eV}{kT}} - 1 \right) \\
 &= J_0 \left(e^{\frac{eV}{kT}} - 1 \right) \quad \dots(2.4.7)
 \end{aligned}$$

$$= \left(\frac{e D_n P_p}{L_p} + \frac{e D_p L_n}{L_p} \right)$$

= Saturation current density

$$= \frac{1}{A}$$

$$= I_0 \left(e^{\frac{eV}{kT}} - 1 \right) \quad \dots(2.4.8)$$

Sometimes it is modified as,

$$I = I_0 \left(e^{\frac{V}{nV_T}} - 1 \right)$$

Where $V_T = \frac{kT}{e}$ = Thermal voltage

n = ideality factor (Typically 1 or depending on diode) (1 for Ge, 2 for Si)

For forward bias V is positive and for Reverse bias V is negative hence the exponential term approaches zero.

The current remains very small and close to $-I_0$, till break down occurs.

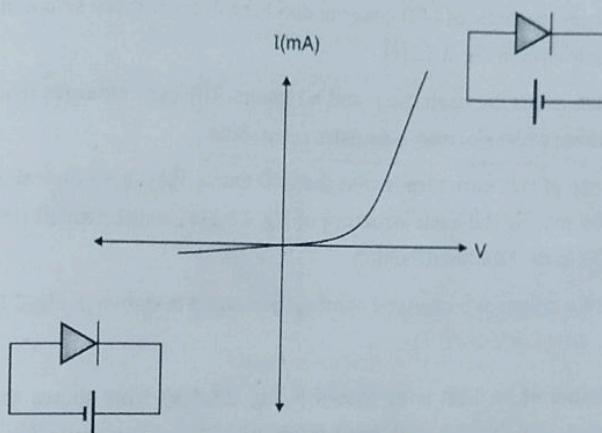


Fig. 2.4.3

2.5 Light Emitting Diode (LED) and its Working

- In this section, let us discuss about one of the important light sources which is the Light Emitting Diode (LED).
- An LED emits light when electrical energy is applied to it. LED is a two-terminal device. The terminals are named as anode (A) and the other as cathode (K).
- A p-n junction is formed between the anode and cathode. So, LED is basically a p-n junction diode.
- For proper operation, it is necessary to forward bias the LED as shown in Fig. 2.5.1(a) and the symbol of LED is shown in Fig. 2.5.1(b). This shows that the symbol is same as that of a p-n junction diode with two arrows indicating that it emits light.

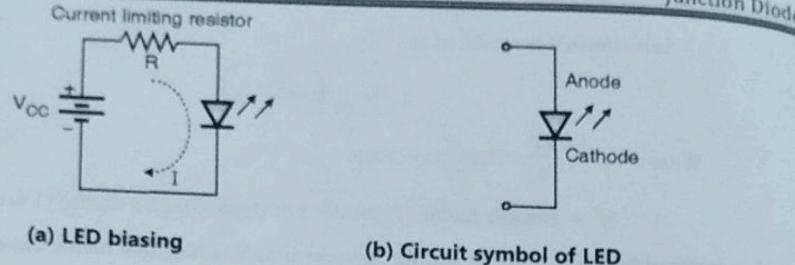


Fig. 2.5.1

Construction of LED

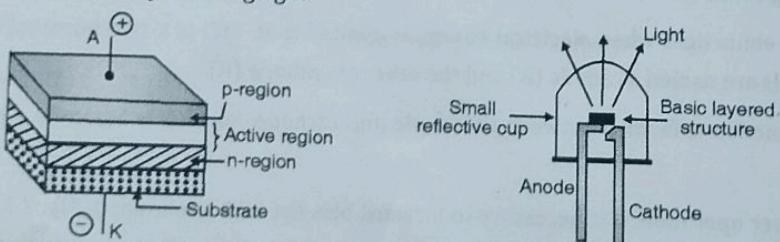
- One of the popular methods of LED construction is to deposit three semiconductor layers on the substrate as shown in Fig. 2.5.2(c).
 - The active region exists between the p and n regions. The light emerges from the active side in all the directions when electron-hole pairs recombine.
 - The disadvantage of this structure is that the LED emits light in all directions. This problem can be solved by placing the basic structure of Fig. 2.5.2(a) inside a small reflective cup, so as to focus the light in the desired direction.
 - Such a structure is called as a cup-type construction and it is shown in Fig. 2.5.2(b).

Circuit symbol

- The circuit symbol of an LED is as shown in Fig. 2.5.2(b). This shows that the symbol is identical to a p-n junction diode with two arrows indicating that it emits light.

Semiconductor materials used

- LEDs are made of Gallium Arsenide (GaAs), Gallium Arsenide Phosphide (GaAsP) and Gallium Phosphide (GaP).
 - Silicon and germanium are not used because they are essentially heat producing materials and are very poor in producing light.



(a) Construction of LED

(b) Cup type construction of LED

Fig. 2.5.2

principle of LED Operation

- When the LED is forward biased, the electrons in the recombine with the holes in the p-type material.
 - These free electrons reside in the conduction band, at the holes in the valence band.
 - When the recombination takes place, these electrons are at a lower energy level than the conduction band.
 - While returning back, the recombining electrons give light. This is shown in Fig. 2.5.3. This process is called an LED emits light. This is the principle of operation.

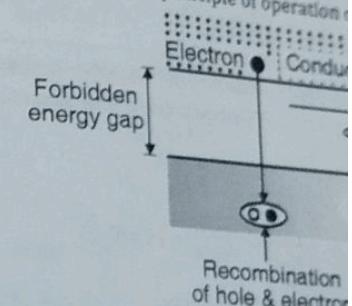
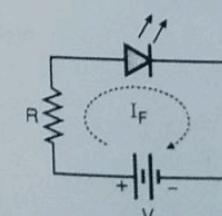


Fig. 2.5.3 : Principle of op-

Output Characteristics of LED

- The graph of Fig. 2.5.4(a) shows the output characteristics dependence of light output on the forward LED current I_F .
 - However, it is not possible to increase I_F indefinitely.



(a) LED is forward biased

(b) Relation b

Fig. 2.5.

Principle of LED Operation

- When the LED is forward biased, the electrons in the n-region will cross the junction and recombine with the holes in the p-type material.
- These free electrons reside in the conduction band, and hence at a higher energy level than the holes in the valence band.
- When the recombination takes place, these electrons return back to the valence band which is at a lower energy level than the conduction band.
- While returning back, the recombining electrons give away the excess energy in the form of light. This is shown in Fig. 2.5.3. This process is called as **electroluminescence**. In this way, an LED emits light. This is the principle of operation of LED.

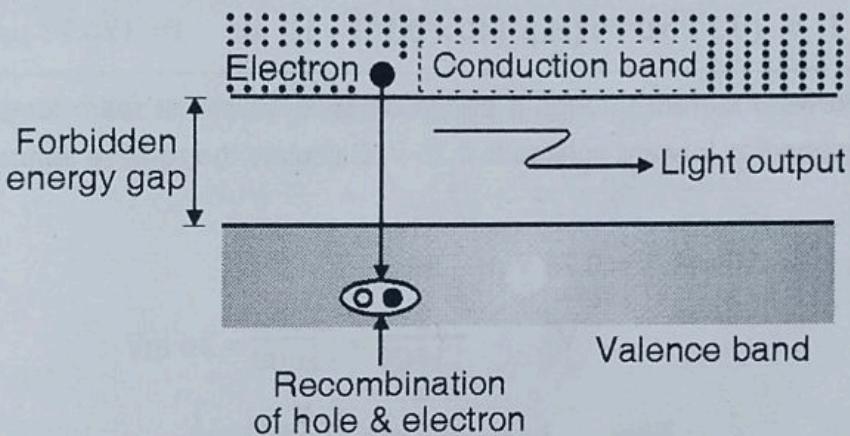
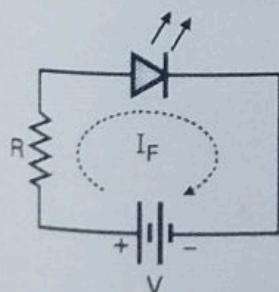


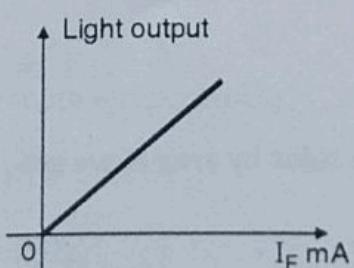
Fig. 2.5.3 : Principle of operation of LED

Output Characteristics of LED

- The graph of Fig. 2.5.4(a) shows the output characteristics of the LED. It shows the linear dependence of light output on the forward LED current.
- However, it is not possible to increase I_F indefinitely. Typically, the maximum value of I_F is 80 mA.



(a) LED is forward biased



(b) Relation between forward current and light output

Fig. 2.5.4

2.6 Solved Problems

Ex. 2.6.1 : The reverse saturation current at room temperature is $0.3 \mu A$ when a reverse bias is applied to a Ge diode. Find the value of current flowing in the diode when $0.15 V$ forward bias is applied at room temperature.

Soln. :

$$\text{Given } I_0 = 0.3 \mu A = 0.3 \times 10^{-6} A \text{ and } V = 0.15 V$$

$$\text{At room temperature } T = 300 K, V_T = 26 mV$$

$$\begin{aligned} I &= I_0 \left[\exp\left(\frac{40}{\eta}\right) - 1 \right] \\ &= I_0 [\exp(40 V) - 1] \end{aligned} \quad (n = 1 \text{ for Ge})$$

Substituting the value of I_0 and V , we get

$$I = (0.3 \times 10^{-6}) [\exp(40 \times 0.15) - 1] \quad \text{or} \quad I = 126.73 \mu A$$

Ex. 2.6.2 : The forward current through a silicon diode is $10 mA$ at room temperature ($27^\circ C$). The corresponding forward voltage is $0.75 V$. Calculate the reverse saturation current.

Soln. :

$$\text{Given, } I = 10 mA, V = 0.75 \text{ Volt and } T = 27^\circ C$$

$$V_T = \frac{T}{11600} = \frac{300}{11600} = 26 mV$$

$$\text{Now } I = I_0 \left[\exp\left(\frac{V}{\eta V_T}\right) - 1 \right]$$

$$\text{or } 10 \times 10^{-3} = I_0 \left[\exp\left(\frac{0.75}{2 \times (26 \times 10^{-3})}\right) - 1 \right]$$

$$\text{Solving, we get, } I_0 = 5.446 nA$$

Ex. 2.6.3 : The saturation current density of P-N junction Ge diode is $250 mA/m^2$ at $300 K$. Find the voltage that would have to be applied across junction to cause forward current density of 10^5 amp./m^2 .

Soln. :

We know that

$$I = I_0 \left[\exp\left(\frac{V}{\eta V_T}\right) - 1 \right]$$

Dividing on both sides by area A , we get

$$\frac{I}{A} = \frac{I_0}{A} \left[\exp\left(\frac{V}{\eta V_T}\right) - 1 \right]$$

$$\text{or } J = J_0 \left[\exp\left(\frac{V}{\eta V_T}\right) - 1 \right] \quad \dots [J = \text{current density}]$$

For Ge, $\eta = 1$ and $V_T = \frac{300}{11600} = 0.02586$

$$\therefore 10^5 = (250 \times 10^{-3}) \left[\exp\left(\frac{V}{0.02586}\right) - 1 \right]$$

$$\text{or } 4 \times 10^5 = [\exp(38.66 \text{ V}) - 1]$$

$$\text{or } \exp[38.66 \text{ V}] = 4 \times 10^5 + 1$$

Taking log of both sides, we get

$$38.66 \text{ V} = 12.8992 + 0$$

$$V = 0.3336 \text{ Volt.}$$

Ex. 2.6.4 : A germanium P-N junction diode have reverse saturation current I_0 of $4 \mu \text{A}$ at 25°C . If a sine wave having peak amplitude of 0.15 V is applied across the junction what is rectification ratio (ratio of forward to reverse peak currents) ?

Soln. :

Given, $I_0 = 4 \times 10^{-6} \text{ A}$. Forward Voltage = 0.15 V

$$\text{Now } V_T = \frac{T}{11600} = \frac{273 + 25}{11600} = \frac{298}{11600} \quad \eta = 1 \text{ for Ge}$$

$$I_F = 4 \times 10^{-6} \text{ A} \left[\exp\left(\frac{0.15 \times 11600}{298}\right) - 1 \right]$$

Solving, we get

$$I_F = 1.32 \times 10^{-3} \text{ A}$$

For negative half cycle, $V = -0.15 \text{ V}$, Therefore, reverse current

$$I_R = 4 \times 10^{-6} \left[\exp\left(\frac{-0.15 \times 11600}{298}\right) - 1 \right] \\ = -4 \times 10^{-6} \text{ A}$$

$$\text{Ratio} = \left| \frac{I_F}{I_R} \right| = \frac{1.32 \times 10^{-3}}{4 \times 10^{-6}} = 330$$

Ex. 2.6.5 : For what voltage, will the reverse current in P-N junction Ge diode reach 90% of its saturation value at room temperature ?

Soln. :

Here, $T = 300 \text{ K}$ (room temperature)

$$V_T = \frac{300}{11600} (\eta = 1 \text{ for Ge})$$

$$I = I_0 \left[\exp\left(\frac{V}{\eta V_T}\right) - 1 \right]$$

$$-0.9I_0 = I_0 \left[\exp\left(\frac{V \times 11600}{300}\right) - 1 \right]$$

$$\exp\left(\frac{V \times 11600}{300}\right) = 0.1$$

Taking log of both sides, we get

$$\begin{aligned} \frac{V \times 11600}{300} &= \log(0.1) = -2.3 \\ V &= -\frac{2.3 \times 300}{11600} \\ &= -0.06 \text{ Volt} \end{aligned}$$

The negative sign indicates that a reverse voltage has to be applied.

Ex. 2.6.6 : Calculate the barrier potential for a silicon pn junction diode at 300° K with $N_A = 1 \times 10^{18}/\text{cm}^3$ and $N_D = 1 \times 10^{15}/\text{cm}^3$. Intrinsic carrier concentration = $1.5 \times 10^{10}/\text{cm}^3$

Soln. :

$$\text{Formula} = V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$\text{Where } V_T = \frac{kT}{e}$$

$$\therefore V_0 = \frac{kT}{e} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

$$= \left(\frac{1.38 \times 10^{-13} \times 300}{1.6 \times 10^{-19}}\right) \ln\left(\frac{1 \times 10^{18} \times 1 \times 10^{15}}{(2.25 \times 10^{20})}\right)$$

$$V_0 = 0.0259 \text{ V}$$

...Ans.

Ex. 2.6.7 : An abrupt SE pn junction $N_A = 10^{18}/\text{cm}^3$ on one side and $N_D = 5 \times 10^{15}/\text{cm}^3$ on the other.

- (a) Calculate the Fermi level positions at 300°K in the p and n region
- (b) Calculate barrier potential

Soln. :

(a) For p region

$$\begin{aligned} E_{ip} - E_F &= kT \ln \frac{P_p}{n_i} = 0.259 \ln \left(\frac{1 \times 10^{18}}{1.5 \times 10^{10}}\right) \\ &= 0.467 \text{ eV} \end{aligned}$$

For n-region

$$\begin{aligned} E_F - E_{in} &= kT \ln \left(\frac{n_n}{n_i}\right) \\ &= 0.259 \ln \left(\frac{5 \times 10^{15}}{1.5 \times 10^{10}}\right) \\ &= 0.329 \text{ eV} \end{aligned}$$

(b) Barrier potential

$$\begin{aligned}V_0 &= \frac{KT}{e} I_n \left(\frac{N_A N_D}{n i^2} \right) \\&= \frac{0.259}{1.6 \times 10^{-19}} \ln \left(\frac{5 \times 10^{38}}{2.25 \times 10^{20}} \right) \\&= 1.53 \times 10^{-19} \text{ V}\end{aligned}$$

...Ans.

Review Questions

- Q.1 What is p-n junction ?
- Q.2 Explain Depletion Layer and Potential Difference in p-n Junction.
- Q.3 Explain Biasing of p-n junction.
- Q.4 Explain Light Emitting Diode (LED) and its working.



3

Important Diodes

Syllabus

Working of : Photo diode, solar cell, Zener diode, Varactor diode, Gunn diode and their applications.

3.1 Introduction

- Diodes play a crucial role in the electronics industry due to their ability to control the direction of current flow. A diode is a semiconductor device that allows current to flow in one direction while blocking it in the opposite direction. This property makes diodes essential for various applications, particularly in power conversion, signal processing, and protection circuits.
- One of the primary uses of diodes is in rectification, where alternating current (AC) is converted into direct current (DC). This is crucial in power supplies for electronic devices, as most electronics require DC to function. Diodes also serve as components in voltage regulation, ensuring that voltage levels remain within a specified range to protect sensitive components.
- Additionally, diodes are integral in signal modulation and demodulation, enabling communication systems like radios, televisions, and mobile devices. Zener diodes, in particular, are used for voltage regulation and surge protection in electronic circuits, protecting sensitive equipment from voltage spikes.
- In modern electronics, diodes are used in LEDs (light-emitting diodes), which are essential for displays, indicators, and energy-efficient lighting. Overall, the versatility and reliability of diodes make them foundational to the advancement and functioning of the electronics industry.

3.2 Photodiode

- **Principle of working :** A photodiode is a type of diode that converts light energy into electrical current. It does this by utilizing the photoelectric effect, where light energy (photons) strikes the material inside the diode, causing the generation of electron-hole pairs.
- Let's get familiar of its structure and working principle.
- **Structure and Operation:** A photodiode is typically made of a P-type or N-type semiconductor material like silicon or germanium. It consists of a PN junction, where the P-type region (positive) and N-type region (negative) are joined together.

Symbol :

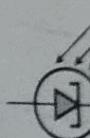


Fig. 3.2.1 : Symbol

- **Reverse Bias :** Photodiodes are usually operated under reverse bias conditions, where no forward current flows due to the built-in electric field of the PN junction. However, a small reverse current does flow through the diode under normal conditions.
- **Photon Absorption :** When light (photons) strikes the photodiode, it is absorbed by the semiconductor material. The energy from the photon is used to free electrons from their bonds, creating electron-hole pairs.
- **Charge Carrier Separation :** The built-in electric field at the PN junction causes these electron-hole pairs to separate. Electrons are swept toward the N-type region, and holes are swept toward the P-type region.
- **Current Generation :** As a result of the separation of charge carriers, a current is generated. The magnitude of this current is proportional to the intensity of the incident light. The higher the light intensity, the greater the current.
- The photo diode is a two terminal junction diode. It is reverse biased and then illuminating it. A reverse biased current I_s due to thermally generated electron-hole pairs is added to the photocurrent.

3.2

Photodiode

Principle of working : A **photodiode** is a type of diode specifically designed to detect light and convert it into electrical current. The principle of a photodiode is based on the **photoelectric effect**, where light energy (photons) is absorbed by the semiconductor material inside the diode, causing the generation of charge carriers (electrons and holes).

Let's get familiar of its structure and working step by step :

Structure and Operation: A photodiode is typically made of semiconductor materials like silicon or germanium. It consists of a **PN junction**, similar to a regular diode, where the P-type region (positive) and N-type region (negative) are brought together.

Symbol :

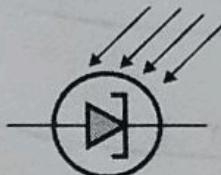


Fig. 3.2.1 : Symbol of Photo diode

- **Reverse Bias :** Photodiodes are usually operated in **reverse bias**. In reverse bias, a small current flows due to the built-in electric field at the junction, but no significant current flows through the diode under normal conditions.
- **Photon Absorption :** When light (photons) strikes the photodiode, it is absorbed by the semiconductor material. The energy from the photons excites the electrons in the material, generating **electron-hole pairs**.
- **Charge Carrier Separation :** The built-in electric field in the depletion region of the PN junction causes these electron-hole pairs to separate. Electrons are swept toward the N-type region, and holes are swept toward the P-type region.
- **Current Generation :** As a result of the separation of charge carriers, a photocurrent is generated. The magnitude of this current is proportional to the intensity of the incident light. The higher the light intensity, the greater the number of charge carriers, and thus the higher the current.
- The photo diode is a two terminal junction device which is operated by first reverse biasing and then illuminating it. A reverse biased pn junction has a small amount of saturation current I_s due to thermally generated electron - hole pairs. In silicon I_s is of few nanoamperes

range. The number of these minority carriers depends on the intensity of light incident on the junction. When the diode is in glass package, light can reach the junction and change the reverse current.

- A lens is used focus in its package to focus maximum light on the reverse bias junction. The characteristics of photo diode is shown in Fig. 3.2.2

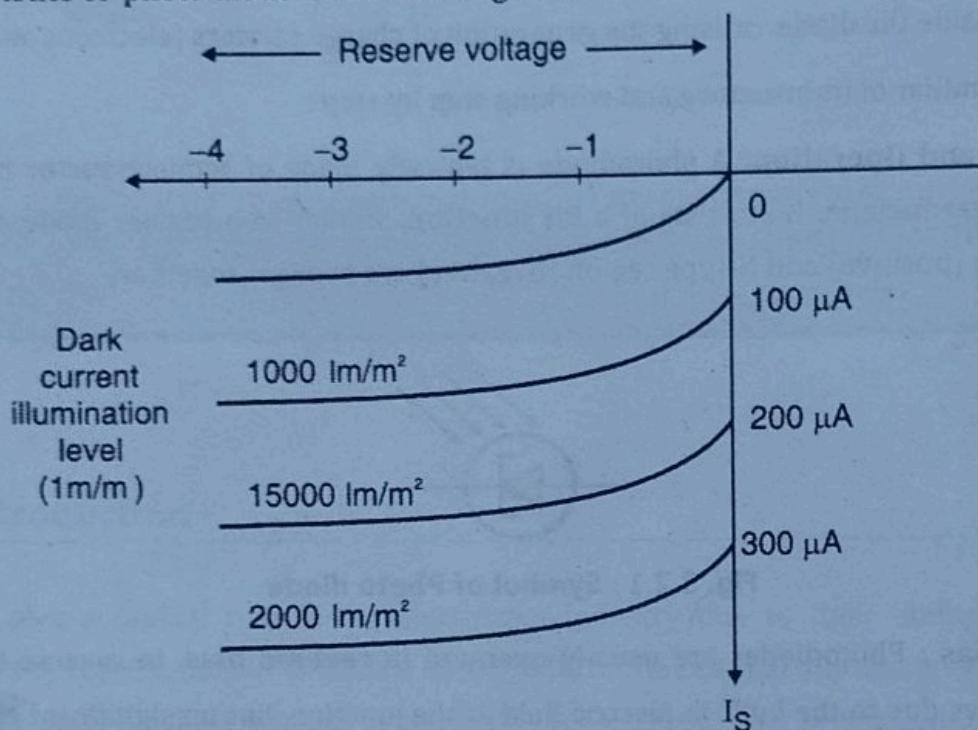
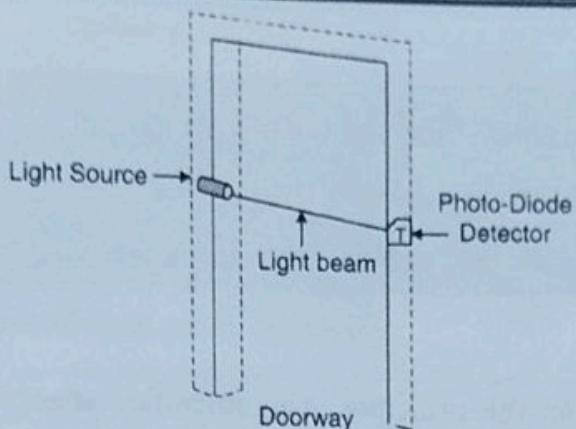


Fig. 3.2.2 : Characteristics at various illumination level lm/m^2

- The characteristics shows that for a given reverse voltage I_s increases with the level of illumination. The dark current refers to the current that flows when no light is incident on pn junction. By changing the illumination level the reverse current can be changed.
- A PIN junction is preferred in photodiode over a simple pn junction. A PIN photodiode is a type of photodetector or semiconductor device used to convert light signals into electrical signals. The name "PIN" is derived from the arrangement of the three semiconductor layers within the device: P-type, Intrinsic (undoped), and N-type

Application

1. **Alarm Circuit Using Photodiode :** The Below Fig. shows the use of photo-diode in an alarm system. Light from a light source is allowed to fall on a photo-diode fitted in the doorway. The reverse current I_R will continue to flow so long as the light beam is not broken. If a person passes through the door, light beam is broken and the reverse current drops to the dark current level. As a alarm is sounded.

**Fig. 3.2.3**

2. A photodiode can turn its current in OFF to ON state in nanoseconds hence its one of the fastest switch.
3. The logic circuits that gets activated by light
4. Character recognition
5. Optical communication equipment
6. Pulse oximeters

3.3 Photovoltaic Cell

- When suitable light falls on a p-n junction, a potential difference is produced across it. This voltage is capable of driving a current through an external circuit. This important phenomenon is called the 'photovoltaic effect'.
- This photovoltaic effect was first invented by E. Becquerel in 1839. He found that certain materials would produce very small amount of electric current when exposed to light. On continuous effort, Bell laboratories in 1954 constructed the first photovoltaic cell, known as a solar battery. Due to the energy crisis, presently photovoltaic technology is becoming the main source of electrical power for many industrial and domestic applications.
- A device is so constructed in which solar energy is converted into electrical energy. Therefore, this device is called as photovoltaic cell or solar cell. In the solar cell, semiconductor material is used. When light energy falls on it, electrons from the semiconductor material get free from the atom in the semiconductor.
- Further, these electrons are made free to move through the semiconductor by applying external potential or voltage. Finally, due to this arrangement electric current is observed in the electrical circuit. The current produced is found to directly depend on light intensity falling on the semiconductor materials. The following section describes the details of solar cell.

Solar Cell

Q. Explain with neat diagram construction and working of solar cell.

Dec. 12, May 14, 5 Marks

Q. Explain the use of P-N junction as solar cell.

Dec. 13, 3 Marks

Q. What is the principle of a solar cell? Write its advantages and disadvantages.

May 17

(a) Principle

- A solar cell works on the principle of photovoltaic effect. It is a device that directly converts the energy in light into electrical energy.
- It was first developed by French physicist Antoine-César Becquerel. He observed the photovoltaic effect while experimenting with a solid electrode in an electrolyte solution when he saw a voltage developed when light fell upon the electrode.

(b) Construction and working

- From construction point of view, generally crystalline silicon (Si) has been used as the light-absorbing semiconductor in most solar cells, even though it is a relatively poor absorber of light and requires a considerable thickness (several hundred microns) of material.
- Presently two types of crystalline silicon are used for production of solar cell namely
 - 1) **Monocrystalline** - It is produced by slicing wafers (up to 150mm diameter and 350 microns thick) from a high-purity single crystal.
 - 2) **Multicrystalline** - It is made by sawing a cast block of silicon first into bars and then wafers.
- For both mono and multicrystalline Si, a semiconductor homojunction is formed by diffusing phosphorus (an n-type dopant) into the top surface of the boron doped (p-type) Si wafer. Construction of the solar cell is as shown in Fig. 3.3.1(a).
- Screen-printed contacts are applied to the front and rear of the cell, with the front contact pattern specially designed to allow maximum light exposure of the Si material with minimum electrical (resistive) losses in the cell.
- The **most efficient production cells** use monocrystalline Si with laser grooved and buried grid contacts for maximum light absorption and current collection.
- Each Si cell generates about 0.5V, so about 36 cells are usually soldered together in series to produce a module with an output to charge a 12V battery.
- The cells are hermetically sealed under tough, high transmission glass to produce highly reliable, weather-resistant models that may be warranted for up to 25 years.

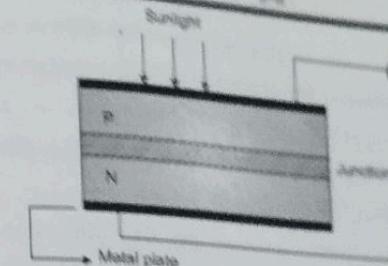


Fig. 3.3.1 (a) : Working of a solar cell

(1) Production and development of pairs of positive and negative charges (electron-hole pairs) in the solar cell by absorbed solar radiation

(2) Distance between positive and negative charges by

First it is essential to select the material or prepare the material which can absorb maximum energy associated with the photons of sunlight. This

$$E = \frac{hc}{\lambda}$$

Where,

E = Energy of a photon

And

λ = Wavelength of theradiation

h = Planck's constant

= 6.62×10^{-34} ergs

c = Velocity of light

= 3×10^8 m/s

• Hence above relation becomes $E = \frac{1.24}{\lambda}$, in which λ is in nanometer. Thus above relation is used to calculate the wavelength of the incident light.

• The only materials suitable for absorbing the light are semiconductors like silicon, cadmium sulphide etc.

• Generally in a semiconductor, the electrons are present in the conduction band.

• The valence band has electrons at a lower energy level and the conduction band has electrons at a higher energy level.

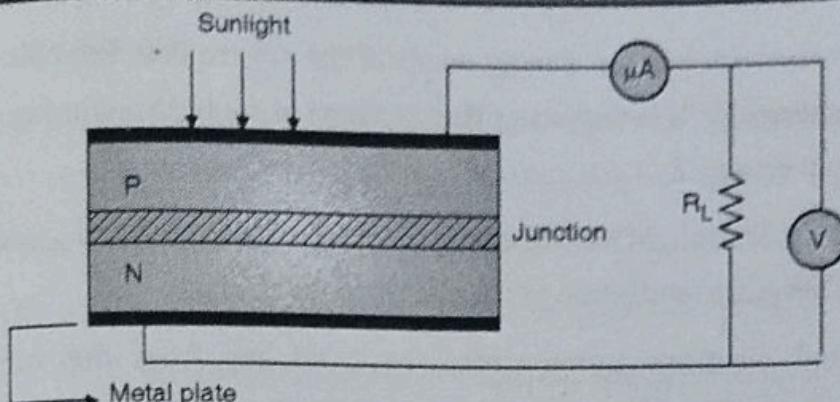


Fig. 3.3.1 (a) : Working of a solar cell

- (1) Production and development of pairs of positive and negative charges (electron-hole pairs) in the solar cell by absorbed solar radiation
- (2) Distance between positive and negative charges by a potential gradient within the cell

First it is essential to select the material or prepare the material which can absorb the energy associated with the photons of sunlight. This can be done using following relation

$$E = \frac{hc}{\lambda} \quad \dots(3.3.1)$$

Where,

E = Energy of a photon

And

λ = Wavelength of theradiation

h = Planck's constant

= 6.62×10^{-27} ergs

c = Velocity of light

= 3×10^8 m/s

- Hence above relation becomes $E = \frac{1.24}{\lambda}$, in which E is the energy in electron-volt (eV) and λ is in nanometer. Thus above relation is used to design a solar cell.
- The only materials suitable for absorbing the energy of the photons of sunlight are semiconductors like silicon, cadmium sulphide, gallium arsenide, etc.
- Generally in a semiconductor, the electrons occupy either valence band or the conduction band.
- The valence band has electrons at a lower energy level and is fully occupied, while the conduction band has electrons at a higher energy level and is not fully occupied.

- The difference between the energy levels of the electrons in the two bands is called the band gap energy E_g . It is necessary that photons of sunlight having energy E greater than the band gap energy E_g .
- Here, photons of sunlight having energy E which is greater than E_g is absorbed by the cell material. Therefore, excitation of the electrons takes place.
- Such excited electrons jump across the band gap from the valence band to the conduction band, but they leave behind holes in the valence band. In this way electron-hole pairs are created, it is as shown Fig. 3.3.2(b).
- Thus, electrons in the conduction band and the holes in the valence band become mobile. They can be separated and made to flow through an external electronic circuit.
- According to the photovoltaic effect, a potential gradient is developed within the cell.
- In the case of silicon, the potential gradient is obtained by making the cell as a sandwich of two types of silicon, i.e. p-type and n-type. Thus, when a composite of the two types of silicon is formed, a jump in energy levels occurs at the junction interface. (See Fig. 3.3.2 (b))

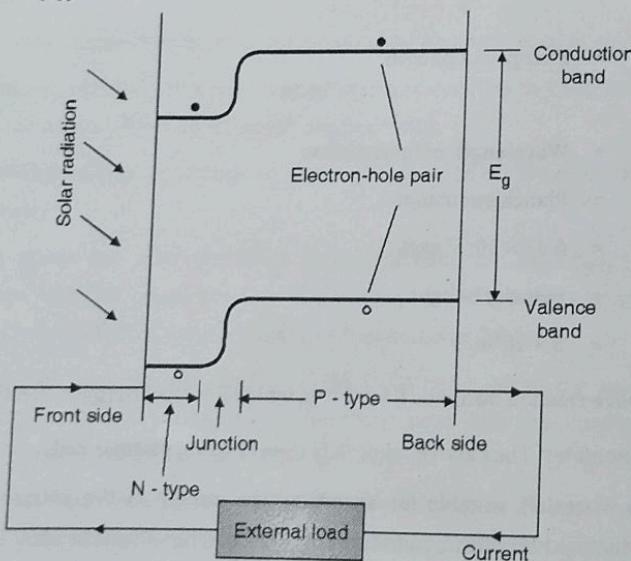


Fig. 3.3.2(b) : Band structure of solar cell

In this way, the developed potential gradient is adequate to separate the electrons and holes, and hence produces a direct electric current to flow in the external circuit with load.

(c) **Advantages of solar cell.**

- Raw material i.e. amount of solar energy cell. Hence, it is more useful in satellite co
- It is pollution free. It is not harmful to hu
- It most useful in remote areas where tra
- They are portable as compared to other e

(d) **Disadvantages of solar cell**

- Operation in the night is not possible.
- It has low efficiency hence presently it is r
- It is a dilute source.

3.3.1 Applications of Solar Cell

1. Solar Powered Pumps

1. Solar Powered Pumps

- Solar water pumping systems are tra providing electricity to farmers from agricultural sector is largely dependent used as artificial means to provide water
- Farmers rely on grid electricity or diesel and economic stress. Hence, effective irri boon for our farmers. It enhances their c supply of water to their fields.
- Solar water pumps are an application o energy into electricity to drive pumping and pollution-causing diesel-powered ve module which helps to pump out surface o

Industrial Solar Applications

Solar-powered manufacturing equipment	Reduc
Solar-powered water pumps and heating systems	Efficie heating

(c) **Advantages of solar cell.**

- Raw material i.e. amount of solar energy is available at no cost for operation of the solar cell. Hence, it is more useful in satellite communication.
- It is pollution free. It is not harmful to human life.
- It is most useful in remote areas where traditional transmission may be difficult.
- They are portable as compared to other electronic energy transmission devices.

(d) **Disadvantages of solar cell**

- Operation in the night is not possible.
- It has low efficiency hence presently it is non-economical.
- It is a dilute source.

3.3.1 Applications of Solar Cell

1. Solar Powered Pumps

2. Solar photovoltaic energy

1. Solar Powered Pumps

- Solar water pumping systems are transforming the agriculture sector in India by providing electricity to farmers from pumping water to harvesting crops. India's agricultural sector is largely dependent on monsoon for natural irrigation. Pumps are used as artificial means to provide water for irrigation.
- Farmers rely on grid electricity or diesel gen-sets to run the pumps, causing huge delays and economic stress. Hence, effective irrigation system like solar water pump is a huge boon for our farmers. It enhances their crop yield by ensuring a reliable and perennial supply of water to their fields.
- Solar water pumps are an application of photovoltaic technology that converts solar energy into electricity to drive pumping systems, thereby replacing erratic grid supply and pollution-causing diesel-powered versions. Solar water pump is powered by solar module which helps to pump out surface or ground water for irrigation.

Industrial Solar Applications	Benefits
Solar-powered manufacturing equipment	Reduced energy costs, lower carbon footprint
Solar-powered water pumps and heating systems	Efficient fluid circulation, sustainable water heating

Industrial Solar Applications	Benefits
Solar energy for warehousing and logistics	Reliable, off-grid power for facility operations
Solar-powered lighting and security systems	Enhanced energy efficiency, improved safety and security

2. Solar Photovoltaic Pumps

- What is photovoltaic (PV) technology and how does it work? PV materials and devices convert sunlight into electrical energy. A single PV device is known as a cell. An individual PV cell is usually small, typically producing about 1 or 2 watts of power.
- These cells are made of different semiconductor materials and are often less than the thickness of four human hairs. In order to withstand the outdoors for many years, cells are sandwiched between protective materials in a combination of glass and/or plastics.
- To boost the power output of PV cells, they are connected together in chains to form larger units known as modules or panels. Modules can be used individually, or several can be connected to form arrays. One or more arrays is then connected to the electrical grid as part of a complete PV system. Because of this modular structure, PV systems can be built to meet almost any electric power need, small or large.
- PV modules and arrays are just one part of a PV system. Systems also include mounting structures that point panels toward the sun, along with the components that take the direct-current (DC) electricity produced by modules and convert it to the alternating-current (AC) electricity used to power all of the appliances in your home.
- Guwahati and Chennai Central Railway stations are solar powered. The largest PV systems abroad is located in California and produce power for utilities to distribute to their customers. The Solar Star PV power station produces 579 megawatts of electricity, while the Topaz Solar Farm and Desert Sunlight Solar Farm each produce 550 megawatts.

3.4 Zener Diode

Zener breakdown (or Zener effect) refers to a phenomenon in semiconductor physics where a **Zener diode** exhibits a sharp breakdown voltage when a reverse voltage is applied. Zener diodes are designed to operate in this breakdown region without being damaged. Here's how it works:

- Zener Diodes are a type of diode designed to allow current direction, but they are also specially engineered to conduct if voltage exceeds a certain threshold, known as the **Zener breakdown voltage**.
- When the reverse voltage reaches a certain point (the Zener breakdown voltage), the diode becomes strong enough to break down the depletion region, allowing current to flow in the reverse direction.
- This breakdown occurs at a precise voltage (called the **Zener breakdown voltage**) allowing Zener diodes to be used in voltage regulation applications that require stable reverse voltage operation.

3.4.1 Physics of Zener Break Down

- In Zener break down, the junction is thin and abrupt. The depletion region is very high such that even a small reverse biasing voltage can cause a large current. $E = V/d$ (junction is thin hence d is small and V is high) across the junction.
- The phenomena of quantum tunneling takes place across the junction as well. Electrons in valance band do not possess enough energy to cross the potential barrier, however under quantum mechanical circumstance electrons can tunnel through the barrier. In special circumstances a sufficiently large number of carriers can tunnel through the barrier resulting in the flow of large current.

Symbol



3.4.2 Application

- Zener diodes are used for **voltage regulation**, where they maintain a constant voltage despite variations in input voltage or load conditions.
- A Zener diode operates in **reverse bias** beyond a certain **breakdown voltage**. In this region, the diode maintains a constant voltage even when the current through it varies (within limits). This makes it useful in voltage regulator circuit, the Zener diode is connected in series with a resistor to limit its current to its Zener voltage (V_z) value.

Zener Diodes are a type of diode designed to allow current to flow normally in the forward direction, but they are also specially engineered to conduct in the reverse direction when the voltage exceeds a certain threshold, known as the **Zener breakdown voltage**.

When the reverse voltage reaches a certain point (the Zener voltage), the electric field across the diode becomes strong enough to break down the **depletion region**, allowing current to flow in the reverse direction.

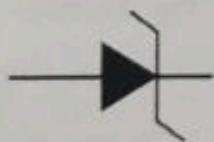
This breakdown occurs at a precise voltage (called the **Zener voltage**) and is non-destructive, allowing Zener diodes to be used in voltage regulation, surge protection, and other applications that require stable reverse voltage operation.

3.4.1 Physics of Zener Break Down

In Zener break down , the junction is thin and abrupt . the doping levels for such junctions is very high such that even a small reverse biasing voltage can create very large Electric fields $E = V/d$ (junction is thin hence d is small and V is high) across the narrow depletion region.

The phenomena of quantum tunneling takes place across the thin junction as it is designed to be abrupt as well. Electrons in valance band do not possess sufficient energy to overcome the barrier , however under quantum mechanical circumstances , due to a thin abrupt depletion layer the carriers cross this potential barrier to sneak in to conduction band and under the special circumstances a sufficiently large number of carriers tunnel to the conduction band resulting in the flow of large current.

Symbol



3.4.2 Application

- Zener diodes are used for **voltage regulation**, where they maintain a constant output voltage despite variations in input voltage or load conditions.
- A Zener diode operates in **reverse bias** beyond a certain voltage known as the **Zener breakdown voltage**. In this region, the diode maintains a nearly constant voltage across it, even when the current through it varies (within limits). This makes it ideal for regulating voltage. When used in a voltage regulator circuit, the Zener diode clamps the output voltage to its Zener voltage (V_z) value.

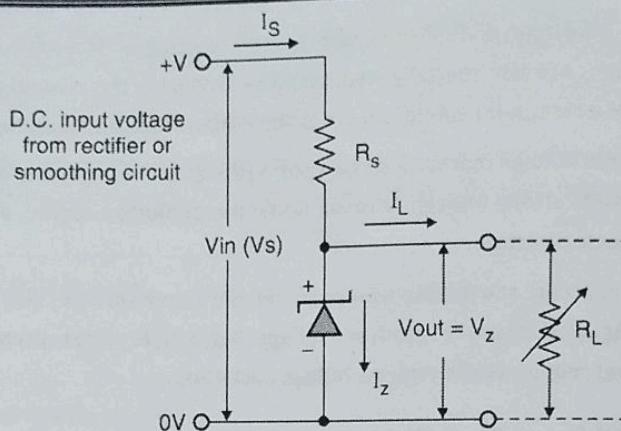


Fig. 3.4.1(a)

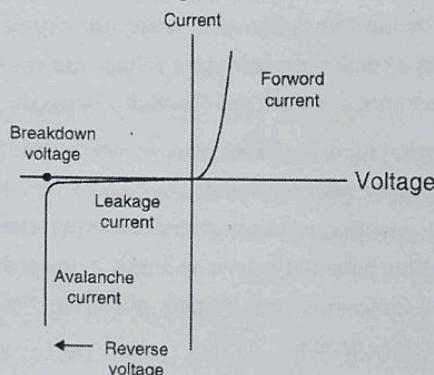


Fig. 3.4.1(b)

Limitations of using Zener diodes as voltage regulators

- Load regulation**: Zener diodes may have poor load regulation, meaning the output voltage can fluctuate with changes in the load current.
- Temperature dependence**: Zener diodes are temperature-sensitive, and their Zener voltage can shift with changes in temperature.
- Power dissipation**: Zener diodes dissipate power in the form of heat, and their efficiency is typically low, especially when there is a large difference between the input and output voltage.
- Current limitations**: The Zener diode has a maximum current rating, and if the load draws more current than the Zener can supply, the voltage will not be regulated.

3.5 Varactor Diode

Varactor diode is a type of diode dependent on reverse voltage. Like photo diode it is a dependent semiconductor device. Several variable capacitance diode

3.5.1 Symbol of Varactor Diode

It is clear that the symbol has two parallel plate capacitor.

3.5.2 Function of Varactor Diode

- The prominent feature function of varactor diode is operated in reverse bias conditions. In reverse bias, depletion layer width increases as the reverse bias voltage increases. As a result, the depletion layer width is more, and vice versa. So if we need to increase the junction capacitance, the reverse bias voltage should be decreased.
- It causes the width of the depletion layer ($c \propto 1/d$). Similarly, increasing the reverse bias voltage decreases the depletion layer width, which increases the junction capacitance. This is the biggest advantage of a varactor diode.

3.5.3 Important Highlights

(A) Varactor Diode Characteristics

Varactor diodes are mostly operated in reverse bias conduction. They are voltage-controlled variable capacitors, although the word varactor is used.

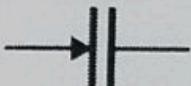
(B) Variable Capacitance Characteristics

Variable capacitance effect is shown by providing the required capacitance.

3.5 Varactor Diode

Varactor diode is a type of diode whose internal capacitance varies with respect to the reverse voltage. Like photo diode it always works in reverse bias conditions and is a voltage-dependent semiconductor device. Several names know varactor diode as Varicap, Voltcap, Voltage variable capacitance diode

3.5.1 Symbol of Varactor Diode



It is clear that the symbol has two parts one representing pn junction diode and other a parallel plate capacitor.

3.5.2 Function of Varactor Diode

- The prominent feature function of the varactor diode is to store charges, so it is always operated in reverse bias conditions. When a forward bias voltage is applied, the electric current flows. As a result, the depletion region becomes negligible, which is undesirable.
- The junction capacitance of a p-n junction diode is inversely proportional to the width of the depletion layer. In other words, if the width of the depletion layer is less, then the capacitance is more, and vice versa. So if we need to increase the capacitance of a varactor diode, the reverse bias voltage should be decreased ($c \propto V$).
- It causes the width of the depletion layer to decrease, resulting in higher capacitance ($c \propto 1/d$). Similarly, increasing the reverse bias voltage should decrease the capacitance. This ability to get different values of capacitances just by changing the voltage applied is the biggest advantage of a varactor diode compared to a normal variable capacitor.

3.5.3 Important Highlights

(A) Varactor Diode Characteristics

Varactor diodes are mostly operated under reverse bias conditions; therefore, there is no conduction. They are voltage-controlled capacitors and are sometimes known as varicap diodes, although the word varactor is widely used.

(B) Variable Capacitance Characteristics

Variable capacitance effect is shown by normal diodes, but varactor diodes are preferred for providing the required capacitance changes. The diodes are uniquely optimized and

manufactured to enable high-range changes in capacitance. Varactor diodes are categorized based on the properties of the diode junction.

(C) Varactor Diode Applications

They are used in the RF (Radio Frequency) design arena and provide a method of varying the capacitance within a circuit by applying control voltage. It provides them with special capability, due to which varactor diodes are used in the RF industry.

Varactor diodes are commonly used as tuners in electronic sets in devices where voltage controlled oscillations are required.

3.6 Gunn Diode

3.6.1 Gunn Effect

High-frequency oscillation of electrical current flowing through certain semiconducting solids. The effect is used in a solid state device, the Gunn diode, to produce short radio waves called microwaves (used in Microwave oven).

3.6.2 Gunn Diode Basics

- A Gunn diode is a passive semiconductor device with two terminals, which consists of only an n-doped semiconductor material, unlike other diodes which consist of a p-n junction. Gunn diodes can be made from the materials which consist of multiple, initially-empty, closely-spaced energy valleys in their conduction band like Gallium Arsenide (GaAs),
- General manufacturing procedure involves growing an epitaxial layer on a degenerate n+ substrate to form three n type semiconductor layers, where-in the extreme layers are heavily doped when compared to the middle, active layer.
- Further the metal contacts are provided at either ends of the Gunn diode to facilitate biasing. The circuit symbol for **Gunn diode** is as shown by Figure given below and differs from that normal diode so as to indicate the absence of p-n junction.

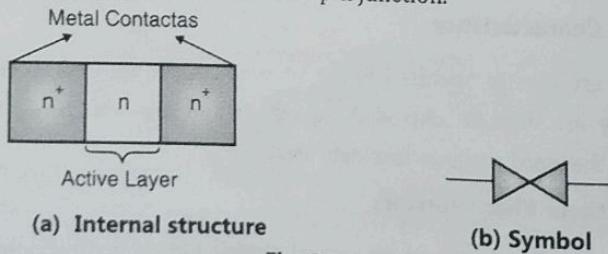


Fig. 3.6.1

3.6.3 Function of Gunn Diode

- When a DC voltage is applied to a Gunn diode especially in the central active region, it shifts the valence band to the lower valley of the conduction band.
- The associated V-I plot is shown by the graph. The current increases with voltage until reaching a certain threshold value (V_t). Beyond this point, the current decreases as shown by the curve in the graph.
- This is because, at higher voltages the electrons move into its higher valley where their mobility is low. The reduction in mobility decreases the current flowing through the diode.
- As a result, the diode exhibits a negative resistance region spanning from the Peak point to the threshold voltage. This negative resistance is due to the electron effect, and Gunn diodes are also known as negative resistance diodes.

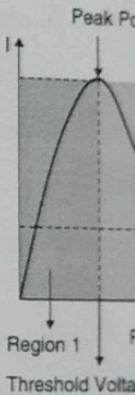


Fig. 3.6.2 : I-V characteristic of Gunn diode

3.6.4 Applications

- Gunn diodes** finds its application in microwave frequency. One such example is police speed radar gun. Police makes use of speed radar gun to calculate the speed of vehicles. Speed radar gun technology. The microwaves used here they are reflected by car or any speed limit sign. The speed is calculated and over speeding is detected.

3.6.3 Function of Gunn Diode

When a DC voltage is applied to a Gunn diode, an electric field develops across its layers, especially in the central active region. Initially, conduction increases as electrons move from the valence band to the lower valley of the conduction band.

The associated V-I plot is shown by the curve in the Region (1) of Figure 7.2. However, after reaching a certain threshold value (V_{th}), the conduction current through the Gunn diode decreases as shown by the curve in the Region 2 of the figure.

This is because, at higher voltages the electrons in the lower valley of the conduction band move into its higher valley where their mobility decreases due to an increase in their effective mass. The reduction in mobility decreases the conductivity which leads to a decrease in the current flowing through the diode.

As a result, the diode exhibits a negative resistance region in the V-I characteristic curve, spanning from the Peak point to the Valley Point. This effect is known as the transferred electron effect, and Gunn diodes are also called Transferred Electron Devices.

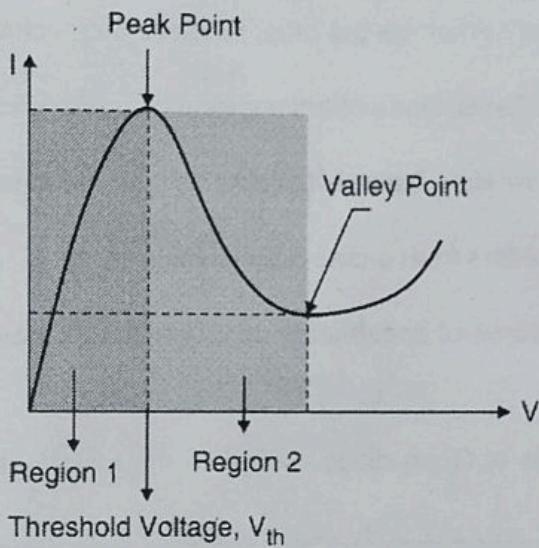


Fig. 3.6.2 : I V characteristics of Gunn Diode

3.6.4 Applications

1. Gunn diodes finds its application wherever we need microwaves of very high frequencies. One such example is police radar / speed car gun.

Police makes use of speed radar guns to detect any case of over speeding and subsequent penalties impositions. Speed radar guns use the Doppler effect that requires a lot of technology. The microwaves used here are generated by Gunn diode which once transmitted they are reflected by car or any speedy vehicles. Using Doppler effect the exact speed is calculated and over speeding is detected.

Review Questions

- Q. 1 What is "Dark current" in context with photo diode ? What is its source ?
- Q. 2 Why Photodiode is preferred in Reverse bias condition ?
- Q. 3 Explain with neat sketch I V characteristics of Photo diode.
- Q. 4 Explain the role of increasing illumination level on IV characteristics of photo diode ?
- Q. 5 Explain principle of Solar cell in detail.
- Q. 6 Write at least three points as the difference between solar cell and LED.
- Q. 7 How do you enhance the performance of Solar cell ? Explain in detail.
- Q. 8 List the challenges faced by a user of solar panel to meet the domestic needs of electricity. write possible solutions.
- Q. 9 What is Zener break down? What are the other break down mechanisms are known to you ?
- Q. 10 Explain the details how a Zener diode offers a typical characteristics in Reverse biased mode ?
- Q. 11 What is Voltage regulation? How Zener is used as voltage regulator ?
- Q. 12 How the Varactor diode differs from ordinary pn junction diode ?
- Q. 13 What are the special features of construction of Gunn diode? How it results in some meaningful application ?
- Q. 14 Explain I V characteristics of Gunn diode. Correlate the main features on IV characteristics with applications.

4

Bipolar Junction Transistors

Syllabus

BJT Structure and Operation - BJT structure, Modes of operation, CB, CE I-V characteristics
BJT Amplification and Switching - Current gain, BJT as a switch,

4.1 BJT Structure and Operation

- A Bipolar Junction Transistor (BJT) is a type of semiconductor device used for amplification and switching. It consists of three layers of semiconductor material, typically made of silicon, and is named for the two types of charge carriers it uses: *electrons* (negative charge) and *holes* (positive charge). The three layers are called the **emitter (doping level are high)**, **base (doping level are low)**, and **collector (doping level are moderate)**, and there are two types of BJTs: NPN and PNP. Their symbols are:

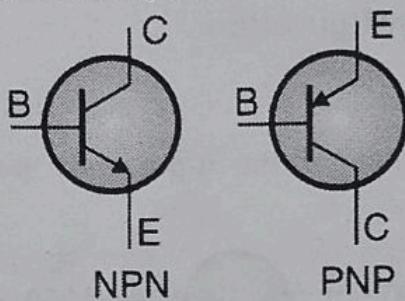


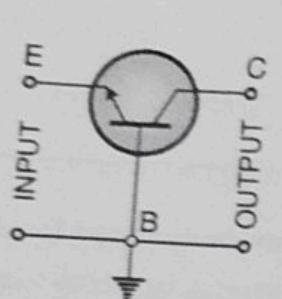
Fig. 4.1.1

- In an NPN transistor, the emitter is made of n-type material, the base is p-type, and the collector is n-type. The operation of a BJT relies on the movement of charge carriers between these regions. When a small current is applied to the base-emitter junction, it controls a much larger current flowing between the collector and emitter.

- BJTs are categorized as current-controlled devices because the current entering the base controls the current flowing between the collector and emitter.
 - Base to Emitter Junction is always Forward biased and Collector to base Junction is always Reverse biased
 - The following equation for current is useful to understand its function
- $$I_E = I_B + I_C$$
- I_B (Base Current) is of the order of micro Amperes (μA) , the reason is very simple :the base region is very small and provides very little scope for recombination of electrons and holes .
 I_C (Collector current) and I_E (Emitter Current) are of the order of mA.

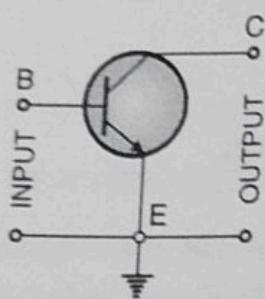
$$\text{Practically } I_C = I_E$$

4.2 Configurations of BJT



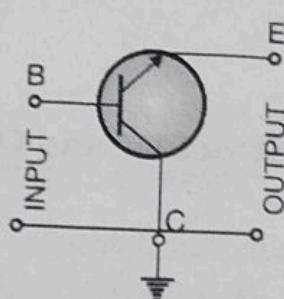
(a) Common Base Configuration

CB



(b) Common Emitter Configuration

CE



(c) Common Collector Configuration

CC

4.2.1 Common Base (CB) Configuration

Circuit diagrams

- The common base configuration for the n-p-n and p-n-p transistors is as shown in Fig. 4.2.1(a) and (b).

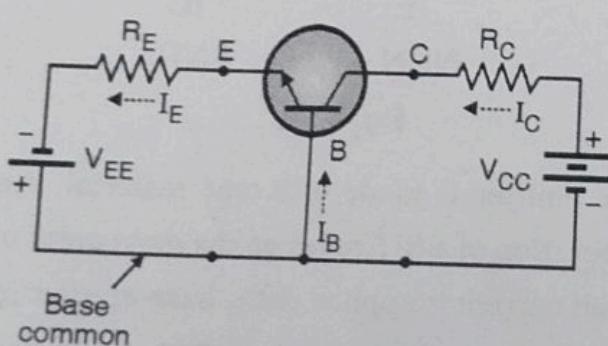


Fig. 4.2.1(a) : Common base configuration for n-p-n transistor

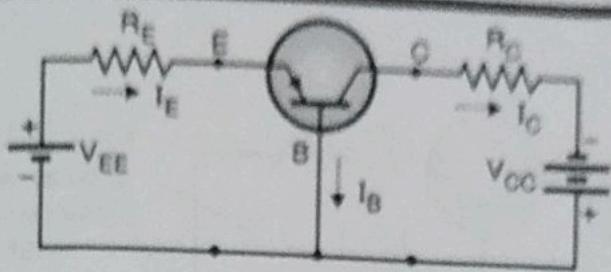


Fig. 4.2.1(b) : Common base configuration for p-n-p transistor

- The base terminal acts as a common terminal between input and output.
- The input is applied between emitter and base. The base acts as the common terminal between the input and output ports.
- The input voltage is therefore V_{EB} and the input current is I_E . The output is taken between collector and base. Therefore the output voltage is V_{CB} and the output current is I_C .

4.2.1(A) Current Relations in CB Configuration

- The collector current I_C of the common base configuration is given by,

$$I_C = I_{C(INJ)} + I_{CBO} \quad \dots(4.2.1)$$

$I_{C(INJ)}$: It is called as the injected collector current and it is due to the number of electrons crossing the collector base junction.

I_{CBO}

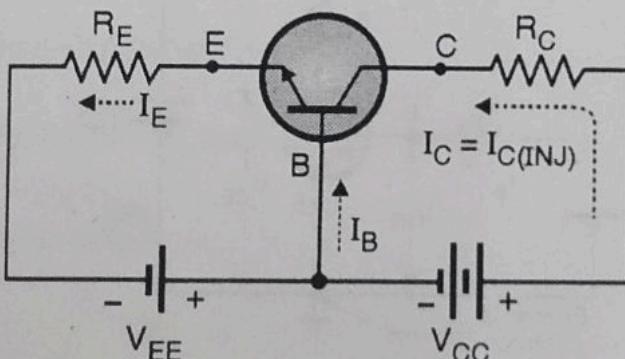
- This is the reverse saturation current flowing due to the minority carriers across the reverse biased collector and base when the emitter is open.
- I_{CBO} flows due to the reverse biased collector base junction.
- As I_{CBO} is negligible as compared to $I_{C(INJ)}$ we can neglect it in practice.

$$I_C = I_{C(INJ)} \dots \text{(practically)} \quad \dots(4.2.2)$$

$$\text{and } I_C = I_{CBO} \dots \text{(with emitter open)} \quad \dots(4.2.3)$$

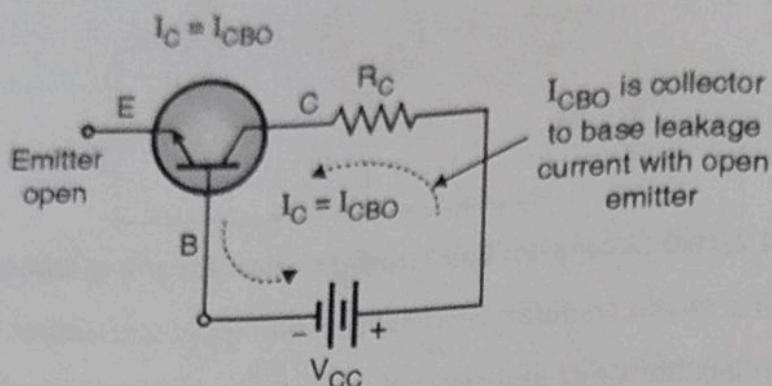
- This is shown in Fig. 4.2.2(a) and (b).

$$I_C = I_{C(INJ)}$$



(a) Normal operation

Fig. 4.2.2 : Components of collector current in CB configuration



(b) With emitter open

Fig. 4.2.2 : Components of collector current in CB configuration

4.2.1(B) Current Amplification Factor or Current Gain (α or α_{dc})

Definition : The current amplification factor or current gain of the CB configuration, is defined as the ratio of its output current (I_C) to its total input current (I_E).

- It is denoted by α_{dc} or simply by α and it is a unit less quantity.

$$\therefore \alpha_{dc} \text{ or } \alpha = \frac{I_C}{I_E} \quad \dots(4.2.4)$$

- The value of α_{dc} for CB configuration will always be less than 1. This is because $I_C < I_E$.
- Typically the value of α_{dc} ranges between 0.95 to 0.995 depending on the thickness of the base region.

4.2.2 Common Emitter (CE) Configuration

Circuit diagrams

- The common emitter configuration for the p-n-p and n-p-n transistors is as shown in Figs. 4.2.3(a) and (b).

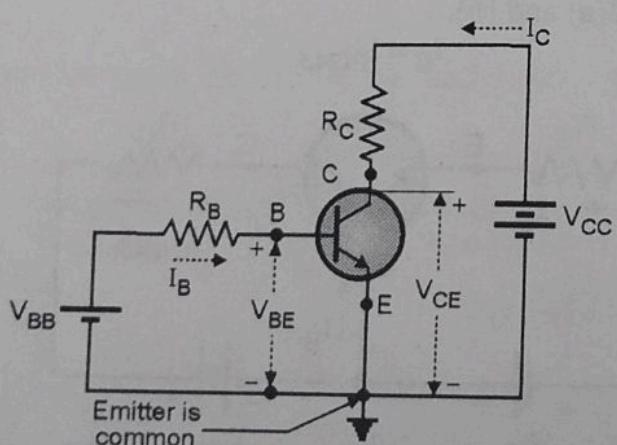


Fig. 4.2.3(a) : Common emitter configuration for n-p-n transistor

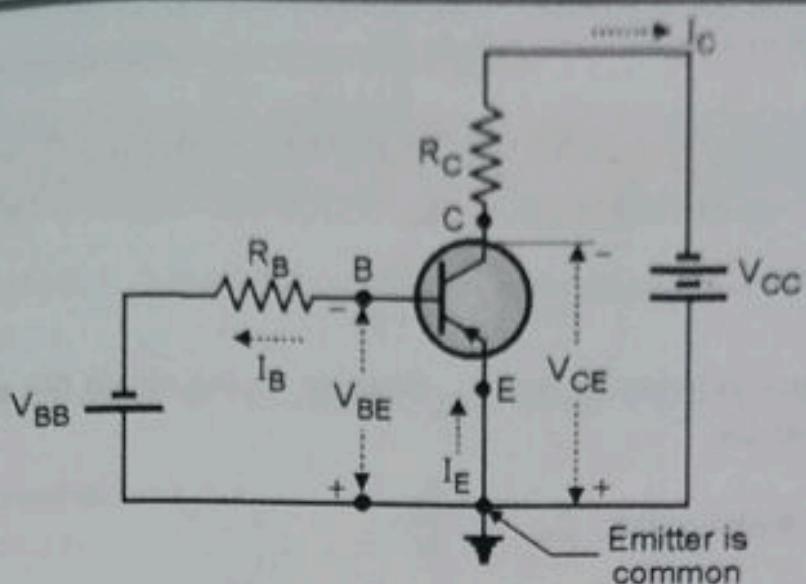


Fig. 4.2.3(b) : Common emitter configuration for p-n-p transistor

Now the emitter acts as a common terminal between input and output.

The input voltage is applied between base and emitter. Hence V_{BB} is the input voltage and I_B is the input current.

The output is taken between the collector and emitter. Therefore V_{CE} is the output voltage and I_C is the output current.

In order to operate the transistor in its active region, the base-emitter (BE) junction is forward biased and the collector-base junction is reverse biased.

4.2.2(A) Current Gain β of CE Configuration :

Definition : The current amplification factor or current gain of the CE configuration, is defined as the ratio of its output current (I_C) to its input current (I_B).

It is denoted by β_{dc} or simply by β and it is a unit less quantity.

$$\therefore \beta_{dc} \text{ or } \beta = \frac{I_C}{I_B}$$

The value of β_{dc} is much higher than α_{dc} .

4.2.2(B) Relation between α_{dc} and β_{dc}

$$\text{We know that } \alpha_{dc} = \frac{I_C}{I_E}$$

$$\text{But } I_E = I_C + I_B$$

$$\therefore \alpha_{dc} = \frac{I_C}{I_C + I_B}$$

- Divide numerator and denominator by I_B to get,

$$\alpha_{dc} = \frac{(I_C / I_B)}{1 + (I_C / I_B)}$$

$$\text{But } (I_C / I_B) = \beta_{dc}$$

$$\therefore \alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}$$

This is the relation between α_{dc} and β_{dc} . Similarly we can obtain the expression for β_{dc} in terms of α_{dc} as follows :

$$\text{We know that, } \beta_{dc} = \frac{I_C}{I_B}$$

$$\text{But } I_B = I_E - I_C$$

$$\therefore \beta_{dc} = \frac{I_C}{(I_E - I_C)}$$

- Divide numerator and denominator by I_E to get,

$$\beta_{dc} = \frac{(I_C / I_E)}{1 - (I_C / I_E)}$$

$$\text{But } (I_C / I_E) = \alpha_{dc}$$

$$\therefore \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

...(4.2.6)

- Thus the relations between α_{dc} and β_{dc} are,

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} \text{ and } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

- If $\alpha_{dc} = 0.99$ then substituting this value, we get $\beta_{dc} = \frac{0.99}{1 - 0.99} = 99$.

- Thus β_{dc} is much higher than α_{dc} .

Reverse leakage current in CE configuration (I_{CEO})

- The reverse leakage current of a transistor operating in the CE configuration is denoted by " I_{CEO} " and is defined as :

$$I_{CEO} = (1 + \beta_{dc}) I_{CBO}$$

...(4.2.7)

- As the value of β_{dc} is much greater than 1, $I_{CEO} \ggg I_{CBO}$. If $I_B = 0$ then we get,

$$I_C = (1 + \beta_{dc}) I_{CBO}$$

$$\therefore I_C = I_{CEO} \text{ for } I_B = 0$$

...(4.2.8)

- The reverse leakage current (I_{CEO}) increases with increase in the temperature.

4.2.3 Input Characteristics of CE configuration

Definition : The input characteristics is defined as the graph of input current versus input voltage at constant output voltage.

For CE configuration, I_B is the input current, V_{BE} is the input voltage and V_{CE} is the output voltage.

At constant output voltage V_{CE} the input characteristics of a n-p-n transistor is as shown in Fig. 4.2.4.

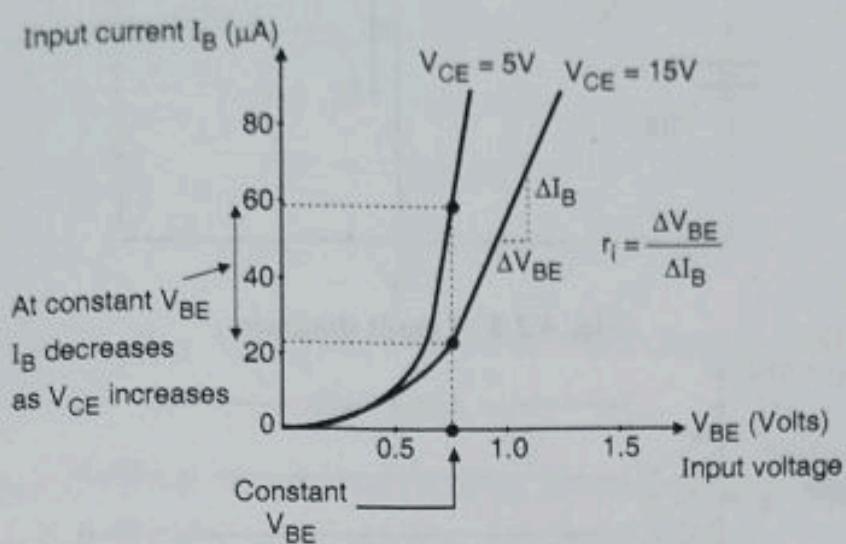


Fig. 4.2.4 : Input characteristics of a transistor in the CE configuration

The input characteristics also shows the effect of change in V_{CE} .

The input characteristics resembles the forward characteristics of a p-n junction diode. The reason is that B-E junction is a forward biased p-n junction.

Dynamic input resistance

The base current increases rapidly as the base-emitter voltage crosses the cut in voltage of the BE, p-n junction. The dynamic input resistance is defined as :

$$r_i = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE} \text{ constant}} \quad \dots(4.2.9)$$

- Its value can be obtained from the input characteristics because " r_i " is equal to the reciprocal of slope of the input characteristics.
- The value of dynamic input resistance " r_i " is low (typically $1\text{ k}\Omega$) for the CE configuration.

4.2.4 Circuit used for CE configuration and DC load line

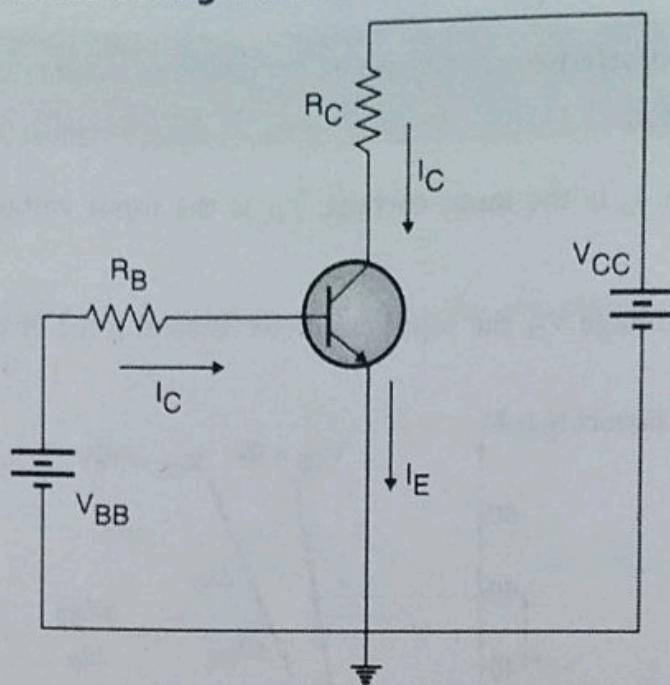


Fig. 4.2.5 : Circuit diagram

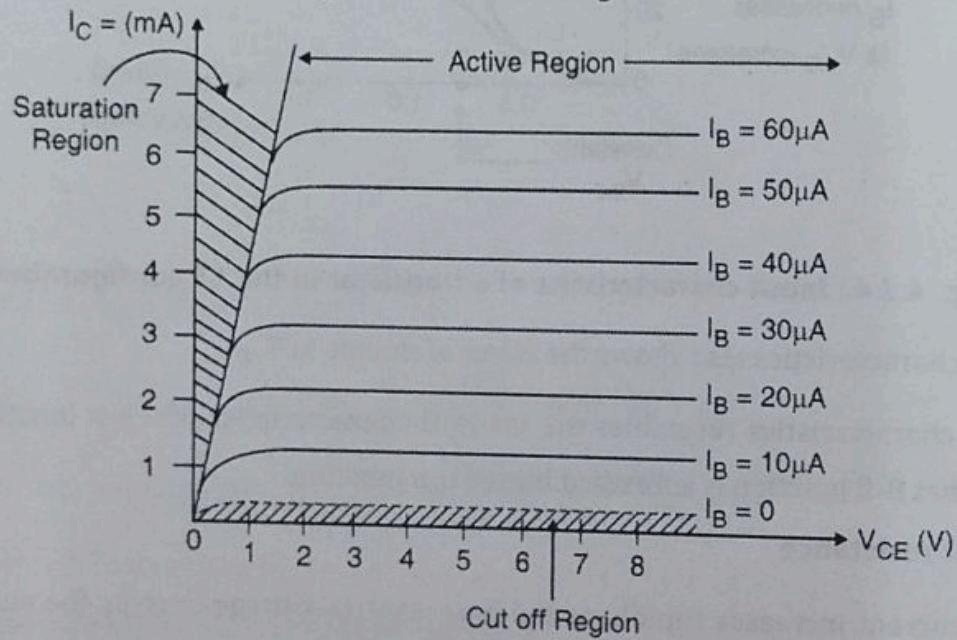


Fig. 4.2.6 : Output characteristics of CE Amplifier

Concept of DC Load line

- The DC load line of a transistor shows the relationship between the current and voltage of the circuit under consideration for a given load. The load line method is quite easy and is frequently used in the analysis of transistor applications.
- The value of collector-emitter voltage at any given time will be

$$V_{CE} = V_{CC} - I_C R_C$$

- The V_{CC} and R_C are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as D.C. Load line. The figure below show the DC load line.

- To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

- The collector emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC} / R_C . This gives the maximum value V_{CE} . This is shown as

$$V_{CE} = V_{CC} - I_C R_C$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}$$

- This gives the point A ($OA = V_{CC}/R_C$) on collector current axis shown in the Fig. 4.2.7.

To obtain B

- When the collector current $I_C = 0$, then collector emitter voltage is maximum and will be equal to the V_{CC} . This gives the maximum value of I_C . This is shown as

$$V_{CE} = V_{CC} - I_C R_C = V_{CC}$$

(As $I_C = 0$)

- This gives the point B, which means ($OB = V_{CC}$) on the collector emitter voltage axis shown in the above figure.
- Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

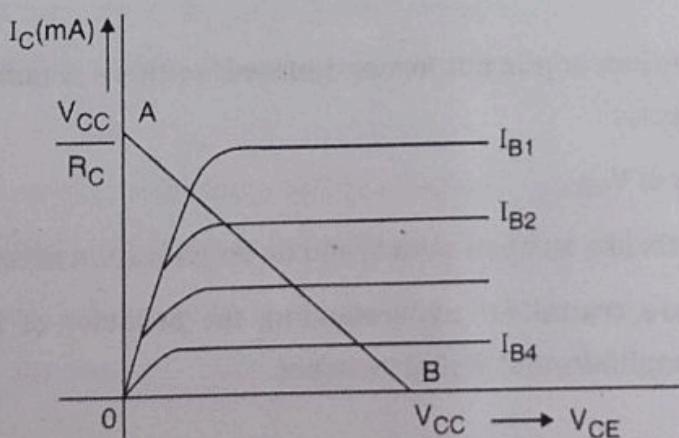


Fig. 4.2.7 : DC load line

4.3 Various Regions of Operations on Output Characteristics

The output characteristics of a **Common Emitter (CE)** configuration for a Bipolar Junction Transistor (BJT) typically show the relationship between the **collector current (I_C)** and the **collector-emitter voltage (V_{CE})** for different values of **base current (I_B)**. These characteristics are crucial for understanding how a BJT behaves in amplification and switching applications. The output characteristics are divided into three main regions:

1. Active Region (or Linear Region)

- In this region, the transistor is **on** and behaves as an amplifier.
- The **collector current (I_C)** is primarily controlled by the **base current (I_B)**, and V_{CE} is high enough (greater than the threshold voltage) to keep the transistor in active mode.
- The collector current increases with an increase in I_B , but for a fixed I_B , I_C remains nearly constant as V_{CE} increases.

2. Saturation Region

- In this region, the transistor is fully "on" and acts as a **switch**.
- The collector-emitter voltage V_{CE} is very low (close to zero) while the collector current is large but relatively insensitive to V_{CE} .
- In saturation, the transistor can no longer amplify, and both the collector-emitter junction and the base-emitter junction are forward-biased.
- The transistor is considered "saturated," and any further increase in I_B does not significantly increase I_C .

3. Cutoff Region

- In this region, the transistor is **off**, and no current flows between the collector and emitter.
- The base-emitter junction is not forward-biased, so there is minimal or no current flow through the collector.
- $I_C \approx 0$ regardless of V_{CE} .
- The transistor acts like an open switch, and no amplification occurs.
- These regions are crucial for understanding the behavior of BJTs in analog circuits, particularly in amplifiers and digital switches.

4.4 BJT Acts as Switch

- A Bipolar Junction Transistor (BJT) can operate in two modes: **saturation** (switch "on") and **cutoff** (switch "off").
- Let us explore it further

1. Cutoff Region (Switch Off)

- In this state, the transistor is **off**, and no current flows from the **base** to the **emitter**.
- For the BJT to be in cutoff, the base-emitter voltage, V_{BE} , must be negative (i.e., the base-emitter voltage, V_{BE} , is negative for NPN silicon BJTs).
- In this condition, the base current (I_B) is zero, and no current flows from the **base** to the **emitter**.
- The BJT behaves like an **open switch** because the collector current is zero, and the device does not conduct.

Conditions for Cutoff

$$V_{BE} < 0$$

$$I_B \approx 0$$

2. Saturation Region (Switch On)

- In this state, the transistor is fully **on**, and a large current flows from the **base** to the **emitter**.
- To drive the BJT into saturation, the base-emitter voltage must be positive ($V_{BE} > 0.7V$), and there must be enough **base current (I_B)**.
- When in saturation, the collector-emitter voltage is very low, around **0.2V or lower**, and the transistor acts like a closed switch.
- In this region, the BJT is said to be in **saturation** because the collector current does not significantly increase the collector-emitter voltage.

4.4

BJT Acts as Switch

- A Bipolar Junction Transistor (BJT) can function as a **switch** by operating in two distinct modes: **saturation** (switch "on") and **cutoff** (switch "off"). Refer 4.4.1 above
- Let us explore it further

1. Cutoff Region (Switch Off)

- In this state, the transistor is **off**, and no current flows between the **collector** and **emitter**.
- For the BJT to be in cutoff, the **base-emitter junction** must be **not forward-biased** (i.e., the base-emitter voltage, V_{BE} , is less than the threshold voltage, typically 0.7V for silicon BJTs).
- In this condition, the base current (I_B) is essentially zero, and consequently, no current flows from the **collector** to the **emitter**.
- The BJT behaves like an **open switch** in this state. The collector-emitter voltage (V_{CE}) is high, and the device does not conduct current.

Conditions for Cutoff

$$V_{BE} < 0.7V \text{ (for silicon BJTs).}$$

$$I_B \approx 0.$$

2. Saturation Region (Switch On)

- In this state, the transistor is **fully on**, allowing maximum current to flow from the **collector** to the **emitter**.
- To drive the BJT into saturation, the **base-emitter junction** must be **forward-biased** ($V_{BE} > 0.7V$), and there must be enough **base current (I_B)** to allow a large **Collector current (I_C)**.
- When in saturation, the **collector-emitter voltage (V_{CE})** drops to a low value, typically around **0.2V or lower**, and the transistor behaves like a **closed switch**.
- In this region, the BJT is said to be in **saturation**, where increasing the base current does not significantly increase the collector current because the transistor is already "fully on".

Conditions for Saturation

- $V_{BE} > 0.7V$ (for silicon BJTs).
- I_B is sufficient to support the required I_C , but not excessive.
- V_{CE} drops to a small value (typically $< 0.3V$), and the transistor can conduct a large current from the collector to the emitter.

How it works as a switch

- When you apply a small **base current (I_B)** to a BJT in the **cutoff region**, the transistor "turns on" and enters saturation, allowing a large **collector current (I_C)** to flow from the collector to the **emitter** (acting as a **closed switch**).
- Conversely, when you **remove the base current**, the transistor enters the **cutoff region**, stopping current flow from the collector to the emitter (acting as an **open switch**).

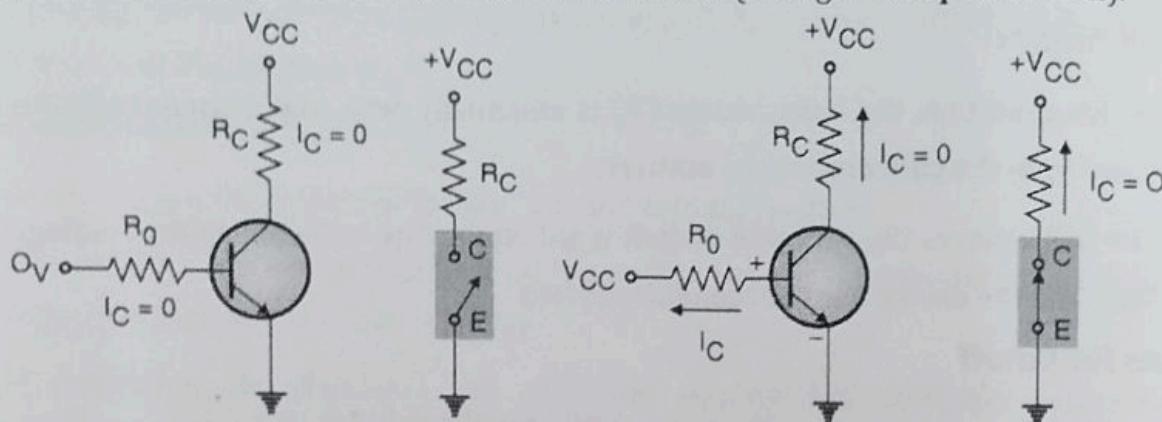


Fig. 4.4.1 : BJT as switch

4.5 Problems

Ex. 4.5.1 : For a transistor, $\alpha = 0.95$ and $I_E = 1 \text{ mA}$, find I_C and I_B .

Soln. :

$$I_C = \alpha I_E = 0.95 \times 1 = 0.95 \text{ mA}$$

$$I_B = I_E - I_C = 1 - 0.95 = 0.05 \text{ mA}$$

Ex. 4.5.2 : Following current readings are obtained in transistor circuit : $I_E = 2 \text{ mA}$ and $I_B = 20 \mu\text{A}$ and $I_C = 20 \mu\text{A}$. Compute value of α and I_C .

Soln. :

$$I_E = I_B + I_C$$

$$\therefore I_C = I_E - I_B$$

$$= 2 \times 10^{-3} - 20 \times 10^{-6}$$

$$I_C = 1.98 \text{ mA}$$

$$\alpha = \frac{I_C}{I_E} = \frac{1.98}{2}$$

$$= 0.99$$

Ex. 4.5.3 : For the given circuit.

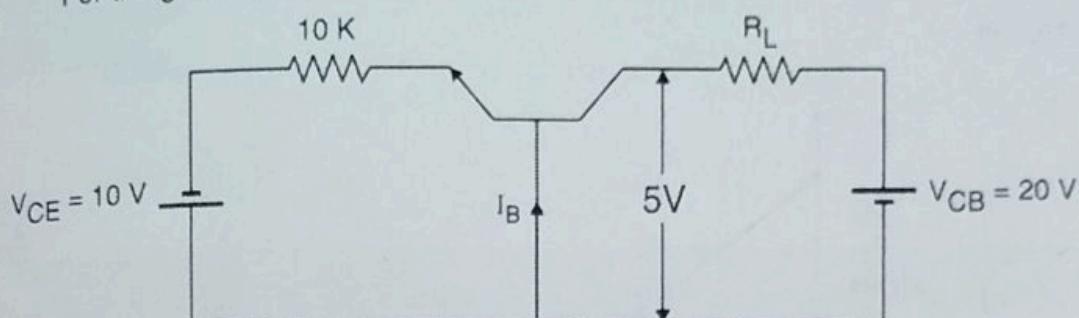


Fig. P. 4.5.3

Find R_L

Soln.:

$$I_E = \frac{V_{EE}}{R_E} = \frac{10V}{10\text{ k}\Omega} = 1 \text{ mA}$$

$$I_C = \alpha I_E \approx I_E \\ = 1 \text{ mA}$$

$$\therefore V_{CC} = I_C R_L + V_{CB}$$

$$\therefore R_L = \frac{V_{CC} - V_{CB}}{I_C} = \frac{20 - 5}{1 \times 10^{-3}} \text{ }\Omega$$

$$\therefore R_L = 15 \text{ k}\Omega \quad \dots \text{Ans.}$$

Ex. 4.5.4 : For the CE configuration in figure below draw the dc load line Assume : $\beta = 100$ neglect V_{BE} .

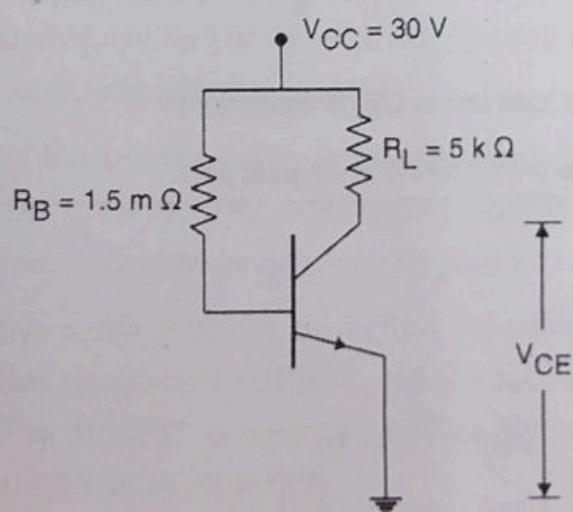


Fig. P. 4.5.4(a)

Soln. :

1. When $I_C, V_{CE} = V_{CC} = 30 \text{ V}$
2. When $V_{CE} = 0, I_C = \frac{V_{CC}}{R_L} = \frac{30}{5 \times 10^3} = 6 \text{ mA}$

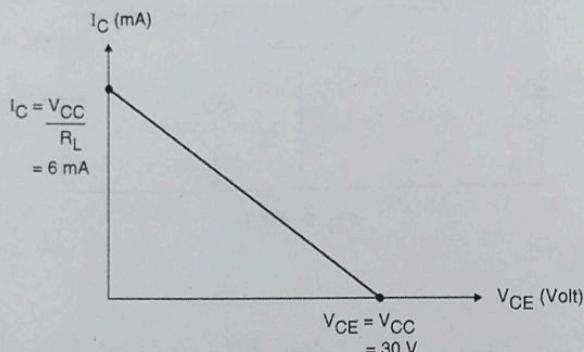
 \therefore dc load line

Fig. P. 4.5.4(b)

Review Questions

- Q. 1** Explain types of Transistors.
- Q. 2** Explain various configurations of transistors. Draw the circuit diagram for each
- Q. 3** Explain physics of transistors for CB configuration
- Q. 4** Draw a circuit used for CE configuration of BJT. Draw its input and output Characteristics
- Q. 5** On output characteristics of BJT in Ce configuration, draw various region of operation. Describe their significance.
- Q. 6** What is the concept of dc load line in CE configurations?
- Q. 7** Explain the use of BJT as switch for CE configurations.

**Field E****Syllabus**

Field-Effect Transistors (FETs) - FET types: J in Detail - MOSFET structure, Enhancement MOSFET Applications - MOSFET as a switch

5.1 Introduction

- A Field-Effect Transistor (FET) is a type of transistor which controls the flow of current. FETs are widely used in electronic circuits.
- The structure of a typical FET consists of three terminals connected together to control the flow of charge carriers through a channel. The field-effect transistor (FET) has three terminals: gate (G), source (S) and Drain (D).
- The FET is voltage controlled device. Just like diodes, there are n-channel and p-channel field effect transistors.
- The term field effect in the name deserves its name because it is controlled by the electric field established by the charges present, which does not require physical contact between the gate and the channel.
- FETs are of three types : the junction field-effect transistor (JFET), the metal-semiconductor field-effect transistor (MOSFET) and the metal-oxide-semiconductor field-effect transistor (MESFET). The MOSFET can be enhancement mode or depletion mode (i.e. D-MOSFET and E-MOSFET).

5

Field Effect Transistor

Syllabus

Field-Effect Transistors (FETs) - FET types: JFET, MOSFET, Structure and operation MOSFETs in Detail - MOSFET structure, Enhancement and depletion modes, Threshold voltage
MOSFET Applications - MOSFET as a switch.

5.1 Introduction

- A **Field-Effect Transistor (FET)** is a type of transistor that uses an electric field to control the flow of current. FETs are widely used in electronics for amplifying or switching electronic signals.
- The structure of a typical FET consists of several key regions and components that work together to control the flow of charge carriers (electrons or holes) through a semiconductor channel. The field-effect transistor (FET) is a three-terminal device. The three terminals are gate (G), source(S) and Drain (D).
- The FET is voltage controlled device. Just as there are npn and pnp bipolar transistors, there are n-channel and p-channel field effect transistors.
- The term field effect in the name deserves some explanation. For the FET an electric field is established by the charges present, which controls the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.
- FETs are of three types : the junction field-effect transistor (JFET), the metal-oxide-semiconductor field-effect transistor (MOSFET), and the metal - semiconductor field-effect transistor (MESFET). The MOSFET category is further broken down into depletion and enhancement (i.e. D-MOSFET and E=MOSFET).

Difference between BJT and FET

BJT	FET
Current controlled device	Voltage controlled device
Bipolar (current conduction due to flow of Holes and electrons)	Unipolar (current conduction due to flow of Majority charge carriers)
Low input impedance as compared to FET	High input impedance
Less temperatures stable	More temperature stable
Larger in size	Smaller in size

Types of FETs

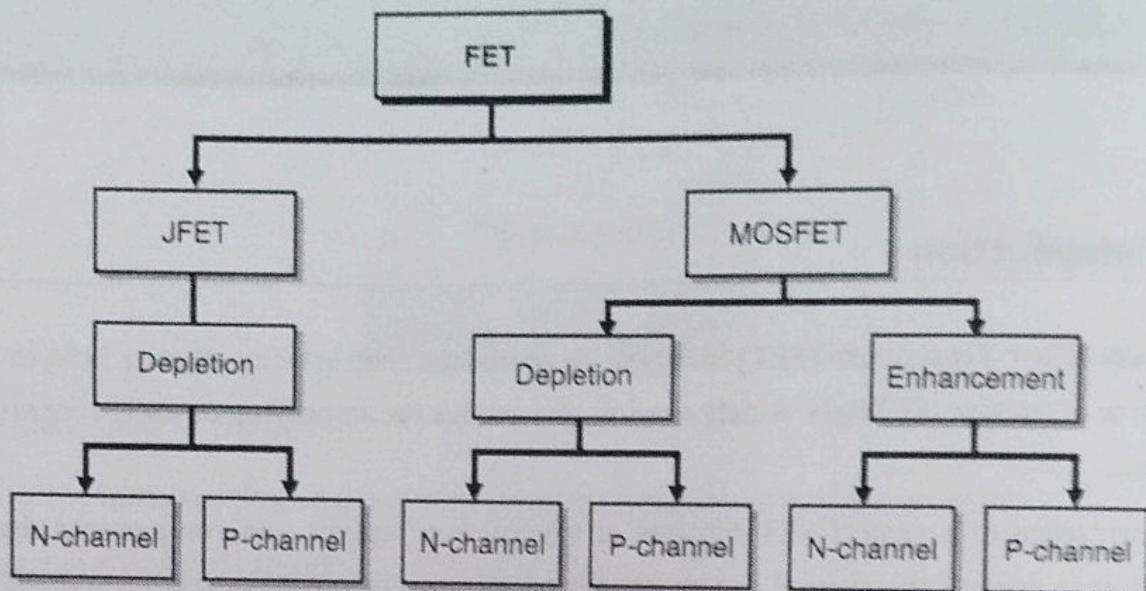


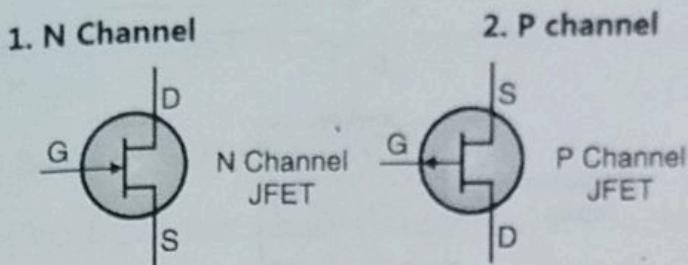
Fig. 5.1.1

5.2 Basic Operating Principle of JFET

This electric-field-based control allows FETs to act as voltage-controlled resistors, where the resistance of the channel can be adjusted depending on the gate voltage.

- A Junction Field-Effect Transistor (JFET) is a type of FET where the flow of current through the channel is controlled by a reverse-biased p-n junction. JFETs are normally normally-on devices, meaning they allow current to flow through the channel (from source to drain) when the gate-source voltage (V_{GS}) is 0V or negative (in an n-channel JFET, for example). The gate controls the current by depleting the channel of charge carriers as the reverse-bias voltage increases.

Types of JFET



5.2.1 Structure of JFET

- Source (S)** : The region where current enters the device. It is connected to the source terminal.
- Drain (D)** : The region where current exits the device. It is connected to the drain terminal.
- Channel** : The region between the source and drain that allows current to flow when it is conductive. In the case of an n-channel JFET, it consists of n-type semiconductor material.
- Gate (G)** : The controlling terminal. It is connected to a p-type semiconductor region that forms a reverse-biased p-n junction with the channel. This reverse-bias voltage controls the size of the conductive channel.
- Gate-Source Voltage (VGS)** : The voltage applied between the gate and the source. The gate is typically reverse-biased to control the channel conductivity.

5.2.2 Physics of JFET Operation

In an **n-channel JFET**:

- In a FET, the current flowing between the source and the drain is carried by charge carriers (electrons in an n-channel FET or holes in a p-channel FET).
- The channel's conductivity is controlled by the voltage applied to the gate. In an n-channel FET, a positive gate voltage attracts electrons to the channel, making it more conductive. Conversely, in a p-channel FET, a negative gate voltage attracts holes, increasing the conductivity.
- The gate is made of p-type material. When a **reverse bias** is applied between the **gate** and the **channel** (i.e., a negative voltage on the gate relative to the source), it causes the p-n junction to become more reverse-biased.

Here's how the reverse bias affects the channel :

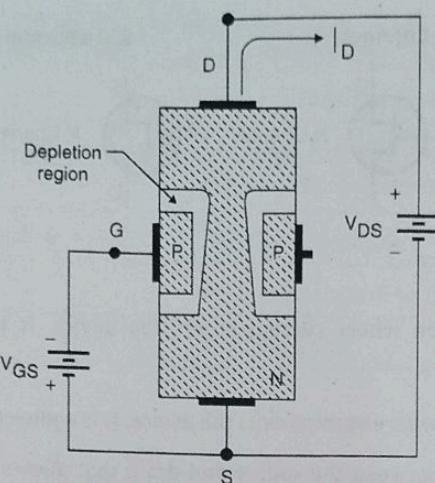


Fig. 5.2.1 : JFET Structure

- Depletion Region :** As the reverse-bias voltage increases, the **depletion region** of the p-n junction widens. This depletes the channel of free charge carriers (electrons in the case of an n-channel JFET).
- Reduced Channel Conductivity :** The widening of the depletion region reduces the effective width of the conductive channel, thereby restricting the flow of current from the **source** to the **drain**.
- Pinch-off :** When the reverse-bias voltage becomes large enough, the depletion regions from both sides of the gate may extend and meet, effectively **pinching off** the channel. At this point, no current can flow between the source and drain, and the JFET is in the **off state**.

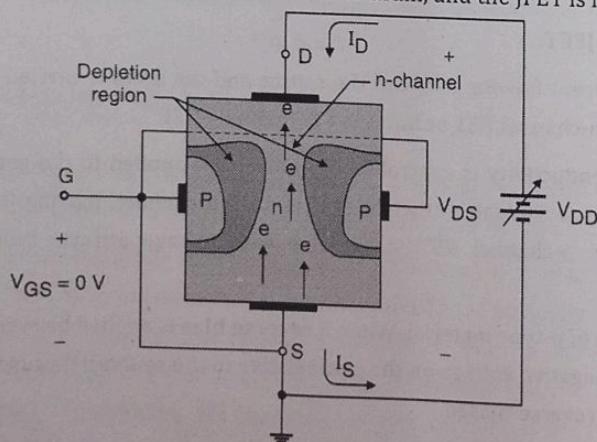


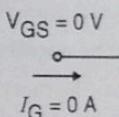
Fig. 5.2.2 : JFET at $V_{GS}=0\text{ V}$ and $V_{DS} > 0\text{ V}$

5.2.3 Operation Modes

The JFET can operate in three distinct drain-source voltage (V_{DS}) :

1. Ohmic or Linear Region (Active Region)

- Condition :** When V_{GS} is less than $V_{GS(\text{th})}$.
- In this region, the JFET behavior is similar to a resistor, where the drain current increases linearly with V_{DS} .
- The channel is wide enough for V_{DS} to be negative, the channel narrows.



$V_{GS} = 0\text{ V}$
 $I_G = 0\text{ A}$

Fig. 5.2.3 : Varying reverse-bias position

2. Saturation (or Pinch-Off) Region

- Condition :** When V_{GS} is sufficiently large enough to cause the channel to pinch off.
- Saturation :** In this region, the drain current is controlled more by the drain voltage V_{DS} but rather on V_{GS} . The transistor is said to be in saturation.
- Pinch-Off :** At the pinch-off point ($V_{GS(\text{th})}$), and any further increase in V_{DS} will not increase I_D .

5.2.3 Operation Modes

The JFET can operate in three distinct regions depending on the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}):

1. Ohmic or Linear Region (Active Mode)

- Condition :** When V_{GS} is less negative (but still in reverse bias), and V_{DS} is small.
- In this region, the JFET behaves like a variable resistor. As V_{DS} increases, the current increases, but the current is controlled by the gate voltage.
- The channel is wide enough for current to flow, but as the gate voltage becomes more negative, the channel narrows.

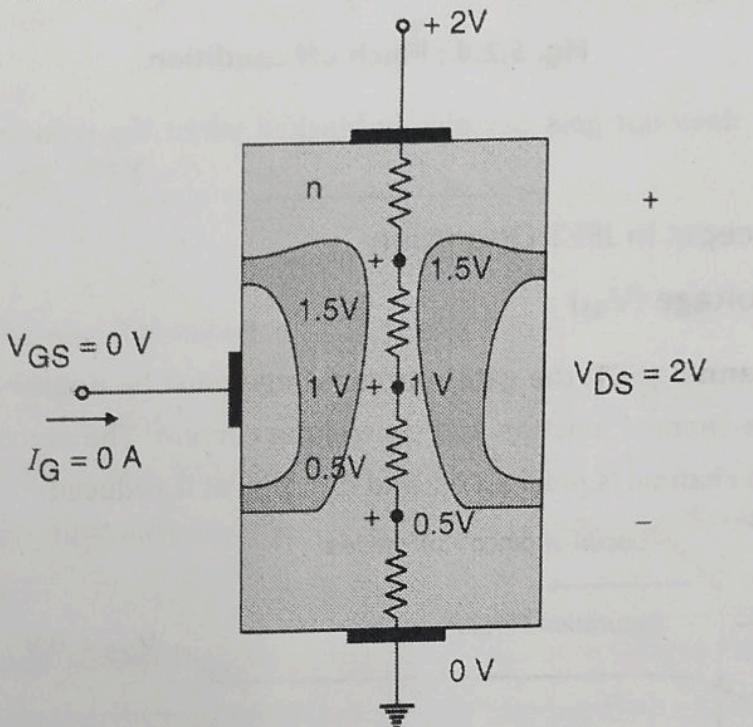


Fig. 5.2.3 : Varying reverse-bias potential across the p-n junction of an n-channel JFET

2. Saturation (or Pinch-Off) Region

- Condition :** When V_{GS} is sufficiently negative (creating a large reverse bias) and V_{DS} is large enough to cause the channel to pinch off.
- Saturation :** In this region, the current becomes almost constant and no longer depends on V_{DS} but rather on V_{GS} . The current is controlled by the gate voltage, and the transistor is said to be in saturation.
- Pinch-Off :** At the pinch-off point, the current through the JFET is at its maximum (for a given V_{GS}), and any further increase in V_{DS} does not significantly increase the current.

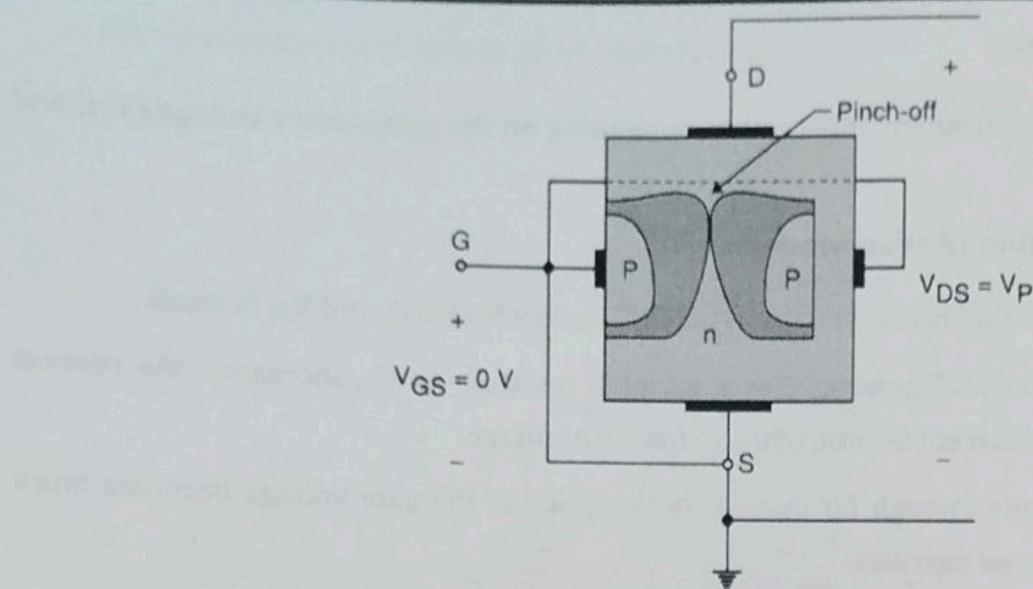


Fig. 5.2.4 : Pinch off condition

Why the channel does not gets completely blocked when V_{DS} is increased further Pinch off Voltage ?

3. Important Concepts in JFET Operation

Gate-Source Voltage (V_{GS}) :

- For an n-channel JFET, the gate-source voltage must be negative ($V_{GS} < 0$) to reverse-bias the gate-channel junction and control the current. The more negative V_{GS} becomes, the more the channel is pinched off, and the current is reduced.

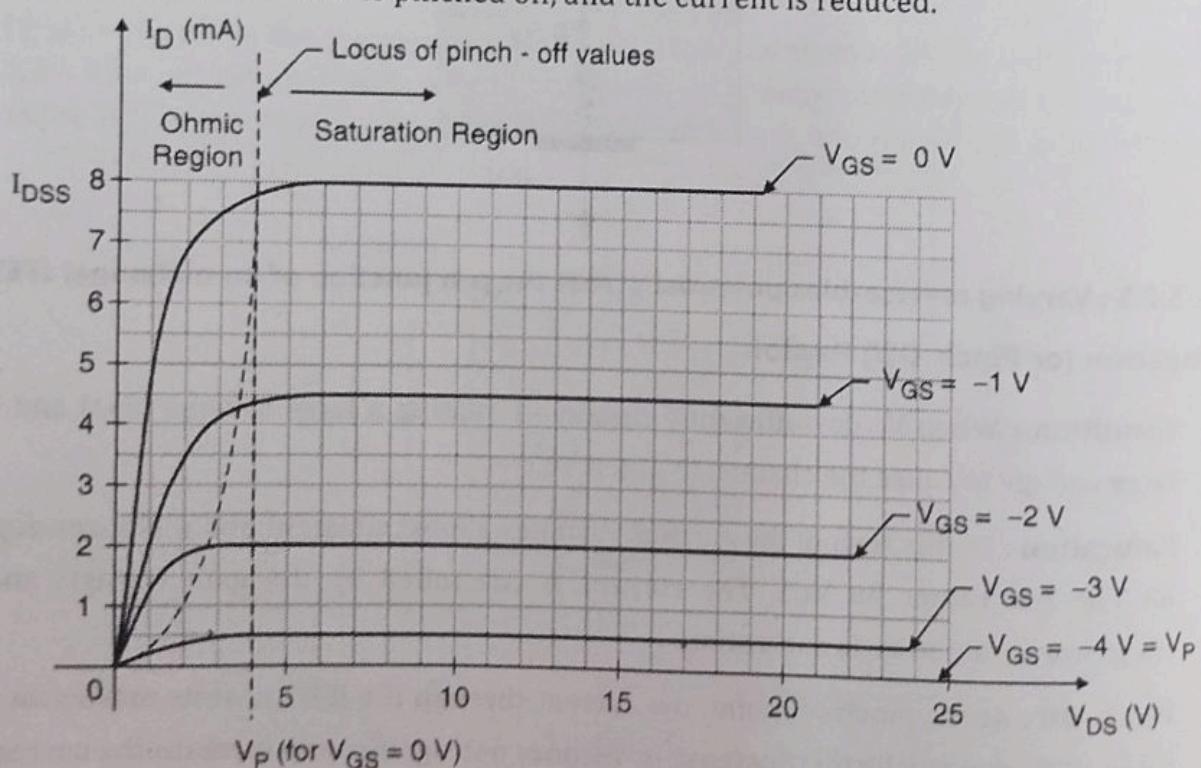


Fig. 5.2.5

Drain-Source Voltage (V_{DS})

- The drain-source voltage must be positive for current to flow from the source to the drain in an n-channel JFET.
- If V_{DS} is too large, the channel will eventually pinch off (saturation region).

Transfer Characteristics

- The transfer characteristic curve (I_D vs. V_{GS}) shows how the drain current (I_D) varies with gate-source voltage (V_{GS}) at a constant V_{DS} .
- For small values of V_{GS} (more negative), the current decreases as the channel becomes depleted. For larger negative values of V_{GS} , the current becomes almost zero. (cutoff region).

5.3 Application of JFET

JFET as Switch

Operation Modes (Switching Behavior):

- "On" State (Conducting) : When the gate-source voltage (V_{GS}) is zero or positive (in an n-channel JFET), the JFET is "on," and current can flow from the source to the drain. This occurs because the depletion region around the gate is narrow enough to allow current flow through the channel.
- "Off" State (Non-Conducting) : When a negative gate-source voltage (V_{GS}) is applied (in an n-channel JFET), it expands the depletion region, narrowing the conductive channel to the point where it blocks current flow. In this state, the JFET behaves like an open switch, preventing current from flowing from the source to the drain.

JFET as a Switch in Practice

- "On" condition : To turn the JFET on, you apply a small (typically zero or slightly positive) voltage to the gate. The channel is conductive, allowing current to flow from source to drain.
- "Off" condition : To turn the JFET off, you apply a negative voltage to the gate, which creates a wide depletion region that blocks the current flow.

JFETs are often used in analog switches, low-power switches, and in circuits where low noise and high input impedance are critical (such as sensor interfaces, audio amplifiers, etc.).

5.4 MOSFET or IGFET

MOSFET stands for Metal - Oxide - Semiconductor Field - Effect Transistor. Or IGFET (Insulated Gate Field Effect Transistor)

MOSFETs are further divided in to two types :

- (1) Depletion type and (D- MOSFET)
- (2) Enhancement type. (E - MOSFET)

The terms depletion and enhancement define their basic mode of operation.

5.4.1 Depletion-type MOSFET (D-MOSFET)

Basic Construction

The basic construction of then-channel depletion-type MOSFET is provided in Fig.5.4.1. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation on which the device is constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labeled *SS*, resulting in a four-terminal device. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a type of insulator referred to as a *dielectric*, which sets up opposing (as indicated by the prefix *di*-) electric fields within the dielectric when exposed to an externally applied field. The fact that the SiO_2 layer is an insulating layer means that:

There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

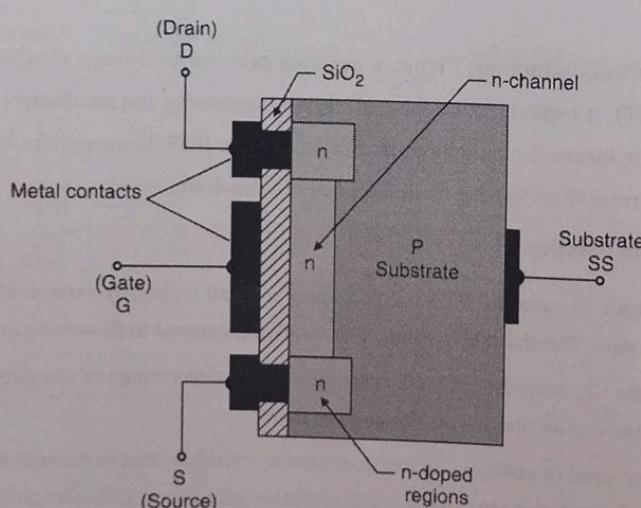


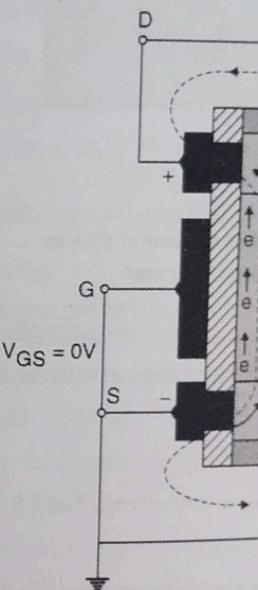
Fig. 5.4.1 : n-Channel depletion type MOSFET

In addition: It is the insulating layer very desirable high input impedance of t

The reason for the label metal-oxide drain, source, and gate connections; semiconductor for the basic structure on

Basic Operation and Characteristics

In Fig. 5.4.2 , the gate-to-source v terminal to the other ,and a voltage V_{DD} is an attraction of the free electrons of result is a current similar to that flowing with $V_{GS} = 0 \text{ V}$ continues to be labeled I_D



In Fig.5.4.2, V_{GS} is set at a negative vo tend to pressure electrons toward the *p*-type the *p*-type substrate (opposite charges magnitude of the negative bias established b and holes will occur that will reduce the nu conduction. The more negative the bias, the h

In addition: It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections; *oxide* for the silicon dioxide insulating layer; and *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused.

Basic Operation and Characteristics

In Fig. 5.4.2, the gate-to-source voltage is set to 0 V by the direct connection from one terminal to the other, and a voltage V_{DD} is applied across the drain-to-source terminals. The result is an attraction of the free electrons of the *n*-channel for the positive voltage at the drain. The result is a current similar to that flowing in the channel of the JFET. In fact, the resulting current with $V_{GS} = 0$ V continues to be labeled I_{DSS} , as shown in Fig. 5.4.2

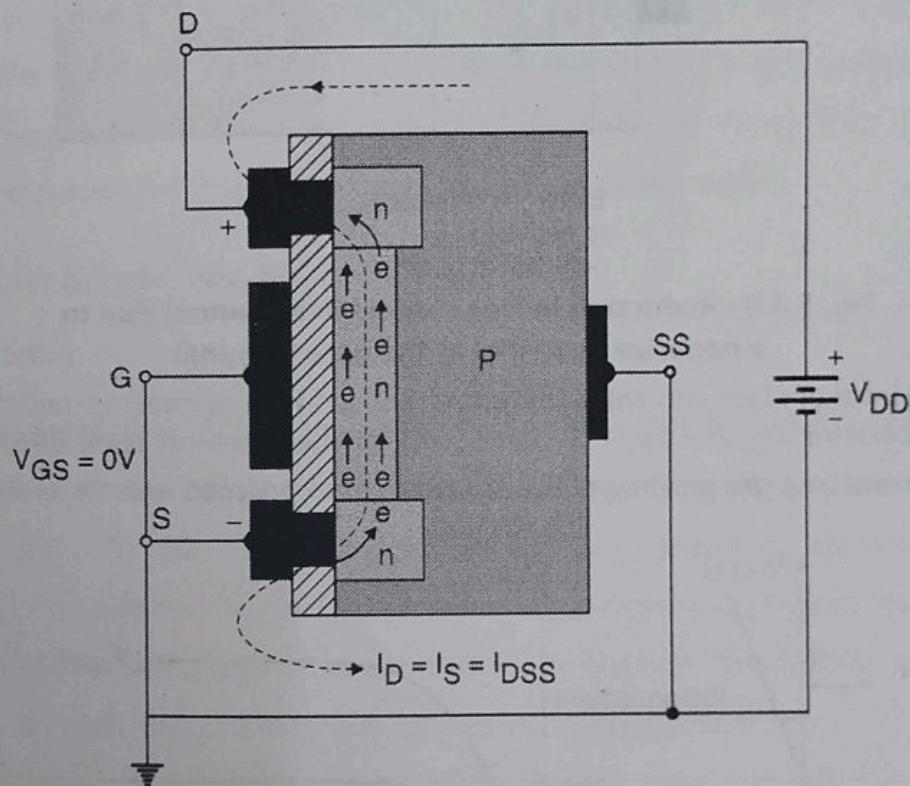


Fig. 5.4.2

In Fig. 5.4.2, V_{GS} is set at a negative voltage such as -1V. The negative potential the gate will tend to pressure electrons toward the *p*-type substrate (like charges repel) and attract holes from the *p*-type substrate (opposite charges attract) as shown in Fig. 5.4.2. Depending on the magnitude of the negative bias established by V_{GS} , a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher is the rate of recombination.

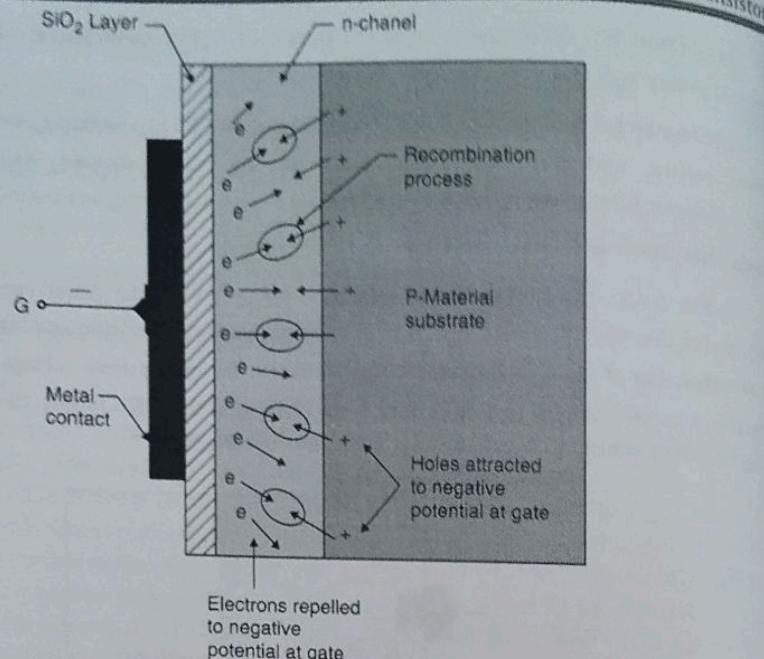


Fig. 5.4.3 : Reduction in free carriers in a channel due to a negative potential at the gate terminal

The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} , as shown in Fig.5.4.3 for $V_{GS} = -1V$, $-2V$, and soon, to the pinch-off level of $-6V$. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

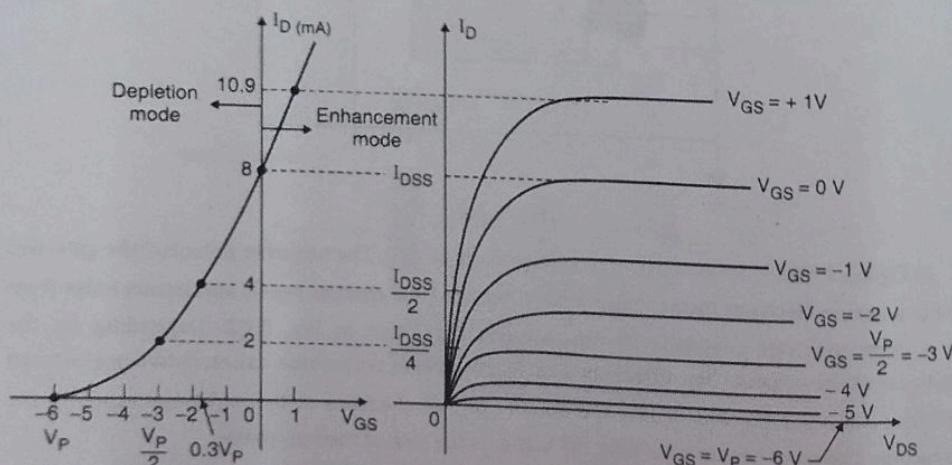


Fig. 5.4.4 : Drain and transfer characteristics for an n-channel depletion type MOSFET

For positive values of V_{GS} , the positive gate will draw electrons from the p-type substrate due to the reverse leakage. The collisions resulting between accelerating particle increase in the positive direction, Fig.5.4.4 reveals the rate for the reasons listed above. The vertical spacing of Fig.5.4.4 is a clear indication of how much the current can be exceeded with a positive gate voltage. That is, for a voltage $V_{GS} = +4 V$ would result in a drain current maximum rating (current or power) for the device. A gate-to-source voltage has "enhanced" the level of current encountered with $V_{GS}= 0 V$. For this reason the transfer characteristics is often referred to as the enhancement cutoff and the saturation level of I_{DSS} referred to as the saturation current.

5.4.2 Enhancement-Type MOSFET

Basic Construction

- The basic construction of the n-channel enhancement-type MOSFET is similar to that of the depletion-type MOSFET. As lab of p-type material is formed from a n-type substrate. As with the depletion-type MOSFET, it is connected to the source terminal, where as in the enhancement-type MOSFET, it is available for external control of its potential level. It is connected through metallic contacts to an n-doped channel between the two n-doped regions. The construction of depletion-type and enhancement-type is a constructed component of the device. The enhancement-type MOSFET is quite similar to the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

For positive values of V_{GS} , the positive gate will draw additional electrons (free carriers) from the p -type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 5.4.4 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 5.4.4 is a clear indication of how much the current has increased for the 1-V change in V_{GS} . Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 5.4.4, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of $IDSS$ referred to as the *depletion region*.

5.4.2 Enhancement-Type MOSFET

Basic Construction

- The basic construction of the n -channel enhancement-type MOSFET is provided in Fig. 5.4.5. As a slab of p -type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, whereas in other cases a fourth lead (labelled SS) is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to n -doped regions, but in Fig. 5.4.5 the absence of a channel between the two n -doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p -type material. Therefore, we can say that the construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.

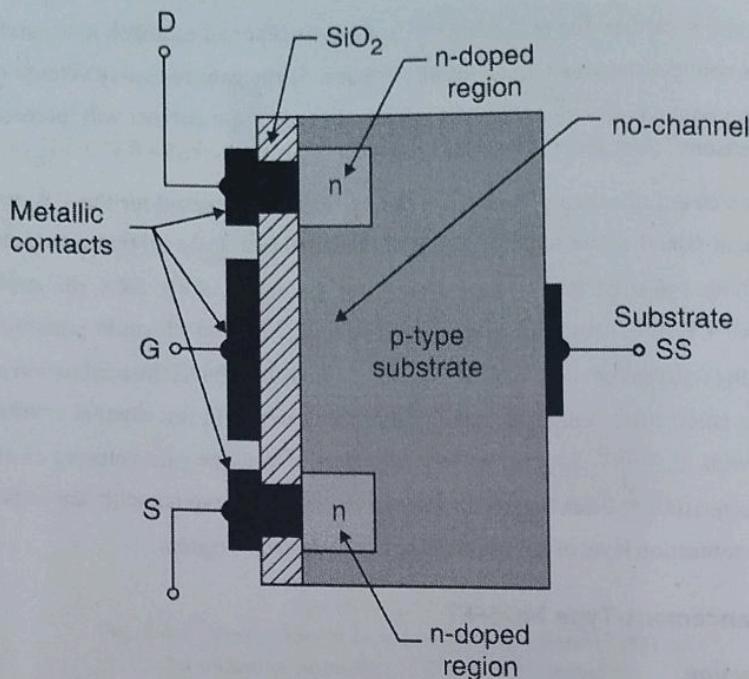


Fig. 5.4.5 : n-Channel enhancement-type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0V and a voltage applied between the drain and the source of the device of Fig. 5.4.5, the absence of an n -channel (with its generous number of free carriers) will result in a current of effectively 0 A, whereas in case of JFET and MOSFET $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and the source (due to the n doped regions) if a path fails to exist between the two. With V_D some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased $p - n$ junctions between the n -doped regions and the p -substrate to oppose any significant flow between drain and source.

In Fig. 5.4.6, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.

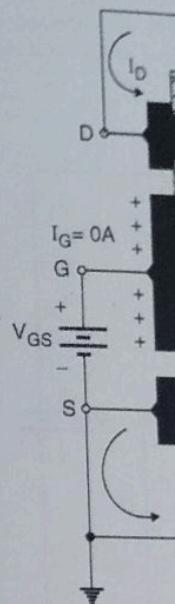
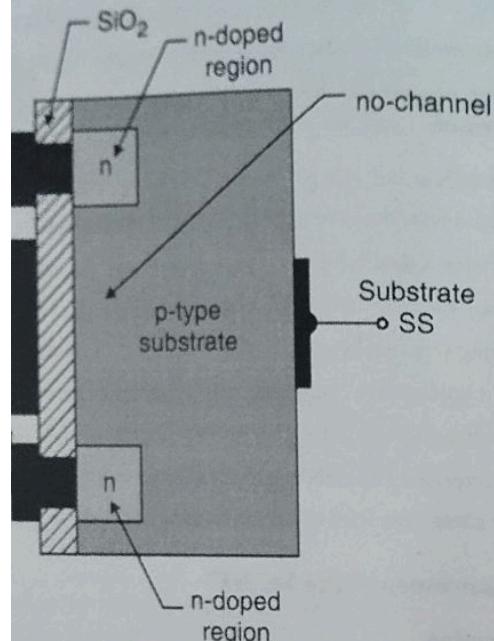


Fig. 5.4.6 : Channel formation

The positive potential at the gate with respect to the substrate along the edge of the SiO_2 substrate, as shown in the figure, creates a region void of holes. However, the electrons can be attracted to the positive gate area. The SiO_2 layer and its insulating qualities increase as V_{GS} increases. The SiO_2 surface increases until eventually it becomes conductive between drain and source. The level at which the SiO_2 becomes conductive is called the *threshold voltage* and is denoted as $V_{GS}(\text{Th})$, although VT is less frequently used. The channel is non-existent with $V_{GS} < VT$. At a certain source voltage, this type of MOSFET begins to operate in the enhancement-mode. The latter since it is its only mode of operation.



n-Channel enhancement-type MOSFET

stics

age applied between the drain and the source of the device of channel (with its generous number of free carriers) will result in a s in case of JFET and MOSFET $I_D = I_{DSS}$. It is not sufficient to have a electrons) at the drain and the source (due to the n doped regions) e two. With V_D some positive voltage, VGS at 0 V, and terminal SS there are in fact two reverse-biased p - n junctions between the n ite to oppose any significant flow between drain and source.

VGS have been set at some positive voltage greater than 0 V, te at a positive potential with respect to the source.

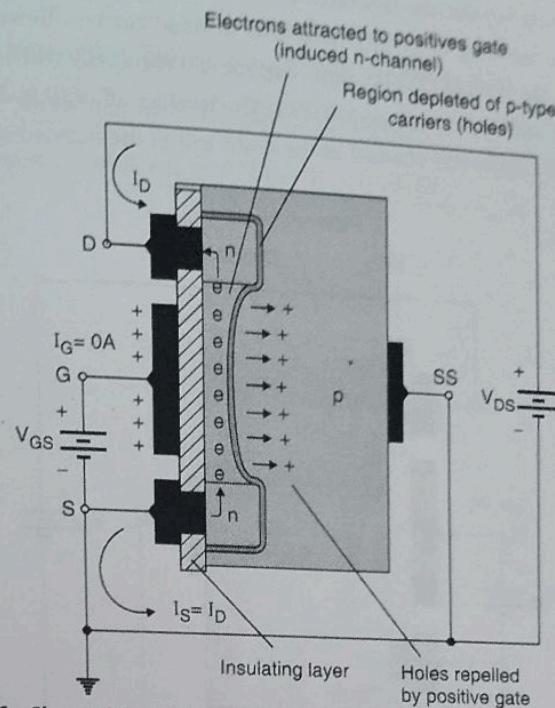


Fig. 5.4.6 : Channel formation in thin-channel enhancement-type MOSFET

The positive potential at the gate will pressure the holes (since like charges repel) in the p - substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p - substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As VGS increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced n-type region can support a measurable flow between drain and source. The level of VGS that results in the significant increase in drain current is called the *threshold voltage* and is given the symbol VT . On specification sheets it is referred to as $VGS(\text{Th})$, although VT is less unwieldy and will be used in the analysis to follow. Since the channel is non-existent with $VGS=0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an enhancement-type MOSFET. Both depletion-and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS} , the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 5.4.7.

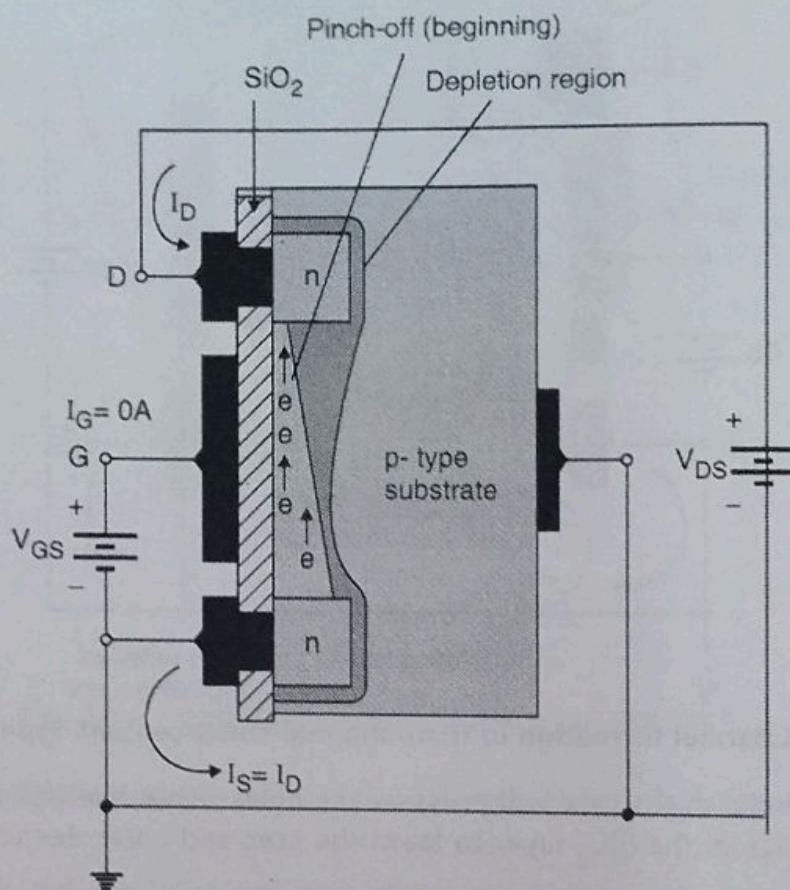


Fig. 5.4.7 : Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

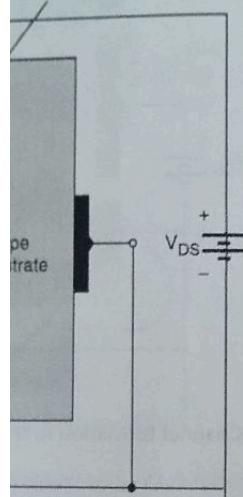
Review Questions

- Q. 1** Give differences and similarities between BJT and FET
- Q. 2** Draw the schematic diagram for construction of n channel JFET.
- Q. 3** How will you connect battery polarities to obtain input and output characteristics of n channel JFET.
- Q. 4** Draw the Drain current vs Drain to source voltage characteristics for JFET and explain why do we get this shape.

level, the density of free carriers in the induced level of drain current. However, if we hold V_{GS} constant the drain current will eventually reach a saturation level as shown in the graph. The leveling off of ID is due to a pinching-off at the drain end of the induced channel as shown in the diagram.

(beginning)

Depletion region



on with increasing level of V_{DS} for a fixed V_{GS}

tions

and FET

n channel JFET.

input and output characteristics of n channel

characteristics for JFET and explain why do we

0.5 Explain use of JFET as switch

0.6 What are the limitations of JFET and how MOSFET overcomes them

0.7 Write in detail the construction and function of E- MOSFET

0.8 Write the differences between E MOSFET AND D- MOSFET



6

Nanotechnology

Syllabus

Introduction to Nanotechnology, Properties (optical, Electrical, Structural, Mechanical)

Importance of surface to Volume ratio, Bonding in solids (Vander walls interactions), Application:

Lithography, Single Electron Transfer (SET), Spin Valves.

6.1 Introduction to Nanotechnology

- We know all materials are composed of atoms with different sizes. If we take a material in which the atoms do not move away from each other and with size in the range of 1 to 100 nano meters, these materials are called nano materials.
- The technology emerged out of this called nanotechnology. Using these highly sophisticated latest technology nano materials can be formed from metals, ceramics polymers and even from liquids.
- Hence we can describe nano science as the study and nano technology as the exploitation of the unique properties exhibited by particles of the size few nano meters.
- Nanotechnology which is multidisciplinary emerging area of fusion between Applied science and Engineering. Nanotechnology is very diverse, ranging from extensions of conventional device physics to completely new approaches based upon molecular with self assembly, from developing new materials with dimensions on the nano scale to investigating whether we can directly control matter on the atomic scale.
- Even though discussions related to nano technology were in air from 1959 (Richard Feynman) to 1986 (Discovery of Buckminster fullerene which was later referred as "bucky balls") but it did not become an experimental science as there were no experimental tools available to the scientists to handle materials at atomic level.

Semiconductor Physics
But the scenario changed with
and AFM (Atomic Force Micros)
In the hot pursuit of fabricating
the attempts to secure them
manufacturing sector in the w

6.2 Properties of Nano

6.2.1 Optical Properties

- The optical properties of nano materials depends on their size, chemical composition etc. The size of the particle has a significant effect on optical properties viz.,
- Surface Plasmon Resonance due to oscillation of conduction band electrons.

6.2.2 Electrical Properties

- Size plays an important role in electrical properties of nano materials.
- Reduction in material's dimension leads to increase in surface area which would result in a reduction in resistivity.
- Reduction in characteristics dimensions of nano materials would result in change of electronic properties like reduction in electrical conductivity of insulators.

6.2.3 Magnetic Properties

- Magnetic properties of nano materials are different from those of bulk materials.
- For small grain sizes, exchange interaction between magnetic moments in neighbouring atoms to align them.
- There exists a small diameter magnetic domains.
- As size of particle decreases, the magnetic moment per unit volume increases.

- But the scenario changed with the development of quantum mechanics and invention of STM and AFM (Atomic Force Microscope).
- In the hot pursuit of fabricating devices that serve the human needs and were hitherto eluded the attempts to secure them some expect that nanotechnology could be one of the largest manufacturing sector in the world.

6.2 Properties of Nanotechnology

6.2.1 Optical Properties

- The optical properties of nanomaterials are highly dependent on the particle size, shape, chemical composition etc. The best part is that it is possible to selectively tune these properties to suit to a give application. The reduction of material dimension has pronounced effect on optical properties viz :
- Surface Plasmon Resonance (SPR) is a process which takes place when there is coherent oscillation of conduction band electrons upon interaction with an electromagnetic field.

6.2.2 Electrical Properties

Size plays an important role in electrical properties and is based on following points :

- Reduction in material's dimensions will increase crystal perfection or reduction of defects which would result in a reduction of resistivity and hence conductivity increases.
- Reduction in characteristics dimension below a critical size i.e. below De-Broglie wavelength result in change of electronic structure which leads to widening of gap which translates into reduction in electrical conductivity. Some metal nano wires undergoes transition to become insulators.

6.2.3 Magnetic Properties

- Magnetic properties of nanomaterials differ to that of bulk.
- For small grain sizes, exchange forces are dominant due to strong coupling causing all spins in neighbouring atoms to align.
- There exists a small diameter, below which material will be single domain.
- As size of particle decreases, saturation magnetisation increases.

6.2.4 Structural Properties

- A nano material is defined when at least one dimension of a system is less than 100 nm. The size of such structure is found to influence the chemical and physical properties of bulk material. These properties are in turn influences :
 - Size, shape and aspect ratio
 - Agglomeration state
 - Size distribution
 - Surface morphology
 - Crystallites and defect structures
 - Solubility

6.2.5 Mechanical Properties

Nanoparticles have attracted intensive scientific attention. Distinctive size dependent properties of nanoparticles are of paramount interest. When the size of a particle approaches nanoscale.

- (a) The periodic boundary conditions of crystalline particles are destroyed or
- (b) Atomic density on the amorphous particle surface is changed. Due to this a lot of the physical properties of nanoparticles are quite different from bulk materials. This has resulted in modified/improved mechanical strength, hardness, elastic modulus, adhesion, friction and many other mechanical properties.

6.3 Importance of Surface to Volume Ratio

- The properties of nano-materials are very much different from those at larger scale. One of the factor which causes this change is "Increased surface area" or "Increased surface to volume ratio".
- This can change or enhance properties such as reactivity, severity and electrical properties.
- Nano material have a relatively large surface to volume ratio compared to same volume of the material produced in larger form.
- Let us consider a sphere of radius 'r'.

$$\therefore \text{Its surface area} = 4\pi r^2$$

$$\text{and its volume} = \frac{4}{3}\pi r^3$$

$$\therefore \text{Surface area to volume ratio} = \frac{4\pi r^2}{\frac{4}{3}\pi r^3} = \frac{3}{r}$$

- When the radius of the sphere decreases, its surface to volume ratio increases.
- This makes nano materials more chemically reactive.

6.4 Bonding in Solids (Vander waals Interaction)

- Vander Waals interactions, in solids refer to weak, temporary attractive forces between neutral atoms or molecules, arising from fluctuations in electron distribution, which hold the solid together, typically resulting in soft, low melting point materials compared to solids with stronger ionic or covalent bonds; essentially, these are the weakest type of bonding found in solids.
- These interactions are important in a variety of chemical and physical processes, even though they are much weaker than covalent or ionic bonds.
- Let's see one more useful aspect in the field of nano technology .Van der Waals interactions are foundational in enabling **self-assembly**, improving the **stability and dispersion** of nanoparticles, and optimizing **surface interactions** for a wide range of nanotechnology applications.
- While these forces are weak compared to chemical bonds, their importance at the nanoscale cannot be overstated. The ability to control and manipulate these forces allows researchers to design and fabricate more efficient, functional, and customizable nanomaterials for various technologies, from sensors and coatings to drug delivery systems and beyond.

Types of Van der Waals interactions :

1. London Dispersion Forces

These are the weakest of the Van der Waals forces and occur due to temporary fluctuations in the electron distribution within atoms or molecules. Even nonpolar molecules can experience these forces because of instantaneous dipoles that arise due to electron movement. These forces are stronger in larger atoms or molecules because they have more electrons.

2. Dipole-Dipole Interactions

These occur between polar molecules, where a partial positive charge of one molecule is attracted to the partial negative charge of another. For this interaction to happen, the molecules need to have permanent dipoles These forces are stronger than London dispersion forces.

3. Hydrogen Bonds

- Although often considered a special case of dipole-dipole interactions, hydrogen bonds are a strong form of Van der Waals interaction. They occur when hydrogen is covalently bonded to a highly electronegative atom (like oxygen, nitrogen, or fluorine), and this creates a strong attraction with another electronegative atom in a nearby molecule. The hydrogen bond is weaker than covalent bonds but stronger than typical dipole-dipole interactions.
- Van der Waals interactions play a critical role in nanotechnology by influencing the behavior of nanoparticles, nanomaterials, and molecular interactions at the nanoscale. These weak forces can be both advantageous and limiting, depending on the specific application. Here's how they are useful in various aspects of nanotechnology:

4. Self-Assembly of Nanomaterials

- **Self-assembly** refers to the spontaneous organization of components into structured patterns or shapes without external guidance. Van der Waals forces are crucial in this process, as they enable molecules or nanoparticles to attract and align with one another in a controlled manner.
- For example, nanoparticles may aggregate into specific shapes or structures by utilizing Van der Waals forces to bind together. This property is particularly useful in creating complex nanostructures and nanodevices like nanowires, nanotubes, and nanoparticle films.

5. Nanocomposites and Coatings

- **Nanocomposites**, which combine nanoparticles with other materials (polymers, metals, ceramics), rely on Van der Waals interactions to bond the nanoparticles to the matrix. These forces help in forming a stable material structure, enhancing properties like strength, thermal stability, and electrical conductivity.
- In **nano-coatings**, Van der Waals forces help molecules or nanoparticles adhere to surfaces, creating coatings that provide protection, water resistance, or improved surface properties (e.g., anti-corrosion or anti-fouling coatings).

6. Molecular Sensing

- **Nanosensors** often rely on Van der Waals forces to detect specific molecules. For example, in **molecular recognition** applications, a molecule may bind to a receptor on a nanoparticle or nanostructure through these weak interactions. Even a small change in the number of Van der Waals interactions (due to the presence of target molecules) can trigger a measurable response, useful for detecting gases, biomolecules, or contaminants.

- These interactions are critical in the development of sensitive, low-cost sensors for a wide range of applications, such as environmental monitoring or medical diagnostics.

7. Surface Chemistry and Interactions

- The behavior of **nanomaterials at surfaces** is heavily influenced by Van der Waals interactions. At the nanoscale, the surface area-to-volume ratio is high, so the influence of surface forces like Van der Waals becomes much more significant compared to bulk materials.
- The ability to control these interactions at the surface level allows for the modification of nanomaterials, including changing their adhesion properties, wettability, or interaction with other materials.

8. Nanomedicine and Drug Delivery

- In **nanomedicine**, particularly in drug delivery, Van der Waals forces are often used to **stabilize drug-loaded nanoparticles** and enable their interaction with biological targets.
- Nanoparticles may be designed to adhere to certain cells or tissues, either by functionalizing their surfaces to enhance or inhibit these interactions or by taking advantage of the weak forces to improve the bioavailability and controlled release of drugs.

9. Molecular Motors and Nano-machines

- Van der Waals forces are often involved in the functioning of **molecular motors** or **nano-machines**, where the attraction between different parts of the nanostructure helps in the movement or interaction of components.
- This is particularly important in the design of nanoscale systems that need precise control over molecular movements.

10. Stability of Nanostructures

- At the nanoscale, structures are more prone to changes due to small forces acting on them. Van der Waals interactions help stabilize these structures, preventing unwanted disassembly or collapse, especially in the case of delicate structures like carbon nanotubes or graphene sheets.
- Proper tuning of these interactions can enhance the **mechanical and thermal stability** of nanomaterials.

6.5 Applications of Nanotechnology

6.5.1 Lithography

Thin film devices are conquering many aspects of today's life, and continuous shrinking of building block dimensions of these structures enhances their performances and makes them economically attractive. Here is an overview of one of the lithography techniques used to fabricate thin film functional structures. Several aspects of pattern transfer are addressed with emphasis on the limits of these lithography techniques.

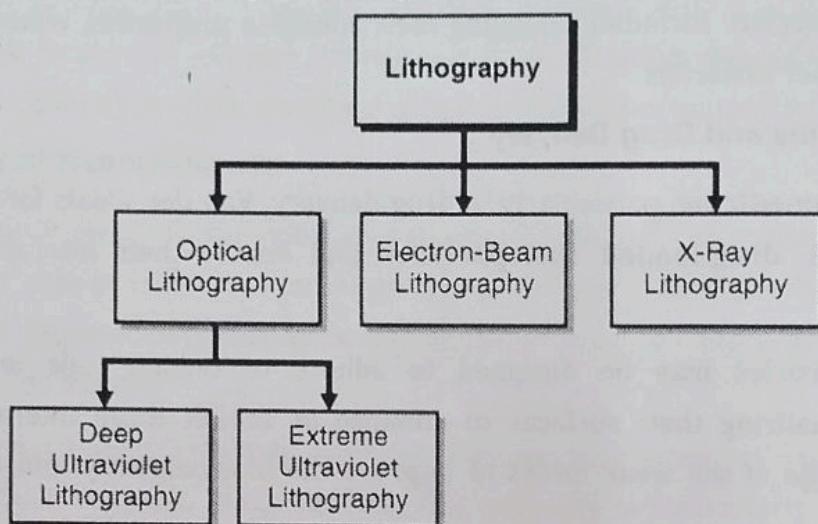


Fig .6.5.1 : Types of lithography

A] Electron Beam Lithography

- Electron Beam Lithography, e-Beam Lithography or EBL, emerged during the 1960s to produce tailored intricate patterns on a surface. This method, categorized as maskless lithography, employs a high-energy electron beam directed at a surface covered with an electron-sensitive film called resist.
- When the electron beam interacts with the resist, it facilitates the selective elimination of material from the exposed or unexposed surface areas by modifying the resist's solubility. This allows for the selective removal of exposed or unexposed regions using a solvent.
- The main goal is to create tiny structures in the resistance. These structures can then be transferred to the substrate, often through etching.
- Main feature of the Electron Beam Lithography system/ equipment :
 - The electron source is commonly referred to as an electron gun.

- The electron column consists of aperture, condenser, and deflector components. It helps narrow the electron beam and guide it along the desired path.
- A stage holds the material on which the pattern is to be created.
- A computer control system is employed to manage the stage and various components of the electron column system.

Applications of Electron Beam Lithography

Electron beam lithography (EBL) is a direct write technique. It uses a focused beam of electrons to create patterns on a substrate. It is a versatile technique that can be used for a wide variety of applications, including :

- The fabrication of integrated circuits (ICs).
- The manufacturing of microelectromechanical systems (MEMS).
- The production of photomasks.
- The creation of prototypes and models.
- The repair of damaged devices.
- The study of materials at the nanoscale.

[B] Nano imprint methods

- Nanoimprint lithography has attracted considerable attention in academic and industrial fields as one of the most prominent lithographic techniques for the fabrication of the nanoscale devices. Effectively controllable shapes of fabricated elements, extremely high resolution, and cost-effectiveness of this especial lithographic system have shown unlimited potential to be utilized for practical applications. In the past decade, many different lithographic techniques have been developed such as electron beam lithography, photolithography, and **nanoimprint lithography**.
- Among them, nanoimprint lithography has proven to have not only various advantages that other lithographic techniques have but also potential to minimize the limitations of current lithographic techniques. Here, we summarize current lithography techniques and, furthermore, investigate the nanoimprint lithography in detail in particular focusing on the types of molds. Nanoimprint lithography can be categorized into three different techniques
 - hard-mold
 - soft-mold
 - hybrid nanoimprint

- Depending upon the molds for imprint with different advantages and disadvantages. With numerous studies and improvements, nanoimprint lithography has shown great potential which maximizes its effectiveness in patterning by minimizing its limitations.
- This technique will surely be the next generation lithographic technique which will open the new paradigm for the patterning and fabrication in nanoscale devices in industry.

6.5.2 Single Electron Transfer

- The inventions and progress of Nano technology has given birth to a whole new domain of physics wherein we need to look at fundamental entities like electron in a different way. In quantum mechanics we have experienced a limitation – Is electron a wave or a particle? This issue has been further advance by certain applications/ domains where we need a single electron – may be in an isolated form to that needs to the transfer of one electron at a time between a molecule and an electrode or between different regions of a nanomaterial. Single electron transfer (SET) plays an important role in nanotechnology, particularly in the areas of molecular electronics, quantum dots, and nanoscale devices. This process has several implications and applications in nanotechnology:
- The list includes the topics from next level industrial revolution which is knocking our doors.
 - A] A very interesting aspect of future electronics is the capability of controlling with the highest possible accuracy the amount of charge in a tiny region, i.e. control the addition or the subtraction to the region of a single electron. The new field of single electron device covers digital and analogical circuits, metrological standards, Quantum information processing, etc. The concept of Single Electron Transistor (SET) is based on the behavior of 0 Dimension nanometric structures, such as Quantum dots, in which electrons are distributed in discrete energy levels. One of the most interesting properties of these structures, associated to energy level quantification, is the so-called Coulomb blockade effect. When the tiny conducting material is extremely small (also called “island”), the electrostatic potential significantly increases even when only one electron is added to it.

It is also known that for the correct operation of SETs two conditions have to be met :

1. The change in electric energy when an electron enters or leaves the quantum dot, i.e. the charging energy, has to be much larger than kT , which in terms of the capacitance is expressed as $C \ll e^2/kT$.
2. The resistance RT of the tunnel junction must be large enough compared to the quantum resistance in order to avoid fluctuations in the number of electrons in the quantum dot as a consequence of the Heisenberg uncertainty principle.

- B] SET has potential applications in highly sensitive nanoscale sensors, where individual electron detection could lead to the development of extremely sensitive detection mechanisms. These could be used in fields such as biosensors, environmental monitoring, and even quantum computing
 - C] SETs are a class of devices that rely on single electron transfer to control electrical current. The fundamental working principle is that the device can be turned on or off depending on the number of electrons that have been transferred, and the current is controlled through the tunneling of individual electrons across a small island in the presence of an external gate.
 - D] In molecular electronics, SET plays a role in creating devices where individual molecules can function as electronic components like transistors or diodes. Single electron transfer allows these devices to operate at very low power and potentially at much smaller scales than traditional semiconductor-based devices.
- Single electron transfer is a fundamental phenomenon in nanotechnology, providing unique opportunities for designing tiny, efficient devices, especially in molecular electronics, quantum computing, and energy applications. However, challenges remain in fully harnessing this effect for widespread practical use.

6.5.3 Spin Valves

- A spin valve is a remarkable device, composed of two or more conducting magnetic materials, whose electrical resistance gracefully shifts between two distinct values, governed by the relative alignment of the magnetization within its layered structure. This variation in resistance is a manifestation of the giant magneto resistive effect (GMR), a phenomenon of notable significance in modern electronics.
- Spin valves, as a refined class of magnetic multilayered constructs, find their most illustrious applications in the realms of magneto resistive (MR) devices and memory storage technologies. They deftly harness the captivating principle of "spin-dependent electron transport," whereby the electrical resistance of the material is finely tuned by the influence of an external magnetic field.
- The quintessential architecture of a spin valve consists of several meticulously arranged layers, often alternating between ferromagnetic (FM) and non-magnetic (NM) materials. The essential framework typically unfolds as follows :
 1. **Ferromagnetic Layer (FM1)**: A steadfast layer, with a magnetization direction that remains fixed, unwavering in its orientation.

2. **Non-Magnetic Spacer Layer (NM):** A delicate, thin interlayer, composed of non-magnetic materials such as copper (Cu) or silver (Ag), serving as a boundary that separates the two ferromagnetic layers.
 3. **Ferromagnetic Layer (FM2):** A dynamic layer, wherein the magnetization direction is malleable and can be manipulated, often through the application of an external magnetic field.
- When the magnetization directions of the two ferromagnetic layers align in parallel, the electrical resistance is minimized. However, when their magnetization is set in opposition, in an antiparallel arrangement, the resistance increases. This elegant shift in resistance, driven by the relative orientation of magnetization, is known as Giant Magnetoresistance (GMR).
 - Due to their unparalleled sensitivity to minute magnetic fields, spin valves have earned their place in various cutting-edge technologies, such as the read heads of hard disk drives, Magnetoresistive Random Access Memory (MRAM), and other spintronic devices. Their ability to integrate seamlessly with semiconductor technologies further enhances their profound utility in the ever-evolving landscape of electronics.

Review Questions

- Q. 1** What is nano technology ? Write its significance in in the field of technology.
- Q. 2** List the electrical, mechanical properties of nanoparticles and explain one in detail.
- Q. 3** What is surface to volume ration in nano technology? Write its significance.
- Q. 4** Discuss bonding in solids in the reference of van der waals interactions.
- Q. 5** Explain in detail electron lithography and few of its applications in the field of technology.
- Q. 6** Explain in detail "Single electron transfer" (SET) in the context of latest applications in the field of technology.
- Q. 7** What is spin valves why do they spin ?

