Design Project 1.2 - 64-bit Adder

Summary Report

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The project began by establishing an organized and efficient work environment. A dedicated GitHub repository and structured project directory were created to ensure smooth version control and collaboration.

The core technical task involved the design and implementation of four distinct 64-bit adder candidates:

1. Ripple-Carry Adder implemented on a Cyclone IV FPGA (baseline device),
2. Ripple-Carry Adder implemented on an Arria II FPGA,
3. Conditional-Sum Adder implemented on a Cyclone IV FPGA, and
4. Conditional-Sum Adder implemented on an Arria II FPGA.

To verify each candidate's correctness, two testbenches were developed, one for the Ripple-Carry architecture and one for the Conditional-Sum architecture. Numerous test vectors, including edge cases, were applied to both testbenches to ensure proper functionality across all possible input conditions. This included both signed and unsigned operations, as well as carry-out and overflow scenarios.

Simulation workflows were automated using custom simulation scripts (.do files) that generated transcript files for output validation. All four design candidates were successfully synthesized on their respective target FPGA devices using Intel Quartus Prime, confirming their implementability in hardware.

* sources for device costs are documented on the report

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Cost Analysis

Design Candidate	Target Device	Total Device LEs/ALMs	Device Price * (CAD)	Resources Used (LEs/ALMs)	Cost per LE/ALM (CAD)	Candidate Cost (CAD)	Normalized Cost
1 (Baseline)	Cyclone IV (EP4CE115F29C7)	114480	1029.5647	161	0.008993403	$1.45	1
2 (Ripple)	ARRIA II (EP2AGX45DF29C6)	36100	1273.0389	147	0.035264235	$5.18	3.58015555
3 (CSA)	Cyclone IV (EP4CE115F29C7)	114480	1029.5647	271	0.008993403	$2.44	1.68322981
4 (CSA)	ARRIA II (EP2AGX45DF29C6)	36100	1273.0389	188	0.035264235	$6.63	4.57870234

As shown in the table, the Conditional-Sum Adder (CSA) topology is more costly than the Ripple-Carry Adder topology. This higher cost directly reflects the increased efficiency of the Conditional-Sum design compared to the sequential carry-propagation of the Ripple-Carry design (although efficiency was not analyzed in this project).

It is also evident that, regardless of topology, Arria II implementations require fewer logic resources due to the device's 8-input Adaptive Logic Modules (ALMs). However, the Arria II device itself carries a higher base price and provides fewer total resources compared to the Cyclone IV, resulting in a higher overall implementation cost despite its lower resource utilization.

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