Final Project

Summary Report

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Design Candidate	**Target Device**	**Normalized Cost** (W.R.T. Baseline LEs)	**Performance** (W.R.T. Baseline Simulation)	**Performance to Cost Ratio**
1 (Baseline)	Cyclone IV	1.000	1	1
2 (RCA + IEEE FN)	ARRIA II	1.847	0.956	0.517
3 (RCA + Barrel Shifter)	Cyclone IV	1.059	0.967	0.913
4 (RCA + Barrel Shifter)	ARRIA II	1.877	1.027	0.830
5 (CBA+ IEEE FN)	Cyclone IV	1.237	1.288	1.04
6 (CBA+ IEEE FN)	ARRIA II	2.237	1.497	0.669
7 (CBA + Barrel Shifter)	Cyclone IV	1.157	1.14	0.985
8 (CBA + Barrel Shifter)	ARRIA II	2.192	1.536	0.701

The optimal 64-bit execution unit design depends on the primary constraint: for the best performance-to-cost ratio, use the Carry-Bypass Adder with IEEE shift functions on Cyclone IV (Candidate 5, ratio 1.04); for maximum pure performance, use the Carry-Bypass Adder with a barrel shifter on Arria II (Candidate 8, 1.54× faster); and for minimal cost, use the Ripple-Carry Adder with a barrel shifter on Cyclone IV (Candidate 3, 1.06× cost).