```vhdl
entity EN_LACG4 is
    generic (N: natural := 4);
    port (
        Gin, Pin  : in std_logic_vector (N-1 downto 0);
        Gout, Pout  : out std_logic;
        Cin : in std_logic;
        C : out std_logic_vector (N-1 downto 1)
    );
end EN_LACG4;
```