Group #:
G 12

Design Project 2

ENSC 350 1257

Project Submitted in Partial Fulfillment of the
Requirements for Ensc 350
Towards a Bachelor Degree in Engineering Science.

Last Name:	Last Name:	Last Name:
Saghafi	Schaufele	Singh
SID: 30145	SID: 30145	SID: 30139
5814	4255	4671

Table of Contents

1 - Introduction

Outline the purpose of the project and introduce topics used

```
entity EN_Adder is
    generic (N: natural := 64);
    port (
        A, B  : in std_logic_vector (N-1 downto 0);
        S : out std_logic_vector (N-1 downto 0);
        Cin : in std_logic;
        Cout, Ovfl : out std_logic
    );
end EN_Adder;
```

Figure 1: Adder Entity Definition within EN_Adder.vhd

2 - Experimental Procedures

Flowchart for the flow of the procedure

3 - Design Candidates

Design Topologies

Ripple-Carry Adder

Brief description of topology purpose and implementation

Image of the topology for a smaller case (Ripple-carry Adder)

Conditional-Sum Adder

Brief description of topology purpose and implementation

Image of the topology for a smaller case (Conditional-Sum Adder)

Look Ahead Tree Adder

Brief description of topology purpose and implementation

Image of the topology for a smaller case (Look Ahead Tree Adder)

Brent-Kung Adder

Brief description of topology purpose and implementation

Image of the topology for a smaller case (Brent-Kung Adder)

Ladner-Fischer Adder

Brief description of topology purpose and implementation

Image of the topology for a smaller case (Ladner-Fischer Adder)

Design Implementations

Brief discussion of the devices used and their primitive elements

Candidate Estimations

Cost

State assumptions, formulas, and method for each topology

Estimation Calculations examples for each topology

Timing

State assumptions, formulas, and method for each topology

Estimation Calculations examples for each topology

Post-Fitting Analysis

Annotated Post fitting images

Brief discussion of what's interesting about these post fittings

4 - Testbenches

Brief description of test vectors and tvs file format

Flowchart for the flow of the testing

Sample Annotated Wave Output

5 - Cost Analysis

The costs for the design candidates were calculated using this formula:

$$Cost\ per\ LE/ALM\ =\ Device\ price\ \div\ Total\ Device\ LEs/ALMs$$

This method of calculating the cost factors accounts for the total resources available to the board and the fraction of those resources used by the circuit. Resource data was obtained from the Quartus synthesis reports. LEs were selected as the unit of cost, and all ALMs were converted to LEs using a conversion factor. The normalized cost is obtained by dividing each candidate cost by the baseline cost. The boards used to synthesize the architectures are currently obsolete. This inflates the price and makes cost calculations inaccurate. To account for these inaccuracies, the Cyclone IV Nano and the ARRIA 10 GX 480 were considered. These are comparable to the devices used in synthesis, but they have more accurate pricing because they are currently active on DigiKey, indicating they are still widely used and in production. The following calculations assume that the LEs and ALMs on the available devices cost the same as the original board's elements.

Device	Total Device LEs/ALMs	Device Price (CAD)	Cost per LE/ALM (CAD)	Normalized Cost in terms of LEs
Cyclone IV Nano	22320	169.49[3]	$0.00759184	1
Arria 10 GX 480	181790	3937.25[4]	$0.02165823	2.85

Discussion of the effect of topology

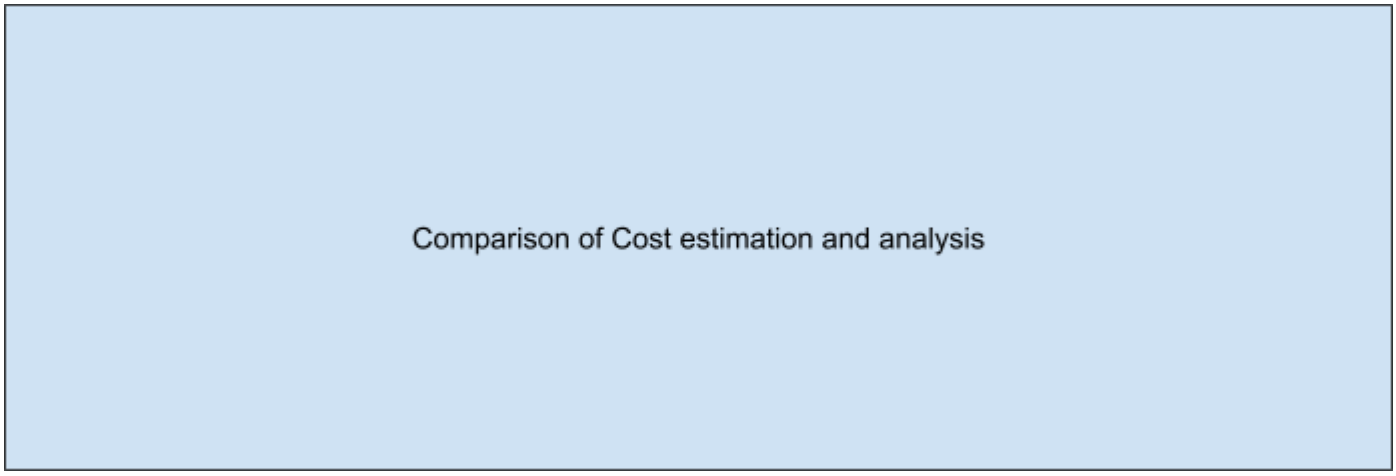
Discussion of the effect of implementation

Comparison of Cost between all candidates

Design Candidate	Target Device	Resource Usage Predications (LEs/ALMs)	Resources Used (LEs/ALMs)	Predicted Cost (CAD)	Candidate Cost (CAD)	Cost (LEs)	Normalized Cost (W.R.T. Baseline LEs)
1 (Baseline)	Cyclone IV	130	161	$0.99	$1.22	161	1
2 (RCA)	ARRIA II	66	147	$1.43	$3.18	418.95	2.60
3 (CSA)	Cyclone IV	960	271	$7.29	$2.06	271	1.68
4 (CSA)	ARRIA II	667	188	$14.45	$4.07	535.8	3.33
5 (LATA)	Cyclone IV						
6 (LATA)	ARRIA II						
7 (BKA)	Cyclone IV						
8 (BKA)	ARRIA II						
9 (LDA)	Cyclone IV						
10 (LDA)	ARRIA II						

Figure 9: Cost Calculations of Design Candidates

The conversion factor from LEs to ALMs was 2.85, slightly more than double.



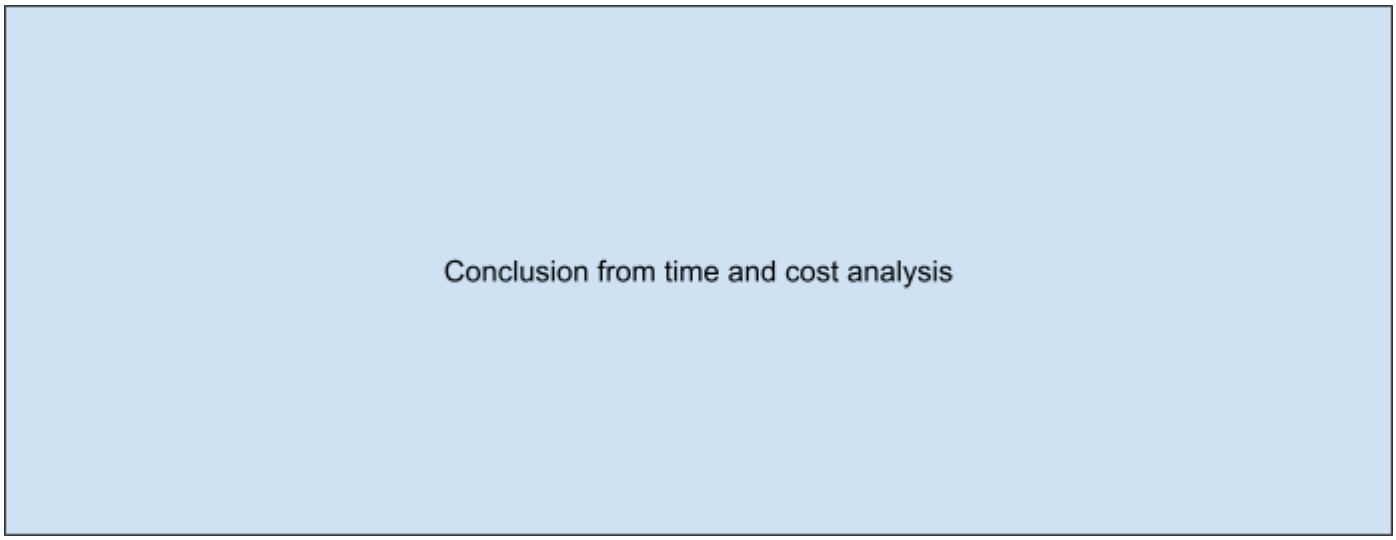
6 - Timing Analysis

Brief description of tools used for timing analysis

Design Candidate	Target Device	Estimation	Simulation Results	Normalized Time (W.R.T. Baseline Simulation)
1 (Baseline)	Cyclone IV	130	161	1
2 (RCA)	ARRIA II	66	147	2.60
3 (CSA)	Cyclone IV	960	271	1.68
4 (CSA)	ARRIA II	667	188	3.33
5 (LATA)	Cyclone IV			
6 (LATA)	ARRIA II			
7 (BKA)	Cyclone IV			
8 (BKA)	ARRIA II			
9 (LDA)	Cyclone IV			
10 (LDA)	ARRIA II			

Comparison of time estimation and analysis

7 - Results Analysis



8 - Appendix

A.1 Directory Structure

(folder) Documentation

- (folder) ActivityLogs
  - a folder including each group member's activity log worksheets
- (folder) Images
  - a folder containing all the images used in the report
- (folder) OutputFiles
  - (file) Quartus-Summaries.text
    - Includes summary reports from the synthesis of each design candidate
  - (file) Sim-Transcript-CSA.text
    - Includes the transcript from the conditional sum adder testbench, displays the test vector index, as well as the test vectors, and the status of each tested test vector
  - (file) Sim-Transcript-Ripple.text
    - Includes the transcript from the ripple-carry adder testbench, displays the test vector index, as well as the test vectors, and the status of each tested test vector
- (file) VHDLSrc_EN_Adder.pdf
  - A PDF listing of the VHDL code for the Adder Entity and Architectures
- (file) VHDLSrc_TB_Adder_CSA.pdf
  - A PDF listing of the VHDL code for the testbench written for the conditional sum adder topology
- (file) VHDLSrc_TB_Adder_RIP.pdf
  - A PDF listing of the VHDL code for the testbench written for the ripple adder topology
- (file) DP2-Report-G12-350-1257.pdf
  - Project Report, including cost and efficiency analysis (this document)
- (file) DP2-Summary-G12-350-1257.pdf
  - A summary of tasks completed in this project, as well as a brief overview of the cost and efficiency analysis

(folder) Simulation

- (folder) questa
  - folder created by modelsim, includes pre-compiled netlists
- (folder) TestVectors
  - Adder00.tvs
    - File including all the test vectors used by the testbenches
  - gen_testVec.py
    - a python script to append randomly generated test vectors to the Adder00.tvs file
- (files) DP1.cr.mti / DP1.mpf
  - Modelsim project files for simulation and testing
- (file) run_CSA.do
  - Script to compile, add waves, run simulation and create a simulation transcript for the conditional-sum adder topology testbench
- (file) run_ripple.do
  - Script to compile, add waves, run simulation and create a simulation transcript for the ripple-carry adder topology testbench
- (file) TB_Adder_CSA.vhd
  - Conditional-sum adder testbench written in VHDL
- (file) TB_Adder_RIP.vhd
  - Ripple-Carry adder testbench written in VHDL

(folder) SourceCode

- (file) EN_Adder.vhd
  - Defines the adder entity as well as a ripple adder, fast ripple adder, and conditional sum adder architectures in VHDL

(file) DP2.qpf / DP2.qsf

- Quartus project files for synthesis and analysis of the digital circuits

A.2 References

[1] "DigiKey," 2 November 2009. [Online]. Available: https://www.digikey.ca/en/products/detail/altera/EP4CE115F29C7/2260452. [Accessed 12 October 2025].

[2] "DigiKey," 2 February 2009. [Online]. Available: https://www.digikey.ca/en/products/detail/altera/EP2AGX45DF29C6/2349475. [Accessed 12 October 2025].

[3] "DigiKey," 28 October 2014. [Online]. Available: https://www.digikey.ca/en/products/detail/terasic-inc/P0082/2625112. [Accessed 25 October 2025].

[4] "DigiKey," 29 September 2023. [Online]. Available: https://www.digikey.ca/en/products/detail/iwave-global/IW-G24D-CU0F-4D004G-S008G-NCI/15780313. [Accessed 25 October 2025].