```
4   entity EN_Logic is
5       Generic ( N : natural := 16 );
6       Port (
7           A, B : in std_logic_vector(N-1 downto 0);
8           LogicFN : in std_logic_vector(1 downto 0);
9           Y : out std_logic_vector(N-1 downto 0)
10      );
11  end entity EN_Logic;
```