Design Project 2.1 - 64-bit Adder

Summary Report

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The project began by establishing an organized and efficient work environment. A dedicated GitHub repository and structured project directory were created to ensure smooth version control and collaboration.

The core technical task involved the design and implementation of 10 distinct 64-bit adder candidates:

1. Ripple-Carry Adder (RCA) implemented on a Cyclone IV FPGA (baseline device),
2. Ripple-Carry Adder (RCA) implemented on an Arria II FPGA,
3. Conditional-Sum Adder (CSA) implemented on a Cyclone IV FPGA,
4. Conditional-Sum Adder (CSA) implemented on an Arria II FPGA,
5. Look-Ahead Carry Tree Adder (LACTA) implemented on a Cyclone IV FPGA,
6. Look-Ahead Carry Tree Adder (LACTA) implemented on an Arria II FPGA,
7. Brent-Kung Adder (BKA) implemented on a Cyclone IV FPGA,
8. Brent-Kung (BKA) Adder implemented on an Arria II FPGA,
9. Carry-Bypass (CBA) Adder implemented on a Cyclone IV FPGA, and
10. Carry-Bypass (CBA) Adder implemented on an Arria II FPGA

To verify each candidate’s correctness and evaluate propagation delay, a testbench was developed. Numerous test vectors, including edge cases and worst timing cases, were applied to the testbench. This was achieved using a configuration file to easily switch architectures

Simulation workflows were automated using custom simulation scripts (.do files) that generated transcript files for output validation and ensured correct configuration. All design candidates were successfully synthesized on their respective target FPGA devices using Intel Quartus Prime, confirming their implementability in hardware. All candidates also generated .vho and .sdo files, which were used to perform timing tests to measure the candidates' respective performance.

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Results Analysis

Design Candidate	Target Device	Normalized Cost (W.R.T. Baseline LEs)	Performance (W.R.T. Baseline Simulation)	Performance to Cost Ratio
1 (Baseline)	Cyclone IV	1	1	1
2 (RCA)	ARRIA II	2.60	1.275	0.490
3 (CSA)	Cyclone IV	1.68	1.834	1.092
4 (CSA)	ARRIA II	3.33	2.773	0.833
5 (LACTA)	Cyclone IV	1.84	2.300	1.250
6 (LACTA)	ARRIA II	4.09	3.559	0.870
7 (BKA)	Cyclone IV	3.57	3.660	1.025
8 (BKA)	ARRIA II	9.61	3.847	0.400
9 (CBA)	Cyclone IV	1.55	1.143	0.737
10 (CBA)	ARRIA II	3.89	2.765	0.711

The ARRIA II, although more expensive, consistently delivers better performance across all topologies. For a purely cost-optimized solution, the baseline candidate is the best option. For a strictly performance-optimized solution, the best option is the BKA on the ARRIA II. The option with the best performance-to-cost ratio is the LACTA on the Cyclone IV

These findings underscore that advanced adder architectures provide diminishing returns as complexity increases, with parallel-prefix designs, such as the Brent-Kung design, offering marginal performance gains at substantial cost penalties. The hierarchical inverted tree structure of the LACTA strikes an effective balance for practical implementations where both performance and cost constraints must be considered.