Design Project 1.1 - 64-bit Adder

Summary Report

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This document concisely summarizes the key objectives completed for Design Project 1. The project began with setting up an organized and efficient work environment. A GitHub repo and properly organized project folders were created. The core technical task involved the design and implementation of four distinct 64-bit adder candidates. These included a baseline Ripple Carry Adder on a Cyclone IV FPGA, a Ripple Carry Adder on an Arria II FPGA, a Conditional-Sum Adder on a Cyclone IV FPGA, and a Conditional-Sum Adder on an Arria II FPGA. To verify each candidate's robustness and correctness, two test benches were created. One to test the ripple architecture and one to test the conditional sum architecture. Many test vectors were fed into these test benches, including edge cases. This ensured correct functionality for all inputs, including signed and unsigned operations as well as carry and overflow scenarios. This process was automated with custom simulation scripts to generate transcripts for validation. All four design candidates were successfully synthesized on their respective target FPGA devices using Quartus to confirm their implementability.