Group #:
G12

Design Project 1

ENSC 350 1257

Project Submitted in Partial Fulfillment of the
Requirements for Ensc 350
Towards a Bachelor Degree in Engineering Science.

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1- Table of Contents

2 - Introduction

Outline the purpose of the project and introduce topics used

A listing of the adder entity in vhdl

3 - Experimental Procedures

Explain the flow of the procedure and procedure steps

Flowchart for the flow of the procedure

4 - Design Candidates

Baseline Device: Ripple Adder On a Cyclone IV FPGA

Architecture of the device in vhdl

RTL netlist or circuit diagram

Explain how the architecture works

Explain the specific theories for the architecture and how they affect it

Design Candidate 1: Ripple Adder On an ARRIA II

Architecture of the device in vhdl

RTL netlist or circuit diagram

Explain how the architecture works

Explain the specific theories for the architecture and how they affect it

Design Candidate 2: Carry-Select Adder On a Cyclone IV FPGA

Architecture of the device in vhdl

RTL netlist or circuit diagram

Explain how the architecture works

Explain the specific theories for the architecture and how they affect it

Design Candidate 3: Carry-Select Adder On an ARRIA II

Architecture of the device in vhdl

RTL netlist or circuit diagram

Explain how the architecture works

Explain the specific theories for the architecture and how they affect it

5 - Testbenches

General description of testbenches	General procedure flow chart

Baseline Device: Ripple Adder On a Cyclone IV FPGA

Testbench 1:

Description of test vector
Short Discussion of results and output - Point out any important results

Testbench 2:

Description of test vector
Short Discussion of results and output - Point out any important results

Design Candidate 1: Ripple Adder On an ARRIA II

Testbench 1:

Description of test vector

Short Discussion of results and output
- Point out any important results

Testbench 2:

Description of test vector

Short Discussion of results and output
- Point out any important results

Design Candidate 2: Carry-Select Adder On a Cyclone IV FPGA

Testbench 1:

Description of test vector

Short Discussion of results and output
- Point out any important results

Testbench 2:

Description of test vector

Short Discussion of results and output - Point out any important results

Design Candidate 3: Carry-Select Adder On an ARRIA II

Testbench 1:

Description of test vector

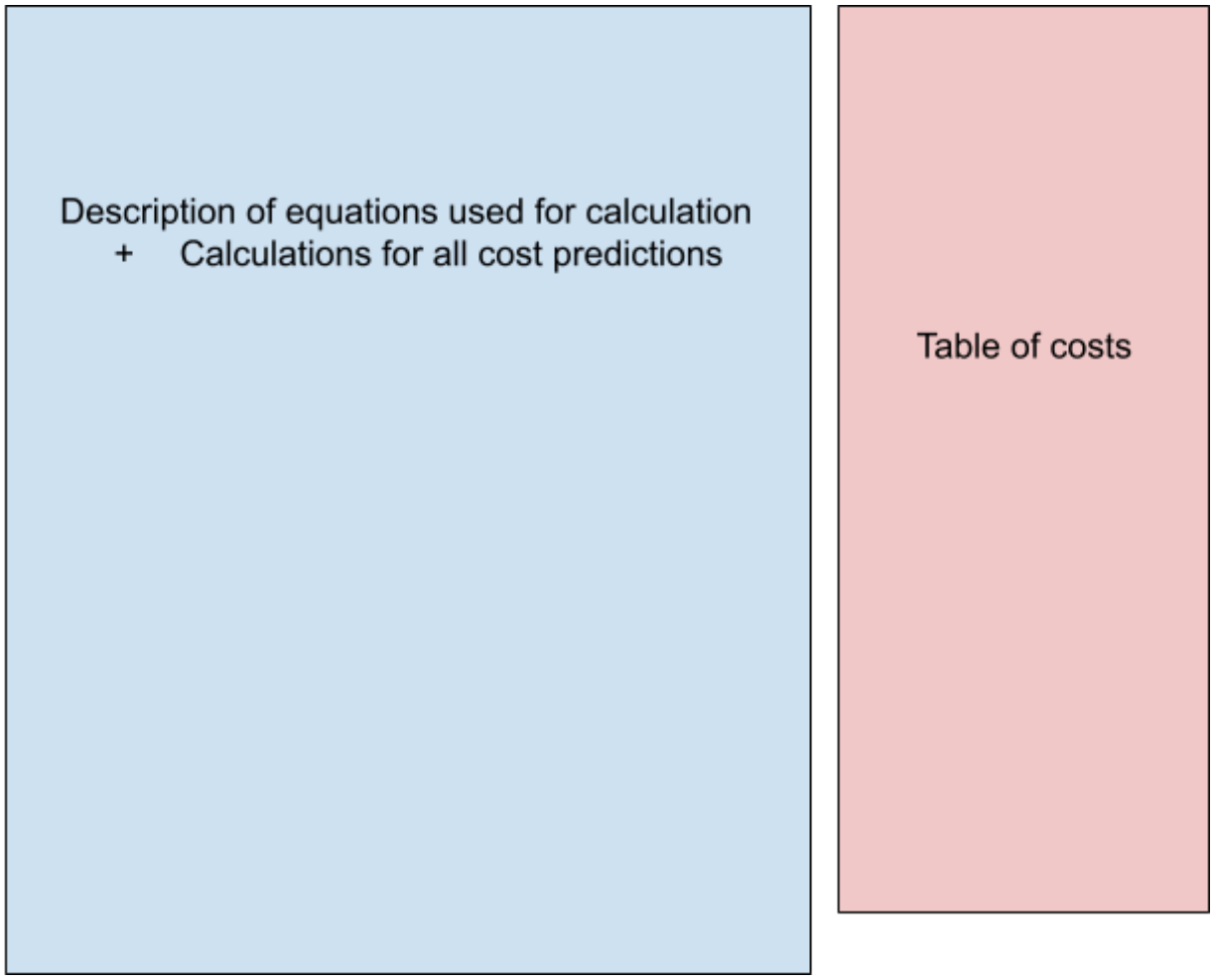
Short Discussion of results and output - Point out any important results

Testbench 2:

Description of test vector

Short Discussion of results and output - Point out any important results

6 - Cost Analysis



Comparison of predictions and experimental costs
+ Discuss differences and sources of discrepancy

Discussion of efficiency and cost of each device compared to the other candidates

7 - Results Analysis and Conclusion

Compare results, cost, and efficiency of each candidate and discuss when/ where they would be helpful