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DIPS-01: DIGILENT VIDEO MEMORY ACCESS SPECIFICATION

This specification defines the specifications for Digilent Video Memory Access IP Core.

Revision Log

Revision #	ROIN	Change	Author	Date
1.0	All	Initial Release	WANG, Tinghui	20FEB2011

DIPS-01-001 Module Overview

- DVMA (**D**igilent **V**ideo **M**emory **A**ccess) IP Core, as shown in Fig. 1, reads 2D video data from VFBC (**V**ideo **F**rame **B**uffer **I**nterface) interface of MPMC (**M**ulti-**P**ort **M**emory **C**ontroller) and transfers the video data into standard XSVI (**X**ilinx **S**treaming **V**ideo **I**nterface).
- Features:
  - 32-bit PLB slave interface
  - Configurable 8, 16, 32-bit VFBC Interface.
  - Configurable XSVI video data bit width.
  - Configurable output video timing parameters.

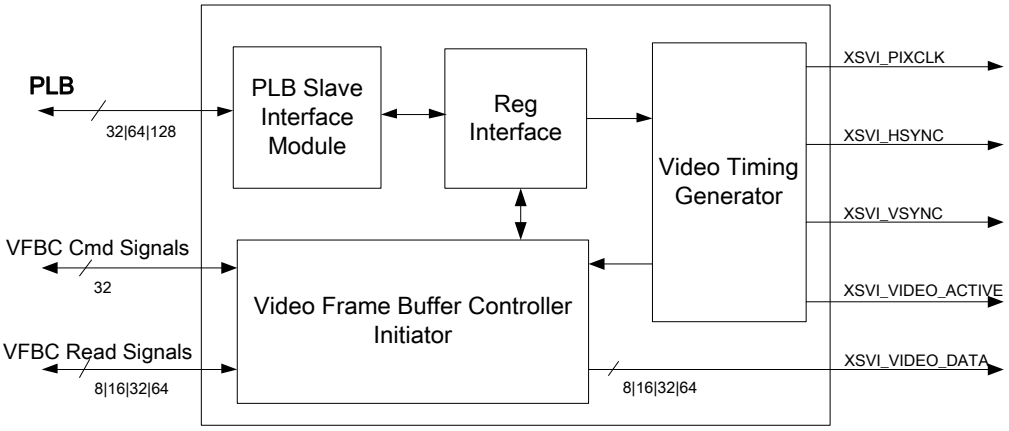

Fig. 1 Block Diagram of VDMA v1.0

DIPS-01-002 I/O Signals

- DVMA I/O Signals are shown in Table 1.

Table 1 DVMA IP Core I/O Signals Description

NO.	SIGNAL NAME	INTERFACE	I/O	INIT ST.	DESCRIPTION
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P4	PLB_PAValid	PLB	I	-	PLB primary address valid
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P8	PLB_size[0 : 3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bits
P12	PLB_SAValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P18	PLB_lockErr	PLB	I	-	PLB lock error
P19	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P20	PLB_rdBurst	PLB	I	-	PLB burst read transfer
P21	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P22	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P23	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P24	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P25	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
P26	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P27	Sl_addrAck	PLB	O	0	Slave address acknowledge
P28	Sl_SSize[0 : 1]	PLB	O	0	Slave data bus size
P29	Sl_wait	PLB	O	0	Slave wait
P30	Sl_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	Sl_wrDAck	PLB	O	0	Slave write data acknowledge
P32	Sl_wrComp	PLB	O	0	Slave write transfer complete
P33	Sl_rdDBus[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	Sl_rdDAck	PLB	O	0	Slave read data acknowledge
P35	Sl_rdComp	PLB	O	0	Slave read transfer complete
P36	Sl_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	Sl_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	Sl_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P39	Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	Sl_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P41	Sl_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	Sl_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
DVMA Signals					
P43	PIXCLK_I	DVMA	I	-	Video Pixel Clock
P44	PLL_LOCKED_I	DVMA	I	-	Pixel Clock PLL Locked
P45	DEBUG_O	DVMA	O	0	Debug Signal Output
VFBC Command Interface Signals					

NO.	SIGNAL NAME	INTERFACE	I/O	INIT ST.	DESCRIPTION
	VFBC_CMD_CLK	VFBC	O	0	VFBC Command Clock
	VFBC_CMD_RESET	VFBC	O	0	VFBC Command Reset
	VFBC_CMD_DATA[31 : 0]	VFBC	O	0	VFBC Command Data
	VFBC_CMD_WRITE	VFBC	O	0	VFBC Command Write Enable
	VFBC_CMD_END	VFBC	O	0	VFBC Command End
	VFBC_CMD_FULL	VFBC	I	-	VFBC Command Full
	VFBC_CMD_ALMOST_FULL	VFBC	I	-	VFBC Command Almost Full
	VFBC_CMD_IDLE	VFBC	I	-	VFBC Command Idle
VFBC Read Interface Signals					
	VFBC_RD_CLK	VFBC	O	0	VFBC Read Data Clock
	VFBC_RD_RESET	VFBC	O	0	VFBC Read Data Reset
	VFBC_RD_READ	VFBC	O	0	VFBC Read Data Read Enable
	VFBC_RD_END_BURST	VFBC	O	0	VFBC Read Data End Burst
	VFBC_RD_FLUSH	VFBC	O	0	VFBC Read Data Flush
	VFBC_RD_DATA [C_VFBC_RDWD_DATA_WIDTH-1:0]	VFBC	I	-	VFBC Read Data
	VFBC_RD_EMPTY	VFBC	I	-	VFBC Read Data Empty
	VFBC_RD_ALMOST_EMPTY	VFBC	I	-	VFBC Read Data Almost Empty
XSVI Signals					
	XSVI_PIXCLK	XSVI	O	0	XSVI Video Clock
	XSVI_HSYNC	XSVI	O	0	XSVI Horizontal Synchronize
	XSVI_VSYNC	XSVI	O	0	XSVI Vertical Synchronize
	XSVI_ACTIVE_VIDEO	XSVI	O	0	XSVI Video Active
	XSVI_VIDEO_DATA [C_NUM_DATA_CHANNELS* C_DATA_WIDTH/(C_DDR_OUT+1)-1:0]	XSVI	O	0	XSVI Video Data

DIPS-01-003 Software Register Mapping

- DVMA core contains the registers listed in Table 3.

Table 2 Register Name and Descriptions of DVMA

REGISTER NAME	ADDRESS	ACCESS
Control Register (CR)	C_DVMA_BASEADDR + 0x00	Read/Write
Frame Width Register (FWR)	C_DVMA_BASEADDR + 0x04	Read/Write
Frame Height Register (FHR)	C_DVMA_BASEADDR + 0x08	Read/Write
Frame Base Address Register (FBAR)	C_DVMA_BASEADDR + 0x0c	Read/Write
Frame Line Stride Register (FLSR)	C_DVMA_BASEADDR + 0x10	Read/Write
Horizontal Synchronize Register (HSR)	C_DVMA_BASEADDR + 0x14	Read/Write
Horizontal Front Porch Register (HFPR)	C_DVMA_BASEADDR + 0x18	Read/Write
Horizontal Back Porch Register (HBPR)	C_DVMA_BASEADDR + 0x1c	Read/Write
Horizontal Total Register (HTR)	C_DVMA_BASEADDR + 0x20	Read/Write
Vertical Synchronize Register (VSR)	C_DVMA_BASEADDR + 0x24	Read/Write
Vertical Front Porch Register (VFPR)	C_DVMA_BASEADDR + 0x28	Read/Write
Vertical Back Porch Register (VBPR)	C_DVMA_BASEADDR + 0x2c	Read/Write
Vertical Total Register (VTR)	C_DVMA_BASEADDR + 0x30	Read/Write

- **Control Register (CR)**

  Bit 31: DVMA Enable (“1” – enable; “0” – disable)

  Bit 0-30: Reserved

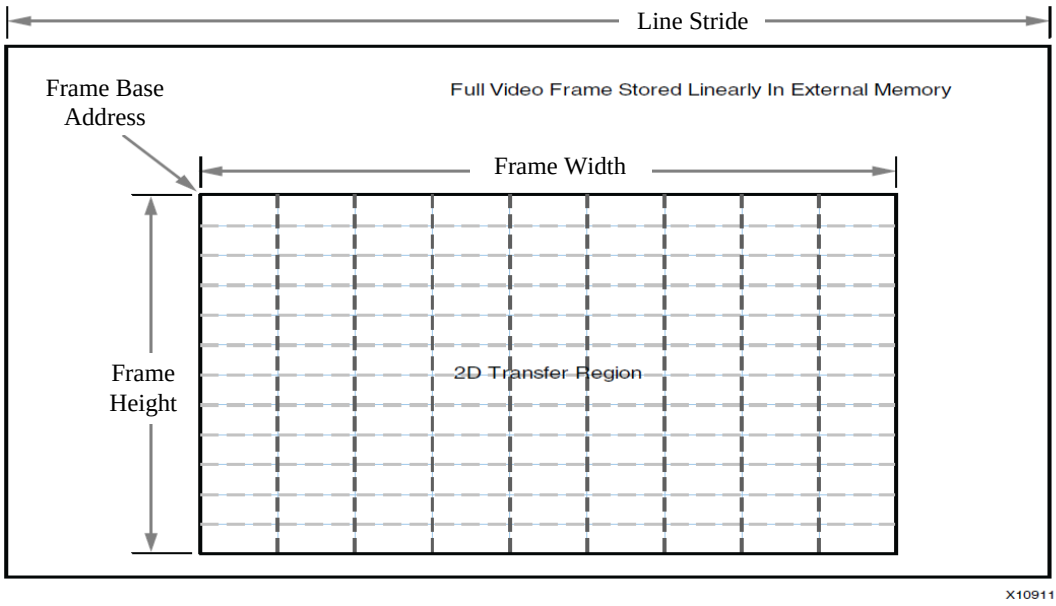

Fig. 2 VFBC 2D Transfer Parameters

- **Frame Width Register (FWR)**

  Width of output frame, counted in pixels (as shown in Fig 2)

- **Frame Height Register (FHR)**

  Height of output frame, counted in lines

- **Frame Base Address Register (FBAR)**

  Base address of output frame in physical memory (only last 31 bits are valid) (as shown in Fig 2)

- **Frame Line Stride Register (FLSR)**

  Number of pixels between the beginning of two adjacent lines in memory (as shown in Fig 2).

- **Horizontal Synchronize Register (HSR)**

  The width of horizontal synchronize signal, counted in pixels (as shown in Fig 3).

- **Horizontal Front Porch Register (HFPR)**

  Number of pixels between the start of Horizontal Synchronize and the end of Horizontal Front Porch (as shown in Fig 3)

- **Horizontal Back Porch Register (HBPR)**

  Number of pixels between the start of Horizontal Synchronize Signal and the beginning of Horizontal Front Porch (as shown in Fig 3)

- **Horizontal Total Register (HTR)**

  Total pixels per line (as shown in Fig 3)

- **Vertical Synchronize Register (VSR)**

  The width of Vertical Synchronize Signal, counted in lines (as shown in Fig 3)

- **Vertical Front Porch Register (VFPR)**

Number of lines between the start of Vertical Synchronize Signal and the end of Vertical Front Porch (as shown in Fig 3)

- **Vertical Back Porch Register (VBPR)**

  Number of pixels between the positive edge of Hsync signal and the beginning of Horizontal Front Porch (as shown in Fig 3)

- **Vertical Total Register (VTR)**

  Total lines per frame (as shown in Fig 3)

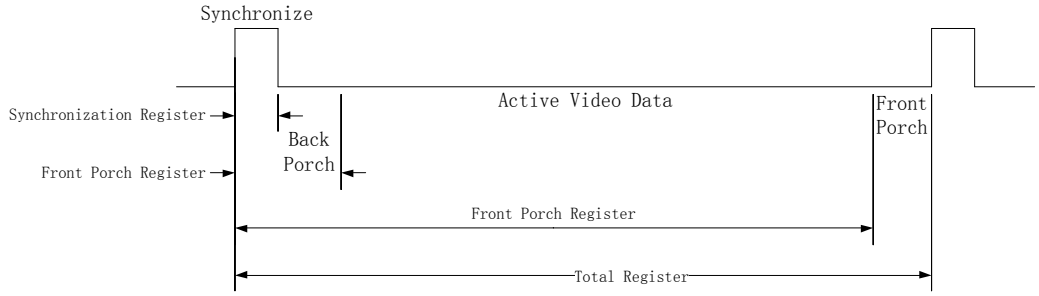

Fig. 3 Register Values for Video Synchronization