25A, No.1369,Dongfang Road, Shanghai
Tel:+86-021-58893151 Fax: +86-021-58894598

DIPS-02: DIGILENT VMODCAM CONTROLLER SPECIFICATION

This specification defines the specifications for Digilent VmodCAM Controller IP Core.

Revision Log

Revision #	ROIN	Change	Author	Date
1.00a	All	Initial Release	WANG, Tinghui	01APR2011

DIPS-02-001 Module Overview

- VmodCAM Controller IP Core, as shown in Fig. 2. The controller takes in all the video signals that camera sensor sends, writes all the data to external memory via VFBC (**V**ideo **F**rame **B**uffer **C**ontroller) interface through MPMC (**M**ulti-**P**ort **M**emory **C**ontroller).
- Features:
  - 32-bit PLB slave interface
  - 8-bit VFBC Interface
  - Support video format whose horizontal synchronization not aligned to burst boundary.
  - Camera frame format auto detect
  - DFL (**D**igilent **F**rame **L**ock) Supported.

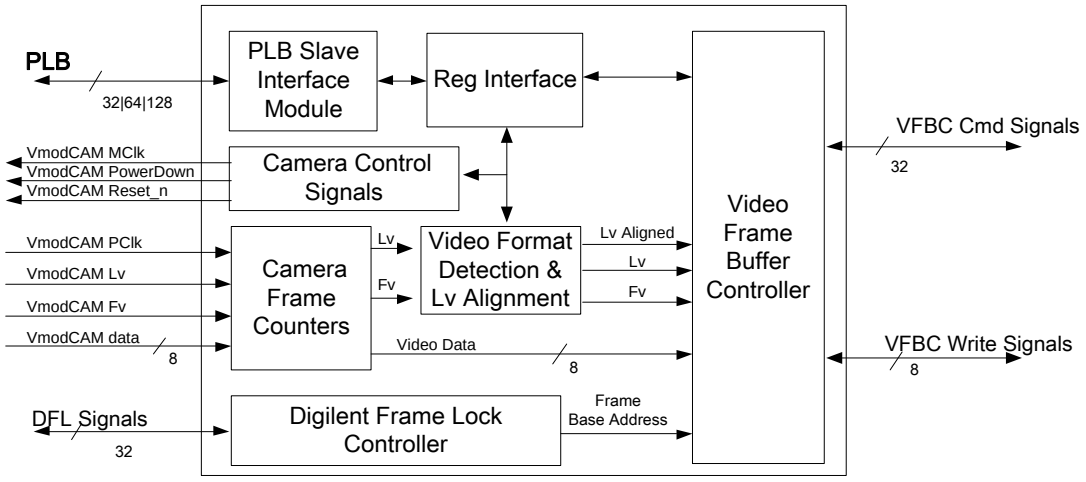

Fig. 1 Block Diagram of VmodCAM Controller v1.0

DIPS-02-002 I/O Signals

- VmodCAM Controller I/O Signals are shown in Table 1.

Table 1 VmodCAM Ctrl IP Core I/O Signals Description

NO.	SIGNAL NAME	INTERFACE	I/O	INIT ST.	DESCRIPTION
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P4	PLB_PAValid	PLB	I	-	PLB primary address valid
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P8	PLB_size[0 : 3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bits
P12	PLB_SAValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P18	PLB_lockErr	PLB	I	-	PLB lock error
P19	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P20	PLB_rdBurst	PLB	I	-	PLB burst read transfer
P21	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P22	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P23	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P24	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P25	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
P26	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P27	Sl_addrAck	PLB	O	0	Slave address acknowledge
P28	Sl_SSize[0 : 1]	PLB	O	0	Slave data bus size
P29	Sl_wait	PLB	O	0	Slave wait
P30	Sl_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	Sl_wrDAck	PLB	O	0	Slave write data acknowledge
P32	Sl_wrComp	PLB	O	0	Slave write transfer complete
P33	Sl_rdDBus[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	Sl_rdDAck	PLB	O	0	Slave read data acknowledge
P35	Sl_rdComp	PLB	O	0	Slave read transfer complete
P36	Sl_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	Sl_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	Sl_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P39	Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	Sl_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P41	Sl_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	Sl_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
Vmodcam_ctrl Signals					
P43	CLK24M_I	Vmodcam_ctrl	I	-	Bypassed to sensor master clock
P44	CLK24M_LOCKED_I	Vmodcam_ctrl	I	-	CLK24M stable flag
P45	DEBUG_O	Vmodcam_ctrl	O	0	Debug Signal Output
VFBC Command Interface Signals					

NO.	SIGNAL NAME	INTERFACE	I/O	INIT ST.	DESCRIPTION
P46	VFBC_CMD_CLK	VFBC	O	0	VFBC Command Clock
P47	VFBC_CMD_RESET	VFBC	O	0	VFBC Command Reset
P48	VFBC_CMD_DATA[31 : 0]	VFBC	O	0	VFBC Command Data
P49	VFBC_CMD_WRITE	VFBC	O	0	VFBC Command Write Enable
P50	VFBC_CMD_END	VFBC	O	0	VFBC Command End
P51	VFBC_CMD_FULL	VFBC	I	-	VFBC Command Full
P52	VFBC_CMD_ALMOST_FULL	VFBC	I	-	VFBC Command Almost Full
P53	VFBC_CMD_IDLE	VFBC	I	-	VFBC Command Idle
VFBC Write Interface Signals					
P54	VFBC_WD_CLK	VFBC	O	0	VFBC Write Data Clock
P55	VFBC_WD_RESET	VFBC	O	0	VFBC Write Data FIFO Reset
P56	VFBC_WD_FLUSH	VFBC	O	0	VFBC Write Data FIFO Flush
P57	VFBC_WD_WRITE	VFBC	O	0	VFBC Write Data FIFO Push
P58	VFBC_WD_DATA [C_VFBC_RDWD_DATA_WIDTH-1:0]	VFBC	O	0	VFBC Write Data FIFO Data
P59	VFBC_WD_END_BURST	VFBC	O	0	VFBC Write Burst End
P60	VFBC_WD_FULL	VFBC	I	-	VFBC Write Data FIFO Full
P61	VFBC_WD_ALMOST_FULL	VFBC	I	-	VFBC Write Data Almost Full
VmodCAM Signals					
P62	CAM_MCLK	VmodCAM	O	0	Master Clock for Camera Sensor
P63	CAM_RST_N	VmodCAM	O	0	Camera Sensor Reset
P64	CAM_POWERDOWN	VmodCAM	O	0	Camera Power Down
P65	CAM_PCLK	VmodCAM	I	-	Pixel Clock from camera
P66	CAM_FV	VmodCAM	I	-	Frame Valid
P67	CAM_LV	VmodCAM	I	-	Line Valid
P68	CAM_DATA [7 : 0]	VmodCAM	I	-	Pixel Data

DIPS-02-003 Software Register Mapping

- DVMA core contains the registers listed in Table 3.

Table 2 Register Name and Descriptions of DVMA

REGISTER NAME	ADDRESS	ACCESS
Control Register (CR)	C_CAMCTRL_BASEADDR + 0x00	Read/Write
Frame Width Register (FWR)	C_CAMCTRL_BASEADDR + 0x04	Read/Write
Frame Height Register (FHR)	C_CAMCTRL_BASEADDR + 0x08	Read/Write
Frame Base Address Register (FBAR)	C_CAMCTRL_BASEADDR + 0x0c	Read/Write
Frame Line Stride Register (FLSR)	C_CAMCTRL_BASEADDR + 0x10	Read/Write
Frame Width Detection Register (FWDR)	C_CAMCTRL_BASEADDR + 0x14	Read Only
Frame Height Detection Register (FHDR)	C_CAMCTRL_BASEADDR + 0x18	Read Only
Frame Rate Detection Register (FRDR)	C_CAMCTRL_BASEADDR + 0x1c	Read Only

- **Control Register (CR)**

  Bit 31: Camera Controller Enable (“1” – enable; “0” – disable)

  Bit 30: DFL Enable (“1” – enable; “0” – disable)

  Bit 29: Set to “1” if image data per line is not 32 words aligned.

  Bit 28~0: Reserved

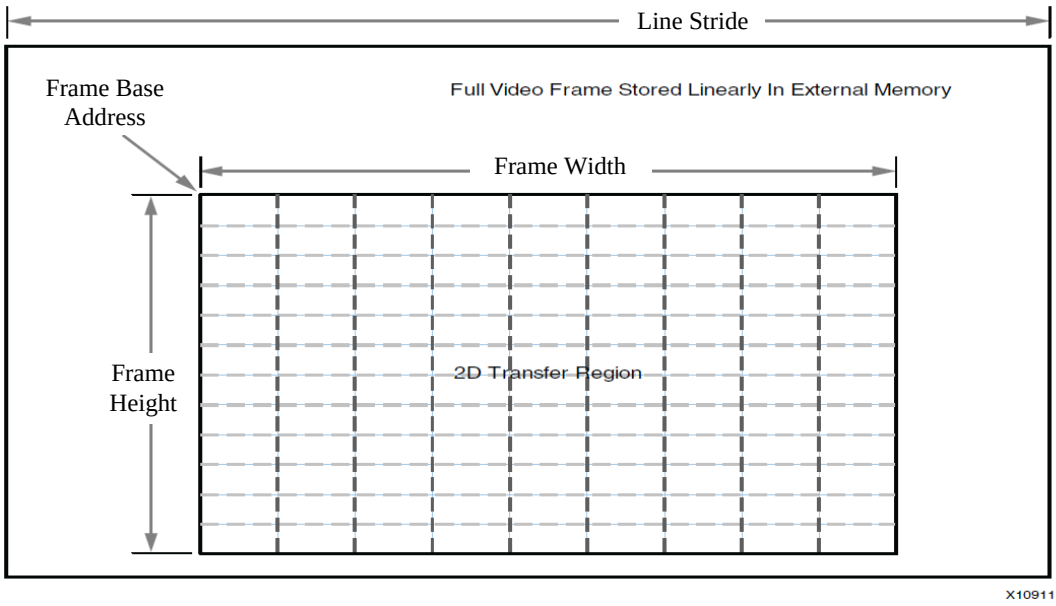

Fig. 2 VFBC 2D Transfer Parameters

- **Frame Width Register (FWR)**

  Width of output frame, counted in pixels (as shown in Fig 2)
- **Frame Height Register (FHR)**

  Height of output frame, counted in lines
- **Frame Base Address Register (FBAR)**

  Base address of output frame in physical memory (only last 31 bits are valid) (as shown in Fig 2)
- **Frame Line Stride Register (FLSR)**

  Number of pixels between the beginning of two adjacent lines in memory (as shown in Fig 2).
- **Frame Width Detection Register (FWDR)**

  Auto-counted width of last transmitted frame
- **Frame Height Detection Register (FHDR)**

  Auto-counted lines of last transmitted frame
- **Frame Rate Detection Register (FRDR)**

  Number of clock cycles per frame, used to calculate frame rate.

DIPS-02-004 Hardware Resource Consumption

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