

# Course Overview

Computer Organization

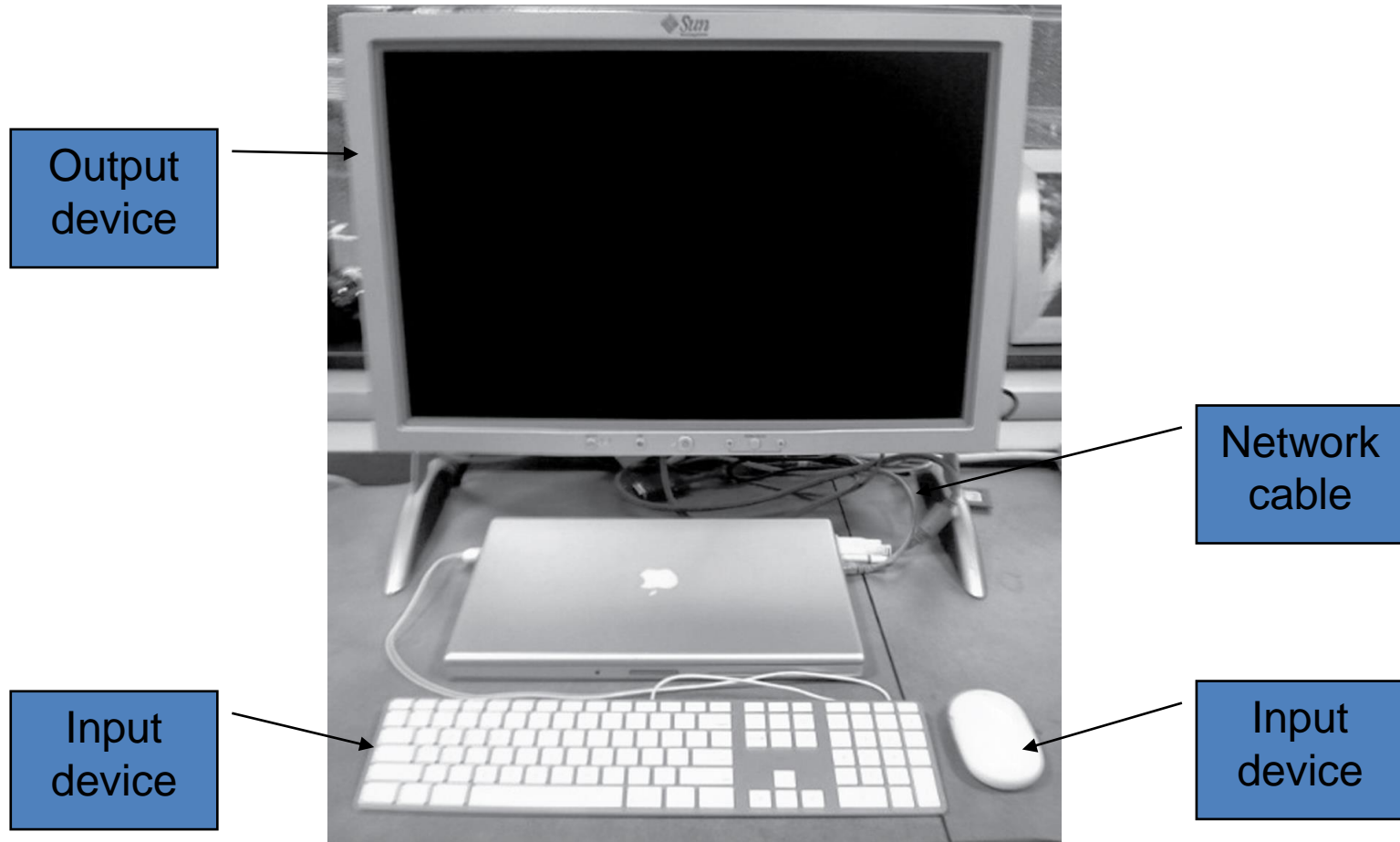
# The Computer Revolution

- Progress in computer technology
  - Reinforced by Moore's Law
- Makes novel applications feasible
  - Computers in automobiles
  - Cell phones
  - Human genome project
  - World Wide Web
  - Search Engines
- Computers are pervasive

# Classes of Computers

- Desktop
    - single user, general purpose, with a typical set up of display, keyboard, and mouse
- Critical: cost, performance

# Desktop Computer



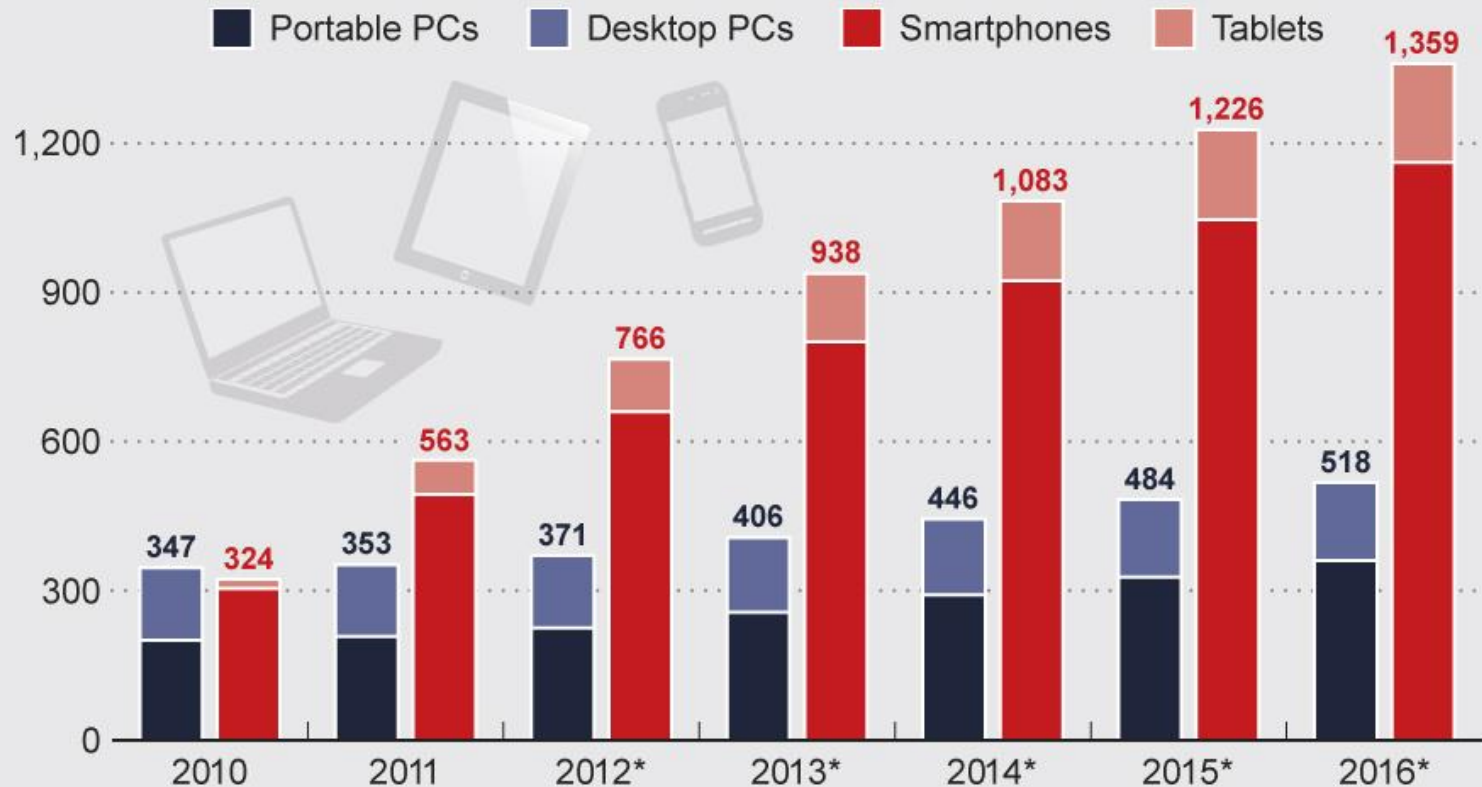
# Classes of Computers

- Desktop
  - single user, general purpose, with a typical set up of display, keyboard, and mouse
  - Critical: **cost, performance**
- Personal Mobile Device (PMD)
  - single user, general purpose, small-size touchscreen
  - Critical: **power, cost**

# The Post-PC Era

## The Post-PC Era Has Arrived

Global smartphone, tablet and PC shipments (in millions)



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  - run larger programs in parallel for multiple users, typically accessed remotely
  - Critical: **performance, capacity, security, reliability**

# Server



Server

Rack





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  - clusters with hundreds to thousands of processors, terabytes of memory and petabytes of storage
  - Critical: performance, capacity, expandability

# Supercomputer



## Frontier,

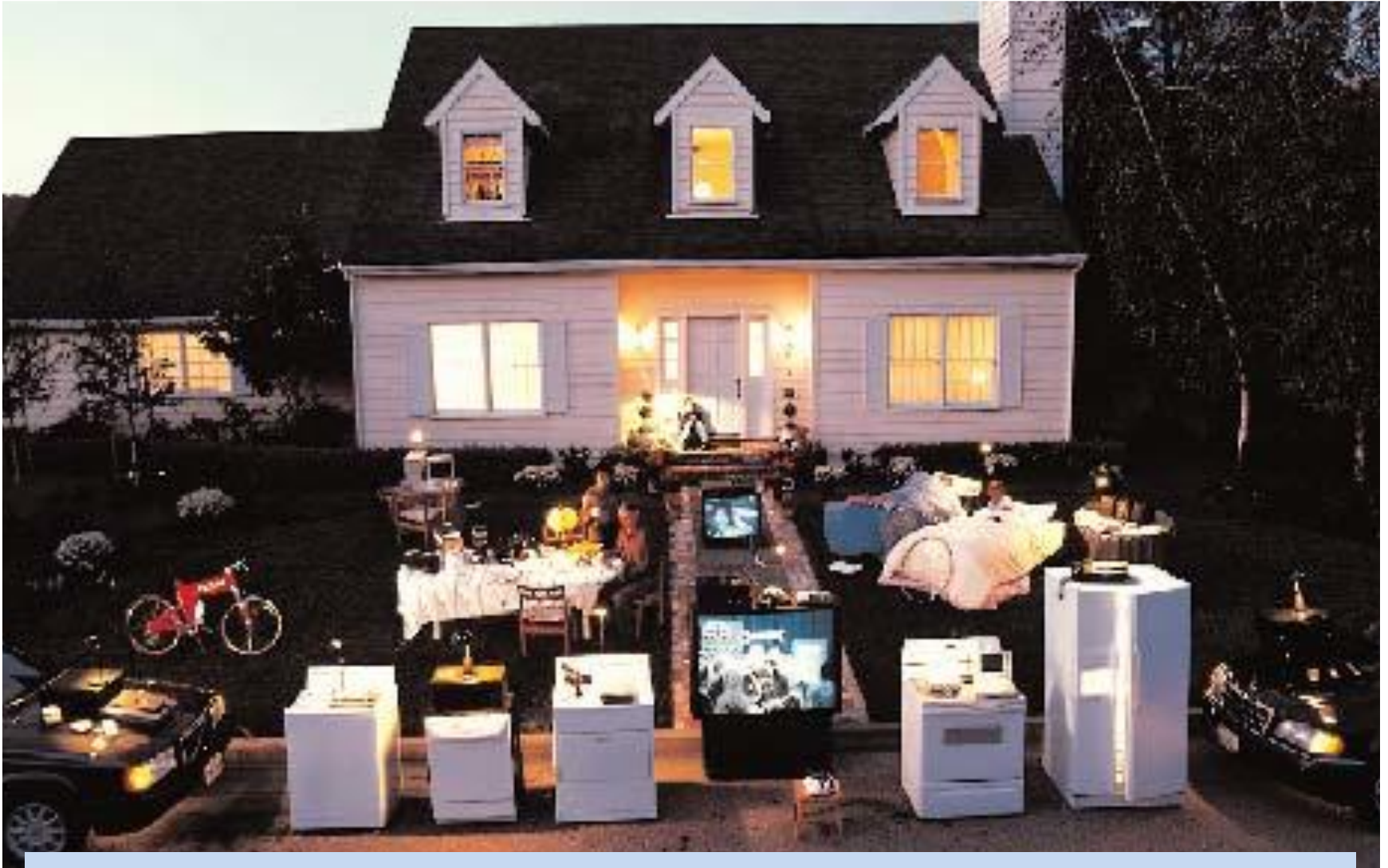
Oak Ridge National Laboratory and the USA Department of Energy @ Tennessee, United States

Currently the world's most powerful supercomputer with 606,208 cores  
9,472 AMD Epyc 7A53s each with 64 core @ 2 GHz and 37,888 Radeon GPUs  
with a peak performance of **1.685 exaFLOPS** power consumption of **21 MW**  
the current lowest power supercomputer with **62.68 gigaflops/watt**

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- Embedded
  - hidden component of a system, running a predefined program
  - Critical: cost, power, performance

# Embedded Computers



Over 99% of processor sales are for embedded systems!

# Issues in Embedded Systems

Specific issues when programming embedded systems:

- Real-time requirements
  - Often worst-case is more important than average-case
- Resource constraints
  - Power and memory
- Reliability
  - Safety critical systems
  - Difficult access
- Diversity
  - Heterogeneity of computing architectures
  - Diverse set of input/output devices

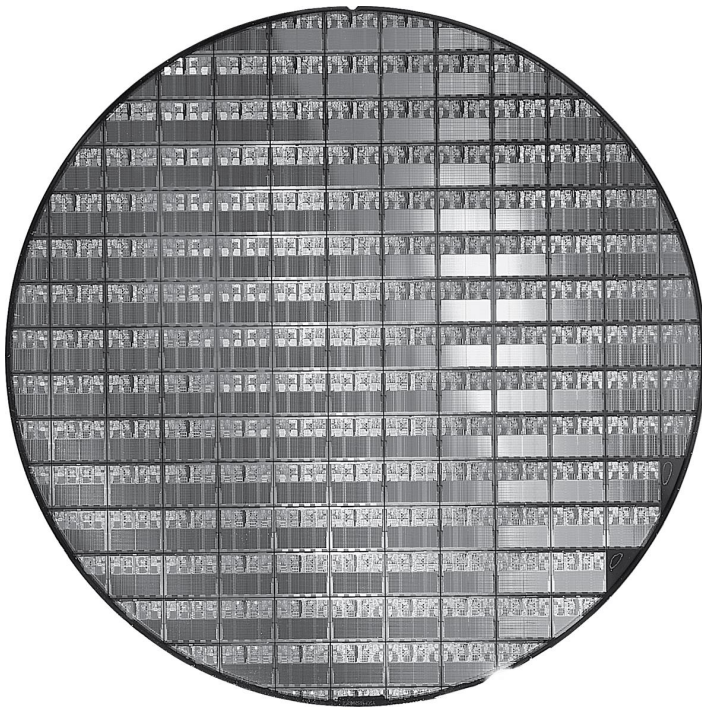
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# Technology Trends

- The transistor density increases about 35% per year.
- The circuits area increases about 10% to 20% per year.
- The number of transistors per circuit increases about 55% per year.

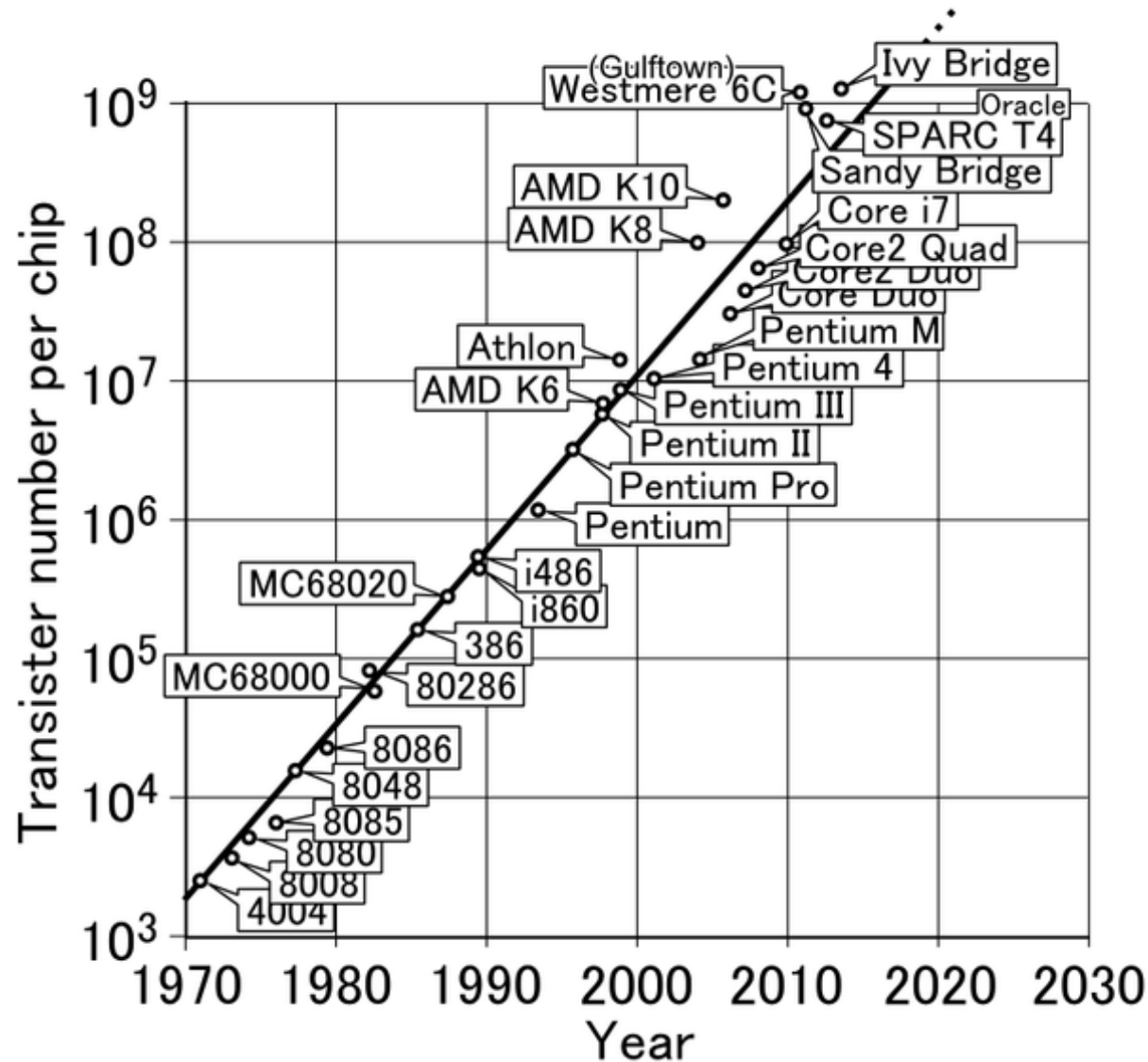


## Moore's Law (1965):

“The number of transistors per square-centimeter of integrated circuit doubles every 18 months.”

- In practice, the density increased about 1,000,000x in the last 45 years!

# Moore's Law in Practice

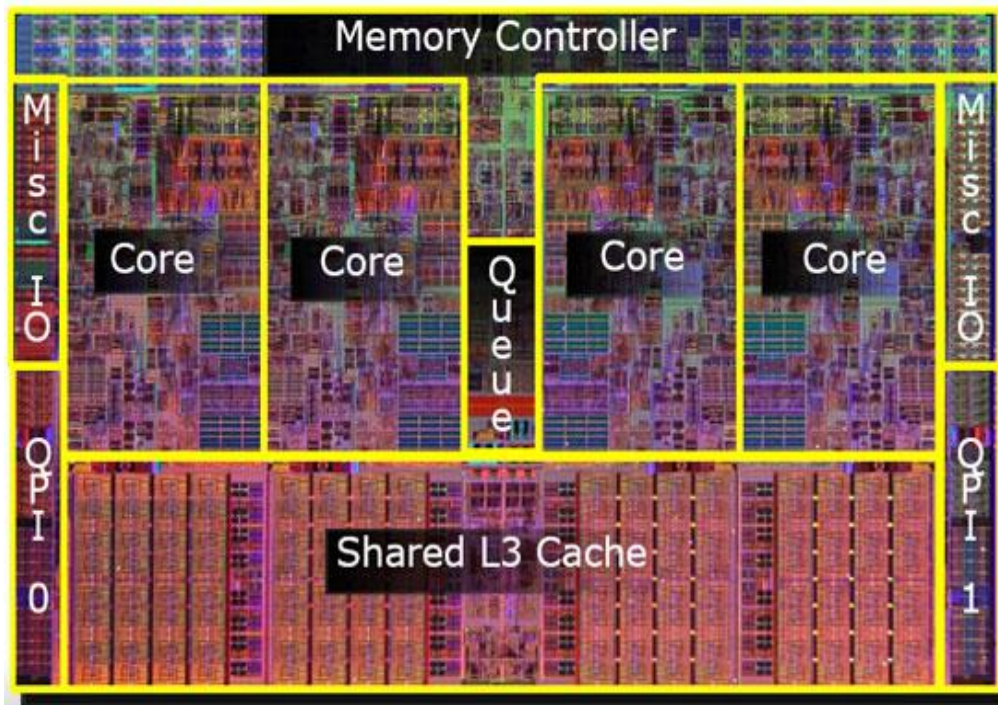




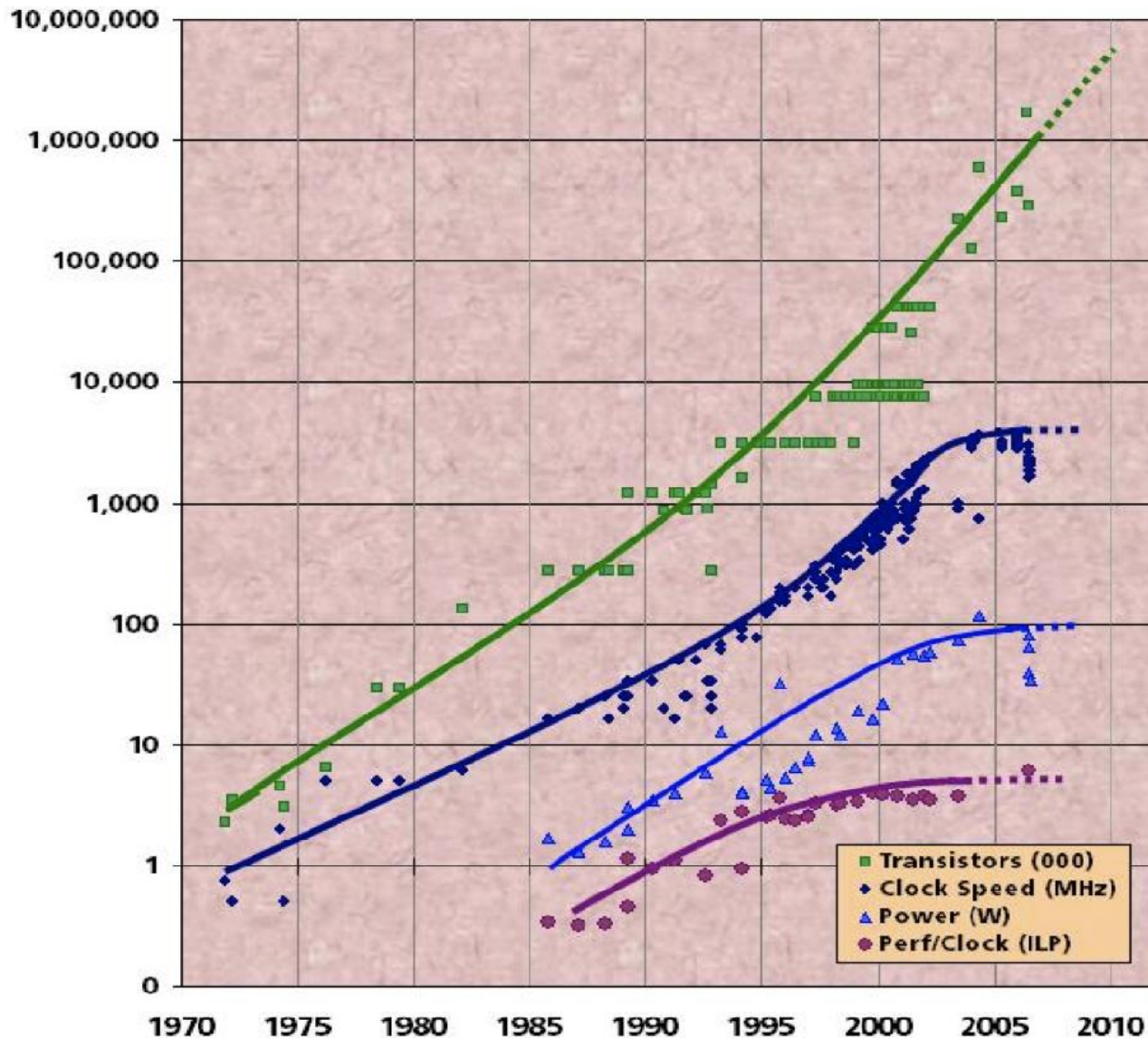
# Inside the Processor

Intel Core i7:

4 processor cores,  $1.3 \times 10^9$  transistors



# Technology Trends



# Power Trends

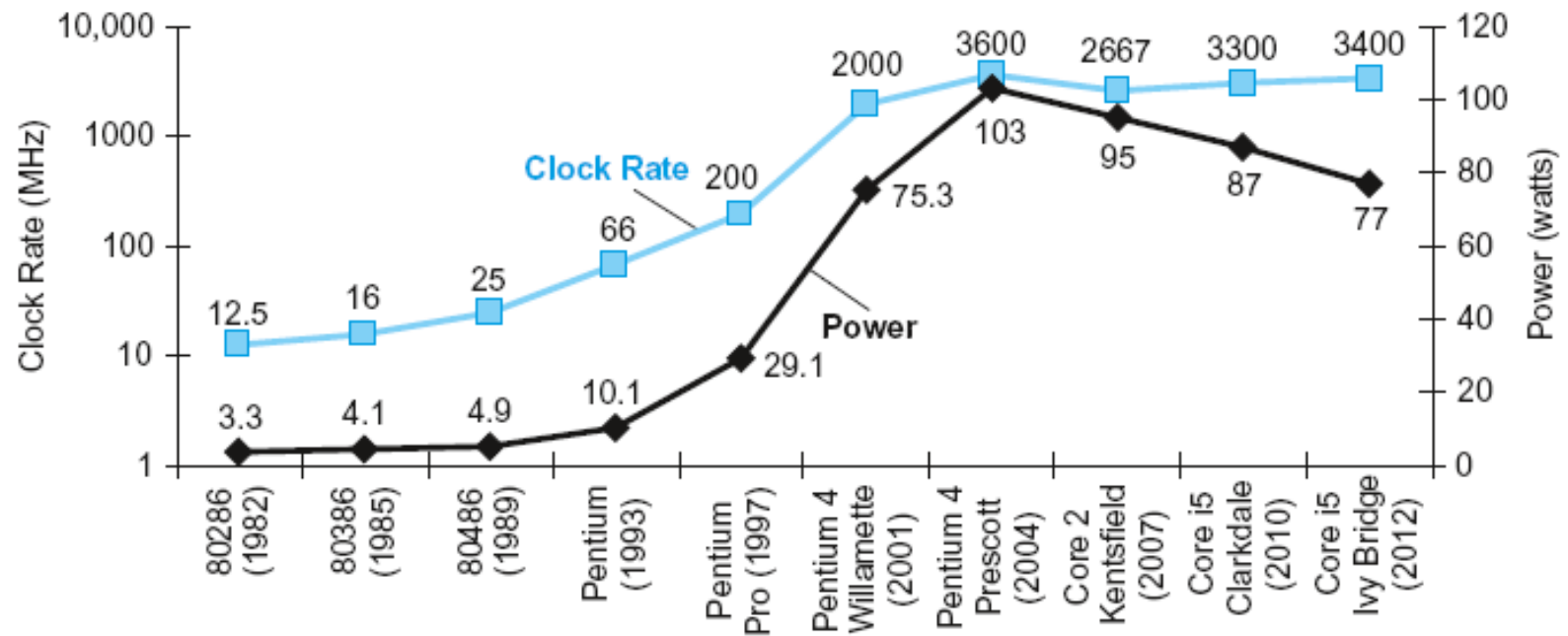
In CMOS IC technology

$$\text{Power} = \text{Capacitive load} \cdot \text{Voltage}^2 \cdot \text{Frequency}$$

×30

5V → 1V

×1000



The power wall!

# Multiprocessors

The power wall:

- can't reduce voltage further
- can't remove more heat

How else can we improve performance?

## ➔ Multicore microprocessors

- More than one processor per chip

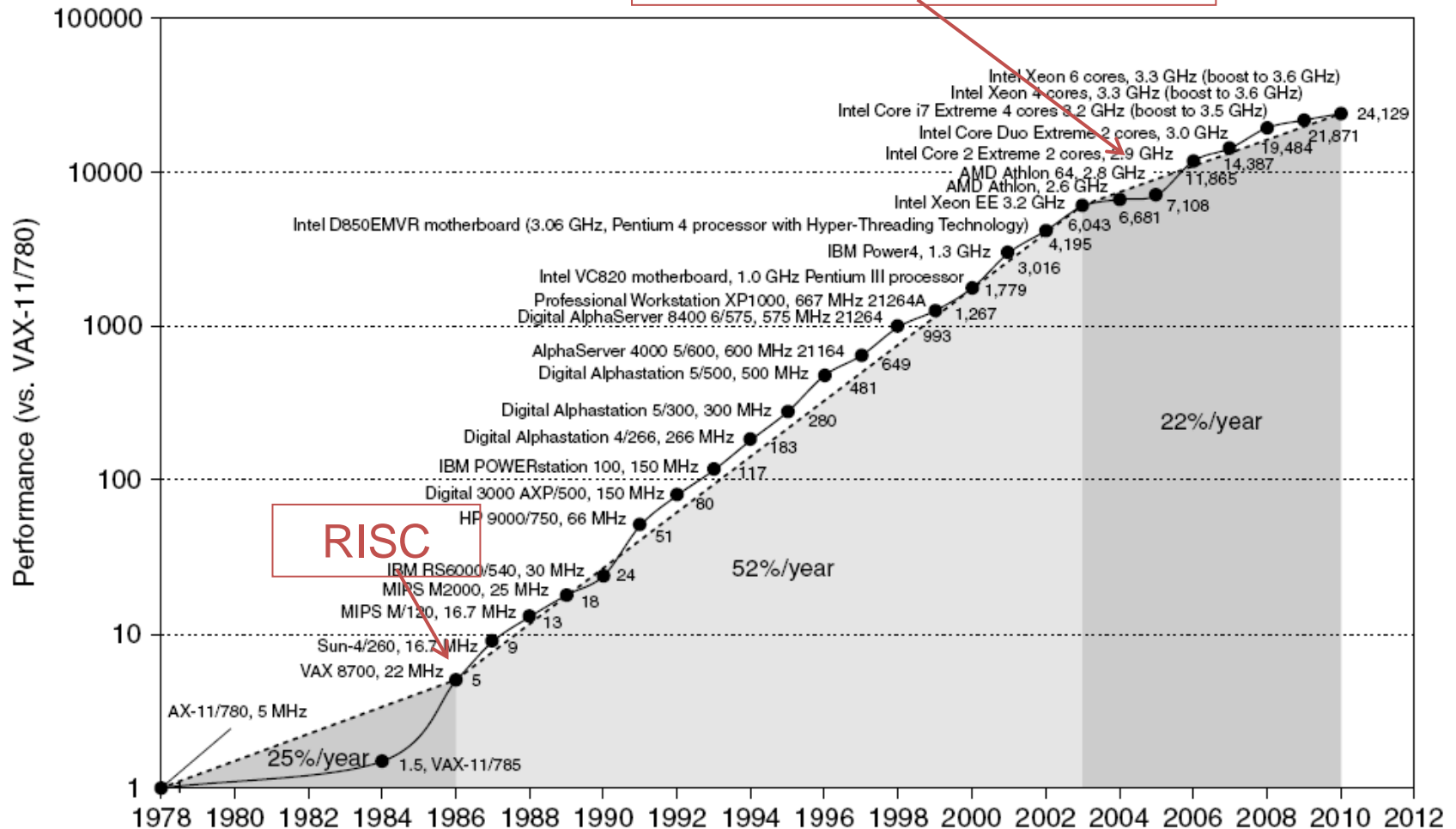
New paradigm!

Requires explicitly parallel programming:

- Compare with instruction level parallelism
  - Hardware executes multiple instructions at once
  - Hidden from the programmer
- Hard to do
  - Programming for performance
  - Load balancing
  - Optimizing communication and synchronization

# Processor Performance

## Move to multi-processor





# Check@home: Trends in Technology

- Integrated circuit technology
  - Transistor density: 35%/year
  - Die size: 10-20%/year
  - Integration overall: 40-55%/year
- DRAM capacity: 25-40%/year (slowing)
- Flash capacity: 50-60%/year
  - 15-20X cheaper/bit than DRAM
- Magnetic disk technology: 40%/year
  - 15-25X cheaper/bit than Flash
  - 300-500X cheaper/bit than DRAM

# Check@home: Bandwidth and Latency

- Bandwidth or throughput
  - Total work done in a given time
  - 10,000-25,000X improvement for processors
  - 300-1200X improvement for memory and disks
- Latency or response time
  - Time between start and completion of an event
  - 30-80X improvement for processors
  - 6-8X improvement for memory and disks

# What You Will Learn

- Architecture of current processors
  - Performance metrics
- Integrated view of the computer system
  - Memory hierarchy
  - Input/Output system
- How to improve program performance
- Features related to embedded systems
- What is parallel processing
- Future trends



# Teaching Staff

Senior Lecturers:

Alameda → Ricardo Chaves @INESC-ID

Taguspark → Alberto Cunha

All relevant information published on **Fénix**.  
Check it frequently.

Couse email:

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Taguspark → [oc-t-leic@tecnico.ulisboa.pt](mailto:oc-t-leic@tecnico.ulisboa.pt) Sub:[OC] ...

# Teaching Staff

## Teaching assistants:

- Diogo Cardoso
- Afonso Fernandes
- Inês Pissarra
- Catarina Bento
- David Valente
- Diogo Dinis
- Hugo Mantinhas
- Vasco Correia
- Guilherme Baracho

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# Class Schedule

	Seg 9/11	Ter 9/12	Qua 9/13	Qui 9/14	Sex 9/15
07:00					
08:00	08:00 - 10:00 T FA3			08:00 - 09:00 L F4	
09:00		09:00 - 10:00 L E8	09:30 - 10:30 T GA3	08:30 - 09:00 L F3	08:30 - 09:00 L F8
10:00	10:00 - 12:00 T VA3	10:30 - 11:30 T GA3		10:00 - 11:00 T VA6	
11:00				11:00 - 12:00 T VA5	
12:00	12:00 - 13:00 L F2	12:00 - 13:00 L F3		12:00 - 13:00 L F8	12:00 - 13:00 L F3
13:00	12:00 - 13:00 L F4	12:00 - 13:00 L F4		12:00 - 13:00 L V1.34	12:00 - 13:00 L V1.11
14:00	12:00 - 13:00 L V1.1	12:00 - 13:00 L Q4			

# Grade assessment

- Final grade =  $70\% \cdot \max\{[\max(\text{MAP45\_a}, \text{Ex\_a}) + \max(\text{MAP45\_b}, \text{Ex\_b})]/2, \text{EE}\} + 30\% \cdot \text{L}$
- MAP1+2 or Recov. Exam , Min. grade = 7.5
- Labs = (L1 + L2 + L3) , Min. grade = 8

## MAP (45 min test):

- mini-Test: October 6 @ 18:00
- mini-Test: October 25 @ 18:00

## Recov. Exam:

- Recov. Exam: November 9 @ 15:30
  - Two part recovery (MAP\_a and/or MAP\_b)

# Grade assessment

## Labs (30%)

- 2 + 1 labs, 15% + 15%
- groups of 3 elements, from the same registration slot
- lab grade defined individually at the oral discussions
- can be reused - grade from labs submitted in the last 2 years (2021/2022)
- Report / Code to be submitted at the beginning on the second practical class of the respective week.

- **Important dates (weeks):**

- **Publication Lab1** : Sep 11 week
- **Publication Lab2** : Sep 18 week
- **Delivery & Demo of Lab 1** : Sep 25 week
- **Publication Lab3** : Sep 25 week
- **Delivery of Lab 2** : Oct 9 week
- **Delivery of Lab 3** : Oct 16 week
- **Oral evaluation** : Oct 23 and Oct 30 Weeks

# Grade assessment

## Labs 1 and 3 (15%)

- Guided work
  - PAPI
  - WinMIPS
- To submit:
  - Report pages with results

## Labs 2 (15%)

- Cache simulator to be written in C code
- Basic simulator and tests are provided
- To submit:
  - 2 page report describing what you did
  - Code (with comments)
  - Results (given the provided Memory times)

# Bibliography

## Main book:

*Computer Organization and Design: The Hardware/Software Interface*

D. Patterson, J. Hennessy

Morgan Kaufmann, 5<sup>th</sup> Edition, 2014, ISBN: 978-0-12-407726-3

## Secondary Bibliography:

- *Structured Computer Organization*  
A. Tanenbaum, T. Austin  
Prentice-Hall, 6<sup>th</sup> Edition, 2013, ISBN: 978-0273769248
- *Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools*  
J. Fisher, P. Faraboschi, C. Young  
Morgan Kaufmann, 4<sup>th</sup> Edition, 2005, ISBN: 978-1558607668
- *Computer Architecture: A Quantitative Approach*  
J. Hennessy, D. Patterson  
Morgan Kaufmann, 5<sup>th</sup> Edition, 2011, ISBN: 978-0123838728

# Next Class

- Review of basic concepts on computer architecture
- Performance metrics



# Course Overview

Computer Organization