Vector Processing

Computer Organization

Thursday, 27 October 2022

Many slides adapted from:
Computer Organization and Design,
Patterson & Hennessy
5th Edition, © 2014, MK
and from Prof. Mary Jane Irwin, PSU

TÉCNICO LISBOA

Summary

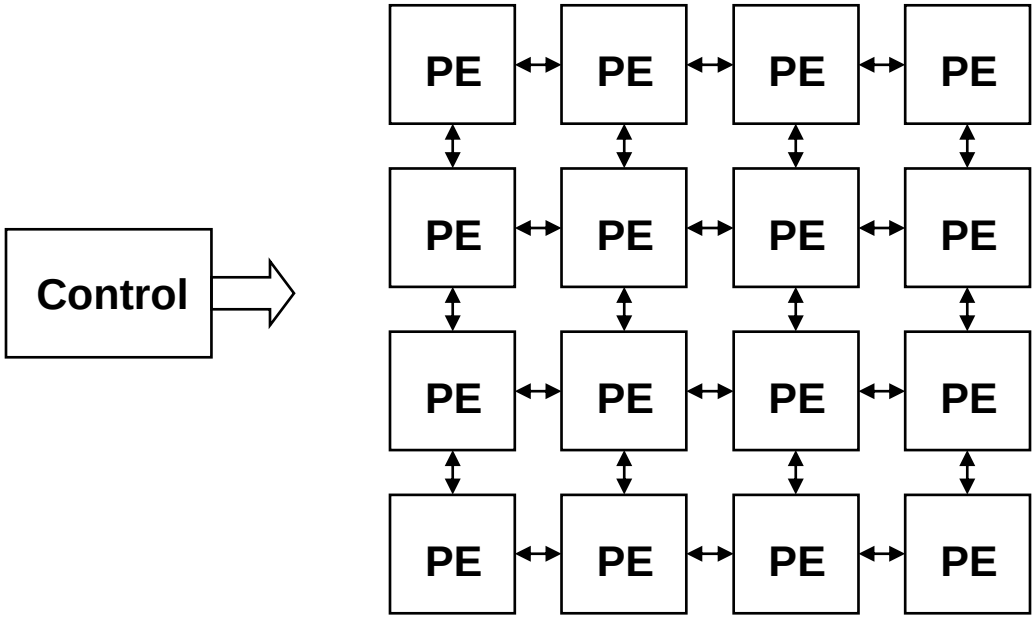
- Previous class
  - Thread-level Parallelism
- Today
  - Vector Processors
    - SIMD
    - GPUs

Flynn's Classification Scheme

- SISD: single instruction, single data stream
  - aka uniprocessor: what we have covered until last class
- SIMD: single instruction, multiple data streams
  - single control unit broadcasting operations to multiple datapaths
- MISD: multiple instruction, single data
  - no such machine
- MIMD: multiple instructions, multiple data streams
  - aka multiprocessors (SMPs, MPPs, clusters, NOWs)

Now obsolete terminology except for . . .

SIMD Processors



- Single control unit (one copy of the code)
- Multiple datapaths (Processing Elements – PEs) running in parallel, executing the same instruction
  - PEs are interconnected (usually via a mesh or torus) and exchange/share data as directed by the control unit
  - Each PE performs the same operation on its own local data

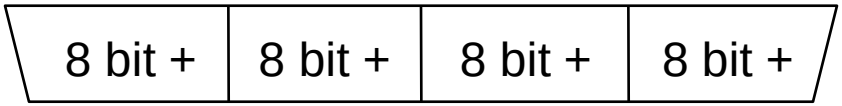
Example SIMD Machines

	Maker	Year	# PEs	# b/ PE	Max memory (MB)	PE clock (MHz)	System BW (MB/s)
Illiac IV	UIUC	1972	64	64	1	13	2,560
DAP	ICL	1980	4,096	1	2	5	2,560
MPP	Goodyear	1982	16,384	1	2	10	20,480
CM-2	Thinking Machines	1987	65,536	1	512	7	16,384
MP-1216	MasPar	1989	16,384	4	1024	25	23,000

- Did SIMDs die out in the early 1990s ??

Multimedia SIMD Extensions

- The most widely used variation of SIMD is found in almost every microprocessor today
  - Basis of MMX and SSE instructions added to improve the performance of multimedia programs
  - A single, wide ALU is partitioned into many smaller ALUs that operate in parallel

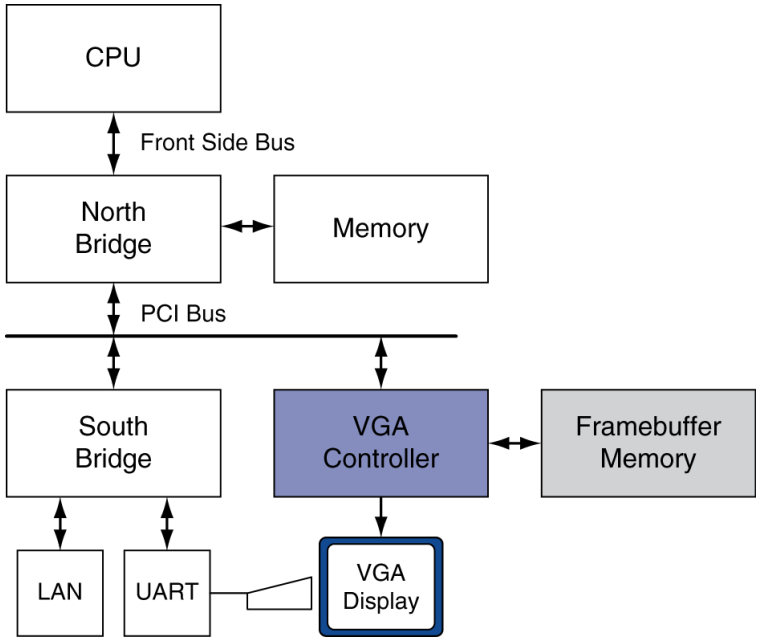


    - Loads and stores are simply as wide as the widest ALU, so the same data transfer can transfer one 32 bit value, two 16 bit values or four 8 bit values
- There are now hundreds of SSE instructions in the x86 to support multimedia operations

History of GPUs

- Early video cards
  - Frame buffer memory with address generation for video output
- 3D graphics processing
  - Originally high-end computers (e.g., SGI)
  - Moore's Law ⇒ lower cost, higher density
  - 3D graphics cards for PCs and game consoles
- Graphics Processing Units
  - Processors oriented to 3D graphics tasks
  - Vertex/pixel processing, shading, texture mapping, rasterization

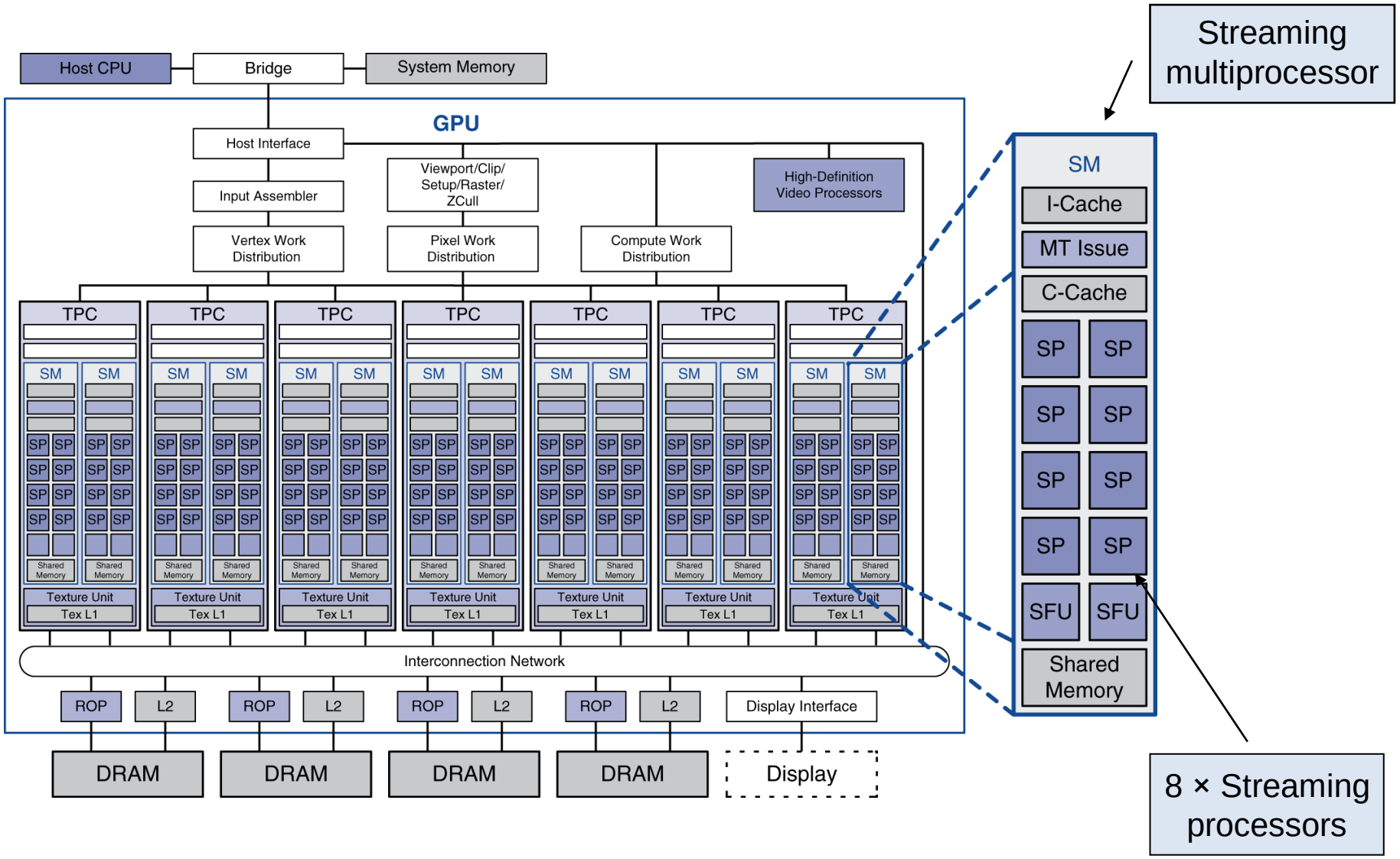
Graphics in the System



GPU Architectures

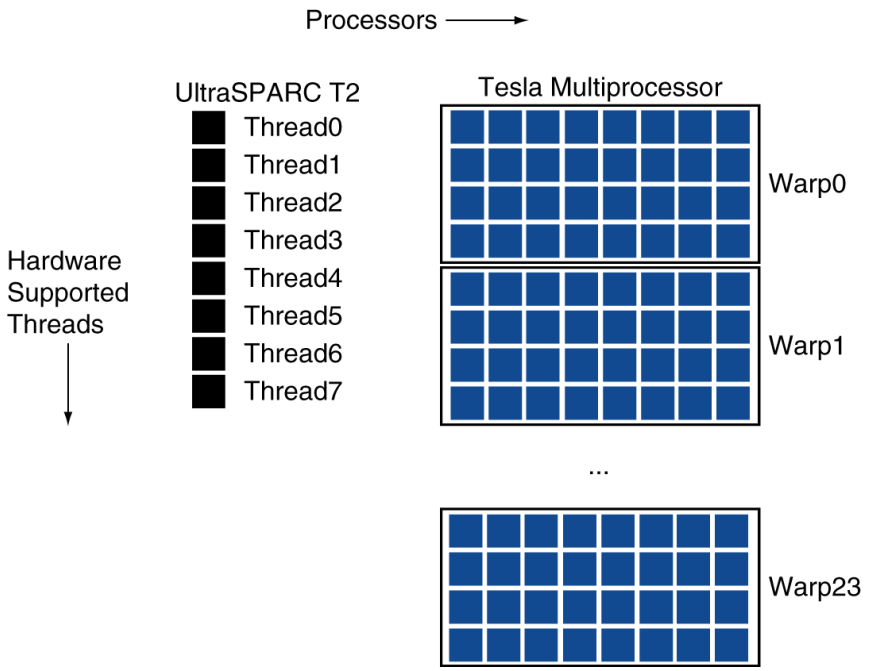
- Processing is highly data-parallel
  - GPUs are highly multithreaded
  - Use thread switching to hide memory latency
    - Less reliance on multi-level caches
  - Graphics memory is wide and high-bandwidth
- Trend toward general purpose GPUs
  - Heterogeneous CPU/GPU systems
  - CPU for sequential code, GPU for parallel code
- Programming languages/APIs
  - DirectX, OpenGL
  - C for Graphics (Cg), High Level Shader Language (HLSL)
  - Compute Unified Device Architecture (CUDA)

Example: NVIDIA Tesla



Example: NVIDIA Tesla

- Streaming Processors
  - Single-precision FP and integer units
  - Each SP is fine-grained multithreaded
- Warp: group of 32 threads
  - Executed in parallel, SIMD style
    - 8 SPs
      × 4 clock cycles
  - Hardware contexts for 24 warps
    - Registers, PCs, …



Classifying GPUs

- Don’t fit nicely into SIMD/MIMD model
  - Conditional execution in a thread allows an illusion of MIMD
    - But with performance degradation
    - Need to write general purpose code with care

	Static: Discovered at Compile Time	Dynamic: Discovered at Runtime
Instruction-Level Parallelism	VLIW	Superscalar
Data-Level Parallelism	SIMD or Vector	**Tesla Multiprocessor**

GPGPU Programming Model

- General Purpose GPU (GPGPU) programming model reflects GPU hardware architecture:
  - GPU seen as massively data parallel co-processor
  - large local memory
  - CPU batches threads to the GPU, together with the data to process
    - GPU threads extremely light-weight (little overhead)
    - GPU requires 1,000s of threads for full efficiency

GPGPU Programming Difficulties

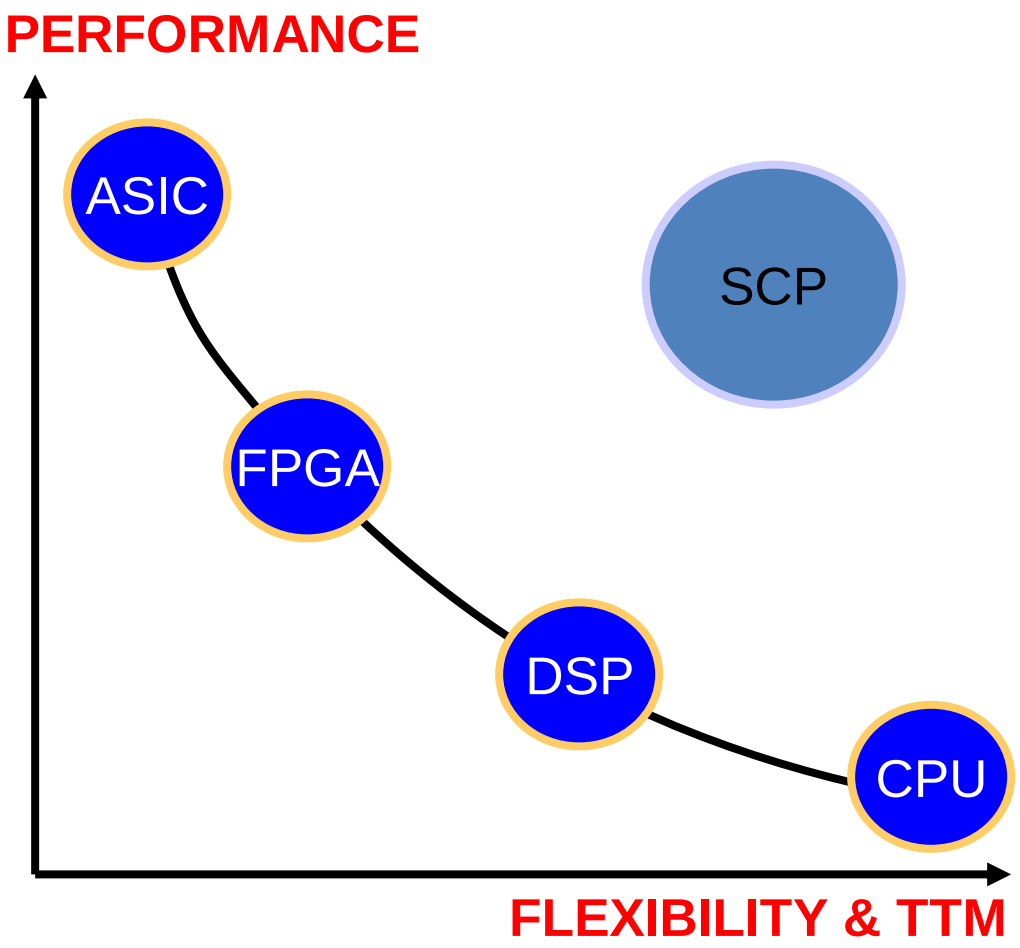
- Drawbacks of the GPGPU approach:
  - Tough learning curve, particularly for those outside graphics
  - Need to SIMD-ipify code
  - Highly constrained memory layout and access model
  - Need for many passes drives up bandwidth consumption

GPGPU Programming Example

```
#include "cuda_runtime.h"

#include "basic_timer.hpp"
#include "idivup.hpp"
#include "mini_cutil.h"

#include <cmath>
#include <cstdio>

// calculates one exp per thread on the GPU.
__global__ void exp_kernel(float * v, int size)
{
    int const t = threadIdx.x +
                  blockIdx.x * blockDim.x;
    if (t < size)
        v[t] = exp(-(float)t) ;
}

int main(int argc, char * argv[])
{
    int n_elem = 10000 ;
    if (argc > 1)  n_elem = atoi(argv[1]);

    // Allocate memory on the device
    float * vector_on_gpu = 0;
    cudaError_t err = cudaMalloc(
        &vector_on_gpu, n_elem*sizeof(float));
    // ... check error
```

```
// Setup execution configuration
dim3 block_size(256) ; // <-- how to pick this number?
dim3 grid_size(idivup(n_elem, block_size.x)) ;

// Launch the GPU computation.
exp_kernel<<<grid_size, block_size>>>(vector_on_gpu, n_elem);

// Wait for the GPU to finish.
err = cudaThreadSynchronize();
// check error ...

float *vector_on_cpu = (float*) malloc(n_elem*sizeof(float));
// Copy the results back to the CPU.
err = cudaMemcpy(
    (void*)vector_on_cpu, /// destination on the CPU
    (void*)vector_on_gpu, /// source on the GPU
    n_elem * sizeof(float), /// copy size
    cudaMemcpyDeviceToHost) ; /// copy direction*//

cudaFree((void*)vector_on_gpu) ; // Free the gpu memory

// Now do the same on the cpu to compare times
basic_timer timer ;
for (int t = 0 ; t < n_elem ; ++t)
    vector_on_cpu[t] = exp(-(float)t) ;
double elapsed = timer.elapsed() ;
printf("cpu time %gs", elapsed) ;

free(vector_on_cpu);
}
```

Performance-Flexibility Curve



ASIC: Application-Specific Integrated Circuit

FPGA: Field-Programmable Gate Array

DSP: Digital Signal Processor

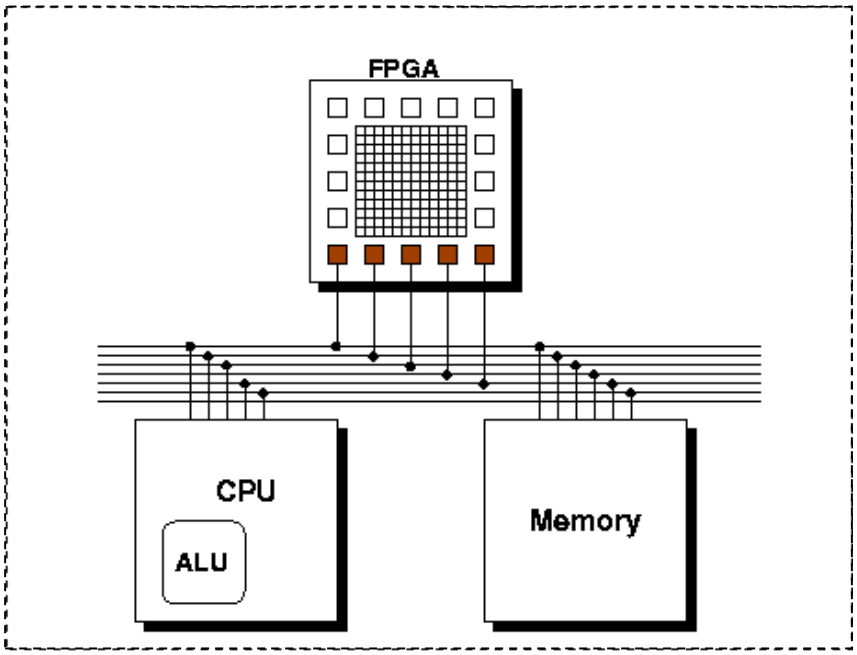
CPU: Central Processing Unit

SCP: Software Configurable Processor

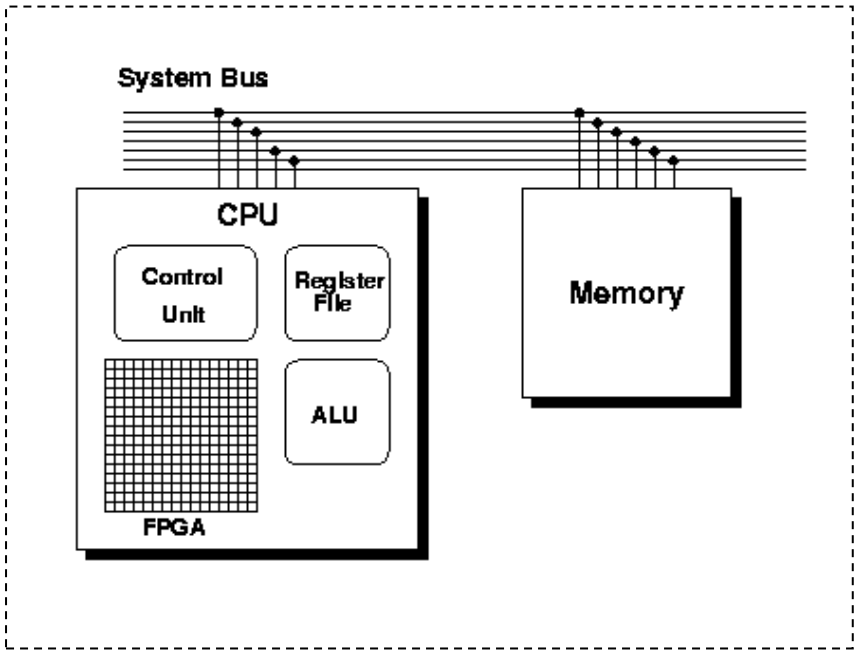
Reconfigurable Co-Processors

Standard processor coupled with embedded programmable logic where application specific functions are dynamically remapped depending on the performed algorithm

1: *Coprocessor model*



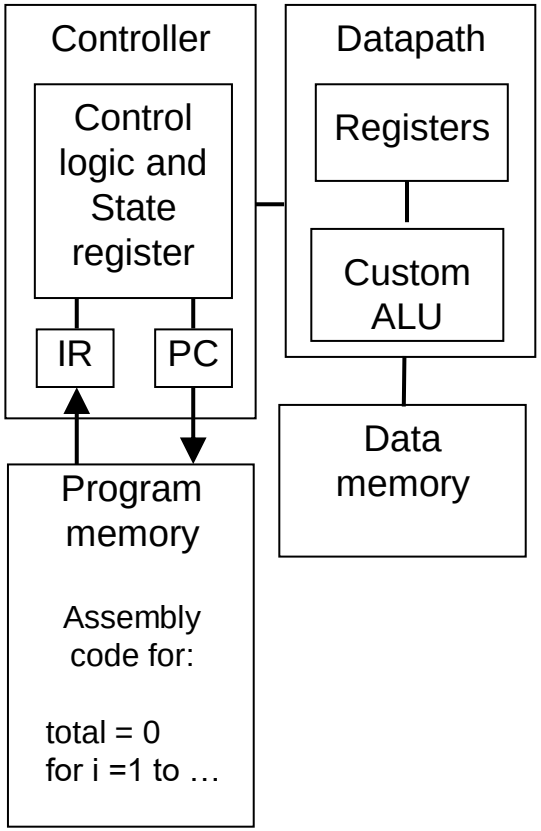
2: *Function unit model*



Application-Specific Processors (ASIPs)

ASIP: Application-Specific Instruction-Set Processor

- Programmable processor optimized for a particular class of applications having common characteristics
  - Compromise between general-purpose and ASIC (custom hardware)
- Features
  - Program memory
  - Optimized datapath
  - Special functional units
- Benefits
  - Some flexibility, good performance, size and power
- Examples
  - DSPs, Video Signal Processors, Network Processors, ...



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