Function generator

Date: Jun 2024

circuify
SEMICONDUCTORS

RTL

Description

Function generator module. The module has a selector to choose between the following four functions:

- Sine
- Cosine
- Triangular
- Square

1) It is possible to set the output signal amplitude with a range from 1 to 4.
2) The function period is 256 clock cycles. Considering a clock frequency of 100MHz (Period = 10ns), each period of the generated function would be 2.56us and its frequency would be approximately 390.6 Khz.
3) When the reset is activated all the initial signals in position 0 which for each signal is as follows:
    - Sine = 0
    - Cosine = Amplitude
    - Square = 0
    - Triangular = 0
4) When the enable is activated the signal at the output will continue at the point where it stopped previously, if a different function is selected, the new waveform will continue in the direction of the LUT where the previous function stopped since all four functions will use the same direction.

Internal sub-modules:

- Adder module
- Multiplication module
- Register module
- LUT
- FSM module
- Mux module

Input	***Size***	***Description***	***Source***
clk	1	Clock	Clock source
rst	1	Asynchronous reset activated	Main input
en_low_i	1	Operation enable. This enable activates the operation of the module when it is set to zero. When en_low_i = 1, the module stops its operation at the point where it was and all signals retain their value until the enable is re-asserted.	full / FIFO
amp_i	3	Amplitude of the function. It can take the integer values 1, 2, 3 and 4. It determines the amplitude of the output signal.	Main input

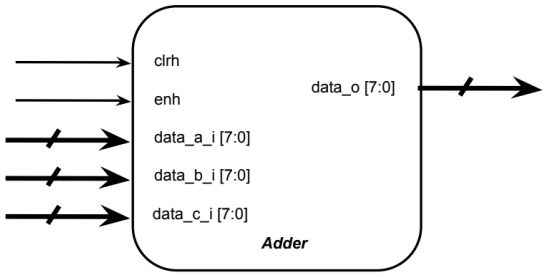
sel_i	2	Function selector Allows to select which waveform is the one we want to obtain in the output of the module. The function of each value of this signal is described in a table below.	Main input

Output	*Size*	*Description*	*Source*
data_o	32	Data of the generated function	Top module
wr_en_o	1	This signal indicates that the data at the output are valid and will be written to a destination memory.	Top module

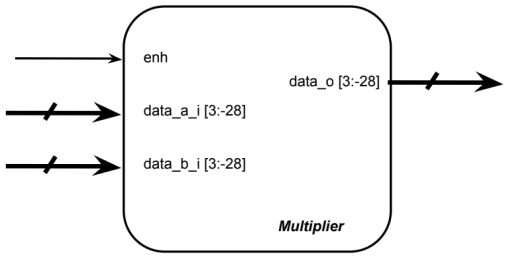
Table 1: Inputs/Outputs description

Sub-modules

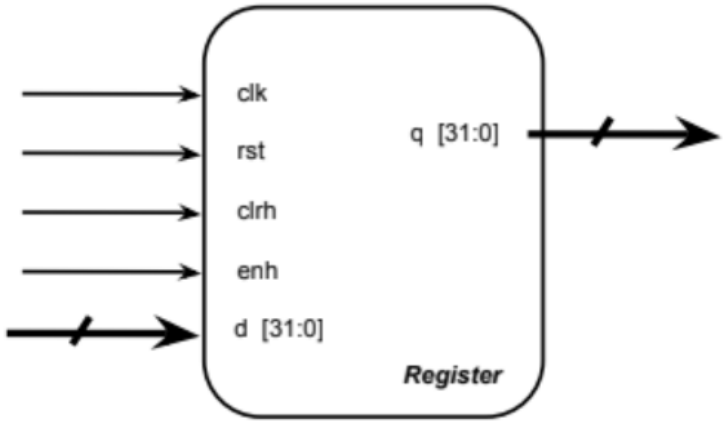
1. Adder: 3-input adder with enable and clear. The addition is performed combinationally when the enable is active. The output is zero when the clear is activated. The clear signal has priority.



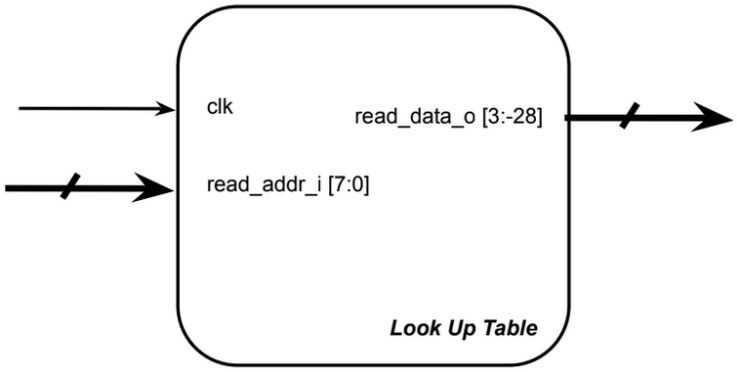
2. Multiplier: 2-input multiplier with enable. Multiplication is performed combinationally when the enable is active.



3. Register: Type D flip flop register activated on positive clock edge with enable active high and clear active high

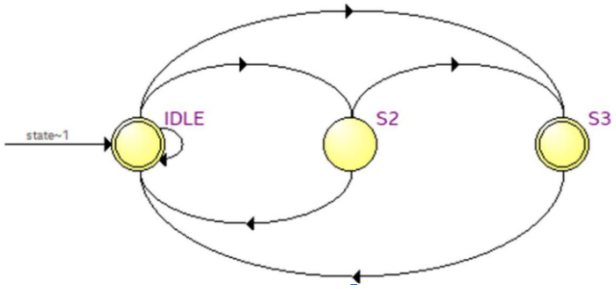


4. LUT: Stores the values of the functions. It only has the operation of reading by means of an address. Its content is loaded by means of a txt file in hexadecimal. The reading is sequential on the positive edge of the clock.

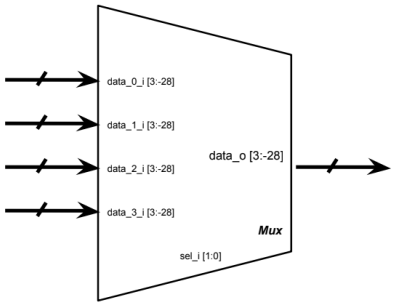


5. FSM: The state machine will control the enable of the internal modules, when to clear the information from the registers and the sequential operation of the whole RTL.

(Diagrama temporal- falta descripcion de los estados)



6. Mux: 4-input 1-output multiplexer with a 2-bit selector switch. The output signal corresponds to the selector value (0 to 3). Inputs and outputs are signed.



sel_i value	Output signal
0	Sine
1	Cosine
2	Triangular
3	Square

Verification

Formal

N#	Name	Description	Code
Assumptions			
1			
Covers			
1			
2			
1			

Table 2: Properties description

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Results

Anexos:

module code