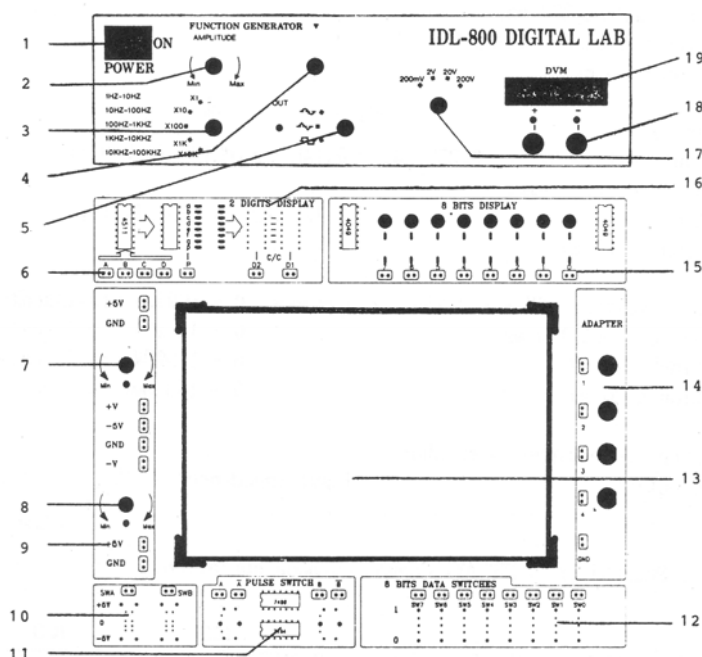


## - Manual de laboratório -

### 1. Placa de Montagens Laboratoriais

As placas de montagens laboratoriais são projectadas para testar circuitos electrónicos e encontram-se particularmente adaptadas ao teste de circuitos digitais. A principal vantagem deste tipo de equipamento prende-se com a disponibilização de forma compacta e organizada de um conjunto de funcionalidades das quais é possível destacar:

- Fonte de alimentação DC (+5V, -5V, 0/+15V, 0/-15V),
- Gerador de sinal,
- Voltímetro;
- *Led's*,
- *Displays* de 7 segmentos;
- *Data Switches*
- ...



**Figura 1** Placa de montagens laboratoriais (exemplo)

## Legenda:

- |  |   |
|--|---|
| 1. Interruptor de alimentação (com led)        | 11. Interruptores lógicos pulsados                  |
| 2. Gerador de Funções – Selector de amplitude  | 12. Interruptores lógicos ( <i>on/off</i> )         |
| 3. Gerador de Funções – Gama de frequências    | 13. Placa <i>deck</i> amovível                      |
| 4. Gerador de Funções – Ajuste de frequências  | 14. Adaptador de pinos a conectores do tipo banana. |
| 5. Gerador de Funções – Forma de onda          |   |
| 6. Entrada BCD (descodificador de 7 segmentos) | 15. Painel de oito <i>led's</i>                     |
| 7. Selector de fonte de tensão (0V a +15V)     | 16. Saída do descodificador de 7 segmentos          |
| 8. Selector de fonte de tensão (0V a -15V)     | 17. Voltímetro digital – gama de tensões            |
| 9. Fonte de tensão DC (+5V)                    | 18. Voltímetro digital – entrada                    |
| 10. Interruptores lógicos (-5V/0V/+5V)         | 19. Voltímetro digital – <i>display</i>             |

## 2. Leitura de datasheets

As folhas com dados (*datasheets*) de circuitos integrados (CI) digitais incluem, além de um esquema lógico e de uma eventual descrição funcional, três grupos de especificações:

- *Absolute Maximum Ratings* (condições máximas de operação) – um exemplo é o valor máximo da tensão de alimentação. São condições (geralmente relativas a valores DC, ou à dissipação) que, a serem excedidas, podem danificar o circuito.
- *DC Characteristics* (características DC) – englobam a corrente de alimentação, os níveis de tensão “0” e “1”, etc.
- *AC Characteristics* (características de temporização) – incluem tempos de propagação, frequência máxima de relógio, etc.

Naturalmente, grande parte das especificações não necessita de um exame muito aprofundado (pois são idênticas para todos os circuitos de uma mesma família – por exemplo, as especificações relativas ao *fan-out* são idênticas para a quase totalidade dos circuitos da família 74LS) o que vai permitir reduzir a leitura do *datasheet* a alguns pontos essenciais.

No entanto, a verificação estrita das especificações indicadas muitas vezes não é

suficiente, uma vez que:

- A apresentação das especificações tende a levar o projectista principiante a conclusões erradas;
- Especificações indirectas;
- Alguns requisitos (que devem ser cumpridos) simplesmente não são incluídos nas especificações; muitas vezes isto acontece por a sua enunciação ser muito complicada ou por apenas dizerem respeito a modos de funcionamento raramente utilizados.

Indicam-se a seguir alguns pontos que justificam um maior cuidado.

## 2.1. Condições máximas de operação

Um exemplo de uma especificação que não consta dos *datasheets* prende-se com a sensibilidade das entradas de circuitos TTL *standard*. A entrada desses circuitos é geralmente constituída por um transístor de emissores múltiplos (cada emissor está directamente ligado a uma entrada). Um diferencial de tensão entre emissores superior a 3 Volts pode provocar a rotura do transístor e, se a corrente que então circular for elevada, o circuito pode ser danificado. Assim, entradas não utilizadas não devem ser ligadas directamente a  $V_{cc}$ , mas sim através de uma resistência de  $1K\Omega$  ou superior. Já a generalidade dos circuitos LS TTL tem entradas por díodos e não requer esta preocupação (notar que há alguns – poucos – circuitos LS TTL que têm entradas de emissores múltiplos).

## 2.2. Características DC

Muitos dos circuitos utilizados são “TTL – compatíveis”. Esta indicação só diz respeito aos níveis de tensão:

$$V_{OL} < 0,4V \quad V_{OH} > 2,4V \quad V_{IL} < 0,8V \quad V_{IH} > 2,0V$$

Note-se que a diferença nas especificações de  $V_{IL}$  e  $V_{IH}$  não quer dizer que os circuitos TTL tenham dois limiares de transição – na realidade, existe apenas um limiar, e a zona de transição é muito curta (poucos décimos de Volt).

Assim, todos os circuitos “TTL–compatíveis” apresentam especificações de tensão idênticas a estas e na maioria dos casos basta uma rápida confirmação ao ler o *datasheet*. Por vezes, surgem excepções importantes – em circuitos NMOS ou CMOS pode acontecer que um ou mais pinos de entrada exijam por exemplo  $V_{IH} > 3,5V$  (isto pode acontecer em relação aos pinos de relógio); é então necessário tomar medidas especiais, como por exemplo aplicar uma resistência de *pull-up* à saída TTL que está a

atacar a entrada de relógio.

Os circuitos “TTL – compatíveis” podem ter especificações de corrente muito divergentes. A família LS TTL, por exemplo, especifica:

$$I_{IL} < 0,4\text{mA} \quad I_{IH} < 20\mu\text{A} \quad I_{OL} > 8\text{mA} \quad I_{OH} > 0,4\text{mA}$$

mas já para a quase totalidade dos circuitos NMOS e CMOS “TTL–compatíveis” são especificados os seguintes valores:

$$I_{IL}, I_{IH} < \pm 10\mu\text{A} \quad I_{OL} > 2\text{mA} \quad I_{OH} > 0,4\text{mA}$$

O *fan-out* poderá estar limitado, não pelas correntes, mas sim pelas capacidades dos pinos, sendo que o único ponto a reter para o exame do *datasheet* consiste em verificar se as especificações dos CI's condizem com as regras gerais acima indicadas ou não.

### 2.3. Características de temporização

O primeiro aspecto a ter em atenção na leitura das características de temporização é de que elas constam de requisitos – isto é, condições que são necessárias para assegurar o correcto funcionamento do CI (por exemplo, não exceder a frequência máxima de relógio) – e de prestações, que são os tempos garantidos pelo CI. Do ponto de vista do projectista, pode-se dizer que ele tem de garantir os requisitos de todos os CI's e que para isso pode contar com as prestações dos (outros) CI's.

Contudo, a maioria dos fabricantes não distingue explicitamente requisitos e prestações, apresentando todas as especificações reunidas numa única tabela. Quando a distinção é feita, aparece uma tabela de *timing requirements* (requisitos) e outra de *timing responses* (prestações).

## 3. Lista de CI's TTL com resumo das *datasheets*

Apresenta-se a seguir uma lista de vários CI's contendo informação pertinente para o projecto e construção de circuitos simples em que se utilizem CI's da família TTL. Ela é constituída por um resumo do que podemos encontrar nos *datasheets* existentes nos “TTL Data Books” editados pelos vários fabricantes de CI's lógicos. A consulta destes livros é indispensável para um conhecimento mais completo das características dos CI's em projectos com requisitos mais exigentes, especialmente quanto às características de temporização.

Esta não pretende ser uma lista exaustiva de todos os CI's TTL existentes, procurando antes abranger os componentes que os alunos irão seleccionar para implementar a solução dos trabalhos propostos.

O aluno deve, durante a preparação do trabalho, fazer uma lista dos CI's que irá precisar com base no resumo que aqui lhe é apresentado. Caso o aluno constate que irá necessitar de um CI TTL inexistente nesta lista resumida e cuja funcionalidade não pode ser obtida a partir dos existentes (nem à custa da mala digital) então não hesite em contactar previamente o professor dando-lhe conta do problema.

## PORTAS LÓGICAS ELEMENTARES

FUNÇÃO	Nº DE ENTRADAS	REFERÊNCIA	PÁGINA
AND	2	'08	7
	3	'11	8
	4	'21	9
NAND	2	'00	10
	3	'10	11
	4	'20	12
	8	'30	13
OR	2	'32	14
NOR	2	'02	15
	3	'27	16
	4	'23 / '25	17
	5	'260	18
NOT	1	'04	19
XOR	2	'86	20

## FLIP-FLOPS

FUNÇÃO	Nº DE ENTRADAS	REFERÊNCIA	PÁGINA
Flip-flop D	2	'74	21
	4	'175	22
Flip-flop J-K	2	'73	23
	2	'76	24
	2	'78	25
	2	'107	26
	2	'109	27
	2	'114	28

## MULTIPLEXERS

FUNÇÃO	Nº DE ENTRADAS	REFERÊNCIA	PÁGINA
Mux 2:1	2	'157	29
Mux 4:1	4	'153	30
Mux 8:1	8	'151	31

## CONTADORES

FUNÇÃO	Nº DE ENTRADAS	REFERÊNCIA	PÁGINA
Contador	0	'93	33
Contador	4	'163	35

FUNÇÃO: AND  
 REFERÊNCIA: '08  
 Nº DE ITENS POR CI: 4

# TYPES SN5408, SN54LS08, SN54S08, SN7408, SN74LS08, SN74S08 QUADRUPLE 2-INPUT POSITIVE-AND GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7408, SN74LS08 and SN74S08 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

## logic diagram (each gate)

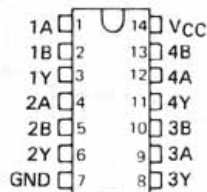


## positive logic

$$Y = A \cdot B \text{ or } Y = \overline{\overline{A} + \overline{B}}$$

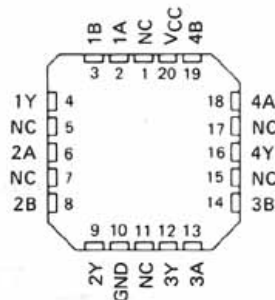
SN5408, SN54LS08, SN54S08 ... J OR W PACKAGE  
 SN7408 ... J OR N PACKAGE  
 SN74LS08, SN74S08 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS08, SN54S08 ... FK PACKAGE  
 SN74LS08, SN74S08

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

FUNÇÃO: AND  
REFERÊNCIA: '11  
Nº DE ITENS POR CI: 3

**TYPES SN54LS11, SN54S11  
SN74LS11, SN74S11  
TRIPLE 3-INPUT POSITIVE-AND GATES**  
REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

These devices contain three independent 3-input AND gates.

The SN54LS11 and SN54S11 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS11, and SN74S11 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE (each gate)**

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

3

**logic diagram (each gate)**



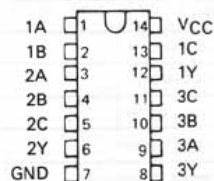
TTL DEVICES

**positive logic**

$$Y = A \cdot B \cdot C \text{ or } Y = \overline{\overline{A} + \overline{B} + \overline{C}}$$

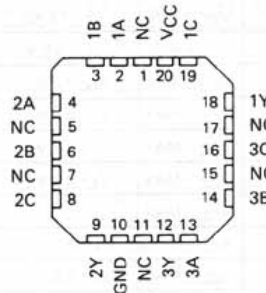
**SN54LS11, SN54S11 ... J OR W PACKAGE  
SN74LS11, SN74S11 ... D, J OR N PACKAGE**

**(TOP VIEW)**



**SN54LS11, SN54S11 ... FK PACKAGE  
SN74LS11, SN74S11**

**(TOP VIEW)**



NC - No internal connection

3-56

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**TEXAS  
INSTRUMENTS**



FUNÇÃO: AND  
 REFERÊNCIA: '21  
 Nº DE ITENS POR CI: 2

## TYPES SN54LS21, SN74LS21 DUAL 4-INPUT POSITIVE-AND GATES

REVISED APRIL 1985

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent 4-input AND gates.

The SN54LS21 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS21 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

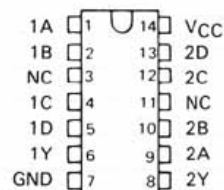
### logic diagram (each gate)



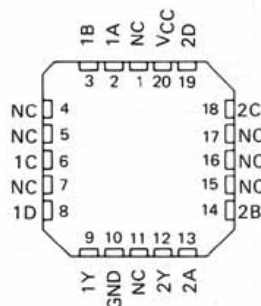
### positive logic

$$Y = A \cdot B \cdot C \cdot D \text{ or } Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$$

SN54LS21 ... J OR W PACKAGE  
 SN74LS21 ... D, J OR N PACKAGE  
 (TOP VIEW)



SN54LS21 ... FK PACKAGE  
 SN74LS21  
 (TOP VIEW)



NC - No internal connection

**FUNÇÃO:** NAND

**REFERÊNCIA:** '00

**Nº DE ITENS POR CI:** 4

**TYPES SN5400, SN54L00, SN54LS00, SN54S00,  
SN7400, SN74LS00, SN74S00  
QUADRUPLE 2-INPUT POSITIVE-NAND GATES**

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

These devices contain four independent 2-input NAND gates.

The SN5400, and SN54LS00, and SN54S00 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7400, SN74LS00, and SN74S00 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

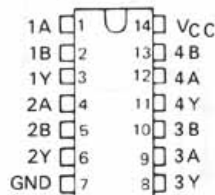
**logic diagram (each gate)**



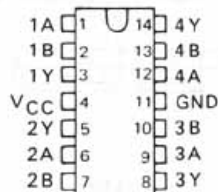
**positive logic**

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

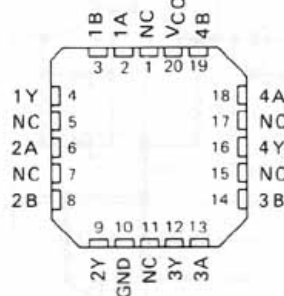
**SN5400 ... J PACKAGE**  
**SN54LS00, SN54S00 ... J OR W PACKAGE**  
**SN7400 ... J OR N PACKAGE**  
**SN74LS00, SN74S00 ... D, J OR N PACKAGE**  
 (TOP VIEW)



**SN5400 ... W PACKAGE**  
 (TOP VIEW)



**SN54LS00, SN54S00 ... FK PACKAGE**  
**SN74LS00, SN74S00**  
 (TOP VIEW)



NC - No internal connection

**3**

**TTL DEVICES**

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**TEXAS  
INSTRUMENTS**

3-3

**FUNÇÃO:** NAND

**REFERÊNCIA:** '10

**Nº DE ITENS POR CI:** 3

**TYPES SN5410, SN54LS10, SN54S10  
SN7410, SN74LS10, SN74S10  
TRIPLE 3-INPUT POSITIVE-NAND GATES**  
REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

These devices contain three independent 3-input NAND gates.

The SN5410, SN54LS10 and SN54S10 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7410, SN74LS10 and SN74S10 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE (each gate)**

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

**logic diagram (each gate)**

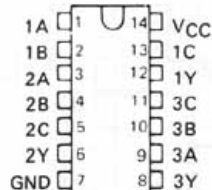


**positive logic**

$$Y = \overline{A \cdot B \cdot C} \text{ or } Y = \overline{A} + \overline{B} + \overline{C}$$

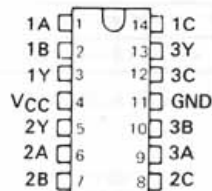
**SN5410 ... J PACKAGE**  
**SN54LS10, SN54S10 ... J OR W PACKAGE**  
**SN7410 ... J OR N PACKAGE**  
**SN74LS10, SN74S10 ... D, J OR N PACKAGE**

**(TOP VIEW)**



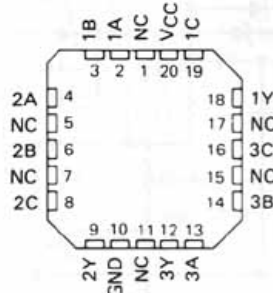
**SN5410 ... W PACKAGE**

**(TOP VIEW)**



**SN54LS10, SN54S10 ... FK PACKAGE**  
**SN74LS10, SN74S10**

**(TOP VIEW)**



NC - No internal connection

**3**

**TTL DEVICES**

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**TEXAS  
INSTRUMENTS**

3-51

**FUNÇÃO:** NAND

**REFERÊNCIA:** '20

**Nº DE ITENS POR CI:** 2

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

These devices contain two independent 4-input NAND gates.

The SN5420, SN54LS20 and SN54S20 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7420, SN74LS20 and SN74S20 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

#### logic diagram (each gate)



#### positive logic

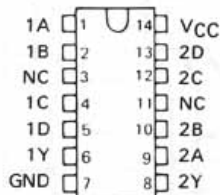
$$Y = \overline{A \cdot B \cdot C \cdot D} \text{ or } Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$

### TYPES SN5420, SN54LS20, SN54S20 SN7420, SN74LS20, SN74S20 DUAL 4-INPUT POSITIVE-NAND GATES

REVISED DECEMBER 1983

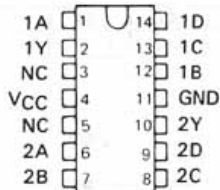
SN5420 ... J PACKAGE  
SN54LS20, SN54S20 ... J OR W PACKAGE  
SN7420 ... J OR N PACKAGE  
SN74LS20, SN74S20 ... D, J OR N PACKAGE

(TOP VIEW)



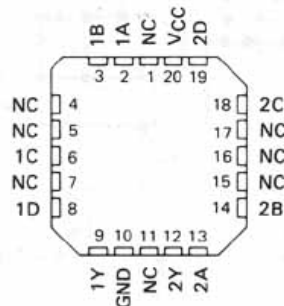
SN5420 ... W PACKAGE

(TOP VIEW)



SN54LS20, SN54S20 ... FK PACKAGE  
SN74LS20, SN74S20

(TOP VIEW)



NC - No internal connection

3  
TTL DEVICES

**FUNÇÃO:** NAND

**REFERÊNCIA:** '30

**Nº DE ITENS POR CI:** 1

**TYPES SN5430, SN54LS30, SN54S30,  
SN7430, SN74LS30, SN74S30  
8-INPUT POSITIVE-NAND GATES**

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

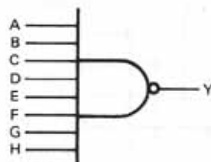
These devices contain a single 8-input NAND gate.

The SN5430, SN54LS30, and SN54S30 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7430, SN74LS30, and SN74S30 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE**

INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

**logic diagram**

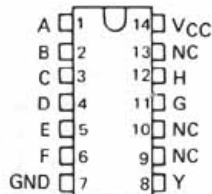


**positive logic**

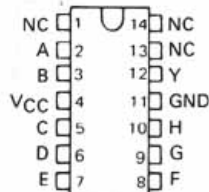
$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \quad \text{or}$$

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

**SN5430 ... J PACKAGE**  
**SN54LS30, SN54S30 ... J OR W PACKAGE**  
**SN7430 ... J OR N PACKAGE**  
**SN74LS30, SN74S30 ... D, J OR N PACKAGE**  
**(TOP VIEW)**

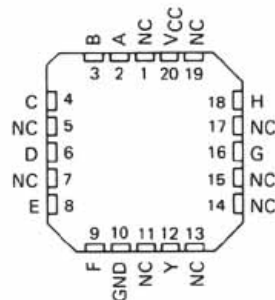


**SN5430 ... W PACKAGE**  
**(TOP VIEW)**



**SN54LS30, SN54S30 ... FK PACKAGE**  
**SN74LS30, SN74S30**

**(TOP VIEW)**



NC - No internal connection

**3**

**TTL DEVICES**

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**TEXAS  
INSTRUMENTS**

3-123

FUNÇÃO: OR  
 REFERÊNCIA: '32  
 Nº DE ITENS POR CI: 4

# TYPES SN5432, SN54LS32, SN54S32, SN7432, SN74LS32, SN74S32 QUADRUPLE 2-INPUT POSITIVE-OR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain four independent 2-input OR gates.

The SN5432, SN54LS32 and SN54S32 are characterized for operation over the full military range of -55°C to 125°C. The SN7432, SN74LS32 and SN74S32 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

## logic diagram (each gate)

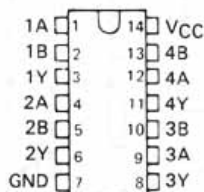


## positive logic

$$Y = A + B \text{ or } Y = \overline{\overline{A} \cdot \overline{B}}$$

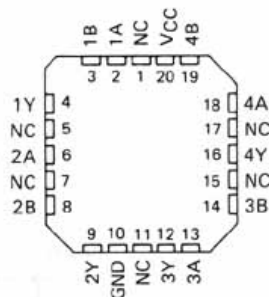
SN5432, SN54LS32, SN54S32 ... J OR W PACKAGE  
 SN7432 ... J OR N PACKAGE  
 SN74LS32, SN74S32 ... D, J or N PACKAGE

(TOP VIEW)



SN54LS32, SN54S32 ... FK PACKAGE  
 SN74LS32, SN74S32

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

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TEXAS  
 INSTRUMENTS

3-133

FUNÇÃO: NOR

REFERÊNCIA: '02

Nº DE ITENS POR CI: 4

**TYPES SN5402, SN54LS02, SN54S02,  
SN7402, SN74LS02, SN74S02**  
**QUADRUPLE 2-INPUT POSITIVE-NOR GATES**  
REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

**description**

These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02 and SN54S02 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7402, SN74LS02 and SN74S02 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**FUNCTION TABLE (each gate)**

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

**3**

**logic diagram (each gate)**



positive logic

$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A + B}$$

**TTL DEVICES**

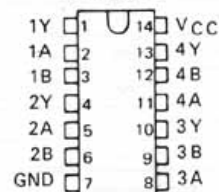
**SN5402 ... J PACKAGE**

SN54LS02, SN54S02 ... J OR W PACKAGE

SN7402 ... J OR N PACKAGE

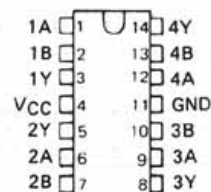
SN74LS02, SN74S02 ... D, J OR N PACKAGE

(TOP VIEW)



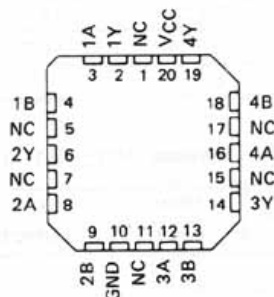
**SN5402 ... W PACKAGE**

(TOP VIEW)



**SN54LS02, SN54S02 ... FK PACKAGE**  
**SN74LS02, SN74S02**

(TOP VIEW)



NC - No internal connection

FUNÇÃO: NOR

REFERÊNCIA: '27

Nº DE ITENS POR CI: 3

# TYPES SN5427, SN54LS27, SN7427, SN74LS27 TRIPLE 3-INPUT POSITIVE-NOR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain three independent 3-input NOR gates.

The SN5427 and SN54LS27 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7427 and SN74LS27 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

3

TTL DEVICES

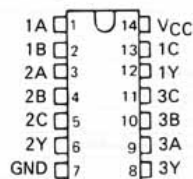
logic diagram (each gate)



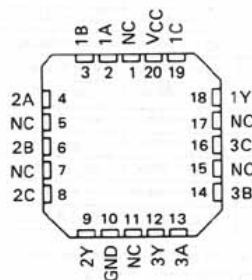
positive logic

$$Y = \overline{A + B + C} \text{ or } Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$$

SN5427, SN54LS27 ... J OR W PACKAGE  
SN7427 ... J OR N PACKAGE  
SN74LS27 ... D, J OR N PACKAGE  
(TOP VIEW)



SN54LS27 ... FK PACKAGE  
SN74LS27  
(TOP VIEW)



NC - No internal connection

3-114

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TEXAS  
INSTRUMENTS



**FUNÇÃO:** NOR

**REFERÊNCIA:** '23 / '25

**Nº DE ITENS POR CI:** 2

## TYPES SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain dual 4-input positive NOR gates with strobe. The SN5423 and SN7423 are expandable, and perform the Boolean functions:

$$1Y = 1G(1A \cdot 1B \cdot 1C \cdot 1D) \cdot X \text{ and}$$

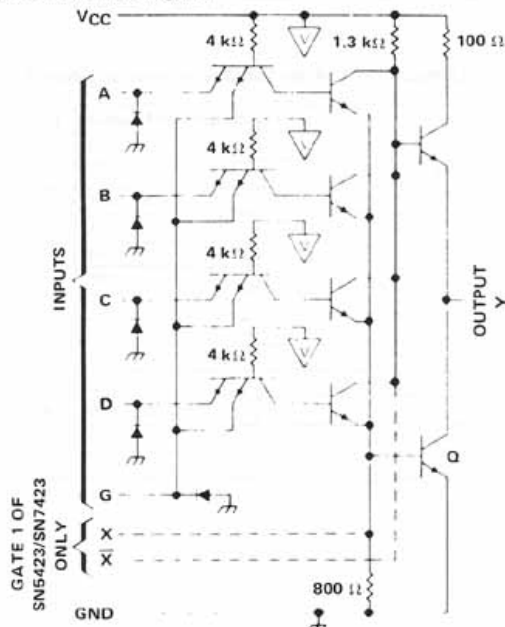
$$2Y = 2G(2A \cdot 2B \cdot 2C \cdot 2D)$$

with X output of SN5460/SN7460. The SN5425 and SN7425 perform the Boolean function:

$$Y = G(A \cdot B \cdot C \cdot D)$$

The SN5423 and the SN5425 are characterized for operation over the full military temperature range of 55 C to 125 C. The SN7423 and the SN7425 are characterized for operation from 0 C to 70 C.

### schematic (each gate)

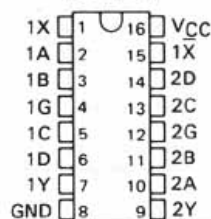


- Notes:
- Component values shown are nominal.
  - Both expander inputs are used simultaneously for expanding.
  - If expander is not used leave X and X open.
  - A total of four expander gates can be connected to the expander inputs.

VCC bus

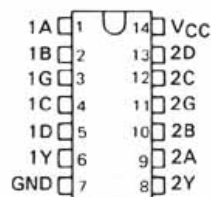
SN5423 ... J OR W PACKAGE  
SN7423 ... J OR N PACKAGE

(TOP VIEW)

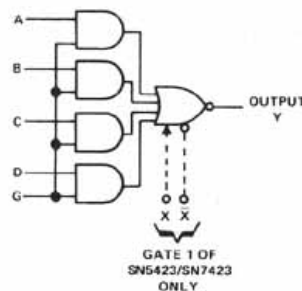


SN5425 ... J OR W PACKAGE  
SN7425 ... J OR N PACKAGE

(TOP VIEW)



### logic diagram



### TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open,  
H: high level, L: low level, X: irrelevant

3

TTL DEVICES

TEXAS  
INSTRUMENTS

3-107

FUNÇÃO: NOR

REFERÊNCIA: '260

Nº DE ITENS POR CI: 2

## TYPES SN54S260, SN74S260 DUAL 5-INPUT POSITIVE -NOR GATES

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs

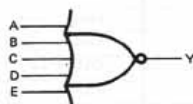
- Dependable Texas Instruments Quality and Reliability

### description

These devices contain two independent 5-input positive -NOR gates. They perform the Boolean function  $Y = A + B + C + D + E$  in positive logic.

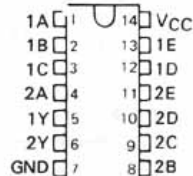
The SN54S260 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74S260 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### logic diagram (each gate)



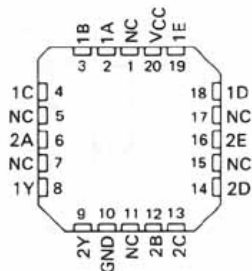
SN54S260 ... J OR W PACKAGE  
SN74S260 ... D, J OR N PACKAGE

(TOP VIEW)



SN54S260 ... FK PACKAGE  
SN74S260

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

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TEXAS  
INSTRUMENTS

3-715

FUNÇÃO: NOT  
 REFERÊNCIA: '04  
 Nº DE ITENS POR CI: 6

# TYPES SN5404, SN54LS04, SN54S04 SN7404, SN74LS04, SN74S04 HEX INVERTERS

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

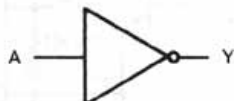
These devices contain six independent inverters.

The SN5404, SN54LS04 and SN54S04 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7404, SN74LS04 and SN74S04 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each inverter)

INPUTS	OUTPUT
A	Y
H	L
L	H

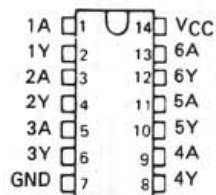
## logic diagram (each inverter)



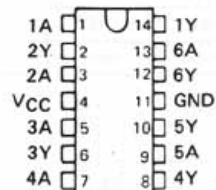
positive logic

$$Y = \bar{A}$$

SN5404 ... J PACKAGE  
 SN54LS04, SN54S04 ... J OR PACKAGE  
 SN7404 ... J OR N PACKAGE  
 SN74LS04, SN74S04 ... D, J OR N PACKAGE  
 (TOP VIEW)

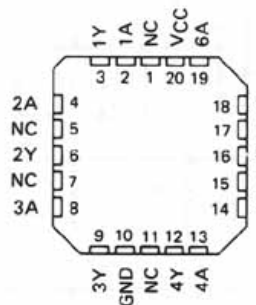


SN5404 ... W PACKAGE  
 (TOP VIEW)



SN54LS04, SN54S04 ... FK PACKAGE  
 SN74LS04, SN74S04

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

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TEXAS  
 INSTRUMENTS

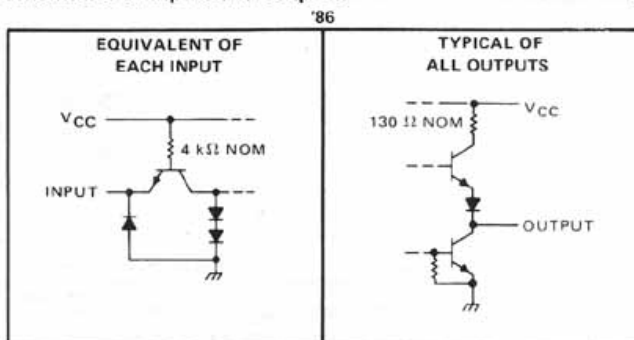
3-23

FUNÇÃO: XOR  
 REFERÊNCIA: '86  
 Nº DE ITENS POR CI: 4

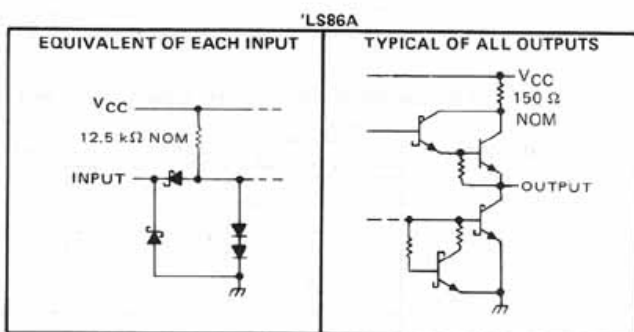
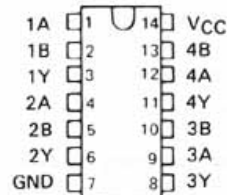
**TYPES SN5486, SN54LS86A, SN54S86,  
 SN7486, SN74LS86A, SN74S86  
 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

DECEMBER 1972 - REVISED DECEMBER 1983

**schematics of inputs and outputs**

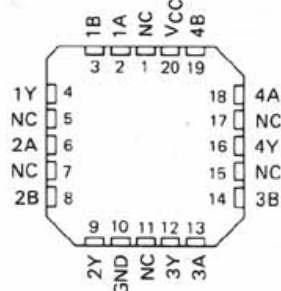


SN5486, SN54LS86A, SN54S86 ... J OR W PACKAGE  
 SN7486 ... J OR N PACKAGE  
 SN74LS86A, SN74S86 ... D, J OR N PACKAGE  
 (TOP VIEW)



SN54LS86A, SN54S86 ... FK PACKAGE  
 SN74LS86A, SN74S86

(TOP VIEW)



NC - No internal connection

**FUNCTION TABLES**

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

**TYPE**

'86  
 'LS86A  
 'S86

**TYPICAL AVERAGE  
 PROPAGATION  
 DELAY TIME**

14 ns  
 10 ns  
 7 ns

**TYPICAL  
 TOTAL POWER  
 DISSIPATION**

150 mW  
 30.5 mW  
 250 mW

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**TEXAS  
 INSTRUMENTS**

3-271

**3**

**TTL DEVICES**

FUNÇÃO: Flip-flop D  
 REFERÊNCIA: '74  
 Nº DE ITENS POR CI: 2

# TYPES SN5474, SN54LS74A, SN54S74 SN7474, SN74LS74A, SN74S74 DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

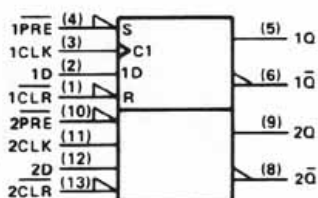
The SN54' family is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74' family is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels in  $V_{OH}$  if the lows at preset and clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

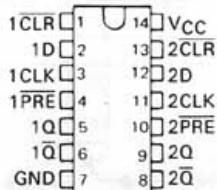
## logic symbol



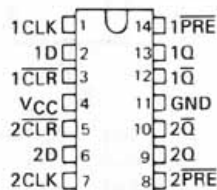
Pin numbers shown on logic notation are for D, J or N packages.

SN5474 ... J PACKAGE  
 SN54LS74A, SN54S74 ... J OR W PACKAGE  
 SN7474 ... J OR N PACKAGE  
 SN74LS74A, SN74S74 ... D, J OR N PACKAGE

(TOP VIEW)

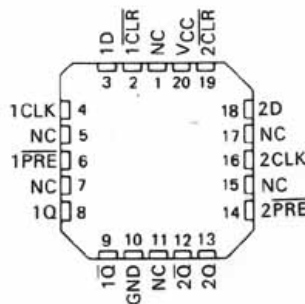


SN5474 ... W PACKAGE  
 (TOP VIEW)



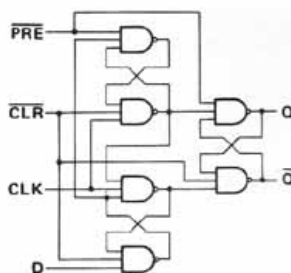
SN54LS74A, SN54S74 ... FK PACKAGE  
 SN74LS74A, SN74S74

(TOP VIEW)



NC - No internal connection

## logic diagram



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TEXAS  
 INSTRUMENTS

3-235

3

TTL DEVICES

**FUNÇÃO:** Flip-flop D

**REFERÊNCIA:** '175

**Nº DE ITENS POR CI:** 4

# TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

DECEMBER 1972—REVISED DECEMBER 1983

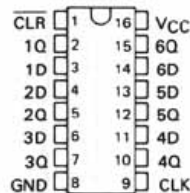
'174, 'LS174, 'S174 ... HEX D-TYPE FLIP-FLOPS

'175, 'LS175, 'S175 ... QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:  
Buffer/Storage Registers  
Shift Registers  
Pattern Generators

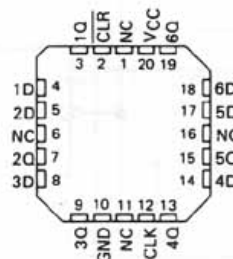
SN54174, SN54LS174, SN54S174 ... J OR W PACKAGE  
SN74174 ... J OR N PACKAGE  
SN74LS174, SN74S174 ... D, J OR N PACKAGE

(TOP VIEW)



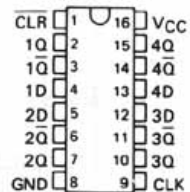
SN54LS174, SN54S174 ... FK PACKAGE  
SN74LS174, SN74S174

(TOP VIEW)



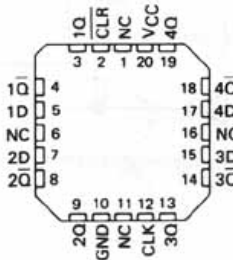
SN54175, SN54LS175, SN54S175 ... J OR W PACKAGE  
SN74175 ... J OR N PACKAGE  
SN74LS175, SN74S175 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS175, SN54S175 ... FK PACKAGE  
SN74LS175, SN74S175

(TOP VIEW)



NC - No internal connection

## description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

FUNCTION TABLE  
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	Q <sub>0</sub> -bar

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↑ = transition from low to high level

Q<sub>0</sub> = the level of Q before the indicated steady-state input conditions were established.

† = '175, 'LS175, and 'S175 only

TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

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TEXAS  
INSTRUMENTS

3-559

3

TTL DEVICES

**FUNÇÃO:** Flip-flop J-K  
**REFERÊNCIA:** '73  
**Nº DE ITENS POR CI:** 2

**TYPES SN5473, SN54LS73A  
 SN7473, SN74LS73A  
 DUAL J-K FLIP-FLOPS WITH CLEAR**  
REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

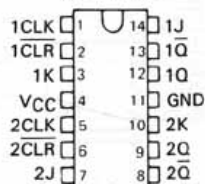
The '73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73 are positive pulsetriggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the  $\bar{Q}$  output high.

The SN5473 and the SN54LS73A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7473 and the SN74LS73A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5473, SN54LS73A ... J OR W PACKAGE  
 SN7473 ... J OR N PACKAGE  
 SN74LS73A ... D, J OR N PACKAGE

(TOP VIEW)



'73  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	TOGGLE

'LS73A  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	TOGGLE
H	H	X	X	$Q_0$	$Q_0$

FOR CHIP CARRIER INFORMATION,  
CONTACT THE FACTORY

3

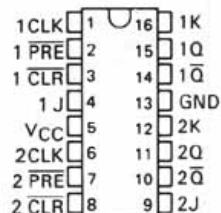
TTL DEVICES

**FUNÇÃO:** Flip-flop J-K  
**REFERÊNCIA:** '76  
**Nº DE ITENS POR CI:** 2

**TYPES SN5476, SN54LS76A,  
 SN7476, SN74LS76A  
 DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR**  
 REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN5476, SN54LS76A ... J OR W PACKAGE  
 SN7476 ... J OR N PACKAGE  
 SN74LS76A ... D, J OR N PACKAGE  
 (TOP VIEW)



**description**

The '76 contain two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 are positive-edge-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476, and the SN54LS76A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C.

**'76  
 FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	

**'LS76A  
 FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

FOR CHIP CARRIER INFORMATION,  
 CONTACT THE FACTORY

**PRODUCTION DATA**  
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**TEXAS  
 INSTRUMENTS**

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**3  
 TTL DEVICES**



**FUNÇÃO:** Flip-flop J-K  
**REFERÊNCIA:** '78  
**Nº DE ITENS POR CI:** 2

## TYPES SN54LS78A, SN74LS78A DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs,
- Dependable Texas Instruments Quality and Reliability

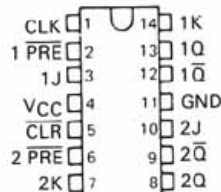
### description

The 'LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN54LS78A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS78A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FOR CHIP CARRIER INFORMATION,  
CONTACT THE FACTORY

SN54LS78A ... J OR W PACKAGE  
SN74LS78A ... D, J OR N PACKAGE  
(TOP VIEW)



'LS78A					
INPUTS					OUTPUTS
PRE	CLR	CLK	J	K	Q Q̄
L	H	X	X	X	H L
H	L	X	X	X	L H
L	L	X	X	X	H† H†
H	H	↓	L	L	Q <sub>0</sub> Q̄ <sub>0</sub>
H	H	↓	H	L	H L
H	H	↓	L	H	L H
H	H	↓	H	H	TOGGLE
H	H	H	X	X	Q <sub>0</sub> Q̄ <sub>0</sub>

† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

3

TTL DEVICES

### PRODUCTION DATA

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TEXAS  
INSTRUMENTS

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**FUNÇÃO:** Flip-flop J-K  
**REFERÊNCIA:** '107  
**Nº DE ITENS POR CI:** 2

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

#### description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low clock transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS107A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the  $\bar{Q}$  output high.

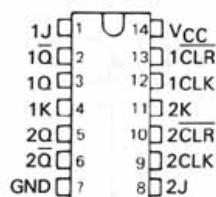
The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74107 and the SN74LS107A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

### TYPES SN54107, SN54LS107A, SN74107, SN74LS107A DUAL J-K FLIP-FLOPS WITH CLEAR

REVISED DECEMBER 1983

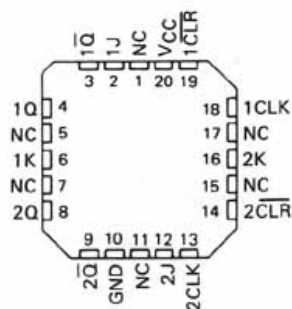
SN54107, SN54LS107A ... J PACKAGE  
 SN74107 ... J OR N PACKAGE  
 SN74LS107A ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS107A ... FK PACKAGE  
 SN74LS107A

(TOP VIEW)



NC - No internal connection

'107  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	TOGGLE

'LS107A  
FUNCTION TABLE

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	$\downarrow$	L	L	$Q_0$	$\bar{Q}_0$
H	$\downarrow$	H	L	H	L
H	$\downarrow$	L	H	L	H
H	$\downarrow$	H	H	TOGGLE	TOGGLE
H	H	X	X	$Q_0$	$\bar{Q}_0$

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TEXAS  
INSTRUMENTS

3-311

3

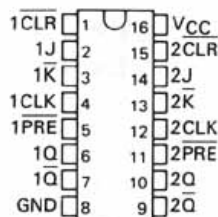
TTL DEVICES

**FUNÇÃO:** Flip-flop J-K  
**REFERÊNCIA:** '109  
**Nº DE ITENS POR CI:** 2

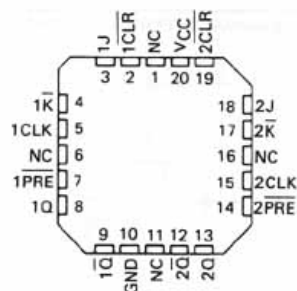
# TYPES SN54109, SN54LS109A, SN74109, SN74LS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR REVISED DECEMBER 1983

- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

SN54109, SN54LS109A ... J OR W PACKAGE  
SN74109 ... J OR N PACKAGE  
SN74LS109A ... D, J OR N PACKAGE  
(TOP VIEW)



SN54LS109A ... FK PACKAGE  
SN74LS109A  
(TOP VIEW)



## description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and tying J high. They also can perform as D-type flip-flops if J and K are tied together.

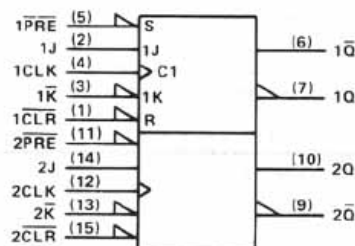
The SN54109 and SN54LS109A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74109 and SN74LS109A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q <sub>0</sub>	Q̄ <sub>0</sub>
H	H	↑	H	H	H	L
H	H	L	X	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels for V<sub>OH</sub> if the lows at preset and clear are near V<sub>IL</sub> maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

## logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

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TEXAS  
INSTRUMENTS

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**FUNÇÃO:** Flip-flop J-K

**REFERÊNCIA:** '114

**Nº DE ITENS POR CI:** 2

# TYPES SN54LS114A, SN54S114A, SN74LS114A, SN74S114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS114A and SN54S114A are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS114A and SN74S114A are characterized for operation from 0°C to 70°C.

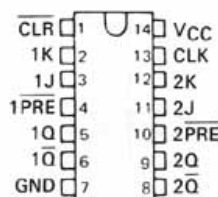
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↓	L	L	Q <sub>O</sub>	$\bar{Q}_O$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q <sub>O</sub>	$\bar{Q}_O$

<sup>†</sup> The output levels in this configuration are not guaranteed to meet the minimum levels for V<sub>OH</sub> if the lows at preset and clear are near V<sub>IL</sub> minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

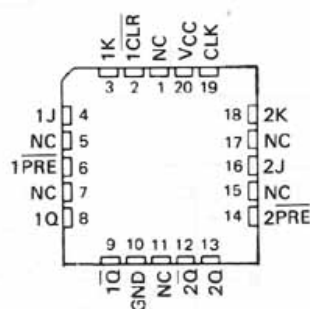
SN54LS114A, SN54S114A ... J OR W PACKAGE  
SN74LS114A, SN74S114A ... D, J OR N PACKAGE

(TOP VIEW)



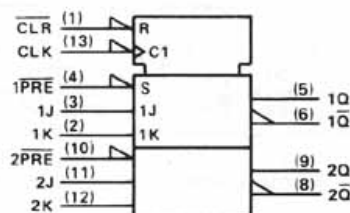
SN54LS114A, SN54S114A ... FK PACKAGE  
SN74LS114A, SN74S114A

(TOP VIEW)



NC - No internal connection

## logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

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TEXAS  
INSTRUMENTS

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3

TTL DEVICES

FUNÇÃO: Mux 2:1  
 REFERÊNCIA: '157  
 Nº DE ITENS POR CI: 4

# TYPES SN54157, SN54L157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

MARCH 1974—REVISED DECEMBER 1983

- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

## applications

- Expand Any Data Input Point
- Multiplex Dual Data Buses
- Generate Four Functions of Two Variables (One Variable Is Common)
- Source Programmable Counters

## description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE G	SELECT A/B	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

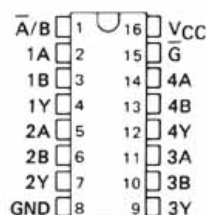
## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	7 V
Input voltage: '157, 'L157, 'S158	5.5 V
'LS157, 'LS158	7 V
Operating free-air temperature range: SN54'	–55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

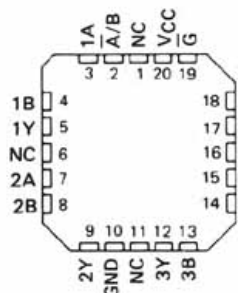
SN54157, SN54LS157, SN54S157,  
 SN54LS158, SN54S158 ... J OR W PACKAGE  
 SN54L157 ... J PACKAGE  
 SN74157 ... J OR N PACKAGE  
 SN74LS157, SN74S157,  
 SN74LS158, SN74S158 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS157, SN54S157, SN54LS158  
 SN54S158, SN74LS157, SN74S157,  
 SN74LS158, SN74S158 ... FK PACKAGE

(TOP VIEW)



NC - No internal connection

3

TTL DEVICES

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TEXAS  
 INSTRUMENTS

3-463

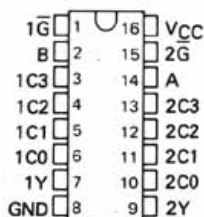
FUNÇÃO: Mux 4:1  
 REFERÊNCIA: '153  
 Nº DE ITENS POR CI: 2

# TYPES SN54153, SN54LS153, SN54S153 SN74153, SN74LS153, SN74S153 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

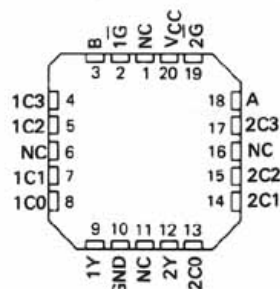
DECEMBER 1972—REVISED DECEMBER 1983

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL Circuits

SN54153, SN54LS153, SN54S153 ... J OR W PACKAGE  
 SN74153 ... J OR N PACKAGE  
 SN74LS153, SN74S153 ... D, J OR N PACKAGE  
 (TOP VIEW)



SN54LS153, SN54S153 ... FK PACKAGE  
 SN74LS153, SN74S153  
 (TOP VIEW)



NC - No internal connection

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES			TYPICAL POWER DISSIPATION
	FROM DATA	FROM STROBE	FROM SELECT	
'153	14 ns	17 ns	22 ns	180 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

## description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.  
 H = high level, L = low level, X = irrelevant

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '153, 'S153	5.5 V
'LS153	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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TEXAS  
 INSTRUMENTS

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3  
 TTL DEVICES

**FUNÇÃO:** Mux 8:1 (pag. 1)

**REFERÊNCIA:** '151

**Nº DE ITENS POR CI:** 1

# TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151 DATA SELECTORS/MULTIPLEXERS

DECEMBER 1972—REVISED DECEMBER 1983

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	13 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	13 ns	30 mW
'LS152	13 ns	28 mW
'S151	4.5 ns	225 mW

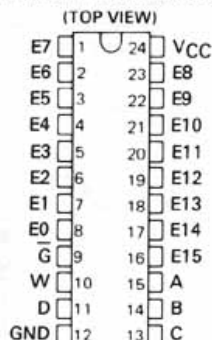
## description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

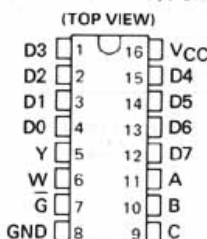
The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

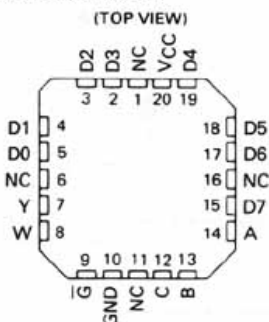
SN54150 ... J OR W PACKAGE  
SN74150 ... J OR N PACKAGE



SN54151A, SN54LS151, SN54S151 ... J OR W PACKAGE  
SN74151A ... J OR N PACKAGE  
SN74LS151, SN74S151 ... D, J OR N PACKAGE

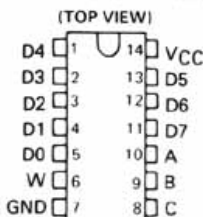


SN54LS151, SN54S151 ... FK PACKAGE  
SN74LS151, SN74S151



NC - No internal connection

SN54152A, SN54LS152 ... W PACKAGE



For SN54LS152 Chip Carrier Information, Contact The Factory.

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TEXAS  
INSTRUMENTS

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TTL DEVICES

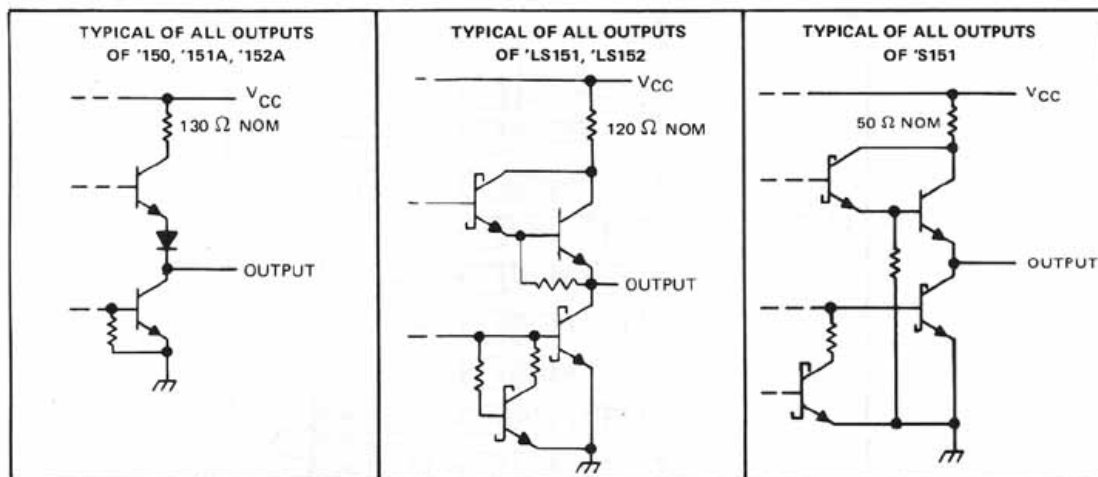
FUNÇÃO: Mux 8:1 (pag. 2)

REFERÊNCIA: '151

Nº DE ITENS POR CI: 1

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151  
SN74150, SN74151A, SN74LS151, SN74S151  
DATA SELECTORS/MULTIPLEXERS

schematics of inputs and outputs



logic

'150  
FUNCTION TABLE

INPUTS				STROBE $\bar{G}$	OUTPUT W
D	C	B	A		
X	X	X	X	H	H
L	L	L	L	L	$\bar{E0}$
L	L	L	H	L	$\bar{E1}$
L	L	H	L	L	$\bar{E2}$
L	L	H	H	L	$\bar{E3}$
L	H	L	L	L	$\bar{E4}$
L	H	L	H	L	$\bar{E5}$
L	H	H	L	L	$\bar{E6}$
L	H	H	H	L	$\bar{E7}$
H	L	L	L	L	$\bar{E8}$
H	L	L	H	L	$\bar{E9}$
H	L	H	L	L	$\bar{E10}$
H	L	H	H	L	$\bar{E11}$
H	H	L	L	L	$\bar{E12}$
H	H	L	H	L	$\bar{E13}$
H	H	H	L	L	$\bar{E14}$
H	H	H	H	L	$\bar{E15}$

'151A, 'LS151, 'S151  
FUNCTION TABLE

INPUTS			STROBE $\bar{G}$	OUTPUTS	
C	B	A		Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\bar{D0}$
L	L	H	L	D1	$\bar{D1}$
L	H	L	L	D2	$\bar{D2}$
L	H	H	L	D3	$\bar{D3}$
H	L	L	L	D4	$\bar{D4}$
H	L	H	L	D5	$\bar{D5}$
H	H	L	L	D6	$\bar{D6}$
H	H	H	L	D7	$\bar{D7}$

H = high level, L = low level, X = irrelevant  
E0, E1 . . . E15 = the complement of the level of the respective E input  
D0, D1 . . . D7 = the level of the D respective input

'152A, 'LS152  
FUNCTION TABLE

SELECT INPUTS			OUTPUT W
C	B	A	
L	L	L	D0
L	L	H	$\bar{D1}$
L	H	L	$\bar{D2}$
L	H	H	$\bar{D3}$
H	L	L	$\bar{D4}$
H	L	H	$\bar{D5}$
H	H	L	$\bar{D6}$
H	H	H	$\bar{D7}$

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TTL DEVICES



FUNÇÃO: Contador (pag. 1)  
 REFERÊNCIA: '93  
 Nº DE ITENS POR CI: 1

**TYPES SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93  
 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS**

MARCH 1974 - REVISED DECEMBER 1983

**'90A, 'LS90 ... DECADE COUNTERS**

**'92A, 'LS92 ... DIVIDE-BY-TWELVE COUNTERS**

**'93A, 'LS93 ... 4-BIT BINARY COUNTERS**

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW

**description**

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, and 'LS93.

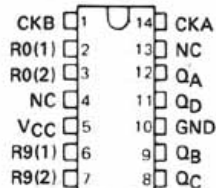
All of these counters have a gated zero reset and the '90A, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q<sub>A</sub> output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, or 'LS90 counters by connecting the Q<sub>D</sub> output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q<sub>A</sub>.

**SN5490A, SN54LS90 ... J OR W PACKAGE**

SN7490A ... J OR N PACKAGE  
 SN74LS90 ... D, J OR N PACKAGE

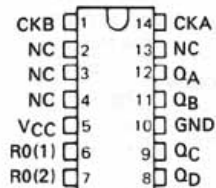
(TOP VIEW)



**SN5492A, SN54LS92 ... J OR W PACKAGE**

SN7492A ... J OR N PACKAGE  
 SN74LS92 ... D, J OR N PACKAGE

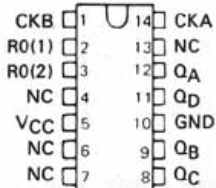
(TOP VIEW)



**SN5493A, SN54LS93 ... J OR W PACKAGE**

SN7493A ... J OR N PACKAGE  
 SN74LS93 ... D, J OR N PACKAGE

(TOP VIEW)



For new chip carrier design, use  
 'LS290, 'LS292, and 'LS293.

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TTL DEVICES

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TEXAS  
 INSTRUMENTS

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FUNÇÃO: Contador (pag. 2)  
 REFERÊNCIA: '93  
 Nº DE ITENS POR CI: 1

TYPES SN5490A, '92A, '93A, SN54LS90, 'LS92, 'LS93,  
 SN7490A, '92A, '93A SN74LS90, 'LS92, 'LS93  
 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

'90A, 'LS90  
 BCD COUNT SEQUENCE  
 (See Note A)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90  
 BI-QUINARY (5-2)  
 (See Note B)

COUNT	OUTPUT			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92  
 COUNT SEQUENCE  
 (See Note C)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90  
 RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R <sub>0</sub> (1)	R <sub>0</sub> (2)	R <sub>9</sub> (1)	R <sub>9</sub> (2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'93A, 'LS93  
 COUNT SEQUENCE  
 (See Note C)

COUNT	OUTPUT			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, 'LS92, '93A, 'LS93  
 RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R <sub>0</sub> (1)	R <sub>0</sub> (2)	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q<sub>A</sub> is connected to input CKB for BCD count.  
 B. Output Q<sub>D</sub> is connected to input CKA for bi-quinary count.  
 C. Output Q<sub>A</sub> is connected to input CKB.  
 D. H = high level, L = low level, X = irrelevant

FUNÇÃO: Contador (pag. 1)  
 REFERÊNCIA: '163  
 Nº DE ITENS POR CI: 1

TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,  
 SN54S162, SN54S163, SN74160 THRU SN74163,  
 SN74LS160A THRU SN74LS163A, SN74S162, SN74S163  
 SYNCHRONOUS 4-BIT COUNTERS

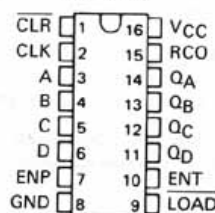
OCTOBER 1976—REVISED DECEMBER 1983

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR  
 '162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE  
 SERIES 74' . . . J OR N PACKAGE  
 SERIES 74LS', 74S' . . . D, J OR N PACKAGE

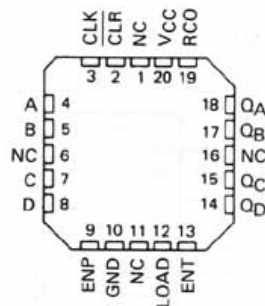
(TOP VIEW)



NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE  
 SERIES 74LS', 74S'

(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

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TEXAS  
INSTRUMENTS

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**FUNÇÃO:** Contador (pag. 2)

**REFERÊNCIA:** '163

**Nº DE ITENS POR CI:** 1

**TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,  
SN54S162, SN54S163, SN74160 THRU SN74163,  
SN74LS160A THRU SN74LS163A, SN74S162, SN74S163  
SYNCHRONOUS 4-BIT COUNTERS**

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the  $Q_A$  output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

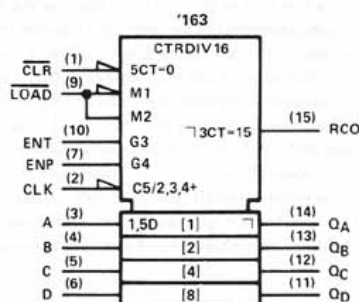
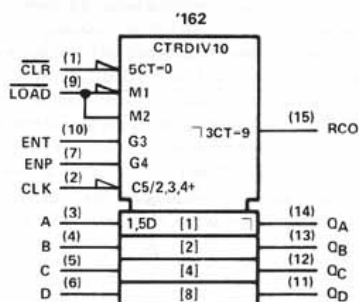
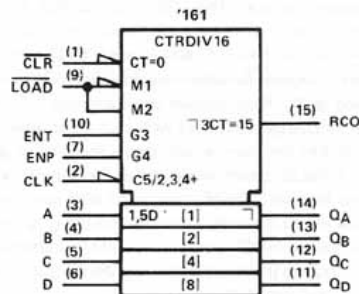
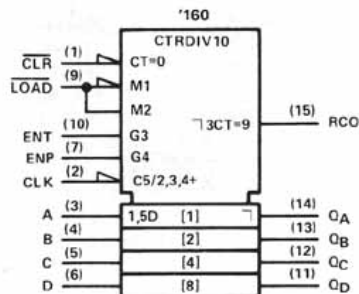
The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents  $I_{IH}$  and  $I_{IL}$ .

**N-BIT SYNCHRONOUS COUNTERS**

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A or 'S163 will count in binary. Virtually any count mode (modulo-N,  $N_1$ -to- $N_2$ ,  $N_1$ -to-maximum) can be used with this fast look-ahead circuit.

logic symbols

**3**  
**TTL DEVICES**



Pin numbers shown on logic notation are for D, J or N packages.