A Detailed DVB-S2 Receiver Implementation: FPGA Prototyping and Preliminary ASIC Resource Estimation

Eduardo R. de Lima, Augusto F. R. Queiroz, Denise C. Alves, Gabriel S. da Silva, Cesar G. Chaves, Jacqueline G. Mertes, Thiago M. Marson
Eldorado Research Institute – Campinas, São Paulo, Brazil
{eduardo.lima, augusto.queiroz, denise.alves, gabriel.silva, cesar.arroyave, jacqueline.mertes, thiago.marson}@eldorado.org.br

***Abstract*—Design and implementation of signal processing and synchronization algorithms for digital receivers are challenging tasks, especially concerning the verification phase that must cover as many functional tests as possible. This paper discloses the entire internal architecture of the receive chain of the ETSI DVB-S2 digital satellite communication standard and the methodology used for implementing it. It covers architectural, algorithm, and RTL design, together with laboratory set-up, FPGA prototyping and VLSI resource estimation in $65nm$ CMOS. The result section demonstrates that our approach is able to synchronize and demodulate an 8-PSK DVB-S2 compliant signal, corrupted by all the impairments expected in a digital receiver.**

I. Introduction

DVB-S2 is the state-of-art ETSI standard for satellite broadcasting [1], [2]. It takes advantage of Low Density Parity Check Code (LDPC) concatenated with Bose-Chaudhuri-Hocquenghem (BCH) code, to achieve near Shannon limit performance [3]. The key characteristics, which allow quasi-error free operation near (0.6 to 1.2 dB) Shannon limit, are: 1) very large LDPC code block length (64800 bits for Normal Frame and 16200 bits for Short Frame); 2) large number of iterations on LDPC (around 50); and 3) the concatenation with BCH. DVB-S2 has been designed for applications such as: broadcast for High Definition Television (HDTV), iterative services for consumer applications, Digital TV distribution and news gathering, distribution of signal to terrestrial transmitters, and others [1]. It achieves about 30% of capacity gain over DVB-S, under the same transmission conditions. Due to its spectral efficiency, DVB-S2 is used as downlink for DVB-RCS2.

The standard has been specified around three key concepts: best transmission performance, total flexibility and reasonable receiver complexity. It supports Variable Coding Modulation (VCM), functionality that allows different modulation (QPSK, 8-PSK, 16-APSK and 32-APSK) and error protection levels (1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10) to be used on a frame by frame basis. DVB-S2 was specified to cope with any existing satellite transponder characteristics, with a large variety of spectrum efficiencies and Carrier-to-Noise ratio (C/N) requirements (it covers from -2.4 to 16 dB). In order to preserve compatibility with DVB-S, DVB-S2 has an optional compatibility mode. Moreover, it can implement Adaptive Coding and Modulation (ACM), when used for interactive services.

The standard was developed by the DVB group in 2003 and ratified by ETSI in 2005. In 2009 it was updated and in February 2014 the steering board of DVB approved the DVB-S2 enhanced specification, known as DVB-S2X. In short, DVB-S2x contains DVB-S2 requirements and more choices of roll-off factors, as well as additional modulation and FEC options. Despite the enhancements under development, DVB-S2 is still not widely used worldwide, and the number of satellite broadcasters that make use of 16-APSK and 32-APSK is low. Information regarding the usage of DVB-S and DVB-S2 in South America can be found in [4]. This shows the potential use of the current features of DVB-S2 on the long term, which makes possible the appearance of new DVB-S2 receiver designs in the market. Due to all previously mentioned DVB-S2 advantages and opportunities, the implementation of DVB-S2 receivers is still a challenging area of research.

This work exposes in detail the implementation of a DVB-S2 digital receiver and the followed methodology. In general, these details are not exposed by integrated circuit vendors. Furthermore, the implementation methodology used in this project can be applied for other wireless communication receivers. Moreover, the receiver presented can be extended straightforward to cope with DVB-S2X requirements.

The remainder of this paper is organized as follows: Section II describes the Design Flow used in the project. Section III presents the full receiver architecture. Section IV is devoted to the explanation of the Signal and Data Processing blocks designed and implemented. Within Section V, the Test Laboratory and FPGA prototyping Methodology are described. Section VI presents the results on the FPGA prototyping and the receiver BER performance. Section VII cites some related work, emphasizing the disclosure level of our work. Section VIII presents the early results for the VLSI implementation in $65nm$ CMOS. Finally, the conclusion is drawn.

II. Design Flow

The definition of the Design Flow to be followed was the first task of the project development. A simplified block

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diagram of the entire process is shown in Fig. 1.

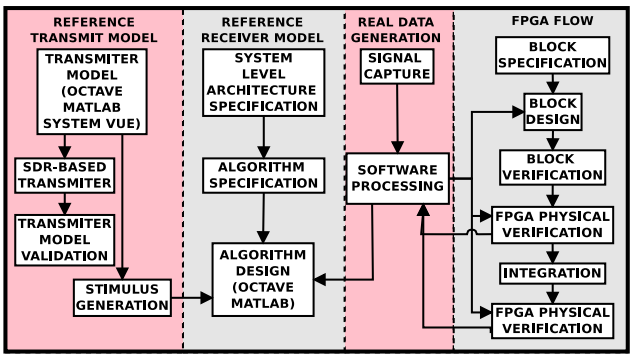

Fig. 1. Simplified Design Flow Chart

One of the major tasks when developing digital receivers is the conception and implementation of a model that can be used for several tasks along the project, e.g. refinement of algorithms and stimulus generation for RTL verification. In general, the very first model to be created is the transmission path, and that was the case in this work. Initially, for convenience, it was used a DVB-S2 reference model provided by the System Vue tool. Nevertheless, in order to be more flexible a transmitter model was created using Matlab and Octave. This model was used to create a DVB-S2 compliant transmission hardware, which was implemented using GNU Radio Companion and USRPN210 SDR platform. The transmitter hardware was validated using a commercial receiver.

The reference transmitter model can generate baseband stimulus for algorithm modeling, RTL design and verification, and physical tests on FPGA. In addition, DVB-S2 compliant stimulus can be used to perform system test to confirm receiver performance, in FPGA. In the next phase of the project, it will be used to generate stimulus for the complete ASIC design flow. It is worth to recall that this work only presents the basic estimates for $65nm$ technology, based on the HDL code that was successfully prototyped in FPGA. This is used to provide initial estimates (e.g. area and power) as well as to find possible bugs, masked by FPGA tool specific optimizations, beforehand.

The design of receiver blocks was done in the following manner: 1) First of all, a receiver architecture was defined, containing all the sub-blocks of a digital Intermediate Frequency (IF) receiver and DVB-S2 specific blocks; 2) Once defined the architecture, algorithms and functionality specifications were done, followed by the models implementation using a high level language (Matlab or Octave); 3) After models validation, block specifications for RTL design were written, followed by the platform independent design, using VHDL, and a simple verification made by the designer of the block; 4) Full block verification was done by an specific Verification Engineer; 5) Once verified the design, synthesis targeting Alteras FPGA (Stratix IV) was performed -refer to [5]- followed by physical verification, i.e. injection of real stimulus into the FPGA synthesized block, capture of block answer and comparison to expected results; 6) After validation through physical verification, integration of the blocks was carried out, followed by new physical tests; 7) System tests were done in order to validate the functionalities of DVB-S2 receiver; 8) A simplified ASIC design flow was also done for early design issues detection. As it can be seen in Fig. 1, real signal capture can be performed at any time to be used for refinements of the models, RTL design or throughput improvements.

III. The Receiver Architecture

Architecture definition is the most impacting activity in the entire design flow, because it is from there that all the receiver design starts. One can design a block in an independent manner, i.e. without architecture definition. Nevertheless, if the architecture specification is not followed, important requirements and features could not be captured and this could cause unnecessary refinements and redesigns. In certain cases the entire design of a block could be compromised.

Fig. 2 introduces the DVB-S2 receiver architecture that shall be implemented at the end of this project. Nevertheless, thanks to functional issues, it is possible to implement the receiver in three incremental phases: the first one, presented in [6] contains all blocks shown in Fig. 2 except by those belonging to Adaptive Equalizer (Feed Forward - FFE and Feedback FBE Filters and Coefficients Calculator), BCH and LDPC decoders. The second presented here, includes the BCH and LDPC decoders. The last will incorporate Adaptive Equalizer.

IV. Receiver Design Units

The design units implemented at this phase of the project are described along this section. For convenience, the units are divided in two partitions; Data Processing and Signal Processing [7] (see Fig. 2).

A. Signal Processing

After being sampled by the ADC, the signal containing all reception impairments feeds the Signal Processing blocks, responsible for IF to Zero-IF conversion, impairments corrections and frame synchronization. Initially, the signal is down-converted from IF to ZIF using a CORDIC [8], a Phase Accumulator, and a Low Pass Filter, obtaining a baseband signal that will be synchronized.

The Timing Recovery loop performs symbol sampling error estimation and correction. The estimator uses Gardners Algorithm [9] while the correction is obtained by Fractional Interpolation based on Farrow Structure with fixed taps [10]. A 2nd order Loop Filter is used to smooth the error estimation, as the NCO accumulates the error and preserves the relation between the input and output samples of the loop. This is achieved by either discarding or retaining the samples in the Fractional Interpolator. The output samples are then filtered by a Root Raised Cosine (RRC) and decimated to Symbol Rate.

Subsequently, Frame Synchronization is performed using the header autocorrelation and the Peak Search Algorithm [11], [12] to detect the frame boundary and the Start-Of-Frame (SOF). The PL header is the first part of the PL frame and contains information regarding the modulation, code rate and frame type. These parameters, protected by a Reed-Muller (RM) code, along with the SOF flag, are used for the Physical Layer Signaling (PLS), being decoded by a Fast algorithm for Walsh Hadamard Transform (FHT) [13]. Before decoding, they

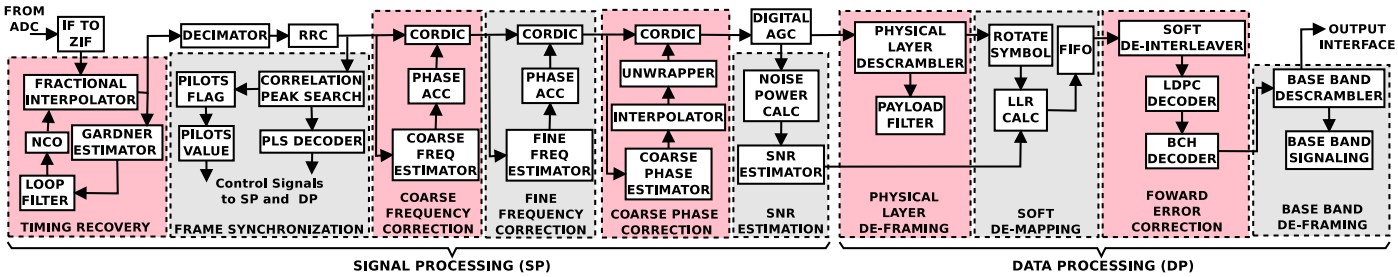

Fig. 2. DVB-S2 Receiver Architecture - tuner and ADC are external blocks

are soft-demapped, descrambled and averaged in a two soft-bit fashion. This process is possible due to the bit repetition established in the DVB-S2 standard [1], allowing the PLS-Decoder to work properly under a lower Signal-to-Noise-Ratio (SNR). The parameters are sent to other units through Pilot Flags, for frequency, phase and amplitude correction.

Thereafter, Frequency Correction is performed in two steps, i.e. Coarse and Fine. In order to estimate the Coarse Frequency error, the proposed receiver uses the scheme presented in [14], which is based on autocorrelation and the algorithm derived by Kay in [15]. The Fine Frequency estimation is performed using the Maximum Likelihood algorithm proposed in [12]. Both estimations are done over a configurable number of frames and provide a single pilot-based estimation. The frequency estimations are applied to their respective Phase Accumulators and CORDIC de-rotator [8].

Afterwards, the baseband constellation only presents phase and amplitude mismatches, which are respectively corrected using a Coarse Phase Corrector and the Automatic Gain Control unit. Coarse Phase Correction uses correlation and pilots to estimate the error as shown in [14]. The phase estimation is evaluated by an Unwrapper to eliminate phase ambiguity, then interpolation between the phase difference of two neighbour pilots is done and applied to the CORDIC de-rotator. Examples of the corrections mentioned above are found in Section VI.

Its worth noticing that the use of the CORDIC algorithm for diverse signal processing operations, other than DDS, reduced the complexity of the DVB-S2 receptor.

B. Data Processing

At a glance, Data Processing blocks convert received Physical Layer (PL) Frames [1] into Transport Stream (TS). For convenience, the first three design units (Physical Layer Descrambler, Payload Filter and Soft-Demapper) are placed in this partition, even working with symbols and not bits.

First of all, the Data Processing partition receives the signal coming from Signal Processing partition in the form of PL Frames. They are descrambled by the Physical Layer Descrambler to recover the original transmitted DVB-S2 sequence of the frames, previously scrambled for energy dispersal purposes. The resulting PL Frames have pilots and header symbols removed by the Payload Filter, outputting only the payload data. Following the sequence, an 8-PSK Soft-Demapper converts the symbols into soft-bits, which are equivalent to the Log-likelihood Ratios (LLRs) representing the probabilities of the bits being '0' or '1'. These probabilities are obtained using the estimated SNR, provided by the SNR Estimator block through the power noise calculated between the known pilots and the received signals. The demapped soft-bits are buffered by the Demapper FIFO, whose size is determined by the De-Interleaver throughput.

Next comes the Forward Error Correction (FEC) sub-system, composed by the De-Interleaver and the LDPC and BCH decoders. Although the De-interleaver is included in the FEC sub-system, it does not correct any errors in the frame, it rearranges the data in the original sequence, previously interleaved in a non-contiguous way, to increase performance in error-correction coding. The structure of the frame provided by the De-Interleaver is illustrated in Fig. 3. The length of each frame segment depends on the adopted code-rate and frame type, as established in [1].

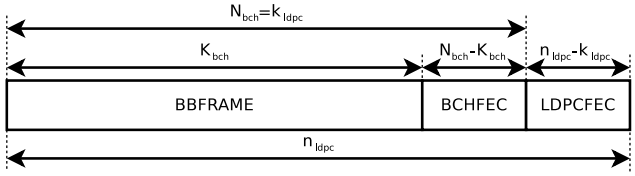

Fig. 3. DVB-S2 FECFRAME

The error correction is made by the concatenation of the LDPC and BCH decoders: the former executes a coarse correction, eliminating most of the errors, while the latter is responsible for a fine correction, by switching up to 12 erroneous bits.

The LDPC Decoder implements the Minimum-Sum algorithm, which is a simplification of the Belief-Propagation algorithm based on LLRs [16]. For each of the 21 frame configurations, a different LDPC coding scheme is applied. The complexity increases because of the need to implement an iterative decoding algorithm that requires a large amount of memory and a reasonable level of parallelism. The architecture of the implemented LDPC decoder is described in [17]. Based on the received soft-bits, the decoder runs a given number of iteration (normally between 30 and 50) and finally delivers to the BCH decoder the payload BBFRAME+BCHFEC and discards the parity bits (LDPCFEC).

Consequently, the BCH-Decoder uses the BCHFEC bits for recovering the original BBFRAME, correcting up to 8, 10 or 12 errors according to the code-rate and frame type. This is accomplished by serially executing three sub-blocks, the syndrome calculator [18], a key equation solver as the

Berlekamp-Massey algorithm [19] and a polynomial roots finder like the Chien Search algorithm [20]. Afterwards, the BBFRAME is forwarded without any FEC parity bits.

At this point, PL Frames are converted into Baseband (BB) Frames and descrambled again, but at this time by the BB-Descrambler, retrieving the original frames scrambled at transmitter. Next, the BB Frames have the header bits removed and the bits related to the Cyclic Redundancy Check (CRC) replaced by synchronization bits [1]. This process is performed by the BB-Signaling block and generates the TS, which contains the user packets. The Data Processing flow ends with the BB-Signaling. Nevertheless, in order to feed external MPEG-TS decoding hardware equipped with Asynchronous Serial Interface (ASI), a Bit-to-ASI conversion is done.

V. Prototyping Methodology

In order to physically test the receiver blocks and validate their integration, in FPGA, it is necessary an environment containing a source of stimulus, DVB-S2 signal transmitter, Spectrum and Vector analyzers, a tuner, an ADC, the synthesized blocks into FPGA and access points to check signal consistency inside the FPGA. Therefore, a Laboratory containing all elements shown in Fig. 4 was assembled.

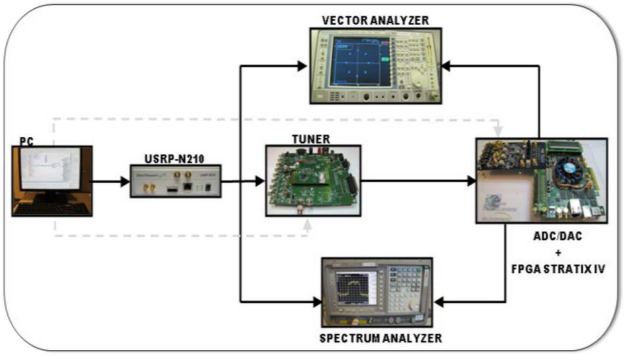

Fig. 4. Laboratory set-up for prototyping and tests.

Using Matlab, a TS file containing MPEG video, passes through all relevant DVB-S2 transmitter blocks described in [1], generating a sequence of PL Frames. Next, they are converted to a binary file and transmitted using the GNU Radio-Companion software and USRP platform. The Radio Frequency (RF) signal is checked using vector and spectrum analyzers. The IF tuner output is sampled and digitally converted by an ADC, this digital data is the IF digital receiver input. Among the design units, several checkpoints have been chosen. The signals captured at each of these points can be sent to a DAC, so the signal consistency can be checked using vector and spectrum analyzers. Moreover, memories have been synthesized and connected to the observing points. By reading these memories it is possible to collect data and subsequently process the information using Matlab. Physical tests can also be done, using Nios (Alteras Embedded Processor) to inject, capture and compare block outputs.

VI. FPGA Prototyping Results

FPGA prototyping is done in order to guarantee the correct functioning of the implemented design. A sample of the implementation results is given in this section: signals acquired from some key points of the synthesized blocks are compared to Matlab models and RTL simulation results. A summary of FPGA resources usage is presented. In addition, an overall BER performance for code rates 3/5, 5/6 and 9/10 is given.

In Fig. 5, the left subfigures show the baseband constellation after resampling, for SNR values of 16 and 21 dB. The subfigures on the right show the same constellations after frequency synchronization (coarse and fine), phase and amplitude correction.

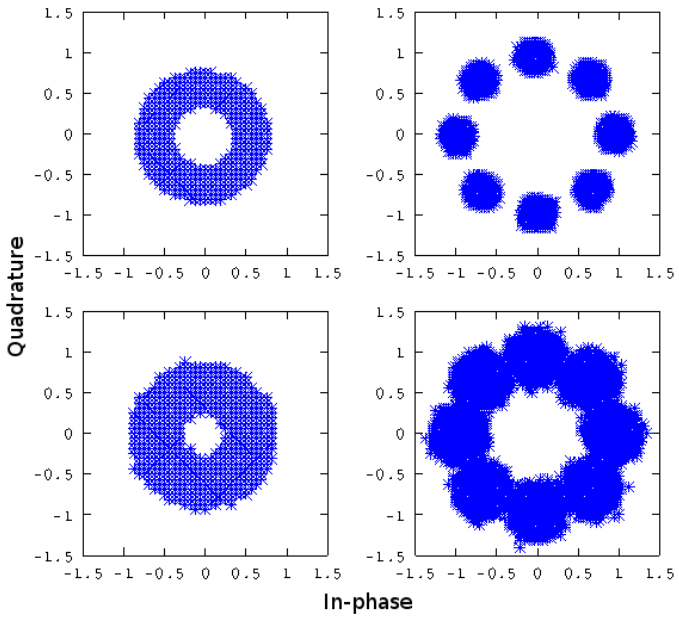

Fig. 5. Constellations captured from the FPGA Prototype for 16 dB (top) and 21 dB (bottom) SNRs.

FPGA implementation results have been summarized in Table I. It gives a brief summary of the consumed logic by design units, split in registers, ALUT's, memory bits and DSPs resources. Refer to [5] for details on this resources.

In order to validate the hardware implementation, the BER was measure for the following receiver configuration: Fs=1.5625 MHz, 8-PSK, Code Rates 3/5, 5/6 and 9/10, Normal Frame with pilots. These measurements are shown in Fig. 6. The BER curves are shifted from the expected quasi-error free target, due to the equalization algorithms which are being characterized and optimized for lower SNR values, the FEC (LDPC+BCH) was tested separately and it is compliant with the ETSI standard.

VII. Related Work

As mentioned in the Introduction of this work, in general, the proposed architecture and algorithms used in the implementation of the DVB-S2 digital receiver are not exposed by IC vendors. This makes a fair comparison not possible. On the other hand, the work exposed in [21] is worth to mention, despite it is a mix of Software-Defined-Radio with FPGA implementation and does not allow a straight implementation results comparison with our work, which targets VLSI implementation with a FPGA prototype phase. There, the FEC is

TABLE I. FPGA PROTOTYPING RESULTS FOR ALTERAS STRATIX IV

	DESIGN UNITS	ALUTS	REGISTERS	MEMORY BITS	DSP ELEMENTS (18-BIT)	DSP ELEMENTS (18x18)
DATA PROCESSING	SOFT DEMAPPER QPSK/8-PSK	879	218	0	6	3
	SNR ESTIMATOR	1487	1301	45	2	1
	BASE BAND SIGNALING	311	126	0	0	0
	BASE BAND DESCRAMBLER	13	18	0	0	0
	BIT TO ASI	25	21	0	0	0
	DEINTERLEAVER	504	212	864000	0	0
	DEMAPPER FIFO	96	37	518400	0	0
	PAYLOAD FILTER	7	35	0	0	0
	PILOT FLAGS	34	26	0	0	0
	LDPC DECODER	53607	59692	4240736	0	0
	BCH DECODER	4928	926	58192	0	0
	PL DESCRAMBLER	129	113	0	0	0
SIGNAL PROCESSING	L. PASS FILTER I	7935	5328	611	0	0
	L. PASS FILTER Q	7935	5328	0	0	0
	NCO + CORDIC	2158	2396	0	0	0
	DECIMATOR	20	37	0	0	0
	RCC I	3387	2252	0	0	0
	RCC Q	3413	2265	352	0	0
	TIMING RESAMPLING	325	455	132	12	7
	FINE FREQUENCY [1]	1882	1385	0	22	4
	AGC	295	205	102	18	10
	COARSE PHASE [2]	2663	2179	1728	18	9
	FRAME SYNC	7127	9862	3275	4	4
	COARSE FREQUENCY	5895	3709	64	48	48
	PILOT FLAGS	34	26	0	0	0
	PILOT VALUES	69	87	0	0	0

[1]Fine Frequency: Also uses one 12x12 and four 36x36 DSP elements.
[2]Coarse Phase: Also uses one 36x36 DSP element.

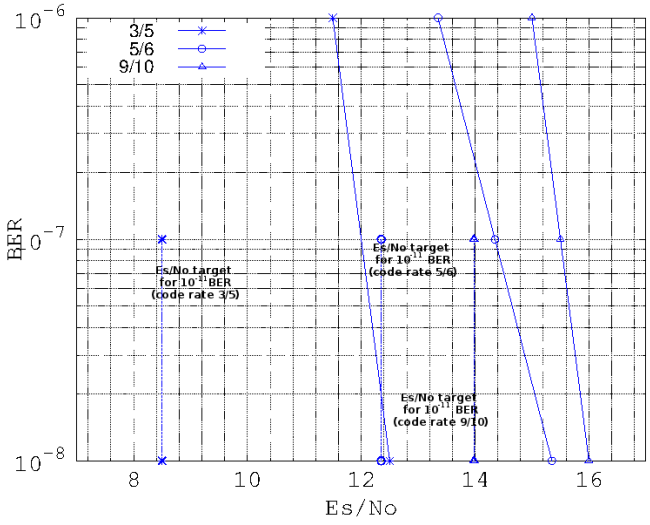

Fig. 6. Normal Frame BER for Code Rates 3/5, 5/6 and 9/10: FPGA Prototype

treated as an external block implemented in FPGA and the DDC is implemented in two stages, also in FPGA. The DDC architecture was presented in [22]. The authors do not show how they decoded the PLS, to configure the receiver blocks. In addition the DDC implementation presented in [22], and the Fine and Coarse Frequency correction presented in [21], make use of a Look-Up Table to generate Sine and Cosine waves. The Coarse and Fine Frequency Correction are also based on Look-Up Tables.

In this work we present the entire digital receiver architecture prototyped in FPGA and the preliminary Synthesis targeting ASIC. The digital receiver proposed in this work contains DDC and FEC in the same design. Sine and Cosine waves and phase rotations are based on the CORDIC algorithm. In addition we also present the performance results for the prototypes which was not presented in [21]. Optimizations will be performed in order to use the same CORDIC for DDC, Coarse and Fine Frequency Estimation. In addition we will also add Fine Phase estimation and correction, that are not implemented at the present moment.

VIII. VLSI IMPLEMENTATION

Synthesis, floorplan and placement with basic constraints were realized in order to estimate the die area, visualize possible design improvements and identify aspects not analyzed in FPGA project. It is worth to mention that detailed timing analysis was not performed since it is not the target at this phase of the project. Fig. 7 shows the amoeba view of the IPs placement. The Signal Processing partition is allocated in the upper part of the die, and the Data Processing partition is spread along the remaining area. The memory IPs used by the FEC blocks, i.e. Deinterleaver, LDPC and BCH decoders, are allocated in a clockwise order from the upper right corner to the upper left, following their respective blocks. The LDPC decoder logic and its memories represent about 80% of the die area. That percentage is justified by the amount of processing units required to achieve the target level of parallelism for LDPC decoding.

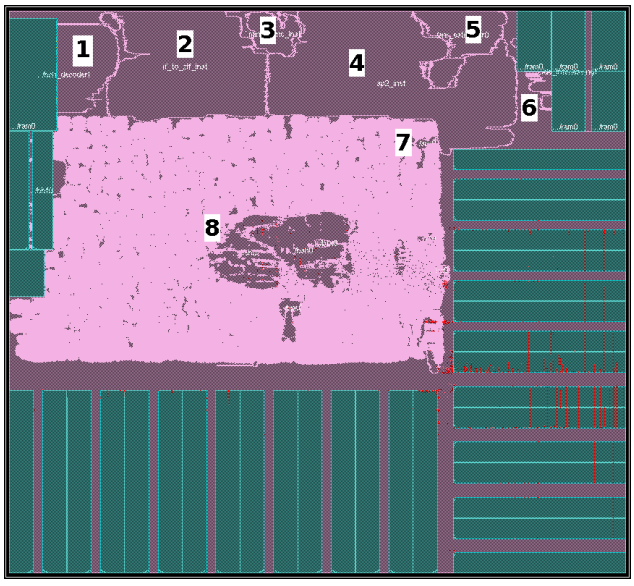

Fig. 7. Amoeba View of the Die: 1) BCH Decoder, 2) IF to ZIF, 3)Time Synchronization and Decimator, 4) Equalization logic, 5)SNR Estimator, 6) Deinterleaver, 7) Glue Logic, 8) LDPC Logic.

Table II presents some synthesis and placement results:

TABLE II. SYNTHESIS AND BACK-END RESULTS

Synthesis	**Cells**	**Area**	**Power**	
	689582	$8941460\mu m$	$596863.272\mu W$	
Back-End	**Die Area**	**STD Cells Area**	**Gates**	**Density**
	$14600000.00\mu m$	$3009818\mu m$	3135227	37.577%

IX. CONCLUSION

In this article, the design flow for a DVB-S2 receiver implementation in FPGA targeting an ASIC is presented. Results for resources utilization of FPGA prototyping and preliminary results for $65nm$ CMOS technology are also given. An overview on the signal processing algorithms and DVB-S2 specific functionalities is also presented.

It is shown that the hardware prototype is able to synchronize and demodulate an 8-PSK DVB-S2 compliant signal, corrupted by all the impairments expected in a digital receiver, with acceptable implementation losses, except for the Code Rate 3/5. Nevertheless, the FEC decoding Physical Verification has shown a BER consistent with the standard. This result will be presented in a specific paper regarding FEC decoding. Moreover, with the VLSI implementation it was observed that a fraction of the die area is spent to fix routing congestion due to the format and amount of the memory IPs. The next phase of the project is to optimize the Signal Processing partition for low Eb/No, the integration of the Adaptive Equalizer and memory studies in order to achieve optimal area.

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