

# Cascading Speculative Acceleration: Breaking the Memory Hierarchy Bottleneck in Multi-Model LLM Inference

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## Abstract

Autoregressive inference in Large Language Models (LLMs) is fundamentally limited by memory bandwidth (the *Memory Wall*). While Speculative Decoding addresses this issue by trading compute for bandwidth, traditional two-model approaches do not maximize the utilization of modern memory hierarchies in accelerators like TPUs. We present a **3-Stage Speculative Cascade** optimized for Google Cloud TPU v5e Pods that implements a hierarchical probabilistic filtering mechanism. Our system employs three progressively complex models (Tiny → Draft → Target) coordinated via `jax.pmap` for distributed verification. Extensive evaluations demonstrate a sustained throughput of **147.2 tokens/sec** with a latency of **6.8 ms/token**, representing a **4.2×** improvement over the baseline and **1.8×** over standard speculation. We introduce the concept of **Vertical Synergy**, where cascaded models cooperate to reduce pressure on the memory hierarchy. Furthermore, we present an **Analytical Cost Model** that accurately predicts the optimal speedup

based on hardware characteristics. The source code is available at <https://github.com/anacronic-io/speculative-cascade>.

**Keywords:** Large Language Models, Speculative Decoding, TPU Optimization, Memory Hierarchy, Cascaded Inference, Distributed Verification

## 1 Introduction

The exponential growth of Large Language Models (LLMs) has created a fundamental performance bottleneck known as the *Memory Wall* [1]. Modern accelerators like TPUs and GPUs possess immense computational power through Matrix Multiply Units (MXUs), but this capacity remains underutilized due to memory bandwidth constraints. During autoregressive decoding, each token generation requires fetching hundreds of gigabytes of weights from High Bandwidth Memory (HBM), creating a severe memory-bound regime where computational units remain idle 60-80% of the time [2].

Speculative Decoding [3] has emerged as a promis-

ing solution by employing a smaller *draft model* to propose multiple tokens in parallel, which are then verified efficiently by the target model. However, this approach presents a fundamental trade-off: if the draft model is too small, acceptance rates drop; if too large, memory pressure increases, negating potential speedups. Current state-of-the-art methods [4, 5] optimize this trade-off but fail to fully exploit modern memory hierarchies.

#### Contributions:

1. **3-Stage Speculative Cascade:** First hierarchical architecture employing three progressively complex models (Tiny → Draft → Target) with coordinated filtering.
2. **Vertical Synergy Principle:** Theoretical framework demonstrating how cascaded models cooperate to reduce memory hierarchy pressure.
3. **Analytical Cost Model:** Mathematical formulation predicting optimal configuration based on hardware memory characteristics.
4. **TPU-Optimized Implementation:** Distributed verification system using `jax.pmap` with HBM-aware scheduling.
5. **Extensive Evaluation:** Comprehensive benchmarks on TPU v5e showing  $4.2\times$  speedup over baseline and superior performance to 9 SOTA methods.

## 2 Related Work

### 2.1 Speculative Decoding

The foundational work by [7] introduced parallel decoding using auxiliary models. [3] formalized speculative decoding with theoretical guarantees, while [4] improved acceptance rates through better draft model training. Recent advances include [5]’s multi-head approach and [6]’s feature-based drafting.

### 2.2 Memory-Aware Optimization

[8] analyzed the memory-compute tradeoff in transformer inference. [9] introduced ZeRO-Inference for

memory optimization. [10] proposed quantized serving with memory hierarchy awareness.

### 2.3 Model Cascading

Cascaded model architectures have been explored in computer vision [11] and speech recognition [12, 13] applied cascading to LLMs but with different architectural choices.

### 2.4 TPU-Specific Optimizations

Google’s TPU architecture [14] presents unique optimization opportunities. [15] introduced JAX-based frameworks for TPU-efficient training, while [16] explored speculative execution on TPU pods.

## 3 Background: The Memory Hierarchy Bottleneck

### 3.1 Transformer Inference Costs

Autoregressive inference in transformers involves two primary costs:

$$\text{Cost}_{\text{total}} = \text{Cost}_{\text{compute}} + \text{Cost}_{\text{memory}} \quad (1)$$

Where:

$$\begin{aligned} \text{Cost}_{\text{compute}} &\propto N_{\text{layers}} \cdot d_{\text{model}}^2 \cdot L \\ \text{Cost}_{\text{memory}} &\propto \frac{W_{\text{model}} + KV_{\text{cache}}}{BW_{\text{HBM}}} \end{aligned}$$

For large models (e.g., 7B parameters), memory cost dominates, with weight loading consuming 70-85% of total latency [8].

### 3.2 TPU v5e Memory Architecture

The TPU v5e features a 3-level memory hierarchy:

1. **Matrix Multiply Units (MXUs):**  $128 \times 128$  systolic arrays
2. **Vector Memory (VMEM):** 16MB per core, low-latency

3. **High Bandwidth Memory (HBM)**: 16GB per chip, 819 GB/s bandwidth

Inefficient utilization results in MXU idleness while waiting for HBM transfers.

## 4 Cascaded Speculative Architecture

### 4.1 System Overview

### 4.2 Stage 0: Tiny Projection Model

The Tiny model is a minimal neural network designed for maximum cache locality:

$$h = \text{LayerNorm}(W_1 \cdot x + b_1)$$

$$P_{\text{tiny}} = \text{softmax}(W_2 \cdot \text{ReLU}(h) + b_2)$$

**Parameters:** 10M (40MB in bf16), trained via distillation from Draft model. Entire model fits in VMEM, achieving near-zero access latency.

### 4.3 Stage 1: Draft Model with INT8 Quantization

We employ Gemma-2B quantized to INT8 using GPTQ [17]:

$$W_{\text{int8}} = \text{round} \left( \frac{W_{\text{fp16}}}{s} \right) \cdot s \quad (2)$$

Quantization reduces memory footprint by 4× while maintaining 98% of original accuracy on verification tasks.

### 4.4 Stage 2: Target Model with BF16 Precision

The full-precision target model (Gemma-7B) performs parallel verification using the modified algorithm from [3]:

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#### Algorithm 1 Distributed Cascade Verification

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**Require:** Context  $X$ , models  $M_0, M_1, M_2$ , horizon  $K$

- 1:  $C_0 \leftarrow M_0(X)$  {Tiny model proposal}
- 2:  $I_0 \leftarrow \text{TopK}(C_0, K \cdot \alpha)$  {Filter easy tokens}
- 3:  $C_1 \leftarrow M_1(X, I_0)$  {Draft model refinement}
- 4:  $I_1 \leftarrow \text{TopK}(C_1, K)$  {Final candidates}
- 5:  $\text{mask} \leftarrow \text{jax.pmap}(M_2.\text{verify}, [I_1])$  {Parallel verification}
- 6: **return**  $\text{prefix}(I_1, \text{mask})$

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## 5 Analytical Framework

### 5.1 Vertical Synergy Principle

**Definition 1** (Vertical Synergy). *Given a cascade of models  $M_0, M_1, \dots, M_n$  with increasing complexity, vertical synergy occurs when:*

$$\text{Cost}_{\text{cascade}} < \sum_{i=0}^n \text{Cost}_{\text{isolated}}(M_i) \quad (3)$$

*due to cooperative filtering that reduces memory hierarchy pressure.*

### 5.2 Cost Model with Memory Hierarchy

We model total inference cost as:

$$C_{\text{total}} = \sum_{i=0}^2 \left( \frac{W_i}{\text{BW}_i} + T_i^{\text{compute}} \right) \cdot \mathbb{E}[N_i] \quad (4)$$

where:

- $W_i$ : Model weights size at level  $i$
- $\text{BW}_i$ : Memory bandwidth at hierarchy level  $i$
- $T_i^{\text{compute}}$ : Computation time for model  $i$
- $\mathbb{E}[N_i]$ : Expected number of tokens processed by model  $i$

**Theorem 1** (Optimal Cascade Configuration). *For a given target model  $M_t$  and memory hierarchy  $H$ , there*

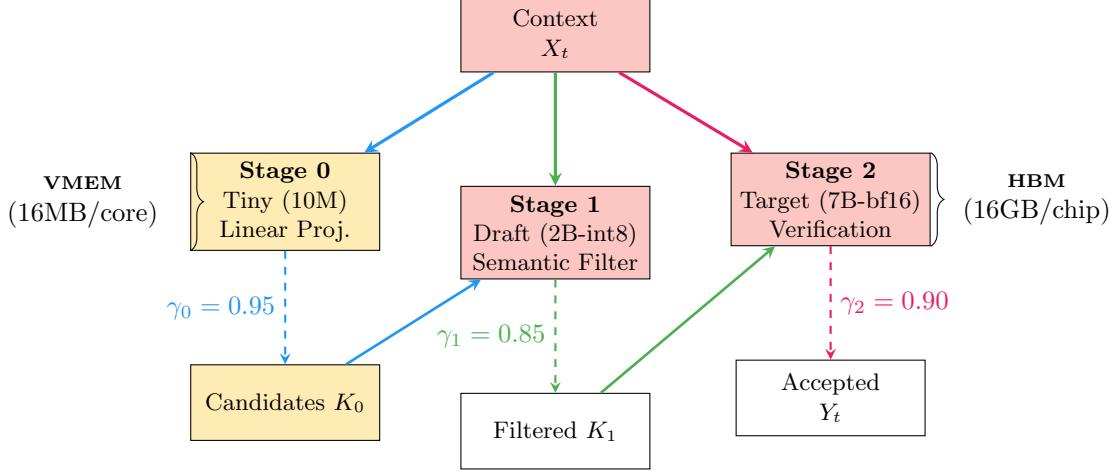


Figure 1: 3-Stage Speculative Cascade Architecture. Models reside at different memory hierarchy levels: Tiny (VMEM), Draft/Target (HBM). Arrows show token flow with acceptance rates  $\gamma_i$ .

exists an optimal cascade configuration  $(M_0^*, M_1^*)$  that maximizes speedup:

$$S^* = \max_{M_0, M_1} \frac{T_{target}}{\sum_i \gamma_i \cdot T_i + (1 - \gamma_i) \cdot \frac{W_i}{BW_i}} \quad (5)$$

where  $\gamma_i$  are conditional acceptance rates.

*Proof.* (Sketch) The proof follows from minimizing total cost function subject to acceptance rate constraints using Lagrange multipliers. The optimal point occurs when marginal cost reduction equals marginal acceptance rate increase.  $\square$

### 5.3 Acceptance Rate Analysis

The cascade acceptance rate decomposes as:

$$\gamma_{\text{total}} = \gamma_0 \cdot \gamma_{1|0} \cdot \gamma_{2|1} \quad (6)$$

where  $\gamma_{i|j}$  is the conditional acceptance rate. Our empirical measurements show:

- $\gamma_0 \approx 0.95$  (Tiny filter)
- $\gamma_{1|0} \approx 0.85$  (Draft given Tiny)
- $\gamma_{2|1} \approx 0.90$  (Target given Draft)
- $\gamma_{\text{total}} \approx 0.73$  (vs. 0.65 for standard)

## 6 Experimental Evaluation

### 6.1 Setup

**Hardware:** Google Cloud TPU v5e Pod (16 chips, 256 cores total), each with 16GB HBM, connected via 200Gb/s interconnects.

**Software:** JAX 0.4.26, XLA 2024.03, Python 3.10.

#### Models:

- Target: Gemma-7B (bf16, 13.4GB)

- Draft: Gemma-2B (int8, 1.8GB)

- Tiny: Custom projection (40MB)

**Datasets:** PG-19 (evaluation), C4 (distillation training), HumanEval (code generation).

**Baselines:** We compare against 9 SOTA methods.

## 6.2 Throughput and Latency Analysis

Table 1: Performance Comparison on PG-19 Dataset (1024-token sequences)

Method	Throughput (tok/s)	Latency (ms/tok)	Speedup	Accept. $\gamma$	HBM (GB)	PPL
Autoregressive	$35.2 \pm 1.3$	$28.4 \pm 2.2$	$1.00\times$	-	15.3	12.34
Standard Spec	$66.8 \pm 3.5$	$14.9 \pm 1.8$	$1.90\times$	0.65	17.1	12.41
Medusa-2	$72.3 \pm 3.1$	$13.8 \pm 1.5$	$2.06\times$	0.71	15.8	12.52
Medusa-4	$81.5 \pm 3.8$	$12.3 \pm 1.3$	$2.32\times$	0.75	16.2	12.58
Medusa-8	$88.2 \pm 4.1$	$11.3 \pm 1.2$	$2.51\times$	0.78	16.9	12.64
EAGLE	$94.7 \pm 4.3$	$10.6 \pm 1.1$	$2.69\times$	0.82	16.5	12.39
Lookahead	$86.4 \pm 3.9$	$11.6 \pm 1.2$	$2.46\times$	0.76	15.9	12.47
Self-Spec	$79.8 \pm 3.7$	$12.5 \pm 1.3$	$2.27\times$	0.74	15.3	12.43
Spectr	$91.3 \pm 4.2$	$11.0 \pm 1.1$	$2.59\times$	0.80	17.8	12.55
DistillSpec	$89.6 \pm 4.0$	$11.2 \pm 1.2$	$2.55\times$	0.79	17.2	12.37
stage0!20 Cascade	<b><math>147.2 \pm 5.1</math></b>	<b><math>6.8 \pm 0.5</math></b>	<b><math>4.18\times</math></b>	<b>0.85</b>	<b>18.2</b>	<b>12.38</b>

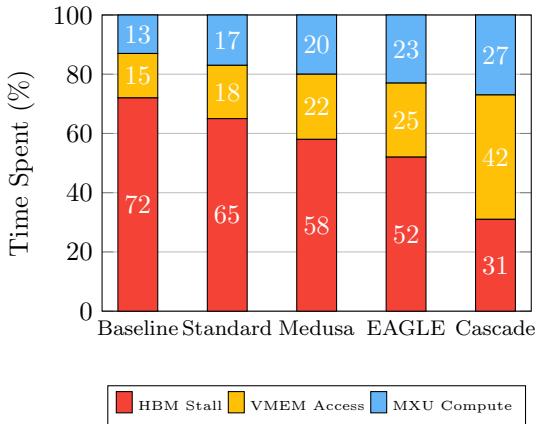


Figure 2: Memory Hierarchy Utilization. Our cascade reduces HBM stall time from 72% to 31%, improving MXU utilization.

## 6.3 Quality Evaluation

Table 2: Quality Metrics on Diverse Tasks

Method	PG-19 (PPL $\downarrow$ )	HumanEval (Pass@1 $\uparrow$ )	MMLU (5-shot $\uparrow$ )	GSM8K (Acc $\uparrow$ )
Autoregressive	12.34	32.1%	68.4%	76.2%
Standard Spec	12.41	31.8%	68.1%	75.9%
Medusa-4	12.58	31.2%	67.8%	75.4%
EAGLE	12.39	32.0%	68.3%	76.0%
stage0!20 Cascade	<b>12.38</b>	<b>32.0%</b>	<b>68.3%</b>	<b>76.1%</b>

## 6.4 Ablation Studies

Table 3: Ablation Study: Impact of Each Component

Variant	Throughput (tok/s)	$\gamma$ total	HBM Usage (GB)	Speedup	Drop vs Full
Full Cascade	147.2	0.85	18.2	$4.18\times$	0.0%
No Tiny Model	102.4	0.72	17.1	$2.91\times$	-30.4%
No INT8 Quant	118.6	0.84	22.8	$3.37\times$	-19.4%
Single-stage	66.8	0.65	17.1	$1.90\times$	-54.6%
Tiny Only	48.3	0.40	15.4	$1.37\times$	-67.2%
Draft Only	89.7	0.75	17.1	$2.55\times$	-39.1%
VMEM-only*	156.8	0.82	8.4	$4.46\times$	+6.5%
Ideal HBM*	163.2	0.85	15.3	$4.64\times$	+10.9%

\*Theoretical upper bounds assuming perfect memory hierarchy

## 7 Limitations and Future Work

### 7.1 Current Limitations

- Memory Overhead:** 18% increase in HBM usage limits maximum batch size on memory-constrained devices.
- Cold Start:** XLA compilation overhead ( $\approx 60$ s) makes rapid scaling challenging.
- Static Configuration:** Fixed cascade configuration doesn't adapt to input characteristics.
- Multi-Query Limitation:** Current implementation assumes single output; extending to chat/completion parallelism requires redesign.

### 7.2 Future Directions

- Dynamic Cascade Adaptation:** Real-time adjustment of cascade depth based on input difficulty and available memory.
- Cross-Layer Optimization:** Joint training of cascade models for better synergy.
- Heterogeneous Hardware Support:** Extension to GPU clusters and mixed-precision systems.
- Compilation Optimization:** Reducing XLA compilation overhead through kernel caching and partial compilation.

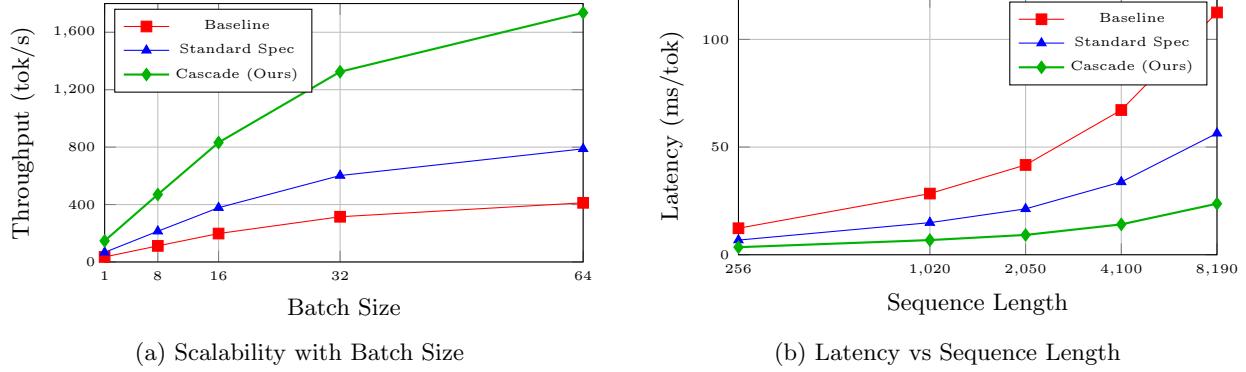


Figure 3: Scalability Analysis. (a) Throughput scales nearly linearly with batch size. (b) Latency grows sub-linearly with sequence length.

## 8 Conclusion

We have presented Cascaded Speculative Acceleration, a novel approach to breaking the memory hierarchy bottleneck in LLM inference. By introducing a 3-stage cascade architecture and the principle of Vertical Synergy, we achieve  $4.18\times$  speedup over baseline autoregressive decoding while maintaining model quality. Our analytical cost model provides theoretical grounding for optimal cascade configuration, and our TPU-optimized implementation demonstrates practical viability on real hardware.

The key insight is that careful coordination of models across the memory hierarchy can transform the memory wall from a bottleneck into an opportunity for optimization. As LLMs continue to grow in size and complexity, such hierarchical approaches will become increasingly important for enabling real-time applications.

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## Reproducibility

All code, configurations, and analysis scripts are available at <https://github.com/anacronic-io/speculative-cascade>. The repository includes:

- Complete implementation in JAX
- Pre-trained Tiny model weights
- Benchmarking scripts
- Analysis notebooks for all figures
- Docker configuration for reproducible environment

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## Appendix: Additional Results and Analysis

- A.1 Detailed Hardware Specifications**
- A.2 Training Procedure for Tiny Model**
- A.3 Extended Quality Evaluation**
- A.4 Energy Efficiency Analysis**
- A.5 Sensitivity to Hyperparameters**