آناهیتا اسدی
9724453

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Performing bidirectional port resolution...

Synthesizing Unit <FIFO256>.
    Related source file is "D:/ISE/FIFO256/FIFO256.vhd".
    Found 8-bit register for signal <dout>.
    Found 1-bit register for signal <full>.
    Found 1-bit register for signal <empty>.
    Found 8-bit 256-to-1 multiplexer for signal <$varindex0000> created at
line 71.
    Found 2048-bit register for signal <ram>.
    Found 8-bit up counter for signal <rd_addr>.
    Found 8-bit up counter for signal <wr_addr>.
INFO:Xst:738 - HDL ADVISOR - 2048 flip-flops were inferred for signal <ram>.
You may be trying to describe a RAM in a way that is incompatible with block
and distributed RAM resources available on Xilinx devices, or with a specific
template that is not supported. Please review the Xilinx resources
documentation and the XST user manual for coding guidelines. Taking advantage
of RAM resources will lead to improved device usage and reduced synthesis
time.
    Summary:
      inferred   2 Counter(s).
      inferred 2058 D-type flip-flop(s).
      inferred   8 Multiplexer(s).
Unit <FIFO256> synthesized.
=========================================================================
HDL Synthesis Report

Macro Statistics
# Counters                                             : 2
 8-bit up counter                                      : 2
# Registers                                            : 259
 1-bit register                                        : 2
 8-bit register                                        : 257
# Multiplexers                                         : 1
 8-bit 256-to-1 multiplexer                            : 1
=========================================================================
=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 2
 8-bit up counter                                      : 2
# Registers                                            : 2058
```

```
 Flip-Flops                                            : 2058
# Multiplexers                                         : 1
 8-bit 256-to-1 multiplexer                            : 1
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s400pq208-4

 Number of Slices:                     1795  out of   3584    50%
 Number of Slice Flip Flops:           2151  out of   7168    30%
 Number of 4 input LUTs:               1374  out of   7168    19%
 Number of IOs:                          22
 Number of bonded IOBs:                  22  out of    141    15%
 Number of GCLKs:                         2  out of      8    25%

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 7.956ns (Maximum Frequency: 125.691MHz)
   Minimum input arrival time before clock: 8.603ns
   Maximum output required time after clock: 7.165ns
   Maximum combinational path delay: No path found
```