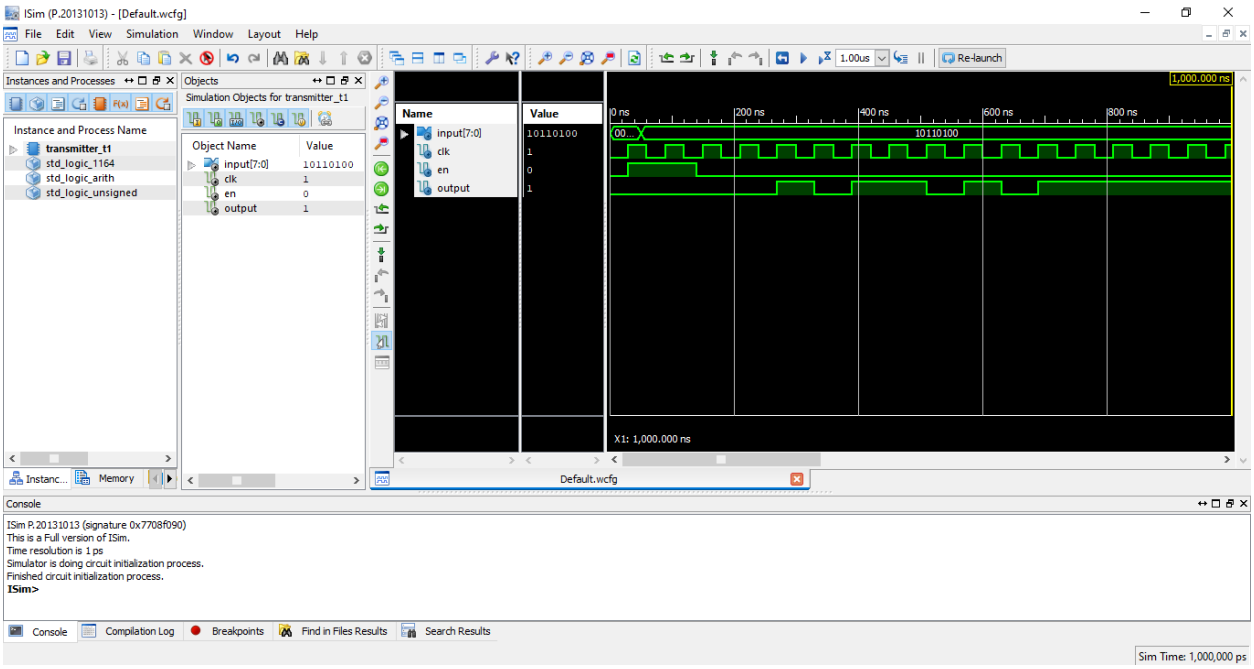
آناهیتا اسدی
9724453

Transmitter

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Performing bidirectional port resolution...

Synthesizing Unit <transmitter>.
    Related source file is "D:/ISE/HW5/UART/transmitter.vhd".
INFO:Xst:2117 - HDL ADVISOR - Mux Selector <pr_state> of Case statement line 70 was
re-encoded using one-hot encoding. The case statement will be optimized (default
statement optimization), but this optimization may lead to design initialization
problems. To ensure the design works safely, you can:
       - add an 'INIT' attribute on signal <pr_state> (optimization is then done
without any risk)
       - use the attribute 'signal_encoding user' to avoid onehot optimization
       - use the attribute 'safe_implementation yes' to force XST to perform a safe
(but less efficient) optimization
    Using one-hot encoding for signal <pr_state>.
WARNING:Xst:737 - Found 11-bit latch for signal <nx_state>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 8-bit latch for signal <parity>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
    Found 1-bit register for signal <flag>.
    Found 8-bit register for signal <in_reg>.
    Found 8-bit adder for signal <parity$addsub0000>.
    Found 11-bit register for signal <pr_state>.
    Summary:
       inferred  20 D-type flip-flop(s).
       inferred   1 Adder/Subtractor(s).
Unit <transmitter> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic
operations in this design can share the same physical resources for reduced device
utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 8-bit adder                                          : 1
# Registers                                            : 3
```

```
 1-bit register                                        : 1
 11-bit register                                       : 1
 8-bit register                                        : 1
# Latches                                             : 2
 11-bit latch                                          : 1
 8-bit latch                                           : 1

=========================================================================
=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                  : 1
 8-bit adder                                           : 1
# Registers                                           : 20
 Flip-Flops                                            : 20
# Latches                                             : 2
 11-bit latch                                          : 1
 8-bit latch                                           : 1
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s400pq208-4

 Number of Slices:                       19  out of   3584     0%
 Number of Slice Flip Flops:             24  out of   7168     0%
 Number of 4 input LUTs:                 19  out of   7168     0%
 Number of IOs:                          11
 Number of bonded IOBs:                  11  out of    141     7%
    IOB Flip Flops:                       8
 Number of GCLKs:                         1  out of      8    12%

TIMING REPORT
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 20    |
parity_or0000(parity_or00001:O)    | NONE(*)(parity_0)      | 1     |
nx_state_not0001(nx_state_not00011:O)| NONE(*)(nx_state_0)   | 11    |
-----------------------------------+------------------------+-------+
(*) These 2 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by
XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert
these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
```

```
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4
   Minimum period: 2.290ns (Maximum Frequency: 436.681MHz)
   Minimum input arrival time before clock: 4.744ns
   Maximum output required time after clock: 13.266ns
   Maximum combinational path delay: No path found
```

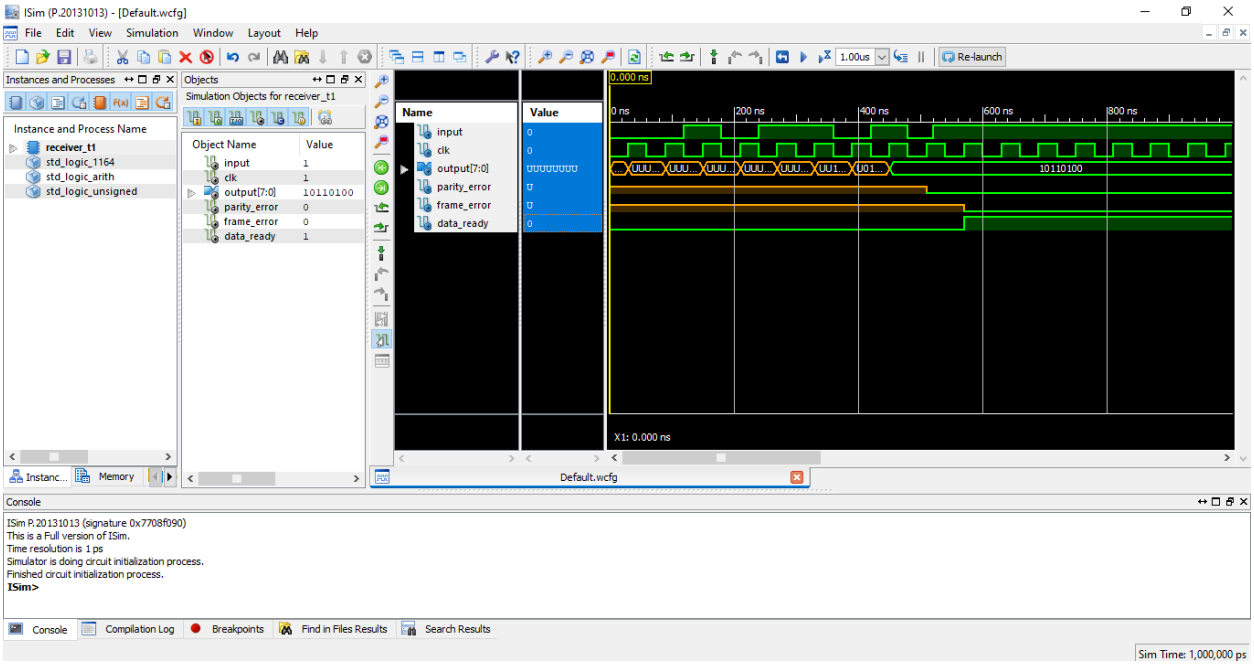


Receiver

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Performing bidirectional port resolution...

Synthesizing Unit <receiver>.
    Related source file is "D:/ISE/HW5/UART/receiver.vhd".
WARNING:Xst:646 - Signal <parity<7:4>> is assigned but never used. This unconnected
signal will be trimmed during the optimization process.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_error>. Latches may be
generated from incomplete case or if statements. We do not recommend the use of
latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_0>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_1>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_2>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_3>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_0>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_1>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_2>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_3>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_4>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_5>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_6>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <frame_error>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_7>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
    Using one-hot encoding for signal <pr_state>.
WARNING:Xst:737 - Found 11-bit latch for signal <nx_state>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
```

```
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <data_ready>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
    Found 11-bit register for signal <pr_state>.
    Summary:
       inferred  11 D-type flip-flop(s).
Unit <receiver> synthesized.
=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                            : 1
 11-bit register                                       : 1
# Latches                                              : 16
 1-bit latch                                           : 15
 11-bit latch                                          : 1
=========================================================================
=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                            : 11
 Flip-Flops                                            : 11
# Latches                                              : 13
 1-bit latch                                           : 12
 11-bit latch                                          : 1
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s400pq208-4

 Number of Slices:                       13  out of   3584     0%
 Number of Slice Flip Flops:             23  out of   7168     0%
 Number of 4 input LUTs:                 10  out of   7168     0%
 Number of IOs:                          13
 Number of bonded IOBs:                  13  out of    141     9%
    IOB Flip Flops:                      11
 Number of GCLKs:                         1  out of      8    12%

TIMING REPORT
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
```

```
------------------
---------------------------------------+------------------------+-------+
Clock Signal                           | Clock buffer(FF name)  | Load  |
---------------------------------------+------------------------+-------+
clk                                    | BUFGP                  | 11    |
pr_state_1                             | NONE(parity_0)         | 2     |
data_ready_not0001(data_ready_not00011:O)| NONE(*)(data_ready)    | 1     |
pr_state_8                             | NONE(output_7)         | 1     |
pr_state_10                            | NONE(frame_error)      | 1     |
pr_state_7                             | NONE(output_6)         | 1     |
pr_state_6                             | NONE(output_5)         | 1     |
pr_state_5                             | NONE(output_4)         | 1     |
pr_state_4                             | NONE(output_3)         | 1     |
pr_state_3                             | NONE(output_2)         | 1     |
pr_state_2                             | NONE(output_1)         | 1     |
pr_state_9                             | NONE(parity_error)     | 1     |
data_ready_and0000(data_ready_and00001:O)| NONE(*)(nx_state_0)    | 11    |
---------------------------------------+------------------------+-------+
(*) These 2 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by
XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert
these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4
   Minimum period: No path found
   Minimum input arrival time before clock: 3.564ns
   Maximum output required time after clock: 7.078ns
   Maximum combinational path delay: No path found
```


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
receiver_t1
std_logic_1164
std_logic_arith
std_logic_unsigned
Objects
Simulation Objects for receiver_t1
Object Name Value
input 1
clk 1
output[7:0] 10110100
parity_error 0
frame_error 0
data_ready 1
Name
Value
0.000 ns
0 ns
200 ns
400 ns
600 ns
800 ns
10110100
X1: 0.000 ns
Default.wcfg
Console
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps

UART

```
=========================================================================
*                            HDL Synthesis                              *
=========================================================================
Performing bidirectional port resolution...

Synthesizing Unit <transmitter>.
    Related source file is "D:/ISE/HW5/UART/transmitter.vhd".
INFO:Xst:2117 - HDL ADVISOR - Mux Selector <pr_state> of Case statement line 67 was
re-encoded using one-hot encoding. The case statement will be optimized (default
statement optimization), but this optimization may lead to design initialization
problems. To ensure the design works safely, you can:
       - add an 'INIT' attribute on signal <pr_state> (optimization is then done
without any risk)
       - use the attribute 'signal_encoding user' to avoid onehot optimization
       - use the attribute 'safe_implementation yes' to force XST to perform a safe
(but less efficient) optimization
    Using one-hot encoding for signal <pr_state>.
WARNING:Xst:737 - Found 11-bit latch for signal <nx_state>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 8-bit latch for signal <parity>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
    Found 1-bit register for signal <flag>.
    Found 8-bit register for signal <in_reg>.
    Found 8-bit adder for signal <parity$addsub0000>.
    Found 11-bit register for signal <pr_state>.
    Summary:
      inferred  20 D-type flip-flop(s).
      inferred   1 Adder/Subtractor(s).
Unit <transmitter> synthesized.


Synthesizing Unit <receiver>.
    Related source file is "D:/ISE/HW5/UART/receiver.vhd".
WARNING:Xst:646 - Signal <parity<7:4>> is assigned but never used. This unconnected
signal will be trimmed during the optimization process.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_error>. Latches may be
generated from incomplete case or if statements. We do not recommend the use of
latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_0>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_1>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
```

```
WARNING:Xst:737 - Found 1-bit latch for signal <parity_2>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <parity_3>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_0>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_1>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_2>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_3>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_4>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_5>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_6>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <frame_error>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <output_7>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
    Using one-hot encoding for signal <pr_state>.
WARNING:Xst:737 - Found 11-bit latch for signal <nx_state>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
WARNING:Xst:737 - Found 1-bit latch for signal <data_ready>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in
FPGA/CPLD designs, as they may lead to timing problems.
INFO:Xst:2371 - HDL ADVISOR - Logic functions respectively driving the data and gate
enable inputs of this latch share common terms. This situation will potentially lead
to setup/hold violations and, as a result, to simulation problems. This situation may
come from an incomplete case statement (all selector values are not covered). You
should carefully review if it was in your intentions to describe such a latch.
    Found 11-bit register for signal <pr_state>.
    Summary:
      inferred  11 D-type flip-flop(s).
Unit <receiver> synthesized.


Synthesizing Unit <UART>.
    Related source file is "D:/ISE/HW5/UART/UART.vhd".
```

```
Unit <UART> synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic
operations in this design can share the same physical resources for reduced device
utilization. For improved clock frequency you may try to disable resource sharing.
=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 8-bit adder                                          : 1
# Registers                                            : 4
 1-bit register                                       : 1
 11-bit register                                      : 2
 8-bit register                                       : 1
# Latches                                              : 18
 1-bit latch                                          : 15
 11-bit latch                                         : 2
 8-bit latch                                          : 1
=========================================================================
=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 8-bit adder                                          : 1
# Registers                                            : 31
 Flip-Flops                                           : 31
# Latches                                              : 15
 1-bit latch                                          : 12
 11-bit latch                                         : 2
 8-bit latch                                          : 1
=========================================================================
Device utilization summary:
---------------------------
Selected Device : 3s400pq208-4

 Number of Slices:                       33  out of   3584     0%
 Number of Slice Flip Flops:             47  out of   7168     0%
 Number of 4 input LUTs:                 26  out of   7168     0%
 Number of IOs:                          21
 Number of bonded IOBs:                  21  out of    141    14%
    IOB Flip Flops:                      19
 Number of GCLKs:                         1  out of      8    12%

TIMING REPORT
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------------------+------------------------+-------+
Clock Signal                                   | Clock buffer(FF name)  | Load  |
-----------------------------------------------+------------------------+-------+
```

```
U1/nx_state_not0001(U1/nx_state_not00011:O)     | NONE(*)(U1/nx_state_10)| 11    |
U1/parity_or0000(U1/parity_or00001:O)           | NONE(*)(U1/parity_0)   | 1     |
clock                                           | BUFGP                  | 31    |
U2/data_ready_and0000(U2/data_ready_and00001:O)| NONE(*)(U2/nx_state_10)| 11    |
U2/pr_state_9                                   | NONE(U2/parity_error)  | 1     |
U2/pr_state_2                                   | NONE(U2/output_1)      | 1     |
U2/pr_state_3                                   | NONE(U2/output_2)      | 1     |
U2/pr_state_4                                   | NONE(U2/output_3)      | 1     |
U2/pr_state_5                                   | NONE(U2/output_4)      | 1     |
U2/pr_state_6                                   | NONE(U2/output_5)      | 1     |
U2/pr_state_7                                   | NONE(U2/output_6)      | 1     |
U2/pr_state_10                                  | NONE(U2/frame_error)   | 1     |
U2/pr_state_8                                   | NONE(U2/output_7)      | 1     |
U2/data_ready_not0001(U2/data_ready_not00011:O)| NONE(*)(U2/data_ready) | 1     |
U2/pr_state_1                                   | NONE(U2/parity_0)      | 2     |
------------------------------------------------+------------------------+-------+
(*) These 4 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by
XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert
these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4
   Minimum period: 2.290ns (Maximum Frequency: 436.681MHz)
   Minimum input arrival time before clock: 4.744ns
   Maximum output required time after clock: 7.078ns
   Maximum combinational path delay: No path found
```