TÉCNICO LISBOA

Circuit Theory and Electronics Fundamentals

Mestrado em Engenharia Física Tecnológica, Técnico, University of Lisbon

Ana Martins (96506), Miguel Moreira (96556), Sara Oliveira (96566)

T2

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1 Introduction

The objective of this laboratory assignment is to study a circuit containing an Independent AC Voltage Souce, $V_s(t)$, a Voltage Controlled Current Source, I_d, a Current Controlled Voltage Source, V_d, a Capacitor C, and seven resistors, R_1 to R_7. The circuit that we were first presented with is displayed in Figure **??**, with some added current directions to ease the process of finding equations in our Analysis section. As we make modifications to the circuit along the report to suit our needs, the circuit used for those will also be displayed.

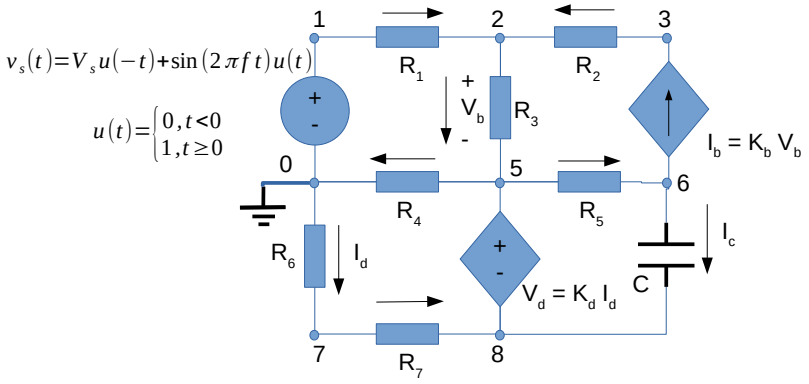

Figure 1: The original circuit, with some current directions added.

In Section 2, a theoretical analysis of the circuit is presented, including the study of what happens for $t < 0$, finding the the equivalent resistor as seen from the capacitor terminals, the natural and forced solutions of the circuit in $t > 0$, as well as frequency analysis.

In Section 3, the circuit is analysed by simulation using the *software Ngspice*, ultimately, studying the same as in the Theoretical Analysis section. The results in each Analsysis are compared 4. The conclusions of this study are outlined in Section 5.

2 Theoretical Analysis

2.1 Node Analysis ($t < 0$)

In this particular section, the circuit is analysed in $t < 0$, therefore, we can apply the usual node analysis, with no sinusoidal tensions in the voltage source Vs: for $t < 0$ $v_s = Vs$.

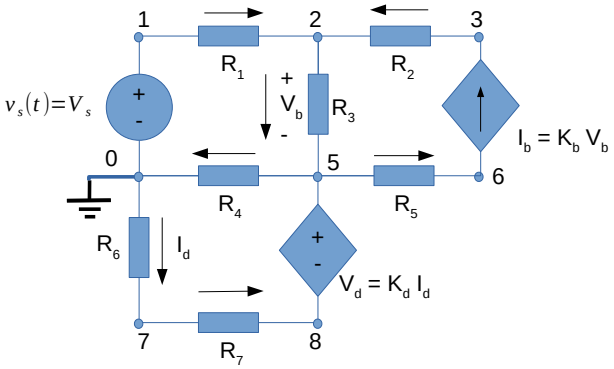

Figure 2: The circuit at $t < 0$

Labels were assigned to identify nodes from zero to eight (no node four given in instructions), and directions to currents as seen in figure (2), to then proceed with the node analysis. We can, therefore, derive direct equations in terms of the voltage at these nodes.

For this procedure, one applies KCL (Kirchoff's Current Law), which states that the sum of currents leaving a node must be the same as the sum of currents entering a node. Because this kind of approach is only possible for the nodes which aren't directly connected to a terminal of a voltage source, it's crucial to find other equations to cover all the unknown variables of the system. In this case, it's important to consider factors like the voltage gain between two nodes separated by a voltage source: for example, from nodes 0 and 1, the terminals of v_s, we can take the equation: $V_1 = V_0 + V_s$. As V_0 is identified as the ground ($V_0 = 0V$) we're left with: $V_1 = V_s$.

Moreover, we can relate the currents associated with the current or voltage controlled sources with the nodes voltages, giving us two more equations, the nineth and tenth.

The equations are as follows:

$$\begin{cases} Node\,0 : V_0 = 0 \\ Node\,1 : V_1 = V_s \\ Node\,2 : \frac{V_1 - V_2}{R_1} + \frac{V_3 - V_2}{R_2} - \frac{V_2 - V_5}{R_3} = 0 \\ Node\,3 : -\frac{V_3 - V_2}{R_2} + I_b = 0 \\ Node\,5 : V_5 - V_8 = V_d \\ Node\,6 : \frac{V_5 - V_6}{R_5} - I_b = 0 \\ Node\,7 : \frac{V_0 - V_7}{R_6} - \frac{V_7 - V_8}{R_7} = 0 \\ Supernode\,5 - 8 : \frac{V_2 - V_5}{R_3} - \frac{V_5 - V_6}{R_5} + \frac{V_7 - V_8}{R_7} - \frac{V_5 - V_0}{R_4} = 0 \\ I_d = \frac{V_0 - V_7}{R_6} \\ I_b = K_b\,(V_2 - V_5) \end{cases} \tag{1}$$

Note that, as there's no sinusoidal excitation ($v_s = constant$), the capacitor behaves like an open circuit and so the current I_c is null and not included in the equations.

Using *GNUOctave*, we computed the values of the node voltages by solving the system KCL equations above with matrixes. The currents in each branch were solved by aplication of Ohm's law ($I = \frac{V}{R}$) in each resistor, for example:

$$I_1 = \frac{V_1 - V_2}{R_1} \tag{2}$$

The value obtained are listed in the next tables:

Name	Currents [A]
I1	2.3690260e-04
I2	-2.4828279e-04
I3	-1.1380187e-05
I4	1.2106395e-03
I5	-2.4828279e-04
I6	9.7373690e-04
I7	9.7373690e-04
Ib	-2.4828279e-04
Id	9.7373690e-04

Table 1: T2 1) Node Analysis Computation Results: Currents (A) computed using Ohm's law

Name	Voltages [V]
V0	-0.0000000e+00
V1	5.1850419e+00
V2	4.9415541e+00
V3	4.4258319e+00
V5	4.9770105e+00
V6	5.7290070e+00
V7	-1.9765220e+00
V8	-2.9546889e+00
Vb	-3.5456366e-02
Vd	7.9316995e+00

Table 2: T2 1) Node Analysis Computation Results: Voltages computed using KCL equations

2.2 Determining the Equivalent Resistance as Seen From Capacitor Terminals

We start by turning off the independent voltage source, v_s, so we can study how the capacitor's charge disspates through the circuit. This is equivalent to connecting the capacitor in series with an equivalent resistor. This will be needed in the following section, where we'll be determining the differential equation that describes the original circuit.

Once we turn off v_s, it's crucial to make sure that there aren't discontinuous jumps in the circuits voltage, otherwise, we would obtain an infinite current as the capactior's equation states (voltage derivative):

$$I_c(t) = C\frac{dv(t)}{dt} \tag{3}$$

Straightfowardly, the voltages at the capacitor's terminals must remain the same as before turning v_s off. To do so, we can, theoretically, substitute the capacitor with an independent voltage source, V_x, where $V_x = V_6 - V_8$, forcing the circuit's equations, while v_s is off, to follow this boundary conditions.

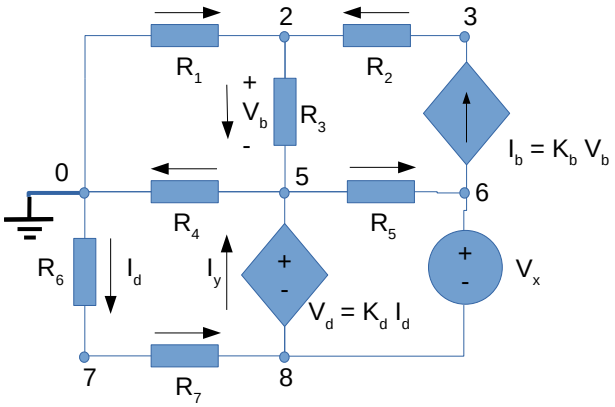

Figure 3: The circuit used to determine R_{eq}

Having done that, the circuit can once again be figured out using nodal analysis, as done in the previous section. However, instead of using supernode equations (which would be problematic since we have a voltage source connected to another voltage source), we created two new variables, I_x and I_y, which, of course, require two new equations: these are now easily obtained since we can write KCL even in nodes connected to voltage sources. We end up with the equations:

$$
\begin{cases}
Node\,0 : V_0 = 0 \\
Node\,2 : \frac{V_0 - V_2}{R_1} + \frac{V_3 - V_2}{R_2} - \frac{V_2 - V_5}{R_3} = 0 \\
Node\,3 : -\frac{V_3 - V_2}{R_2} + I_b = 0 \\
Node\,5.1 : V_5 - V_8 = V_d \\
Node\,6.1 : V_6 - V_8 = V_x \\
Node\,7 : \frac{V_0 - V_7}{R_6} - \frac{V_7 - V_8}{R_7} = 0 \\
Node\,8 : \frac{V_7 - V_8}{R_7} - I_y - I_x = 0 \\
Node\,5.2 : I_y + \frac{V_2 - V_5}{R_3} - \frac{V_5 - V_6}{R_5} - \frac{V_5 - V_0}{R_4} = 0 \\
Node\,6.2 : I_x + \frac{V_5 - V_6}{R_5} - I_b = 0 \\
I_b = K_b\,(V_2 - V_5) \\
V_d = K_d\,\frac{V_0 - V_7}{R_6}
\end{cases}
\tag{4}
$$

The nodal voltages resulting from these equations are compiled in the table 3; I_x and I_y, aswell as the other currents obtained via Ohm's Law are in 4 and the equivalent resistor, R_{eq}, obtained via the equation $R_{eq} = \frac{V_x}{I_x}$, is in the table 5.

Name	Voltages [V]
V0	-0.0000000e+00
V2	-9.4611569e-17
V3	5.4078486e-16
V5	-1.3829564e-16
V6	8.6836959e+00
V7	1.0331506e-16
V8	2.7630332e-16
Vb	4.3684073e-17
Vd	-4.1459897e-16

Table 3: Node Analysis Computation Results: Voltages computed using KCL equations

Name	Currents [A]
Ix	2.8670509e-03
Iy	-2.8670509e-03
I1	9.2052783e-20
I2	3.0589720e-19
I3	1.4020977e-20
I4	-3.3639906e-20
I5	-2.8670509e-03
I7	-1.7220481e-19
Ib	3.0589720e-19
Id	-5.0898337e-20

Table 4: Node Analysis Computation Results: Currents (A) computed using ohms law

Name	Currents [A]
Req	3.0287903e+03

Table 5: Equivalent Resistor as seen from the terminals of the capacitor

2.3 Determining the Natural Solution for $V_6(t)$

After reducing the rather complex circuit to a circuit with one voltage source, one resistor, R_{eq}, (between nodes with voltage V_s and V_6, with this direction of voltage drop) and one capacitor, we can easily determine the natural solution on the system. More specifically, we can observe the behaviour of the capacitor, dissipating voltage through the resistors without any external excitation or driving force.

To study this, we've worked out the voltage natural solution in node six (V_{6n}), in the interval [0, 20] ms.

For a simple RC series circuit (with a voltage source) we can derive the differential equation which describes the system. The natural solution is obtained by removing the voltage source: manipulating the differential equation yields:

$$V_{6n}(t) = Kexp\left(-\frac{t}{RC}\right) \tag{5}$$

,where K is an integration constant.

To determine K, we need an initial condition, such as $V_6(t = 0) = V_x$, determined in the last section. The final expression for $V_{6n}(t)$ is then:

$$V_{6n}(t) = V_x exp\left(-\frac{t}{RC}\right) \tag{6}$$

We used *GNUOctave* to compute and plot V_{6n} against time ([0, 20] ms), using a $1\mu s$ step, obtaining the following graphic:

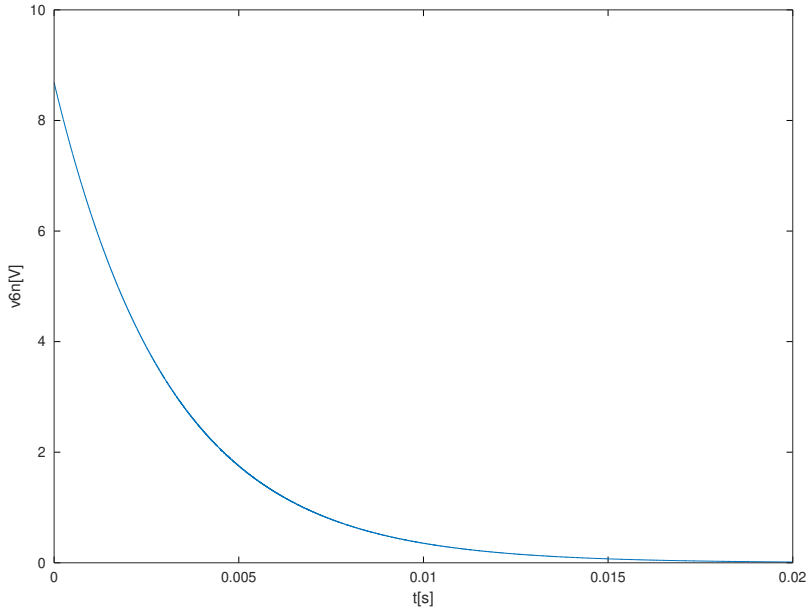

Figure 4: $V_{6n}(t)$, for t $\in$ [0, 20] ms

2.4 Determining the Forced Solution for $V_6(t)$

For $t > 0$, the independent voltage source, v_s, provides a sinusoidal excitation, which means the capacitor will now behave as expected and will dissipate current through it, I_c: this complicates the circuit tremendously. Working with sinusoidal functions in such big circuits requires a lot of computational work, thus, we will not do that. By transfering our voltages, currents and resistors to the complex domain, we can analyse the circuit and obtain complex solutions which, in the end, can be retrievable to the real world. The nodal analysis will be in everything similar to the previous sections, except for the fact that we substitute voltage V_i for phasor $\tilde{V}_i$, current I_i for $\tilde{I}_i$ and resistor R_i for impedance Z_i.

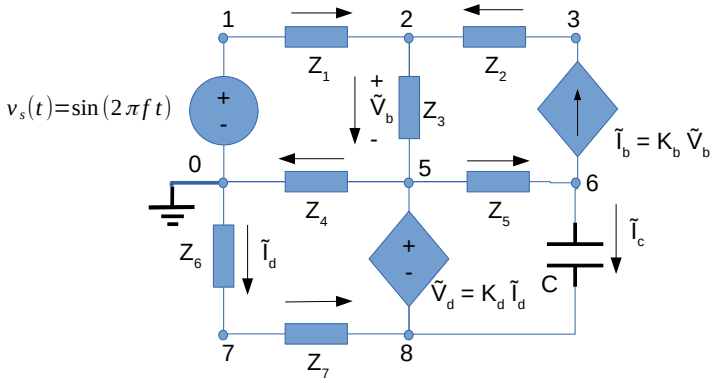

Figure 5: The circuit for $t > 0$, all variables in the complex domain

Moreover, the impedance of the resistor is equal to the resistor itself ($Z_i = R_i$) and the capacitor impedance can be written using the simple expression $Z_c = \frac{1}{j\omega C}$, in which $\omega = 2\pi f$ ($f = 1kHz$), the angular frequency of the source v_s and C is the capacitance, a characteristic of the given capacitor. The equations to solve are then

$$\begin{cases} Node\,0 : \tilde{V}_0 = 0 \\ Node\,1 : \tilde{V}_1 - \tilde{V}_0 = \tilde{V}_s \\ Node\,2 : \frac{\tilde{V}_1 - \tilde{V}_2}{Z_1} + \frac{\tilde{V}_3 - \tilde{V}_2}{Z_2} - \frac{\tilde{V}_2 - \tilde{V}_5}{Z_3} = 0 \\ Node\,3 : -\frac{\tilde{V}_3 - \tilde{V}_2}{Z_2} + \tilde{I}_b = 0 \\ Node\,5 : \tilde{V}_5 - \tilde{V}_8 = \tilde{V}_d \\ Node\,6 : \frac{\tilde{V}_5 - \tilde{V}_6}{Z_5} - \tilde{I}_b - \tilde{I}_c = 0 \\ Node\,7 : \frac{\tilde{V}_0 - \tilde{V}_7}{Z_6} - \frac{\tilde{V}_7 - \tilde{V}_8}{Z_7} = 0 \\ Supernode\,5-8 : \frac{\tilde{V}_2 - \tilde{V}_5}{Z_3} - \frac{\tilde{V}_5 - \tilde{V}_6}{Z_5} + \frac{\tilde{V}_7 - \tilde{V}_8}{Z_7} - \frac{\tilde{V}_5 - \tilde{V}_0}{Z_4} + \tilde{I}_c = 0 \\ \tilde{I}_b = K_b\,(\tilde{V}_2 - \tilde{V}_5) \\ \tilde{V}_d = K_d\,\frac{\tilde{V}_0 - \tilde{V}_7}{Z_6} \\ \tilde{I}_c = j2\pi f C(\tilde{V}_6 - \tilde{V}_8) \\ \tilde{V}_s = 1 \end{cases} \tag{7}$$

Name	Voltages [V]
V0real	-2.7665952e-17
V1real	1.0000000e+00
V2real	9.5304035e-01
V3real	8.5357688e-01
V5real	9.5987855e-01
V6real	-5.6551340e-01
V7real	-3.8119691e-01
V8real	-5.6984862e-01
V0imag	0.0000000e+00
V1imag	0.0000000e+00
V2imag	6.3899467e-16
V3imag	2.7780122e-15
V5imag	4.9193531e-16
V6imag	-8.5097837e-02
V7imag	-1.9536244e-16
V8imag	-2.9204596e-16

Table 6: Node Analysis Computation Results: Voltages computed using KCL equations

2.5 Determining the Final Total Solution for $V_6(t)$

The final solution for node 6, $V_6(t)$, is obtained by summing its natural and forced solutions. We know that the forced solution will oscillate with the same frequency of the source v_s, but we don't know its amplitude yet. Well, that's exatly why we did what we did in the previous section. Since v_s is a sine wave, we want $V_{6f}(t)$ to be a sine wave aswell, so we know we will have to extract the imaginary part of whatever expression we obtain. That expression is as follows

$$V_{6f}(t) = (V6real + j\,V6imag)\,e^{j\omega t} \tag{8}$$

Plotting $v_s(t)$ and $V_6(t)$, we end up with

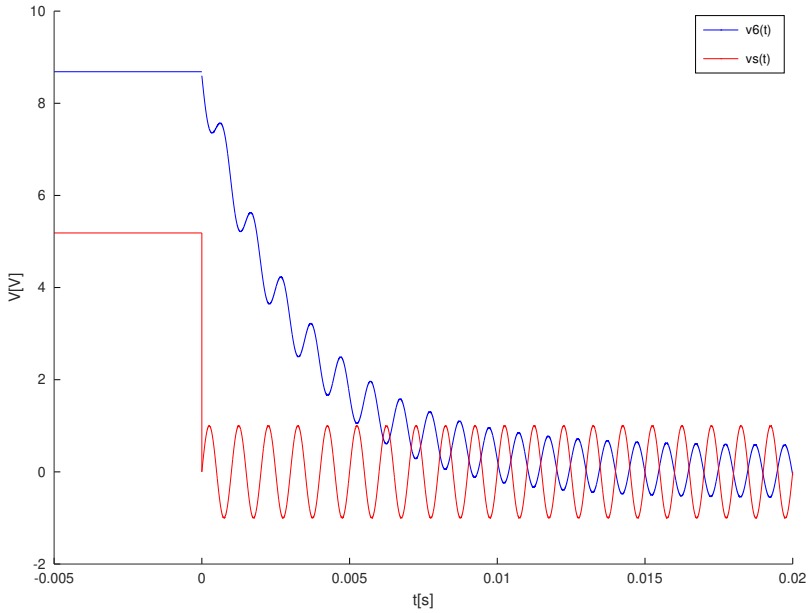

Figure 6: Voltage of V_6 and of the stimulus (V) vs. Time ($\in [0, 20]ms$) - Transient Analysis of the Original Circuit with a Forced Frequency of 1kHz

2.6 Frequency analysis

In this section, we analyse the frequency responses of $V_c(f) = V_6(f) - V_8(f)$ and $V_6(f)$, aswell as the behaviour of the source when we vary the frequency from 0.1 Hz to 1 MHz. This is usually done using a logarithmic scale for the frequency (base 10). We will plot the magnitude expressed in decibel (dB), a unit designed to easily give a human understanding to its value, since this circuit could, for example, be used in an amplifier, aswell as the phase expressed in degrees. Well, so far, every exercise was done using numeric computation, which provides less error, but this cannot be done here, since the nodal analysis requires every variable to be dependent on the frequency, f, otherwise, we would need milions of matrices... We call this symbolic computation. After running the same procedure as we did for subsection 4, even using those equations, we of course end up with nodal voltages, this time dependent on the frequency, $V_i(f)$. To do a bode plot, it is necessary to have a transfer function that depends on a variable, usually called s. s, in this case, is just $j \times f$, and this is very convenient since everywhere that f appears in a given nodal voltage, is in its imaginary part. We therefore end up with an expression for $V_i(f)$ whose numerator and denominator is a polinomial in terms of s. Well, it's exactly in this form ([numerator denominator]) that transfer functions are written in $GNUOctave$, so we are done. All that remains is actually plotting the results, but this is done simply using the $bode$ command.

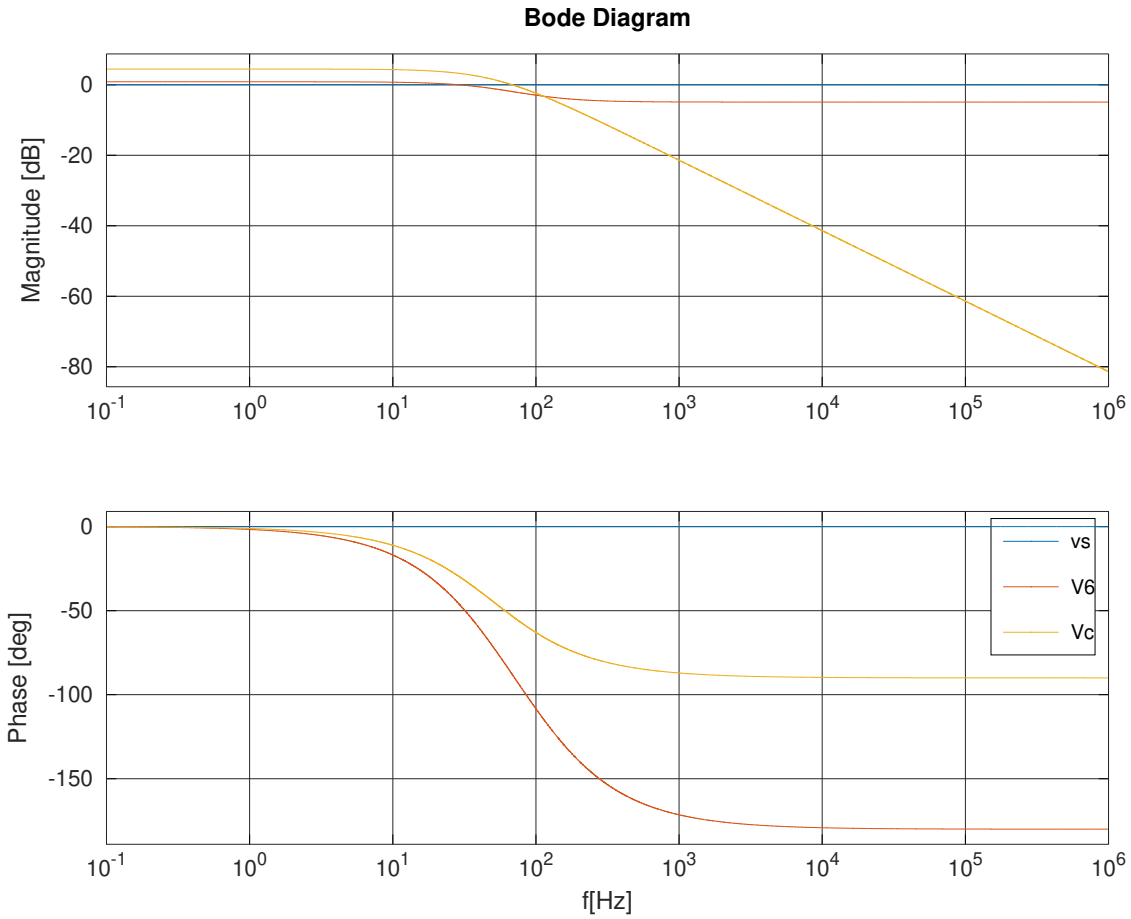

Figure 7: Bode plots for v_s, V_c and V_6, f $\in$ [0.1, 10^6] Hz

The first thing that the reader might notice is that the amplitude of v_s is always zero. This happens because v_s is the voltage source, so it mantains its amplitude constant throughout frequency changes, unlike V_6. It is zero because the amplitude would be 1 in Volts, but, transforming the units into dB, we have to do the base 10 logarithm of the amplitude in Volts, which results in an amplitude in dB of zero.

As we can observe, all of the phases are 0 at $f = 0.1Hz$ and then vary according to the frequency. The phase of v_s is always 0, because its sine wave has no phase.

3 Simulation Analysis

3.1 Operating Point Analysis - The Circuit for $t < 0$

Table 7 shows the simulated operating point results for the circuit under analysis, for $t < 0$.

Name	Value [A or V]
@gb[i]	-2.48284e-04
@r1[i]	2.369027e-04
@r2[i]	-2.48284e-04
@r3[i]	-1.13810e-05
@r4[i]	1.210640e-03
@r5[i]	-2.48284e-04
@r6[i]	9.737374e-04
@r7[i]	9.737374e-04
v(1)	5.185042e+00
v(2)	4.941554e+00
v(3)	4.425830e+00
v(5)	4.977013e+00
v(6)	5.729012e+00
v(7)	-1.97652e+00
v(8)	-2.95469e+00
v(9)	0.000000e+00

Table 7: Operating point results. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

These results and the ones that follow in this section were produced using the *Ngspice software*.

For this range of time, the circuit is time static, which means that the Capacitor C behaves as an open circuit. This is shown in Figure 8. As well as that modification, we also had to add a new Independent Voltage Source with a voltage of 0V whose current would be I_d, in order for *Ngspice* to recognise the Current-Controlled Voltage Source, defined in Figure 8 as H_d. Bearing this in mind the Voltage Source was added between node 0 and a new node 9, with node 9 being placed between the GROUND and the first terminal of R_6.

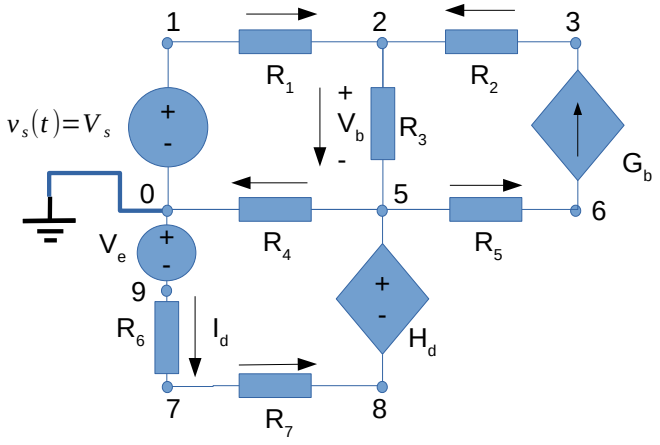

Figure 8: The original circuit at $t < 0$ with an added voltage source of value 0V.

3.2 Operating Point Analysis - Finding the Inital Conditions

In this section, we analyse the following circuit:

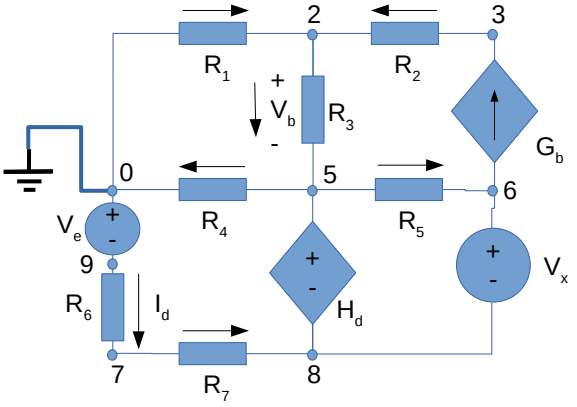

Figure 9: The original circuit with an added voltage source of value 0V.

Once again, the 0V Source is added for Ngspice to be able to recognise H_d. Analysing this circuit is useful for us to be able to find the inital conditions of the original circuit at V_6 and V_8, the nodes that the Capacitor is connected to. We need this information because, from now on, the analysis of the circuit will be time-dependent and we need to know the inital conditions for the circuit.

The results for the Operating Point Analysis are represented in Table 8.

Name	Value [A or V]
@gb[i]	3.571179e-18
@r1[i]	-3.40748e-18
@r2[i]	3.571179e-18
@r3[i]	1.636985e-19
@r4[i]	7.278356e-19
@r5[i]	-2.86705e-03
@r6[i]	5.854099e-19
@r7[i]	5.854099e-19
v(2)	3.502198e-15
v(3)	1.092010e-14
v(5)	2.992175e-15
v(6)	8.683696e+00
v(7)	-1.18828e-15
v(8)	-1.77636e-15
v(9)	0.000000e+00

Table 8: Operating point results. A variable preceded by @ is of type *current* and expressed in Ampere; other variables are of type *voltage* and expressed in Volt.

As expected, these results give us the values we were looking for: $V_6 = 8.683696V$ (which equals $V_6(t<0) - V_8(t<0)$), and $V_8 \approx 0$ (which, compared to the size of V_6, we can assume is actually 0).

3.3 Transient Analysis - No Forced Frequency

For our first time-dependent analysis, we analyse the original circuit in the interval $t \in [0, 20]ms$, with no forced frequency, adding onto it, once again, the 0V Source:

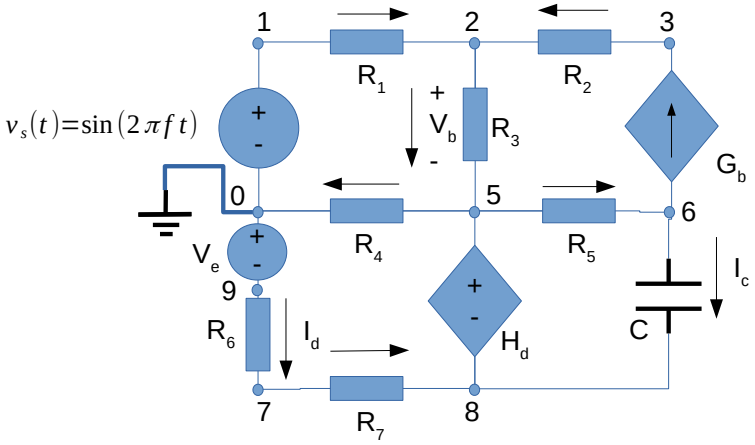

Figure 10: The original circuit with an added voltage source of value 0V.

This schematic of the circuit is the one that will also be followed in the next two sections.

For this analysis, we used the boundary conditions for V_6 and V_8 obtained in the previous section, with the AC Independent Voltage Source V_s following a sinusoidal signal, displayed in Figure 10. Considering the values obtained by *Octave* and *Ngspice* are the exact same until the 5th decimal number for both V_6 and V_8, we used the values obtained by *Octave*, as that was an easier way to automate the production of this report. The same was done in the following sections as well. The result of the Transient Analysis made by *Ngspice* is shown in Figure 11.

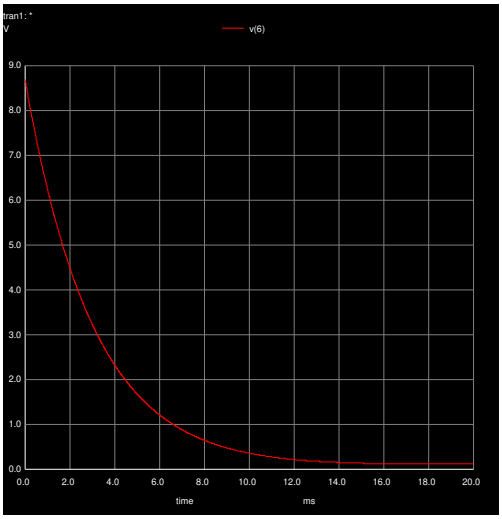

Figure 11: Voltage of V_6 (V) vs. Time ($\in [0, 20]ms$) - Transient Analysis of the Original Circuit with No Forced Frequency

As expected, the voltage of V_6 decays exponentially, as the Capacitor stores more and more energy as time goes by.

3.4 Transient Analysis - Forced Frequency of 1kHz

In this section, we repeat the exact same steps taken in the previous one, except we introduce a forced frequency signal of 1kHz on V_s. In Figure 12, we can observe the stimulus and the response in node 6.

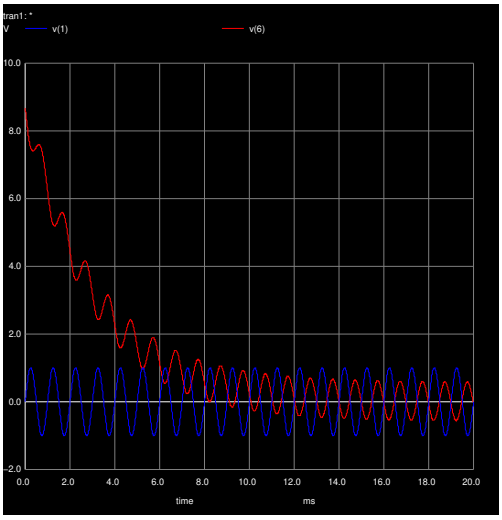

Figure 12: Voltage of V_6 and of the stimulus (V) vs. Time ($\in [0, 20]ms$) - Transient Analysis of the Original Circuit with a Forced Frequency of 1kHz

It is clear that the shape of $V_6(t)$ is the same as before, only now modulated by the stimulus, represented in Figure 12 in blue, with the label v(1), because the voltage in node 1 is made up of a difference in potencial in the GROUND (whose volatge is 0) and by the voltage created by V_s.

3.5 Frequency Analysis

We now look at the original circuit in a range of forced frequencies of 0.1Hz to 1MHz. In Figure fig:simgraph5db, we can observe the Amplitudes of V_6, V_s and V_c in dB, respectively represented by db(v(6)), db(v(1)) and db(v(6) - v(8)), as a function of the logarithm of the ranges of frequencies previously mentioned.

The first thing that the reader might notice is that the amplitude of V_s is always zero. This happens because V_s is the voltage source, so it mantains its amplitude constant throughout frequency changes, unlike V_6. It is zero because the amplitude would be 1 in Volts, but, transforming the units into dB, we have to do the base 10 logarithm of the amplitude in Volts, which results in an amplitude in dB of zero.

Lastly, we take a look at the phase of V_6, V_s and V_c, respectively ph(v(6)), ph(v(1)) and ph(v(6) - v(8)), as a function of the same range of frequencies in Figure 14.

As we can observe, all of the phases are 0 at $f = 0.1Hz$ and then vary according to the frequency. Looking at the whole plot, particularly at the graph of the phase of V_s, we can assume that *Ngspice* calculates the phase as (value for the fase at a certain node - value for the phase of the Voltage Source).

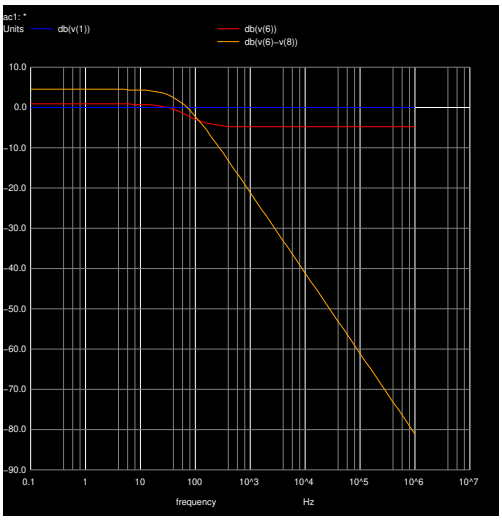

Figure 13: Amplitude of V_6, V_s and V_c (dB) vs. Frequency (Hz) - Frequency Analysis of the Original Circuit

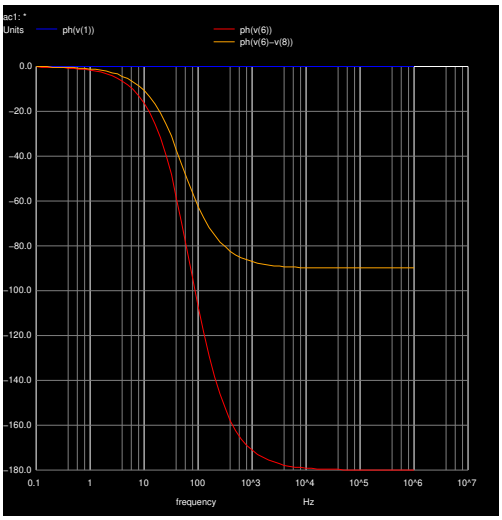

Figure 14: Phase of V_6, V_s and V_c (degrees) vs. Frequency (Hz) - Frequency Analysis of the Original Circuit

4 Comparing the Results

In this section, we will be comparing the results obtained by both the Theoretical Analysis and the Simulation.

4.1 Results for the System at $t < 0$

In the following tables, we can observe the results already presented in previous sections now side by side, with the first 2 tables being part of the Theoretical Analysis and the 3rd one being part of the Simulation. These are displayed in this way as a means of easier representation.

Name	Currents [A]
I1	2.3690260e-04
I2	-2.4828279e-04
I3	-1.1380187e-05
I4	1.2106395e-03
I5	-2.4828279e-04
I6	9.7373690e-04
I7	9.7373690e-04
Ib	-2.4828279e-04
Id	9.7373690e-04

Name	Voltages [V]
V0	-0.0000000e+00
V1	5.1850419e+00
V2	4.9415541e+00
V3	4.4258319e+00
V5	4.9770105e+00
V6	5.7290070e+00
V7	-1.9765220e+00
V8	-2.9546889e+00
Vb	-3.5456366e-02
Vd	7.9316995e+00

Name	Value [A or V]
@gb[i]	-2.48284e-04
@r1[i]	2.369027e-04
@r2[i]	-2.48284e-04
@r3[i]	-1.13810e-05
@r4[i]	1.210640e-03
@r5[i]	-2.48284e-04
@r6[i]	9.737374e-04
@r7[i]	9.737374e-04
v(1)	5.185042e+00
v(2)	4.941554e+00
v(3)	4.425830e+00
v(5)	4.977013e+00
v(6)	5.729012e+00
v(7)	-1.97652e+00
v(8)	-2.95469e+00
v(9)	0.000000e+00

Table 9: Results for the Circuit at $t < 0$

The first thing the reader may notice is that, while the Theoretical Analysis results have 7 decimal places, the Simulation ones only have either 5 or 6, depending on the variable and with Cientific Notation. With this being said, all of the results of the currents are accurate until, at least, 4 decimal places with Cientific Notation, which translates into around 8 accurate decimal places in normal decimal notation. All of the results of the voltages are accurate until either the last number that appears in the Simulation results or the second to last number. Both of these observations are extremely satisfactory and lead us to conclude that our study of the circuit for $t < 0$ was successful.

4.2 Results for the Initial Conditions of the System

Now we take a look at the results of our study of the inital conditions of the circuit.

Name	Currents [A]
Ix	2.8670509e-03
Iy	-2.8670509e-03
I1	9.2052783e-20
I2	3.0589720e-19
I3	1.4020977e-20
I4	-3.3639906e-20
I5	-2.8670509e-03
I7	-1.7220481e-19
Ib	3.0589720e-19
Id	-5.0898337e-20

Name	Voltages [V]
V0	-0.0000000e+00
V2	-9.4611569e-17
V3	5.4078486e-16
V5	-1.3829564e-16
V6	8.6836959e+00
V7	1.0331506e-16
V8	2.7630332e-16
Vb	4.3684073e-17
Vd	-4.1459897e-16

Name	Value [A or V]
@gb[i]	3.571179e-18
@r1[i]	-3.40748e-18
@r2[i]	3.571179e-18
@r3[i]	1.636985e-19
@r4[i]	7.278356e-19
@r5[i]	-2.86705e-03
@r6[i]	5.854099e-19
@r7[i]	5.854099e-19
v(2)	3.502198e-15
v(3)	1.092010e-14
v(5)	2.992175e-15
v(6)	8.683696e+00
v(7)	-1.18828e-15
v(8)	-1.77636e-15
v(9)	0.000000e+00

Table 10: Results for the Circuit Built for finding the Inital Conditions

Considering the extremely low numbers we obtained for most of the variables (e-14, e-15, ..., until e-20), these variables will be considered zero, as they are too small for the computer to actually make accurate calculations.

So, we will be only taking a look at the values for I_5 and V_6. Both of these are, once again, accurate until the last number displayed in the Simualtion results. This is, once again, an extremely satisfactory result that leaves us confident in saying these are the correct results for the Initial Conditions of the circuit.

4.3 Time- and Frequency-Dependent Analysis

Lastly, here are the graphs we obtained by analysing the system side by side, Figures 15, 16 and 17. It is clear that all of them are identical, which leads us to conclude, once more, that the study was succsseful.

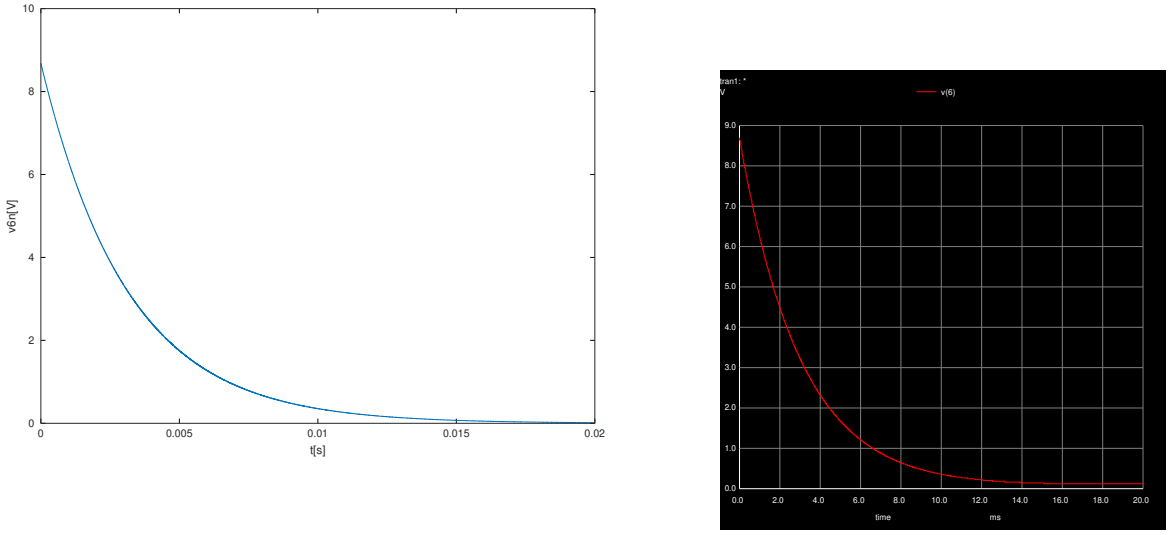

Figure 15: Results for f = 0Hz

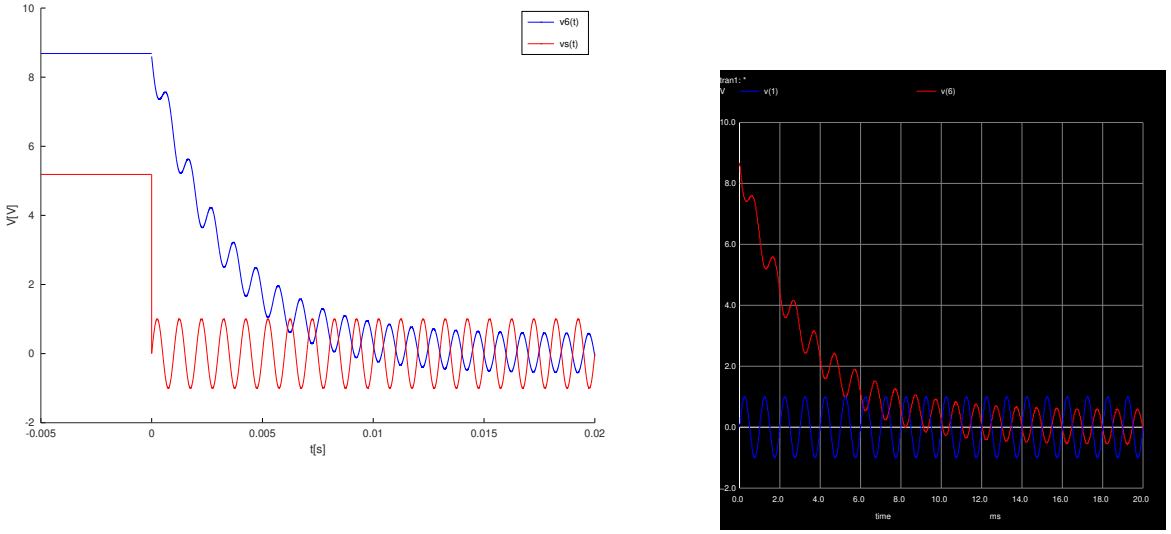

Figure 16: Results for f = 1kHz

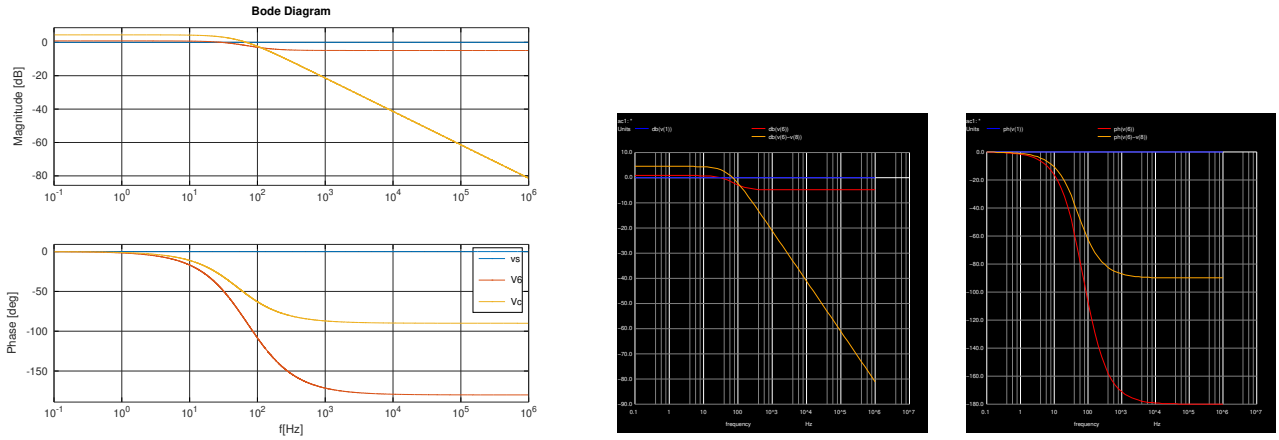

Figure 17: Results for the Frequency-Dependent Analysis

5 Conclusion

In this laboratory assignment the objective of analysing a circuit with several current and voltage sources (two linearly dependent and one independent) and a capacitor in parallel and in series with resistors has been achieved.

The current and voltage theoretical analysis (computed using *GNUOctave*) precisely resembles the circuit simulated by the *Ngspice*.

As seen in the previous section, it's possible to conclude that the simulations follows very closely the theorical model used in the analysis: the node analysis.

To conclude, we find that the study of the circuit we were present with was successful.

References

[1] Phyllis R. Nelson, *Introduction to SPICE Source Files* Slides

[2] *SPICE 'Quick' Reference Sheet*, Stanford University

[3] Holger Vogt *et al*, *Ngspice's User Manual*, Version 34

[4] *GNU Octave* Documentation Files

[5] José Teixeira de Sousa, *Circuit Theory and and Eletronic Fundamentals* Class Slides