

**Fig. 1: Conceptual diagram of the proposed full-duplex front-end.**



**Fig. 2: Detailed transceiver block diagram of the proposed full-duplex front-end.**



**Fig. 3: Detailed circuit diagram of RF/BB adaptive filter.**



**Fig. 4: Measured self-interference mitigation results with PA operates @25dBm.**



**Fig. 5: Chip measurement setup.**



**Fig. 6: Performance summary and comparison with other state-of-the-art designs.**



**Fig. 7: Chip micrograph.**



**Fig. S1: Detailed mathematical description of the proposed LO sideband cancellation.**



**Fig. S2: Detailed circuit diagram and measurement results for the power amplifier.**



**Fig. S3: Measurement results of the integer-N synthesizer.**