TABLE I

supply voltage	2.5 - 3.1 V
supply current	200 μA
temperature range	32°C to 44°C
accuracy	± 0.1°C, see text
error due to supply voltage changes	0.04°C [for the voltage range 2.5V-3.1V] 0.01°C [for the voltage range 2.6V-3.3V]
reference frequency	30 kHz
frequency ratio p	$12(R_4/R_2)(T - T_Z)/T_Z$

Analysis showed that the maximum error is within ±0.1°C, provided that perfect trimming is performed at a wafer temperature of about 38°C. The error is mainly caused by internal power dissipation, spreading in the base–emitter voltage and finite current gain of the n-p-n transistors.

The main measurement results are listed in Table I. The factor of 12 in the frequency ratio p represents the current-mirror transfer ratio of Q_{16} and Q_{17}.

The greatest sensitivity of the frequency ratio to drift in the supply voltage is found at its lowest value (2.5 V). The changes in I_T and I_{ref} partially compensate for each other. For changes in I_T and I_{ref} separately we measured changes of about 1 percent in the nominal voltage range.

As mentioned in Section II, with a single-point calibration the required accuracy can only be achieved when a process with low spreading in V_{BE} values is used. In other cases a two-point calibration is necessary unless the circuit is modified. A possible improvement is introduced in [4]: for both the currents I_T and I_{ref} the same base–emitter voltage is used. By trimming the emitter area both signals I_T and I_{ref} are adjusted to the right value. Because spreading in the PTAT voltage is much less than that in V_{BE}, no special precautions are required.

VI. Conclusions

The temperature information of the transducer described in this paper is converted into a frequency ratio. In this way the need for absolute accuracy of the signal transfer is eliminated and inaccurate passive on-chip components can be applied. The temperature transducer is a four-terminal device with complete on-chip microcomputer interfacing.

High accuracy and very high resolution is obtained by using fundamental properties of bipolar transistors. Calibration is simple and can be performed in a single step.

The transducer contains a low-voltage ultra-linear $I-f$ converter and two new accurate low-voltage current mirrors. With these circuits accurate signal transfer at a supply voltage of only 2.5 V is achieved.

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Fully Differential Operational Amplifiers with Accurate Output Balancing

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***Abstract*—Design considerations are presented for attaining accurate output balancing in fully differential operational amplifiers, over the useful operating frequency of the differential signals. Such output balancing is obtained by merging the common-mode feedback and the differential gain paths as close to the front end of the amplifier as possible, ensuring maximum sharing of circuit components. Two circuit designs implemented in a 5-V, 1.75-μm process are presented, one based on a two-stage topology and one based on a folded cascode topology. Experimental results for both designs are given.**

I. Introduction

A balanced-output operational amplifier is a special case of the well-known differential-output (or "fully differential") operational amplifier [1]. For a regular differential-output amplifier, having output terminal potentials V_{o1} and V_{o2}, the output quantity of interest is $V_{od} = V_{o1} - V_{o2}$. No precise design requirements are imposed with respect to the output common-mode component $V_{oc} = (1/2)(V_{o1} + V_{o2})$, although its value should not interfere with the proper operation of the circuit or of the load driven by it. The value of V_{oc} can even be signal dependent due to finite input common-mode rejection, circuit nonlinearities, and device mismatches. In contrast to this situation, the balanced-output operational amplifier has a V_{oc} that is precisely set to V_{bal}, a predetermined *signal-independent* value. Then, the two outputs are said to be balanced with respect to V_{bal}. If V_{bal} is chosen to

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be zero (as is often the case), then $V_{o1} = -V_{o2} = V_{od}/2$. Accurate output balancing is important for achieving maximum benefits from differential circuits in the presence of practical nonidealities. This is because such balancing ensures that the output will not contain common-mode components that could otherwise be present due to circuit nonlinearities or power supply noise. Thus, no problems will be created by these components in the case of a following stage with limited input common-mode rejection. Accurately balancing the outputs has the added advantage that the even-order nonlinearities of certain circuit elements are canceled. For example, such a cancellation can reduce distortion in switched-capacitor circuits and is the basic principal behind MOSFET-C continuous-time filters [2].

Differential-output amplifiers usually contain common-mode feedback circuitry [3]. However, the outputs of certain designs are not balanced. There are two potential causes for this. First, the circuit that detects the output common-mode signal V_{oc} may have a nonlinear characteristic, as, for example, in [1]. This problem can be avoided by using linear common-mode detectors such as a pair of two identical resistors, or the corresponding switched-capacitor equivalent for sampled-data circuits [4], [5]; transistor-only nonsampled circuits are also possible [6]. Second, the open-loop gain of the common-mode feedback may not be sufficiently large due to the topology used. For example, the fully differential circuit in [4] passes the differential-mode signal through two gain stages and the common-mode signal through only one, resulting in relatively small common-mode loop gain.

In this communication we discuss the design of differential amplifiers with output common-mode control that inherently have a dc gain and a gain–bandwidth product of the common-mode circuitry as large as the respective quantities for the differential-mode circuitry. We accomplish this by having the differential- and common-mode paths share as much circuitry as possible, thus treating the two respective signals as equally as possible. It will be seen that this approach does not impose any unusual circuit design constraints. The circuit examples to be presented have nonswitched common-mode signal detectors but the ideas discussed here are valid with switched capacitors as well. The operational amplifiers presented here are capable of driving resistive loads. Such amplifiers are needed to drive off-chip circuits, anti-aliasing and reconstruct filters, MOSFET-C filters, and other continuous-time circuits. The two-stage balanced operational amplifier in Section III was used in the output section of a production switched-capacitor filter where it was necessary to drive the resistive load of a balanced Rauch smoothing filter [7].

II. Design Considerations

In designing a balanced-output operational amplifier, the following considerations are particularly important.

a) The amplifier should inherently have as high a common-mode open-loop gain as possible (similar to the differential-mode gain).

b) The (high-gain) bandwidth of the common-mode loop has to be at least as large as the highest frequency at which output balancing is desired. In many applications this bandwidth should be the same as the differential-mode bandwidth of the amplifier.

c) In order to ensure common-mode stability, common-mode loop compensation is necessary in general. This requirement comes in addition to the usual amplifier compensation needs for the differential-mode feedback.

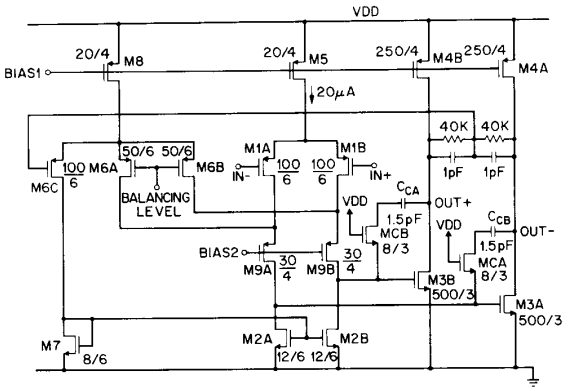

Fig. 1. Circuit diagram of the "two-stage" balanced operational amplifier fabricated in 1.75-μm CMOS technology.

d) If the common- and differential-mode signal paths are merged at the very front end of the amplifier and their small remaining separate parts are identical or equivalent, then objectives a)–c) above can be achieved automatically by the regular design of the differential-mode path [8]. In the examples to be discussed below it will be seen that this strategy imposes no fundamental restrictions on the design.

e) The common-mode signal detector that generates V_{oc} should have a linear characteristic.

f) There are practical situations when the outputs of the operational amplifier need to be balanced even if the differential-mode input stage turns off. Such turn-off can occur, for example, in some circuits containing latching states due to positive dc feedback [9]. These states, normally avoided by differential operation, can be induced by the presence (even momentary presence) of large common-mode signal components (e.g., during power turn-on transients). Therefore, it is desirable that the output balancing is independent of the differential-input stage; many operational amplifiers have no built-in provision for this and instead their output terminals "swing" to the power supply rails if the input differential stage turns off.

With the above considerations in mind, existing single-output operational-amplifier topologies can be used as the starting point to produce designs with accurate output balancing. Two possibilities are presented in the rest of this paper.

III. Two-Stage Design

The two-stage amplifier of Fig. 1 was designed to be a general-purpose circuit with maximum output swing, resistor driving capability, moderate bandwidth, relatively small power dissipation, and a single 5-V power supply operation. The output quiescent level (V_{bal}) is 2.5 V, with respect to which balancing of the two outputs is desired. P-type differential pairs were used with sources and substrates connected together for small V_{DD} noise coupling.

The differential-mode input stage consists of transistors *M1A*, *M1B*, *M2A*, *M2B*, *M9A*, *M9B*, and *M5*. The common-gate devices, *M9A* and *M9B*, increase the gain of the operational amplifier, as well as reduce the differential input capacitance. The two output stages are formed with transistors *M3A*, *M4A*, *M3B*, and *M4B*. Standard Miller compensation is achieved with *CCA*, *MCA*, *CCB*, and *MCB*. According to consideration d) in

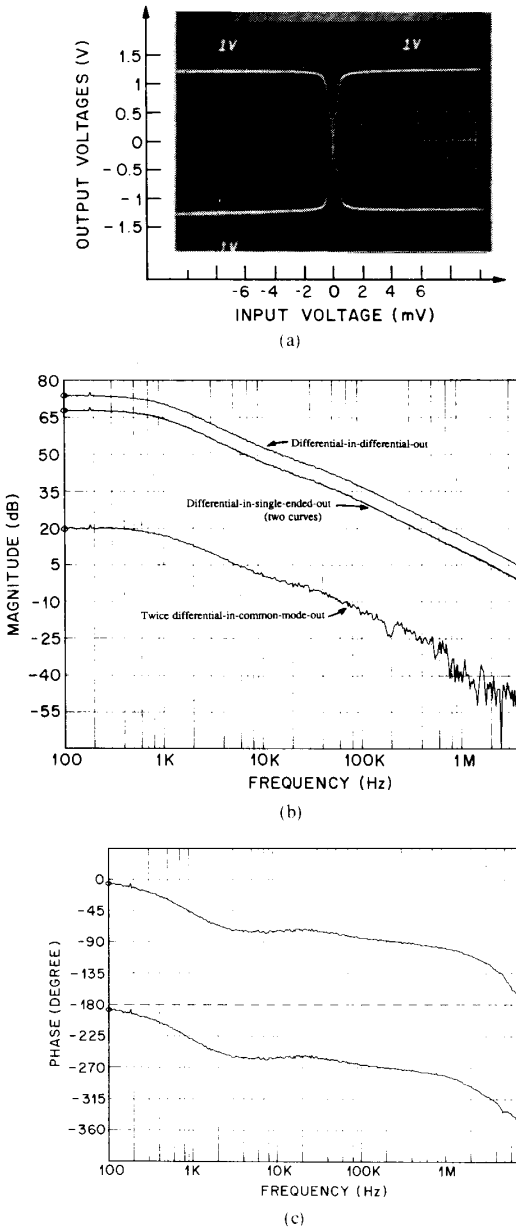

Fig. 2. (a) DC transfer characteristics for the "two-stage" design showing symmetry about the balancing level (output voltages with respect to V_{bal} = 2.5 V). (b) Magnitude parts of "two-stage" amplifier frequency responses. (c) Phase parts of differential-in/single-ended-out frequency responses for the "two-stage" design.

TABLE I
OPERATING CONDITIONS AND TYPICAL MEASURED PERFORMANCE OF THE EXPERIMENTAL BALANCED OPERATIONAL AMPLIFIERS

Parameter	"Two-stage" Design	Folded Cascode Design
Power supply	5 V (single)	5 V (single)
Power dissipation	3 mW	6 mW
Balancing level	2.5 V	3.5 V
Single-ended output range for specified balancing level	0.2 V - 4.8 V	2.5 V - 4.5 V
Maximum differential output signal for specified balancing level	9 Vp-p	4 Vp-p
Input common-mode range	0.6 V - 3.5 V	2.3 V - 4.5 V
Differential input offset	Mean=1.8 mV St.Dev.=1.2 mV	Mean=0.5 mV St.Dev.=0.9 mV
Output common-mode offset from balancing level	Mean=6.9 mV St.Dev.=1.9 mV	Mean=25 mV St.Dev.=3.5 mV
Differential DC gain	74 dB	66 dB
Differential unity-gain bandwidth	7 MHz	45 MHz
Differential slew rate	7 V/μs	100 V/μs
Open loop output resistance	33 KΩ	700 Ω
Input referred differential noise	96 nV/√Hz at 1KHz 25 nV/√Hz at 100KHz	49 nV/√Hz at 1KHz 28 nV/√Hz at 100KHz
CMRR	58 dB at 10 KHz 38 dB at 1 MHz	61 dB at 10 KHz 60 dB at 1 MHz
PSRR for VDD line	90 dB at 1 KHz 90 dB at 100 KHz 70 dB at 1 MHz	63 dB at 10 KHz 63 dB at 1 MHz 48 dB at 10 MHz
PSRR for ground line	58 dB at 1 KHz 50 dB at 100 KHz 35 dB at 1 MHz	48 dB at 10 KHz 48 dB at 1 MHz 30 dB at 10 MHz

the previous section, the common-mode feedback circuitry is merged with the differential-mode circuitry at the very front end of the amplifier. Namely, transistors $M6A$, $M6B$, $M6C$, $M7$, and $M8$ form the common-mode input stage which is equivalent to the differential-mode input stage. Transistors $M6A$ and $M6B$ have half the sizes of $M1A$ and $M1B$ but $M7$, $M2A$, and $M2B$ operate as a differential-to-single-ended converter for the common-mode input circuitry. Therefore, the equally amplified common-mode feedback signal and differential-mode input signal are combined as currents into the loads $M2A$ and $M2B$. From there on to the outputs the signals share the same circuitry including the compensation network.

The common-mode signal detector is formed with two 40-kΩ resistors in parallel with 1-pF capacitors. The purpose of the latter elements is to provide a high-frequency bypass of the distributed capacitance between the n-well resistors and the substrate to maintain stability of the common-mode feedback loop. The voltage coefficient of the n-well resistors was minimized by making them 20 μm wide.

The operational amplifier uses common-source output stages to achieve maximum output swing. In order to prevent the resistors in the common-mode signal detector from severely degrading the amplifier dc gain, the transconductances of $M3A$ and $M3B$ were designed to be relatively high. Source followers were avoided because they limit signal swing and degrade the noise performance of switched-capacitor filters. Recall that this amplifier is used in the output section of a switched-capacitor filter that must drive the resistive input of a continuous-time reconstruct filter.

It can be noticed that objective f) of the previous section is met. If the two differential inputs are biased at V_{DD}, $M1A$ and $M1B$ turn off; however, current from $M6A$ and $M6B$ continues to bias $M2A$ and $M2B$. Consequently, the gate-to-source voltages of $M3A$ and $M3B$ are kept at their nominal bias, ensuring

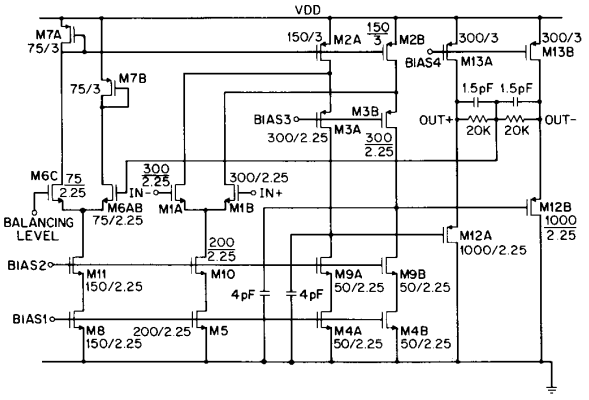

Fig. 3. Circuit diagram of the folded cascode balanced operational amplifier fabricated in 1.75-μm CMOS technology.

that V_{oc} is kept equal to $V_{bal} = 2.5$ V. If the drains of *M6A* and *M6B* were connected to ground, rather than to the cascode devices, the balanced operational amplifier would not meet objective f).

The amplifier was fabricated in a 1.75-μm CMOS technology [10]. The chip capacitors were implemented with double-polysilicon structures. Fig. 2 shows typical measured data. The dc transfer characteristics show symmetry about the balancing level. The common-mode feedback loop is effective even for the strongly nonlinear portions of the curves. The magnitude parts of the relevant measured frequency responses can be seen in Fig. 2(b): differential-in/differential-out, differential-in/single-ended-out (two responses almost totally overlapping), and twice differential-in/common-mode-out. The latter curve was generated by vectorially adding the single-ended measurements with the network analyzer. The ratio of the differential response to the common-mode response at dc is more than 60 dB. This illustrates the earlier point on the advantage of merging the two signals at the front end of the amplifier. The accurate phase balancing seen in Fig. 2(c) is evidenced by the fact that a 180° phase difference is maintained even at high frequencies. The phase margins that can be observed are degraded substantially by the loading of the test setup. Typical performance parameters are given in Table I. The relatively small number for the differential offset voltage shows that the common-mode signal injection technique used does not degrade drastically this parameter.

IV. Folded Cascode Design

The folded cascode amplifier of Fig. 3 was designed for a high-frequency MOSFET-C continuous-time filter application [11]. In this environment the required balancing level was 3.5 V, and n-type differential stages were used. The differential gain stage is realized with transistors *M1A*, *M1B*, *M10*, and *M5* with cascode loading provided by transistors *M2A*–*M4A*, *M2B*–*M4B*, and *M9A* and *M9B*. The amplifier outputs are buffered with two source-follower stages constructed with transistors *M12A*, *M12B*, *M13A*, and *M13B*. Transistors *M6AB*, *M6C*, *M8*, *M11*, *M7A*, and *M7B* implement the common-mode input stage. The common-mode error signal is injected via *M7A*. No direct current injection of the common-mode signal is used, as opposed to the "two-stage" design, a fact which is responsible for lower than possible common-mode loop gain. This alternative was chosen in order to obtain a differential offset voltage as small as possible. Based on the description of the two-stage amplifier, the reader can convince himself that if the input common-mode range is exceeded, accurate output balancing is still maintained. Similar to the previous design, the common-mode signal detector is realized with two 20-kΩ n-well resistors in parallel with two 1.5-pF capacitors. Frequency compensation of both the differential and common-mode feedback loops is achieved with the 4-pF capacitors connected from the drains of *M9A* and *M9B* to ground.

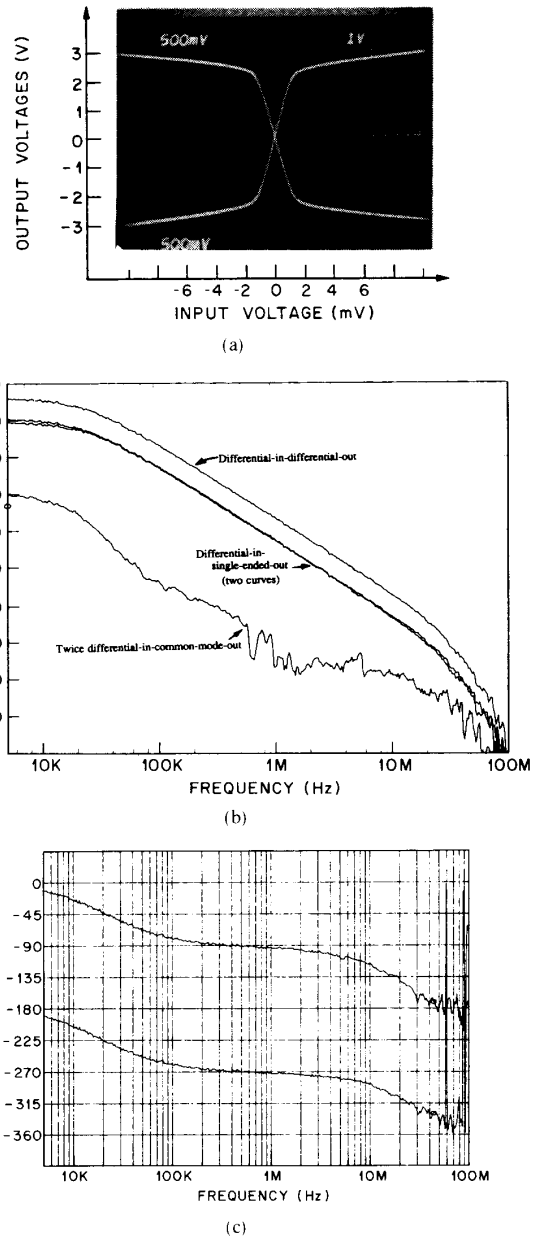

Fig. 4. (a) DC transfer characteristics for the folded cascode design showing symmetry about the balancing level (output voltages with respect to $V_{bal} = 3.5$ V). (b) Magnitude parts of folded cascode amplifier frequency responses. (c) Phase parts of differential-in/single-ended-out frequency responses for the folded cascode design.

The testing of this circuit required the use of active probes and "bias-tee" networks. In this way superpositions of dc and high-frequency ac signals were delivered to the circuits and the on-chip signals were measured reasonably uncorrupted by reflections. The experimental results are shown in Fig. 4 and Table I. The ratio of the differential response to the common-mode response at dc, as illustrated in Fig. 4(b), is only 32 dB. This considerably smaller number than in the "two-stage" case is mainly due to the lower common-mode-signal open-loop gain. However, the differential offset voltage is also smaller. The noisy appearance at high frequencies in the phase curves in Fig. 4(c) is due to measurement inaccuracies. The output swing is limited by the value of the balancing voltage V_{bal}, which for the application intended was 3.5 V.

V. Conclusions

Differential amplifiers with accurately balanced outputs can be easily realized if the differential-mode circuitry and the common-mode circuitry are treated equally in the design process. A convenient way of accomplishing this is to use a topology that combines the two parts as close as possible to the front end of the amplifier. In this way most of the design issues such as gain, compensation, etc. are addressed at the same time for both the differential- and common-mode signal paths. The design strategy discussed in this paper has been verified with two CMOS balanced amplifiers.

Acknowledgment

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A Rail-to-Rail CMOS Op Amp

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***Abstract*—A CMOS op amp is reported which has a rail-to-rail voltage range at its input as well as its output. A new area-efficient output stage has been used. While the entire op amp occupies only 600 mil^2, when used as a unity-gain buffer, and with ±5-V supplies, the op amp can drive a 9-V_{pp}/1-kHz sine wave across a 300-Ω load with −64 dB of harmonic distortion.**

I. Introduction

The first generation of CMOS op amps was limited to transconductance amplifiers. They had modest performance and were able to drive only capacitive loads. The second generation of these op amps, in addition to high-performance transconductance amplifiers, includes general-purpose op amps. These op amps can drive resistive as well as capacitive loads with a level of performance which is comparable to that of their bipolar counterparts [1]. For these op amps folded-cascode amplifiers are commonly used as the input stage. For the output stage, on the other hand, a variety of different circuits have been used [2]–[4]. In this paper a new output stage is presented which, although compared to the previous works uses smaller size output transistors, nevertheless has a very good current driving capability. It is described in Section II, while the overall op amp is covered in Section III. Finally, the measurement results obtained from an integrated test circuit are given in Section IV.

II. The Output Stage

The important criteria for designing an output stage are as follows:

1) low standby power dissipation which is controlled by a, preferably supply-independent, current source;
2) good current driving capability;
3) large small-signal transconductance in order to provide some voltage gain when driving heavy resistive loads and also to move the capacitive load-dependent pole to higher frequencies; and
4) simple circuit configuration so as to avoid additional parasitic poles.

Most of the output stages reported in the literature [2]–[4] have limited driving capability mainly because of the limited V_{GS} of the output devices. Consider now the new output stage which along with its biasing section and the block diagram representation of the input stage is shown in Fig. 1. Here, a differential-output, input stage is employed where an additional common-mode feedback (CMF) circuit sets the dc voltage values of the two differential outputs, i.e., $V_{o1} = V_{o2} = V_n = V_b$. Therefore, assuming that $(W/L)_1/(W/L)_3 = (W/L)_2/(W/L)_4$, the current I_o in the output devices becomes

$$I_o = \left[\frac{(W/L)_2}{(W/L)_5}\right] I_Q \tag{1}$$

which can be made supply independent.

For this circuit, assuming that the input stage does not impose any limit, when the output stage needs to draw its maximum

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