LOW-NOISE WIDE-BAND AMPLIFIERS IN BIPOLAR AND CMOS TECHNOLOGIES

THE KLUWER INTERNATIONAL SERIES IN ENGINEERING AND COMPUTER SCIENCE

VLSI, COMPUTER ARCHITECTURE AND DIGITAL SIGNAL PROCESSING

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by

Zhong Yuan Chang
Catholic University Leuven

Willy M. C. Sansen
Catholic University Leuven

SPRINGER SCIENCE+BUSINESS MEDIA, LLC

Library of Congress Cataloging-in-Publication Data

Chang, Zhong Yuan.
Low-noise wide-band amplifiers in bipolar and CMOS technologies / by Zhong Yuan Chang, Willy M.C. Sansen.
p. cm. — (The Kluwer international series in engineering and computer science ; SECS 117.)
Includes bibliographical references and index.
ISBN 978-1-4419-5124-3 ISBN 978-1-4757-2126-3 (eBook)
DOI 10.1007/978-1-4757-2126-3

1. Linear integrated circuits—Design and construction. 2. Broadband amplifiers. 3. Metal oxide semiconductors, Complementary. 4. Bipolar transistors. I. Sansen, Willy M. C. II. Title. III. Series.
TK7874.C425 1991
621.39'732—dc20 90-19259
CIP

Printed on acid-free paper.

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Preface

Analog circuit design has grown in importance because so many circuits cannot be realized with digital techniques. Examples are receiver front-ends, particle detector circuits, etc. Actually, all circuits which require high precision, high speed and low power consumption need analog solutions. High precision also needs low noise. Much has been written already on low noise design and optimization for low noise. Very little is available however if the source is not resistive but capacitive or inductive as is the case with antennas or semiconductor detectors. This book provides design techniques for these types of optimization.

This book is thus intended firstly for engineers on senior or graduate level who have already designed their first operational amplifiers and want to go further. It is especially for engineers who do not want just a circuit but the best circuit. Design techniques are given that lead to the best performance within a certain technology. Moreover, this is done for all important technologies such as bipolar, CMOS and BiCMOS.

Secondly, this book is intended for engineers who want to understand what they are doing. The design techniques are intended to provide insight. In this way, the design techniques can easily be extended to other circuits as well. Also, the design techniques form a first step towards design automation.

Thirdly, this book is intended for analog design engineers who want to become familiar with both bipolar and CMOS technologies and who want to learn more about which transistor to choose in BiCMOS.

Fourthly, this book is written for analog designers by analog designers. It is not theoretical nor empirical nor descriptive. It is about analog design with all its benefits for the ever developing creative mind of analog circuit designers.

Leuven, Belgium

Z.Y. Chang
W. Sansen

LOW-NOISE WIDE-BAND AMPLIFIERS IN BIPOLAR AND CMOS TECHNOLOGIES

1 INTRODUCTION

In low level integrated signal processing systems such as transducer systems, detector readout systems, radio receivers, etc, electrical noise is a fundamental limiting factor. For instance, the maximum sensitivity of AM/FM receivers or the best resolution of Silicon-detector readout systems is fully determined by the electrical noise. In the design of such systems, it is of crucial importance to optimize the noise performance of preamplifiers, as in a well designed system the noise performance of an entire system is always dominated by the preamplifier noise.

Much is known already about noise optimization of amplifier stages with resistive source. However, the signal source for such detection systems is in most cases of reactive type. This is a result of the necessary signal conversion from for example an electromagnetic field strength to a continues electrical voltage or current. This means that now the signal source at the preamplifier input cannot be represented by a resistance but by an inductance or a capacitance in series (parallel) with a voltage source (current source).

Since the noise performance of an amplifier depends on the source impedance, which varies with frequency, the best noise matching for a reactive source will vary as a function of frequency as well. Noise matching means that the total equivalent input noise is minimized for a given signal source impedance. The concept of equivalent input noise density or spectrum, which is the Fourier transform of the autocorrelation function of noise random process, is used rather than the noise figure. The reason is that the noise figure is only useful when the source impedance is of resistive type having a certain fixed and well determined value. It is completely meaningless however for reactive sources. Furthermore, the concept of equivalent input noise spectrum allows easy determiniation and optimization of the signal-noise ratio of the system.

In discrete realizations, noise matching has been obtained by such means as transformer coupling, input reactive tuning, paralleling several specially selected input

devices such as low-noise JFET transistors [1.1], [1.2]. All of these techniques are concerned with noise matching within a certain narrow frequency band. In many cases such as conventional radio receivers, noise matching must be realized in different frequency bands, corresponding to different transmitters to be received. Tuning of the noise matching condition by changing the transformer ratio or values of input variable capacitance is then unavoidable.

However, such noise tuning techniques do not lend themselves to monolithic realizations due to the high cost required. Together with the fact that for a reactive source the optimal noise matching will generally depend on frequency, this makes the design of monolithic low-noise wide-band amplifiers with a reactive source very cumbersome. In this text, detailed analyses are carried out to determine optimal noise matching conditions for wide-band amplifiers with reactive sources. Three different integrated technologies i.e. standard bipolar, CMOS and BiCMOS technologies are considered, for which theoretical lowest limits of noise levels achievable are determined.

The study of monolithic wide-band noise matching, or low-noise designs in general, has lead to the following design procedures. First, a choice has to be made of a feedback configuration that realizes the required signal transfer requirement and at the same time fulfils the noise specification. Secondly, the technology must be selected that is best suited for the given application. Thirdly, the design parameters for the input transistor must be optimized in order to realize the best noise matching. It is clear that in making the above choices and selections, detailed noise analyses have to be carried out. After the input transistor noise has been determined, the next step is to minimize all noise source contributions other than the ones from the input device. The general strategy for this is to minimize the noise sources at their origins and more importantly the transfer function associated with each noise source to the output. The former is mainly concerned with the design of transistor dimensions and choice of DC bias conditions, while the latter rely on thorough insights into the circuit response with respect to each noise source. Circuit techniques, such as emitter or source degeneration in current sources [1.3], [1.4], adding a dc bypass to the input stage [1.9], inserting an emitter follower in the places where current noise is dominant [1.5], etc, are essential for the minimization of the transfer function associated with each noise source.

Obviously, noise is not the only performance parameter to be optimized for wide-band amplifiers matching reactive sources. In addition, there are many other constraints to be met such as precise gain, bandwidth, distortion, stability, dynamic range, power dissipation, etc. It is evident that in order to fulfil all the requirements simultaneously,

an iterative procedure is required in which many decisions and compromises must be taken.

Since the noise performance of each circuits is determined by the basic IC components comprising the circuits, such as MOS, BJT transistors, resistors and capacitors, the noise characteristics of these components need to be studied first. In chapter 2, the noise behaviour of MOS and BJT transistors is examined both theoretically and experimentally. For each noise source, the physical origin and its associated network model are described. Emphasis is put on the discussion of the 1/f noise mechanism in MOS and BJT transistors which has not been fully known. The relationships of each noise source to the process and design parameters are determined which form foundations of low-noise design. For CMOS process, the noise associated with the poly-gate and distributed substrate resistance is analyzed. Techniques are given to limit these parasitic noise contributions. Measurement methods are developed to measure 1/f noise characteristics in MOS and BJT transistors. From the experimental results, the validity of 1/f noise theories can be verified and technological dependent parameters are determined [1.6].

In chapter 3, design techniques for low-noise wide-band amplifiers matching an inductive source are developed in three IC technologies. This allows the investigation and comparison of noise and other performance characteristics achievable. As the amplifiers are intended to be used as the preamplifier in an upconversion or synchronous detection AM radio receivers, specifications concerning noise, distortion and dynamic range are very stringent. The extremely severe noise requirement together with the required signal transfer function force the use of a combined capacitive and resistive feedback configuration [1.4]. However, capacitive feedback in combination with an inductive source can easily bring the amplifier into oscillation. In BJT realizations, four different core amplifier configurations have been designed and compared in terms of noise and stability. It is shown that from the point of view of noise performance, a voltage core amplifier is by far superior to all other configurations, while in terms of stability the use of transresistance or current core amplifiers results in an easier design. In CMOS realizations, general noise matching conditions are calculated taking both thermal and 1/f noise into account. An important conclusion from this analysis is that despite of much higher 1/f noise in a MOS transistor, better noise performance can be obtained in a CMOS process compared to a bipolar one [1.11]. The design is added of a large swing, high drive and low distortion CMOS output unity gain buffer stage. In BiCMOS, a new core amplifier structure is conceived that has advantages over both bipolar and CMOS

realizations in terms of noise, stability and chip area consumption. As the amplifier must provide a symmetrical output for driving a double balanced mixer, a single-ended to differential conversion is made at the output. Circuit techniques to reduce the noise and the offset of the differential output stage are presented.

In chapter 4, design techniques of low-noise wide-band amplifiers matching capacitive sources are presented. As the amplifier has already been designed in BJT technology elsewhere [1.7], only the design techniques in CMOS and BiCMOS processes are described. In both CMOS and BiCMOS realizations, general noise matching conditions are analytically determined for the case of using a MOS or a BJT input stage. It is shown that with a MOS input stage, the optimal noise matching can be realized independently of frequency, in spite of the fact that the signal source depends on frequency [1.8], [1.9]. This results in an important conclusion that a CMOS approach is capable of achieving a factor of two lower noise level than the BJT realization. In CMOS, a three-stage approach to the amplifier is adopted in order to achieve a minimal noise level and at the same time a rail-to-rail output swing. By this manner, a very high dynamic range of up to 130 dB is achieved. A novel compensation technique is introduced for this class of three-stage amplifiers. By taking advantage of the low input current noise characteristic of MOS transistors and high frequency capability of bipolar ones, better overall performance can be obtained using a simpler circuit in the BiCMOS approach [1.12]. In both CMOS and BiCMOS realizations, design criteria are analytically derived for the class-AB output stages to function linearly over the whole rail-to-rail output swing.

Similar design techniques can be applied as well to other applications. In chapter 5, design techniques of low-noise high-speed Si-detector readout electronics in CMOS process are presented. A comprehensive study is performed from which the theoretically best detector resolution is determined for readout systems consisting of a charge sensitive amplifier (CSA) and a Semi-Gaussian pulse shaper (S-G shaper) of arbitrary order [1.10]. For a given application, the results of this analysis enable circuit designers to determine the optimal design parameters for the CSA and the optimal order and peaking time for the S-G shaper in order to obtain the maximal system resolution. Transient analyses performed on CSAs and S-G shapers provide circuit designers with general design criteria. Based on the theoretical analyses, a complete analog readout system composed of a CSA, a fourth-order S-G shaper is designed and implemented in a standard 3-μm CMOS technology. In order to drive a Multi-Channel-Analyzer, a rail-to-

rail class-AB variable gain buffer is incorporated. Measurements on transient behaviour and detector resolution confirm the theoretical analyses.

As a conclusion, it can be stated that this text brings a wide variety of useful circuit configurations to optimize noise performance for reactive sources. Both inductive and capacitive sources are considered. Moreover, the optimization has been carried out in all important technologies such as bipolar, CMOS and BiCMOS. It has lead to design rules which provide insight into the optimization process. As a result, this text is a must for any designer who has to deal with preamplifiers for inductive and capacitive source impedances and optimum noise performance.

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2 NOISE IN INTEGRATED CIRCUITS: - MECHANISMS AND MODELS

2.1. INTRODUCTION

Noise in integrated circuits is one of the most important factors that determines the performance of low level integrated signal processing systems such as transducer, detector readout systems, AM/FM radio receivers, fiber optical receivers, etc. It represents a lower limit to the size of the electrical signal that can be handled by an integrated circuit without significant deterioration in signal quality. For example, the sensitivity of radio or fiber optical receivers are determined by the noise characteristics of front end circuits. Also, the resolutions of photo spectroscopy systems stand in direct relation with the noise of input charge sensitive amplifiers. Since the noise performance of any integrated systems is determined by the noise characteristic of the basic integrated components comprising the systems, such as MOS and BJT transistors, resistors, capacitors, etc, it is important to know the noise behaviour of each basic component in order to optimize the noise performance of the circuits.

In this chapter the noise behaviours of integrated MOS and BJT transistors are investigated in detail. For each noise source, physical origins and mechanism are discussed and the relationships to the process and design parameters are studied. These relationships form the foundation for low noise circuit design in practice.

In section 2.2 different noise sources in MOS transistors are described. Due to the fact that the 1/f noise in MOSFETs manifests itself over wide frequency ranges and due to the lack of satisfactory theories, emphasis is put on the discussion of the 1/f noise mechanism and its dependence on various process and geometrical parameters. In addition to the basic channel thermal noise and 1/f noise, noise caused by the resistive poly gate and distributed substrate resistance are described as well. Because for ultra low

noise applications, these two noise sources could turn out to be very important and even dominate the channel thermal and 1/f noise, if no special precautions were taken. Layout techniques are given to limit their contribution to the total noise in MOSFETs . The equivalent input noise generator model is derived and restrictions to its practical use are discussed.

In section 2.3 different kinds of noise sources in BJT transistors are studied. The origin of 1/f noise and its relationships to the process and transistor geometry are described. Just like for MOSFET transistors, the different noise sources in BJT transistors can be fully characterized by an equivalent input noise voltage and current generator. However, in contrast with MOSFET, the correlation between both noise generators for BJT transistor is very small in the normal frequency range of interest.

In section 2.4 measurement techniques of the noise in MOSFET and BJT transistors are presented. A measurement system is developed by which the total drain or collector noise current can be directly measured independent of the output conductance of transistor under test. A large number of 1/f noise measurements are carried out on MOSFET transistors with different geometries and under different bias conditions. This allows the determination the dependence of the 1/f noise on the various parameters such as dc biasings and transistor geometries. From the experimental results the validity of 1/f noise theories can be verified and the technological dependent parameters K_F and A_F can be estimated. Also, some noise measurements are also performed on some BJT transistors from an advanced BiCMOS process to investigate its noise performance and to compare actual characteristics with theoretical expected one.

2.2. NOISE SOURCES IN MOSFET TRANSISTORS

According to basic noise mechanisms, two important noise sources can be distinguished in a MOS transistor. The first one is the thermal noise associated with the conducting resistive channel, and the other is the so called flicker or 1/f noise. The mechanism of the channel thermal noise is quite well known since the sixties [2.2] - [2.4]. It is due to the random motion of free carriers within the inverse resistive channel, analogous to that in normal resistors. On the contrary, the mechanism involved in the 1/f noise has been argued over during several decades and still no general satisfactory theory exists which is able to predict the 1/f noise accurately. Therefore, some experimental studies are always necessary in order to characterize the 1/f noise in a specific integrated process.

In most of the cases, the inclusion of these two noise sources is sufficient to calculate and predict the noise performance of CMOS integrated circuits. However, for ultra low noise applications which are the main subject of this book, additional noise sources have to be taken into account. These additional noise sources include: the noise associated with the resistive poly-gate, the noise due to the distributed substrate resistance and shot noise associated with the leakage current of the drain source inverse diodes. Furthermore, for very high frequency applications where sub-micron channel transistors are required, excess channel thermal noise and substrate shot noise have been observed [2.5], [2.6]. The former is due to the channel hot carriers, while the latter is the result of the impact ionisation in the high field region near the drain side. However, as these two phenomena are not important for long channel devices they will not be discussed any further in the text.

2.2.1 Channel Thermal Noise Mechanism

The current flowing between the drain and the source terminals in a MOS transistor is based on the existence of a inverse resistive channel between them. The inverse resistive channel is formed by the minority carriers in the substrate under the appropriate control of the gate voltage. In analogy to a resistance, the random motion of the free carriers within the inverse channel generates thermal noise at the device terminals. In the extreme case where the drain-source voltage $V_{DS} = 0$ V, the inverse channel can be treated as a homogeneous resistance. According to the Nyquist theorem [2.1], the short circuit thermal noise current spectral density i_d^2 is then given by

$$i_d^2 = 4\,kT\,g_o \tag{2.1}$$

where k is the Boltzman constant, T is the absolute temperature and g_o is the channel conductance at zero drain-source voltage.

However, for analog applications MOS transistors are mostly operating in the saturation region in which the channel can not be considered as a homogeneous resistance. In this case, the short-circuit drain current noise (or open-circuit drain voltage noise) must be calculated by dividing the channel into a large number of small sections Δx (see Fig.2.1). For each section Δx, calculate the output current noise due to the noise e.m.f (electromotive force) generated in the section Δx and finally integrate along the whole channel to obtain the total drain current noise. Following this procedure, using

the elementary MOS theory and Nyquist theorem, it can be easily calculated that the short circuit drain current noise spectral density is [2.3], [2.4]

$$i_d^2 = 4\,kT\,\frac{\mu^2 W^2}{L^2 I_{DS}}\int_0^{V_{DS}} Q_n^2(V)\,dV \tag{2.2}$$

In (2.2) W and L are the channel width and channel length, respectively, μ is the effective channel mobility, I_{DS} is the drain-source current and $Q_n(x) = C_{ox}(V_{GS} - V_T(x) - V(x))$ is the inversion channel charge per unit area where C_{ox} is the gate oxide capacitance per unit area and $V_T(x)$ is the threshold voltage at position x. In general $V_T(x)$ depends on the position x or on the channel potential $V(x)$ through the depletion charge $Q_d(x)$ [2.7]. If the dependence of the threshold voltage V_T on the channel potential $V(x)$ is neglected (first order approximation), the above integral can be readily carried out as given by:

$$i_d^2 = 4\,kT\,\mu C_{ox}\frac{W}{L}\,\frac{2}{3}\left[\frac{3(V_{GS}-V_T)V_{DS} - 3(V_{GS}-V_T)^2 - V_{DS}^2}{2(V_{GS}-V_T) - V_{DS}}\right] \tag{2.3}$$

For $V_{DS} << V_{GS} - V_T$, corresponding to the MOSFET operating in the linear region, the expression (2.3) is exactly the same as (2.1). When the MOSFET is operating at the saturation point where $V_{DS} = V_{GS} - V_T$, the above expression is simplified to the widely used expression for the channel thermal noise

$$i_d^2 = 4\,kT\,\frac{2}{3}\mu C_{ox}\frac{W}{L}(V_{GS}-V_T) = 4\,kT\,\frac{2}{3}g_m \tag{2.4}$$

where g_m is the transconductance of the MOSFET. Strictly speaking, equation (2.4) does not hold beyond the saturation point or for $V_{DS} > V_{GS} - V_T$, but it is found experimentally that equation (2.4) remains valid within good approximation in the saturation region as long as the device shows good saturation in *I-V* characteristic [2.2] - [2.4]. This is easily understood because for a device showing good saturation in *I-V* characteristic the cut off region near the drain is much smaller than the resistive inverse channel which is responsible for noise generation.

The above expression (2.4) does predict the channel thermal noise behaviour of MOSFETs with negligible substrate effect. However, many experimental results shown higher thermal noise than expression (2.4) predicts [2.8] - [2.10]. This discrepancy

between the simple theory and experiments can be accounted for by taking into account the dependency of V_T on the channel potential $V(x)$. In this case, the calculation of the integral in (2.2) is rather involved and the result can be written in a short form as:

$$i_d^2 = 4\,kT\,\gamma\,g_m \tag{2.5}$$

where γ is a very complex function of the basic transistor parameters and bias conditions [2.4], [2.8].

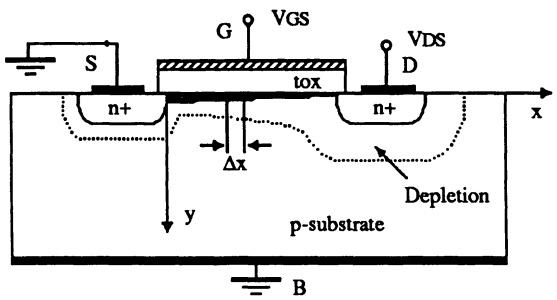

Fig.2.1. Cross section of nMOS transistor.

In general, a numerical approach is required to interpret the dependences of γ and so the expression (2.5). However, because the dependence of V_T on the channel potential $V(x)$ comes from the substrate effect (the dependence of the depletion charge variation), it can be expected that this effect is less pronounced for MOSFETs with lower substrate doping N_B and thinner oxide thickness t_{ox}, corresponding with a lower K_2 ($K_2 = \sqrt{2\,\varepsilon_{si}\,qN_B\,/\,C_{ox}}$) factor [2.7]. Indeed, it can be shown that for K_2 approaching zero, the value of γ approaches 2/3 and therefore equation (2.5) reduces to (2.4). From previous experimental results, it is concluded that for MOSFETs with $t_{ox} < 100$ nm and $N_B < 10^{16}$ cm^{-3} the factor $\gamma \leq 1$ [2.4], [2.8] - [2.10]. Therefore, for modern CMOS processes where t_{ox} is of the order of 50 nm and N_B of about 10^{15} -10^{16} cm^{-3} the factor γ is situated between $0.67 < \gamma < 1$.

The random motion of the free carriers in the inverse channel generates not only the output drain current noise, but also input gate current noise via the gate-channel capacitance $C_{ox}WL$. Indeed, the thermal noise e.m.f generated in each section Δx gives

rise to a channel voltage fluctuation $\Delta V(x)$ that causes a fluctuation in the charges stored on the gate channel capacitance. The fluctuation in charges per unit time results in the gate current fluctuation. As the noise arises from a capacitive coupling effect, it may be anticipated that this noise is proportional to the f^2. Detailed calculations shown that the gate current noise is approximately given by [2.11], [2.12]:

$$i_g^2 \approx 4\,kT\frac{1}{5\,g_m}\left(2\,\pi f\right)^2 C_{GS}^2 \approx 4\,kT\frac{g_m}{5}\left(\frac{f}{f_T}\right)^2 \tag{2.6}$$

where C_{GS} is the gate-source capacitance and $f_T \approx g_m/2\pi C_{GS}$ is the cut off frequency of the MOSFET. Comparing with the drain current noise, the effect of the gate current noise is only important for frequency $f > f_T$. Therefore, in most practical cases this noise term may be neglected.

2.2.2. 1/f Noise in MOS Transistors

Since the first observation of the 1/f noise in vacuum tubes in 1925 [2.13], the 1/f noise phenomenon has been observed in almost all kinds of devices, from homogeneous metal films and different kinds of resistors to semiconductor devices and even chemical concentration cells, etc. This ubiquity of 1/f noise had lead people to think that there must exist a fundamental physical mechanism behind all observed 1/f noise. Unfortunately, in spite of continuous pursuit, no such a mechanism has been found by far. A large experimental evidences shown that there could be several possible mechanisms involved in the generation of 1/f noise.

Among all active integrated devices, MOS transistors show the highest 1/f noise of all due to their surface conduction mechanism. This fact together with the lack of satisfactory theory results in an enormous number of papers in the literature on the discussion of 1/f noise in MOSFETs both theoretically and experimentally. Several competing theories and physical models have been proposed to explain 1/f noise phenomenon in MOSFETs. Although these theories and models are based on physical mechanisms which are different in detail, they all can be considered as modified versions of the two basic 1/f noise theories: the mobility fluctuation model expressed by the Hooge empirical relation [2.14], [2.15] and carrier density or number fluctuation model first introduced by McWhorter [2.16].

Mobility Fluctuation Model. In view of the mobility fluctuation model, the 1/f noise which is further referred to as Δμ-1/f noise is assumed to be attributed to the fluctuation in mobilities of free carriers when they collide with the crystal lattices. The detailed mechanism responsible for this fluctuation has not been known yet. This model is described by the Hooge empirical equation [2.14]

$$\frac{i_f^2}{I^2} = \frac{\alpha_l}{Nf} \tag{2.7}$$

where α_l is so called Hooge 1/f noise parameter, N is the total number of the free carriers in the device and I is the short circuit current through the device. Experiments on different homogeneous metals and semiconductor (Si, GaAs) samples have proved the correctness of (2.7) and have shown that $\alpha_l \approx 2\ 10^{-3}$ for all investigated samples. The near constancy of α_l indicates that Δμ-1/f noise could be a fundamental phenomenon to all materials. Indeed, the Hooge equation (2.7) can be theoretically derived by assuming that the 1/f noise is caused by N independent free carriers, each of which generates 1/f noise due to the mobility fluctuation $\Delta\mu$ [2.17].

Experimentally, it was found that only phonon scattering gives rise to 1/f noise [2.18]. Hence, for one particular device where more than one scattering mechanism exist, for instance, impurity scattering, surface scattering, etc, in MOSFETs, the Hooge 1/f noise parameter α_l should be reduced to

$$\alpha = \alpha_l \left(\frac{\mu_{eff}}{\mu_l} \right)^2 \tag{2.8}$$

where μ_l is the mobility when only lattice scattering present and μ_{eff} is the effective mobility of the device which according to Matthiessen's theorem is given by [2.19]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_l} + \sum_i^n \frac{1}{\mu_i} \tag{2.9}$$

where n denotes the total number of different scattering processes.

It should be noted that the Hooge equation (2.7) is only valid for homogeneous devices. For non homogeneous devices, the differential form of the Hooge equation must be used. For a MOS transistor operating in the linear region with $V_{DS} << V_{SAT} =$

V_{GS} - V_T, the inverse channel may be approximately treated as a homogeneous resistance. In this extreme case, one can apply the Hooge empirical relation to the MOSFET inverse channel to study its 1/f noise in the linear region.

Under strong inversion condition, the total number N of the free charge in the inversion channel is given by:

$$qN = C_{ox} W L \left(V_{GS} - V_T \right) \tag{2.10}$$

For a very small drain source voltage V_{DS} the drain source current I_{DS} through the transistor is given by:

$$I_{DS} = \frac{q \mu_{eff} N}{L^2} V_{DS} \tag{2.11}$$

Fill (2.10) and (2.11) in the Hooge equation (2.7), yields the short circuit drain noise current spectrum as given by:

$$\overline{i_f^2} = \alpha_l \left(\frac{\mu_{eff}}{\mu_l} \right)^2 \frac{q \mu_{eff} I_{DS} V_{DS}}{L^2 f} \tag{2.12}$$

Even for this simplest case, experimental results shown a deviation of an order of 10^3 - 10^4 from the expression (2.12) predicted. This implies that the Hooge equation (2.7) is not valid for the MOS inversion channel. Other mechanisms could be thus at work. In order to explain this large deviation, Vandamme [2.20] has made a more sophisticated calculation in which the profile of the carrier density $n(y)$ and mobility $\mu(y)$, consequently $\alpha(y)$, of the inversion layer perpendicular to Si-SiO2 interface were taken into consideration. In spite of his complex calculations, the final result can be formally regarded as the same as (2.12) where μ_{eff} $(\mu_{eff}/\mu_l)^2$ must be replaced by the so called effective 1/f noise mobility μ_f which depends strongly on the bias conditions and some new fit parameters. By assuming appropriate values of the fit parameters he succeed in explaining his experimental result.

From circuit designers point of view, it is more important to know the 1/f noise behaviour of MOS transistor in the saturation region. When the drain source voltage V_{DS} is larger than the saturation voltage, the channel of a MOSFET can not be treated as a homogeneous layer, even in the x-direction. In this case, the channel must be divided into a number of small section Δx, and for each section Δx the Hooge empirical relation

can be applied. Integrating over the whole channel the total 1/f noise power spectrum at saturation is obtained as given by [2.21]

$$i_f^2 = \alpha_l \frac{q \mu_f (V_{GS} - V_T) I_{DS}}{L^2 f} \tag{2.13}$$

Since the transconductance of a MOS transistor in saturation is related to I_{DS} by

$$g_m = \sqrt{2 \mu_{eff} C_{ox} \frac{W}{L} I_{DS}} \tag{2.14}$$

the equivalent input 1/f noise voltage spectrum density is then

$$v_f^2 = \alpha_l \frac{q \mu_f (V_{GS} - V_T)}{2 \mu_{eff} C_{ox} W L f} \tag{2.15}$$

The above equation says that the equivalent input 1/f noise is proportional to V_{GS} - V_T and inversely proportional to the gate oxide capacitance per unit area C_{ox} and the gate area WL provided that μ_{eff} and μ_f do not change with V_{GS} - V_T. These proportionalities have been observed in some experiments [2.21], [2.22]. However, the overwhelming majority of experimental results on 1/f noise shown quite different dc bias and gate oxide dependences from what expression (2.15) predicted. This majority of experimental results can be successfully accounted for using the number fluctuation model proposed by McWhorter [2.16].

Number Fluctuation Model. In the number fluctuation model, the 1/f noise which is further referred to as Δn-1/f noise, is believed to be caused by the random trapping and detrapping of the mobile carriers in the traps located at Si-SiO_2 interface and within the gate oxide. Each trapping and detrapping event results in a random telegraph signal (RTS) corresponding to a Lorentzian spectrum or generation-recombination spectrum. The superposition of a large number of such Lorentzians with a proper time constant distribution results in the 1/f noise spectrum. According to this model, the Δn-1/f noise should be proportional with the effective trap density near the quasi-Fermi level of the inverse carriers. This has been indeed verified by a large number of experiments.

Recently, more insight into the mechanism of the 1/f noise in MOSFETs has been gained through the study of 1/f noise properties of sub-micro channel transistors. By reducing the gate area to sub-micro range, random telegraph signals (RTS) caused by

individual trapping and detrapping event become visible [2.23], [2.24]. An other key success of the number fluctuation model is achieved through the study of 1/f noise in the weak inversion regime. It is observed that the relative drain 1/f noise current $\overline{i_f^2}/I^2$ shows a plateau in the wake inversion region. This observed plateau can only be successfully explained by the number fluctuation model [2.25]. As the number fluctuation model plays an very important role in studying the 1/f noise characteristics in MOSFET, JFET and BJT transistors, a short explanation of this model is given below.

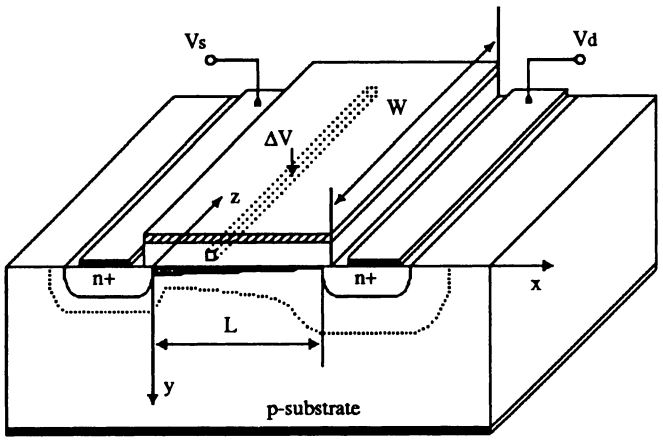

Fig.2.2. Geometrical structure of a nMOS transistor.

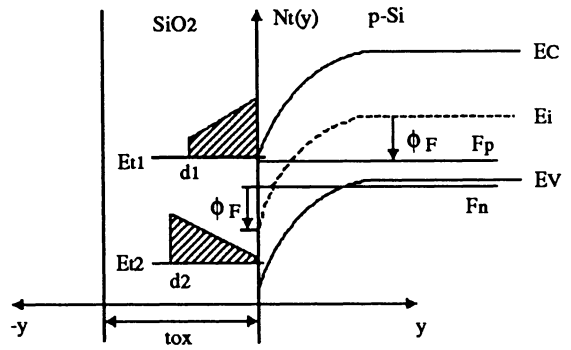

Fig.2.3. Band diagram of a nMOS transistor at strong inversion.

It is well known that in a MOS transistor, additional energy states exist at the Si-SiO_2 interface (interface states) and in the gate oxide (oxide traps). These interface states and oxide traps communicate randomly with the MOS channel free charges obeying Schokley Read Hall (SRH) statistics [2.26]. Using SRH statistics the spectrum of the mean square fluctuation δn_t in the number of the trapped carries in an elemental volume ΔV (= $Wdxdy$) at position (x,y) is given by [2.27] - [2.29] (see Fig.2.2)

$$\delta n_t^2 = \frac{4\tau}{1+\omega^2\tau^2} N_t f_t f_{pt} \Delta V \tag{2.16}$$

where τ = trapping time constant [s]

N_t = trap density [cm^{-3}]

$f_t = \frac{1}{1+e^{(E_t-F_t)/kT}}$ = fraction of filled traps under steady state condition

E_t = trap energy level [eV]

F_t = trap quasi-Fermi level [eV]

The fluctuation δn_t causes fluctuations in the channel free carriers δN which in turn causes fluctuations in the channel current δI_{DS}. Under strong inversion condition, it is shown that $\delta N = \delta n_t$. According to the elementary MOSFET theory the total inverse free carriers N is given by

$$qN = \int_0^L qn(x)\,dx = \int_0^L WC_{ox}\left(V_{GS} - V_T - V(x)\right)dx \tag{2.17}$$

and the drain source current is given by

$$I_{DS} = q\,n(x)\,\mu\frac{dV(x)}{dx} \tag{2.18}$$

where $n(x)$ is the number of free carriers per unit length. From (2.17) and (2.18) the spectrum of the fluctuation of the drain current due to the fluctuation in the trapped carriers in an elementary volume ΔV is

$$\delta i_d^2(f) = \left(\frac{I_{DS}}{L\,n(x)}\right)^2 \delta N^2 = \frac{\mu q^2 I_{DS}}{L^2 W C_{ox}\left(V_{SAT} - V(x)\right)} \frac{dV(x)}{dx} \delta n_t^2 \tag{2.19}$$

In order to calculate the total 1/f noise due to the fluctuations of all traps which are distributed in the space and in the energy band gap, the above expression must be integrated along the channel, over the energy band and into the oxide. The general expression for the drain 1/f current noise spectrum is thus given by

$$i_d^2(f) = \int_0^{VDS} \int_{EV}^{EC} \int_0^{d} \frac{\mu q^2 I_{DS}}{L^2 C_{ox}\left(V_{SAT}-V(x)\right)} \frac{4\,\tau(y,E,V)}{1+\omega^2\tau^2(y,E,V)} N_t(E,y) f_t(E,V) f_{pt}(E,V)\, dy\, dE\, dV \tag{2.20}$$

where E_v and E_c represent the levels of the valence and conduction band, respectively, and d is the depth into which oxide traps are distributed in the oxide. To evaluate this integral the distribution of $N_t(E,y)$, $\tau(y,E,V)$ and function $f_t(E,V)$ must be explicitly determined first.

Consider now a single trap level E_t with a uniform distribution into the oxide so that $N_t(E_t,y) = N_t(E_t)$. The distribution of the trapping time constant $\tau(y,E,V)$ is derived based on the SRH statistics and the tunneling model as proposed by McWhorter.

$$\tau(y) = \tau_o e^{\alpha y} \quad \text{with} \quad \tau_o = \frac{1}{c\left(n_s + n_1\right)} \tag{2.21}$$

where α (= 10^8 cm^{-1}) is the McWhorter tunneling constant, $n_s = n_i e^{(F_n - E_i)/kT}$ is the surface carrier concentration, and $n_1 = n_i e^{(F_t - E_i)/kT}$ and c is the electron capture coefficient (= 10^{-8} cm^3/s). For a practical case where τ_0 = 10^{-10} s and the traps are distributed into the oxide d = 50 Å, the maximal trapping time constant τ_{max} = 5 10^{11} s. It is this wide range of trapping time constant that is responsible for the wide range of the observed 1/f noise. Fill (2.21) in (2.20) the integral into the oxide can be worked out as given by

$$\int_0^{d} \frac{4\,\tau(y,E,V)}{1+\omega^2\tau^2(y,E,V)} N_t(E_t)\, dy = N_t(E_t) \frac{1}{\alpha\,\omega}\left[\arctan \omega\tau_{max} - \arctan \omega\tau_o\right]$$

$$= N_t(E_t) \frac{1}{4\alpha f} \quad \text{for} \quad \frac{1}{2\pi\tau_{max}} < f < \frac{1}{2\pi\tau_o} \tag{2.22}$$

Thus, in the case of constant space trap distribution a pure 1/f noise spectrum is obtained in the frequency range where $1/2\pi\tau_{max} < f < 1/2\pi\tau_0$ or $10^{-13} < f < 10^9$ Hz for the case mentioned above. It is important to realize that the above Δn-1/f noise theory leads to a frequency range $10^{-13} < f < 10^9$ Hz which is sufficient wide to cover all observed 1/f noise in practice. For more general cases where the traps are not uniformly distributed in the oxide, the low frequency noise shows an $1/f^{\alpha}$ spectrum with $\alpha <> 1$. This is easily understood. For example, if the trap distribution is higher in the oxide than at the surface as is the case for E_{t2} shown in Fig.2.3, more traps with large trapping time τ will be active in generating noise. As a result, the lower frequency noise will increase more rapidly than 1/f predicted. Similar qualitative arguments can be given for other case of trap distributions.

For the integral over the trap distribution in the band gap, the exact trap distribution of $N_t(E)$ is of minor important. This is because that only the traps around the electron quasi-Fermi level F_n is effective in the noise generation and the function $f_t f_{pt}$ behaves like a δ-function around F_n. Therefore, a good approximation of the integral over the energy band is given by [2.28]

$$\int_{E_V}^{E_C} N_t(E) f_t(E,V) f_{pt}(E,V)\, dE = 4kTN_t(F_n) f_t(F_n) f_{pt}(F_n) \tag{2.23}$$

where 4 kT represents a small energy band around the electron quasi-Fermi level F_n.

After carrying out the integrations into the oxide and over the energy band, the general Δn-1/f noise expression (2.20) is reduced to:

$$i_d^2(f) = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{kT}{\alpha f} \int_0^{VDS} \frac{1}{\left(V_{SAT}\text{-}V(x)\right)} N_t(F_n) f_t(F_n) f_{pt}(F_n)\, dV \tag{2.24}$$

As the electron quasi-Fermi level F_n varies along the channel, the function $f_t f_{pt}$ in (2.24) varies as well. The general expression of $f_t f_{pt}$ is derived using SRH statistic which for the case of MOS inversion layer is reduced to [2.28], [2.29]

$$f_t(F_n) f_{pt}(F_n) = \frac{n_s^4}{\left(2n_s^2 + n_i^2\right)^2} \tag{2.25}$$

where $n_s(x)$ is the surface density of the inversion electrons in the channel which according to the elementary MOS theory is related to the channel potential as

$$n_s = n_{s0}\frac{V_{SAT} - V(x)}{V_{SAT}} \tag{2.26}$$

where n_{s0} is n_s value at source side of the inversion channel. With (2.25) and (2.26), the integral in (2.24) can be carried out, provided that $N_t(F_n)$ is known. For the simplest case where $N_t(F_n)$ is uniformly distributed in the energy band or at least around F_n the integral is given by

$$i_d^2(f) = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{kTN_t}{\alpha f} \frac{1}{8} ln\left[\frac{2}{2\left(\frac{V_{SAT} - V_{DS}}{V_{SAT}}\right)^2 + \left(\frac{n_i}{n_{so}}\right)^2}\right] \tag{2.27}$$

This is a closed form solution for the Δn-1/f noise spectrum of the drain-source current fluctuation under the assumption that the traps are uniformly distributed within the space and energy band or at least around the electron quasi-Fermi level F_n. It is valid for MOS transistors operating from the linear region till the saturation point $V_{DS} = V_{SAT} = V_{GS} - V_T$. As in the case of the channel thermal noise, in the saturation region $V_{DS} > V_{SAT}$, the noise saturates as well, for devices showing a good I-V saturation characteristic. From (2.27) it can be seen that when $V_{DS} << V_{SAT}$, the second term in the denominator in the *ln*-function can be neglected so that the drain current noise increases with the increase in drain source voltage. In the saturation region where $V_{DS} > V_{SAT}$, equation (2.27) is reduced to

$$i_d^2(f) = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{kTN_t}{\alpha f} \frac{1}{16} ln\left[\frac{\sqrt{2}\, n_{so}}{n_i}\right] = \frac{K_F I_{DS}}{C_{ox} L^2 f} \tag{2.28}$$

where K_F is a constant if $N_t(F_n)$ and n_{so} do not change much with the bias condition. Combining (2.28) and (2.14) the equivalent input 1/f noise can be easily calculated as given by

$$v_f^2(f) = \frac{K_F}{2\mu C_{ox}^2 W L f} = \frac{K_f}{C_{ox}^2 W L f} \tag{2.29}$$

where $K_f = K_F/2\,\mu$. The above expression are widely used in low noise CMOS amplifier design [2.48], [2.49]. Comparing (2.29) with the expression (2.15) derived for Δμ-1/f noise, two important differences can be distinguished between the two 1/f noise models. First, according to (2.29), the input referred 1/f noise voltage is independent of any dc bias conditions, while in terms of mobility fluctuation model, it is directly proportional to the effective gate voltage V_{GS} - V_T. Secondly, equation (2.29) shows that the input referred 1/f noise is inversely proportional to C_{ox}^2, while according to (2.15) it is proportional to C_{ox}. It must be noted that the two discrepancies are not sufficient means to prejudge the correctness of the two models. There are other parameters such as effective mobility μ that may affect the noise dependence on the dc bias conditions and oxide thickness.

On the other hand, the fact that many experiments show strongly dependence of 1/f noise on the surface state density and can be easily fitted to (2.29) means that the dominant mechanism of 1/f noise in MOSFET is due to the carrier density fluctuations. This certainly does not mean that the Δμ-1/f noise does not exist in MOSFETs. As the Δμ-1/f noise could be of fundamental origin, it is reasonable to assume that it also exists in a MOSFET. However, since in normal cases Δn-1/f noise is much higher than Δμ-1/f noise, it is always marked by the Δn-1/f noise so that its effect can not be observed in practice.

For a given CMOS process where the trap distribution is presumedly given, the geometrical and dc bias dependences of 1/f noise as given by (2.28) and (2.29) can be experimentally verified. To that end a large number of experiments have been performed on MOSFET transistors with different geometries and under different bias conditions. The measurement results which will be discussed in the section 3.3 show that expressions (2.28) and (2.29) properly describe the 1/f noise behaviour of the CMOS process which means that the Δn-1/f noise is the dominant mechanism.

2.2.3. Additional Noise Sources

Up to now, the two most important noise sources in MOSFETs are discussed. For most practical cases, the use of these two noise sources is sufficient to predict the noise performance of CMOS circuits. However, for ultra low noise application, these two noise sources must be made extremely low, by using for instance large MOSFETs and high dc bias levels. As a result, other noise sources could turn out to become important.