Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits

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***Abstract*—Thermal noise represents a major limitation on the performance of most electronic circuits. It is particularly important in switched circuits, such as the switched-capacitor (SC) filters widely used in mixed-mode CMOS integrated circuits. In these circuits, switching introduces a boost in the power spectral density of the thermal noise due to aliasing. Unfortunately, even though the theory of noise in SC circuits is discussed in the literature, it is very intricate. The numerical calculation of noise in switched circuits is very tedious, and requires highly sophisticated and not widely available software. The purpose of this paper is twofold. It provides a tutorial description of the physical phenomena taking place in an SC circuit while it processes noise (Sections II–III). It also proposes some specialized but highly efficient algorithms for estimating the resulting sampled noise in SC circuits, which need only simple calculations (Sections IV–VI). A practical design procedure, which follows directly from the estimate, is also described. The accuracy of the proposed estimation algorithms is verified by simulation using SpectreRF. As an example, it is applied to the estimation of the total thermal noise in a second-order low-distortion delta-sigma converter.**

***Index Terms*—Delta-sigma ($\Delta\Sigma$) modulator, switched-capacitor (SC) circuit, thermal noise.**

I. Introduction

ONE of the main limitations of the performance of switched-capacitor (SC) circuits is noise. The sources of noise include the *intrinsic* noise generated in the MOS transistors, as well as the *extrinsic* (interference) noise originating, typically, from the on-chip digital circuitry, and coupled into the sensitive analog stages via the substrate and supply or ground lines.

There are two important intrinsic noise effects in MOS transistors: thermal and flicker noise[1]. Thermal noise is caused by the thermal motion of the charge carriers in the channel of the device. This causes a small amount of random fluctuation in the drain current. If the transistor operates in its triode region, as it does for a conducting switch, the noise can be represented by a voltage source in series with the device. The power spectral density (PSD) of its voltage is white; its estimated value is given by

$$S_{\rm vt}(f) = 4kTR_{\rm on}({\rm V}^2/{\rm Hz}). \tag{1}$$

Here, k is the Boltzmann constant, $k = 1.38 \times 10^{-23}$ J/K, T is the absolute temperature of the device in degrees Kelvin, and $R_{\rm on}$ is its on-resistance in ohms. The mean value of the thermal noise is zero.

Note that here, and in the rest of this paper, all PSDs are regarded as one-sided distributions, so the noise power between f_1 and f_2 is obtained simply by integrating $S(f)$ between f_1 and f_2.

For a MOSFET operating in strong inversion and in its active region, the thermal noise can be modeled by a current source in parallel with the channel. The PSD of the noise current is to a good approximation given by

$$S_{\rm it}(f) = \frac{8}{3}kTg_m({\rm A}^2/{\rm Hz}) \tag{2}$$

where g_m is the transconductance of the device.

Flicker noise or $1/f$ noise is caused by charge carriers getting trapped and later released as they move in the channel. It is usually modeled by a series noise voltage source connected to the gate. The PSD of this voltage is approximately given by

$$S_{\rm vf}(f) = \frac{K}{WLf}({\rm V}^2/{\rm Hz}) \tag{3}$$

where W and L are the width and length of the channel, f is the frequency, and K is a fabrication parameter. Note that $S_{\rm vf}(f)$ is not white; most of its power is concentrated at low frequencies.

The reader is referred to the many available texts (e.g., [1, ch. 4]) for a more detailed discussion of intrinsic device noise.

In many cases, the effects of $1/f$ noise may be reduced using large input devices, and choosing them as pMOS rather than nMOS transistors. Also, correlated double sampling or chopper stabilization [1], [2] may be used to suppress the $1/f$ noise, or to modulate it to out-of-band frequencies.

In this paper, the effects of thermal noise on the performance of SC circuits will be discussed, and an efficient algorithm will be described for estimating the magnitude of these effects. Section II considers the noise effects in the CMOS operational amplifiers (op-amps) commonly used in SC circuits. Section III contains a general analysis of filtered and sampled thermal noise. Section IV describes an algorithm for calculating the

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[1]Shot noise, which is due to the random flow of discrete charges under high electric field conditions, is significant mostly in the forward-biased p-n junctions, which do not exist in common MOS devices. It may occur, however, in deep submicron devices if significant gate current flows.

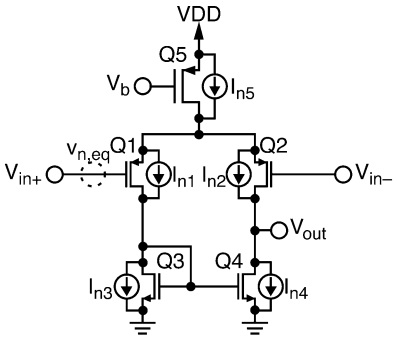

Fig. 1. Noise sources in a simple CMOS op-amp.

input- and output-referred noise power generated in a SC integrator, and proposes a design technique based on it. Section V compares the noise performances of single-ended and differential structures; Section VI gives a numerical example of the estimation process for an integrator. Finally, Section VII describes the application of the estimation algorithm to a SC delta-sigma modulator.

All derivations in this paper assume that the output of the SC circuit is being sampled, and hence, only the discrete-time output noise is of interest. In some applications (e.g., in the analysis of the reconstruction filter of a delta-sigma digital-to-analog converter), the continuous-time output noise must be found. This noise contains a component directly fed from the noise sources to the output with an essentially white spectrum, as well as a sampled-and-held one. Both spectra represent continuous-time signals, and hence, they are not periodic. By contrast, based on physical considerations to be discussed in Section III, all sampled noises considered in this paper will have periodic spectra. The discussions in this paper do not extend to the analysis of continuous-time noise; the reader may consult the available literature, e.g., [3], [9] for an analysis of this condition.

More detailed discussion of some issues mentioned in this paper can be found in [4] and [5].

II. Thermal Noise Effects in CMOS op Amps

Next, the estimation of thermal noise in op-amps will be discussed. As an illustration, a differential pair (which may be the input stage of a multistage op-amp) is shown in Fig. 1, along with its thermal noise current sources. These represent the effect of the noise currents, given in (2). It can readily be seen that the noise current of the tail device Q5 does not contribute to the output current, since it is present in the drain currents of both Q2 and Q4, and hence, cancels in the output current under ideal matching conditions. (This is a good approximation only at frequencies where the gains and delays of the two paths match.[2]) The noise currents of the input devices (assumed to be perfectly matched) can be represented by equivalent noise voltage sources at their gate terminals. From (2), the PSDs of these sources are given by $(8/3)kT/g_{m1}$. The noise current of Q3 can also be represented by a voltage source at the gate of Q1. The PSD of this source is $(8/3)kTg_{m3}/g_{m1}^2$. Similar considerations hold when the noise of Q4 is represented by an equivalent source at the input of Q2.

[2]More importantly, it is a good approximation in fully differential circuits.

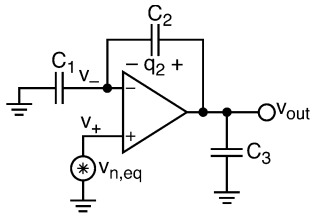

Fig. 2. Op-amp with capacitive feedback and capacitive loading.

Combining these results, the total thermal noise of the stage may be represented by a single equivalent noise voltage source $v_{n,\mathrm{eq}}$ at the gate of Q1 (or Q2). Its PSD is

$$S_{\mathrm{vt}}(f) = \frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right) \approx \frac{16kT}{3g_{m1}}. \tag{4}$$

The first equality of (4) suggests that for low noise $g_{m1} \gg g_{m3}$ should be used, which justifies the approximation made in the last part.

Consider next the op-amp under negative feedback conditions (Fig. 2). Note that the op-amp noise is represented by the equivalent source $v_{n,\mathrm{eq}}$, and that no signal is present since only the noise amplification is analyzed. It will be realistically assumed that the op-amp is properly compensated, so that in the frequency range of interest (where the loop gain is 1 or larger) the closed-loop transfer function can be approximated by the one-pole expression

$$H(s) = \frac{V_{\mathrm{out}}(s)}{V_{+}(s)} = \frac{G_0}{1+s\tau}. \tag{5}$$

Here, G_0 is the dc gain of the stage, and τ is its settling time constant. G_0 is determined by the feedback factor $\beta = C_2/(C_1 + C_2)$ and by the dc gain A_0 of the op-amp. Assuming $A_0 \gg 1/\beta$, we find

$$G_0 = \frac{1}{\beta + 1/A_0} \approx \frac{1}{\beta} = 1 + C_1/C_2. \tag{6}$$

Since the settling time is determined by how fast the op-amp output current can charge the load capacitances, τ will be proportional to $1/g_{m1}$. Also, since feedback reduces τ, it may be written in the form $\tau = C_0/(\beta g_{m1})$, where C_0 depends on the structure of the op-amp. For a two-stage op-amp, $C_0 = C_c$, where C_c is the compensation capacitance connected between the stages ([1, ch. 5]). For a single-stage (folded- or telescopic-cascode) op-amp, C_0 is the load capacitance at the output node of the op-amp: $C_0 = C_{\mathrm{load}} = C_3 + C_1C_2/(C_1 + C_2)$.

The PSD of the white input noise becomes shaped at the output by the first-order low-pass filter function given in (5). The mean-square (MS) value of the output noise may be calculated by integrating the shaped PSD from dc to infinite frequency

$$\overline{v_{\mathrm{out}}^2} = \int_0^\infty S_{\mathrm{vt}}(f)|H(j2\pi f)|^2 df = \left(\frac{16kT}{3g_{m1}}\right)\left(\frac{G_0^2}{4\tau}\right). \tag{7}$$

Substituting the values derived above for G_0 and τ gives

$$\overline{v_{\mathrm{out}}^2} = \left(\frac{4kT}{3}\right)\left(\frac{1+C_1/C_2}{C_0}\right) = \frac{4}{3}\frac{kT}{\beta C_0}. \tag{8}$$

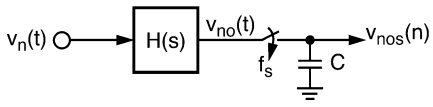

Fig. 3. Noise signals in a sampled system.

The MS value of the output noise voltage for unity-gain feedback can also be obtained, simply by setting $\beta = 1$ $(C_1 = 0)$ in (8)

$$\overline{v_{\rm out}^2} = \frac{4kT}{3C_0}. \tag{9}$$

Notice that even though the PSD of the op-amp's input noise source is determined by g_{m1}, (8) and (9), which give the MS value of its output noise, do not contain g_{m1}. This is because the PSD is inversely proportional to g_{m1}, while the bandwidth of the stage is directly proportional to it. Hence, its effect cancels in the calculation of the MS output noise.

III. Sampled Thermal Noise

The discussions of (5)–(7) can easily be generalized, and extended to sampled noise. As shown, when a thermal noise voltage v_n with a white spectrum $S_v(f)$ is processed by a first-order filter with a transfer function

$$H(s) = \frac{G_0}{1 + s\tau} \tag{10}$$

the result is a noise voltage $v_{\rm no}$ with a low-pass spectrum. Its PSD has a 3-dB bandwidth at $f_{3\ {\rm dB}} = 1/(2\pi\tau)$, and it has a MS value

$$\overline{v_{\rm no}^2} = \frac{G_0^2 S_v}{4\tau}. \tag{11}$$

The time constant τ determines the required settling time of the system, since its transient follows the $e^{-t/\tau}$ response.

Assume next that the thermal noise source feeds a low-pass filter (active or passive) whose voltage output is sampled on a capacitor C (Fig. 3), at a clock rate f_s. Let the continuous-time transfer function $H(s)$ from v_n to $v_{\rm no}$, when C is connected to the filter, be given by (10). If the system must have an N-bit performance, then the settling error at the output of the LPF must be less than half an LSB. For a 2-phase system, this requires that the condition

$$e^{-\frac{1/(2f_s)}{\tau}} < 2^{-(N+1)} \tag{12}$$

or equivalently

$$\frac{f_{3\ {\rm dB}}}{f_s} > \frac{(N+1)\ln 2}{\pi} \tag{13}$$

be satisfied. For example, if $N = 10$ bits, then (13) requires that $f_{3\ {\rm dB}}/f_s > 2.43$. Thus, the PSD of the $H(s)$ block output will be heavily aliased in the sampling process. Due to folding, the spectrum of the sampled noise signal $v_{\rm nos}(n)$ will be very nearly white[3].

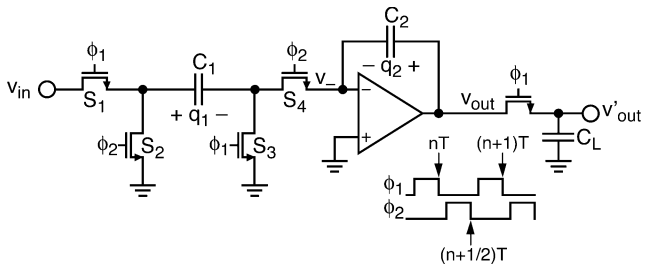

Fig. 4. A stray-insensitive SC integrator.

The aliasing described above increases the PSD of the noise significantly. The MS value of the sampled signal $v_{\rm nos}(n)$ remains the same as that of $v_{\rm no}(t)$, since all its samples are taken from synchronous values of $v_{\rm no}(t)$. Since $v_{\rm nos}(n)$ is a (nearly) white noise, its PSD can be found from

$$S_{\rm nos}(f) = \frac{\overline{v_{\rm no}^2}}{f_s/2} = \frac{G_0^2 S_v}{2\tau f_s}. \tag{14}$$

Since the low-frequency PSD of $v_{\rm no}(t)$ is $G_0^2 S_v$, the PSD has increased by a factor $1/(2\tau f_s)$, which by (12) is larger than $(N+1)\ln 2$. For example, if $N = 10$ bits, the noise PSD is magnified by a factor of 7.6, or 8.8 dB. This represents an inherent disadvantage of sampled-data analog signal processors, such as SC and switched-current filters, as compared to continuous-time ones.

Note that in oversampled SCFs followed by a unity-gain-passband digital LPF, the MS value of the oversampled noise is reduced by the oversampling ratio OSR after digital filtering.

IV. Noise Effects in an SC Integrator

Consider next the stray-insensitive SC integrator shown in Fig. 4. As indicated, the sampling instants $nT, (n+1)T, \ldots$ are at the end of the Φ_1 clock phases. For ideal components, the voltage across the input capacitor C_1 tracks the input voltage $v_{\rm in}$ when Φ_1 is high, and C_1 stores a charge $q_1(n) = C_1 v_{\rm in}(n)$ at the end of the phase. During $\Phi_2 = 1$, C_1 discharges q_1 into the virtual ground created by the op-amp. This causes the charge stored in C_2 at the end of Φ_2 to become

$$q_2(n+1/2) = q_2(n+1) = q_2(n) + C_1 v_{\rm in}(n). \tag{15}$$

Hence, the output voltage $v_{\rm out}$ satisfies

$$v_{\rm out}(n+1) = v_{\rm out}(n) + (C_1/C_2) v_{\rm in}(n). \tag{16}$$

Next, we consider the noise contributed by the switches S_1 through S_4 (Fig. 5). The only significant noise effect introduced

[3]Another possible explanation for this phenomenon is that under conditions (12)–(13) the memory span of the LPF is much shorter than $1/f_s$. Hence, the samples of $v_{\rm no}(t)$ taken at times n/f_s, $n = 1, 2, \ldots$ are very nearly uncorrelated. This property results in a white spectrum for $v_{\rm nos}(n)$.

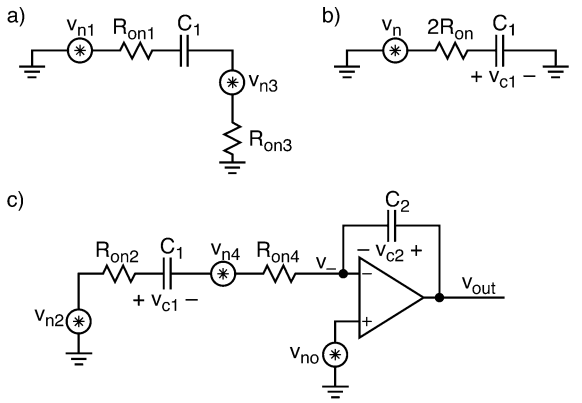

Fig. 5. Noise analysis for the integrator in Fig. 4.

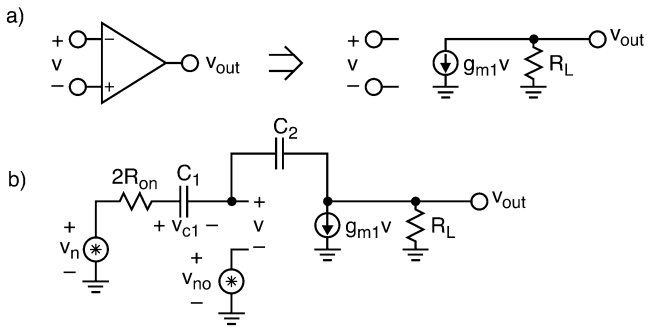

Fig. 6. Noise analysis for a single-stage amplifier.

by these switches is thermal noise[4]. For simplicity, $v_{\rm in} = 0$ will be assumed. We shall first find the noise voltage $v_{c1}(n)$ across C_1 due to the thermal noises generated in switches S_1 and S_3. While Φ_1 is high, the circuit containing C_1 can be represented by the branch shown in Fig. 5(a). Here, the conducting switches S_1 and S_3 have been replaced by their noise voltages and on-resistances. As illustrated in Fig. 5(b), the noise voltages and resistors can be pairwise combined. Assuming that all switches have the same $R_{\rm on}$, the combined switch resistance is $2R_{\rm on}$ and (since v_{n1} and v_{n3} are uncorrelated) the PSD of the associated noise voltage v_n is $4kT(2R_{\rm on}) = 8kTR_{\rm on}$.

The PSD of the noise voltage v_{c1} across C_1 can be expressed in terms of the PSD of v_n as follows:

$$S_{c1}(f) = \frac{2S_{\rm vt}(f)}{1+(2\pi f\tau_0)^2} = \frac{8kTR_{\rm on}}{1+(2\pi f\tau_0)^2} \tag{17}$$

where $\tau_0 = 2R_{\rm on}C_1$ is the time constant of the C_1 branch during $\Phi_1 = 1$. $S_{c1}(f)$ has a low-pass-filtered spectrum; it is no longer white. Its dc value is $8kTR_{\rm on}$, while its 3-dB (half-power) frequency is $f_0 = 1/(2\pi f\tau_0)$.

The total power (mean-square value) of $v_{c1}(t)$ can be obtained by integrating $S_{c1}(f)$ for all frequencies from 0 to infinity. This gives

$$\overline{v_{c1}^2} = \frac{8kTR_{\rm on}}{4\tau_0} = \frac{kT}{C_1} \tag{18}$$

which is independent of $R_{\rm on}$. The explanation is that the dc value of the PSD is proportional to $R_{\rm on}$, while its bandwidth ω_0 is proportional to $1/R_{\rm on}$[5]. The noise charge stored in C_1 is $q_1(t) = C_1v_{c1}(t)$; its mean-square value is $C_1^2kT/C_1 = kTC_1$.

At the end of the nth $\Phi_1 = 1$ period (i.e., at $t = nT$), switches S_1 and S_3 will open, and the charge $q_1(n)$ is trapped in C_1. The sequence $q_1(n)$, $n = 1, 2, \ldots$ has the same mean-square value kTC_1 as $q_1(t)$, since it is constructed from the samples of $q_1(t)$. However, due to the sampling, the PSD of $q_1(n)$ is nearly perfectly white. The reason for this is aliasing, as discussed in Section III, since (13) must hold here for f_o/f_s.

Next, when Φ_2 rises, switches S_2 and S_4 close. The resulting noisy circuit is shown in Fig. 5(c). To make the analysis more specific, we shall assume a single-stage op-amp[6] represented by the model shown in Fig. 6(a), compensated by its capacitive load. The diagram of Fig. 6(b) illustrates the resulting circuit during the time when Φ_2 is high. Note that the on-resistances and noise voltages of the two switches have again been combined.

In the analysis of the circuit, it is reasonable to assume that the loop gain of the stage satisfies the condition $\beta g_{m1}R_L \gg 1$, where $\beta = C_2/(C_1 + C_2)$; this is necessary for suppressing signal distortion caused by op-amp nonlinearity. Under this condition, $1/R_L = 0$ may be assumed, and the calculation simplified.

Using the Laplace transform, the noise voltage across C_1 may be found as

$$V_{c1}(s) = \frac{V_n(s) - V_{\rm no}(s)}{1+s\tau} \tag{19}$$

where

$$\tau = (2R_{\rm on} + 1/g_{m1})C_1. \tag{20}$$

Utilizing the results of Section III, the MS value of the C_1 noise voltage due to the switch noise v_n can be calculated

$$\overline{v_{c1,\rm sw}^2} = \frac{S_n(0)}{4\tau} = \frac{8kTR_{\rm on}}{4(2R_{\rm on}+1/g_{m1})C_1} = \frac{kT/C_1}{1+1/x}. \tag{21}$$

Here, the parameter $x = 2R_{\rm on}g_{m1}$ was introduced.

The noise power in C_1 due to op-amp noise can also be found

$$\overline{v_{c1,\rm op}^2} = \frac{S_{\rm no}}{4\tau} = \frac{(16/3)kT/g_{m1}}{4(2R_{\rm on}+1/g_{m1})C_1} = \left(\frac{4}{3}\right)\frac{kT/C_1}{1+x}. \tag{22}$$

Consider next the total noise power stored in C_1. At the end of clock phase Φ_1, as illustrated in Fig. 5(b), C_1 had acquired a noise voltage $v_{c1,1}$ whose power was given by (18). During phase Φ_2, the noise voltage becomes $v_{c1,\rm sw} + v_{c1,\rm op}$. The

[4]Since the current flow in these switches consists of short pulses occurring at the clock rate, the $1/f$ noise (which is caused by the trapping and release of charge carriers occurring at long intervals) has only a negligible effect here.

[5]An alternative derivation appeals to the physical principle known as Equipartition of Energy, which states that the average energy associated with any degree of freedom in a system at thermal equilibrium is $kT/2$. For a capacitor C charged to a voltage v, the electrical energy is $E = Cv^2/2$ and thus, $\bar{E} = kT/2$ implies $\overline{v^2} = kT/C$.

[6]The single-stage op-amp is the most commonly used active element in SC integrators, and it allows the simplest treatment of the noise issue. Two-stage amplifiers can be analyzed similarly, but require a more elaborate analysis, and are not discussed in this paper.

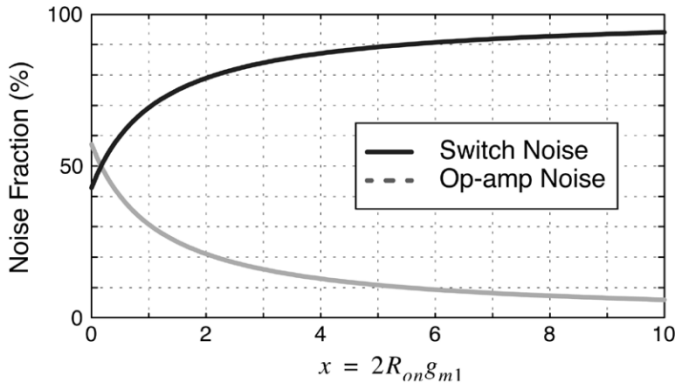

Fig. 7. Relative contributions from the switches and op-amp to the total integrator thermal noise.

components have the noise powers given in (21) and (22). The change in v_{c1} during Φ_2 is hence, $v_{c1,\mathrm{sw}} + v_{c1,\mathrm{op}} - v_{c1,1}$. Since the three noise voltages are uncorrelated, their powers are added. Hence, the total noise power is[7]

$$\overline{v_{c1}^2} = \frac{kT}{C_1}\left(1 + \frac{x}{1+x} + \frac{4/3}{1+x}\right) = \frac{kT}{C_1}\left(\frac{7/3+2x}{1+x}\right) = \frac{2kT}{C_1}\left(1 + \frac{1/6}{1+x}\right). \quad (23)$$

As (20)–(22) show, the ratio of the switch noise power to the op-amp noise power generated during Φ_2 is $3x/4$. Thus, for $x \ll 1$ (i.e., for $g_{m1} \ll 1/R_{\mathrm{on}}$), the op-amp dominates both the bandwidth and the noise, while for $x \gg 1 (g_{m1} \gg 1/R_{\mathrm{on}})$, the switch effects dominate. The overall situation considering both clock phases is shown in Fig. 7.

The total noise power is minimized, and becomes $2kT/C_1$, if $x \gg 1$, i.e., if the condition $g_{m1} \gg 1/R_{\mathrm{on}}$ holds. Under these conditions, all noise is contributed by the switches. The absence of noise from the op-amp is due to the fact that [as (4) shows] the input-referred noise of the op-amp is inversely proportional to g_{m1}.

For a given capacitor size (i.e., for a fixed C_1), the condition $x \gg 1$ yields the minimum achievable noise. For a circuit whose area is dominated by its capacitors, this condition corresponds to the minimum-area solution. However, since realizing a large value of g_{m1} requires a large current, the most power-efficient solution is the one that minimizes g_{m1} subject to constraints on the noise power [cf. (23)] and the settling time [cf. (20)]. Combining these relations leads to

$$g_{m1} = \frac{kT}{\tau \overline{v_{c1}^2}}(7/3 + 2x) \quad (24)$$

which is clearly minimized for $x = 0$. Since, according to (23), the total noise power associated with this solution is $2.33kT/C_1$, the size of C_1 in the minimum-power design is only about 17% larger than the size of C_1 in the minimum-capacitance design.

From (23), the mean-square noise charge stored in C_1 at the end of the $\Phi_2 = 1$ phase is given by

$$\overline{q_{c1}^2} = kTC_1\left(\frac{7/3+2x}{1+x}\right). \quad (25)$$

Consider next the noise charge delivered to C_2 during $\Phi_2 = 1$. C_1 arrives at the virtual ground carrying a charge $C_1 v_{c1,1}$. Since the time constant of the stage is much shorter than $1/2f_s$, this charge will disappear by the end of the Φ_2 phase, and will be replaced by $C_1[v_{c1,\mathrm{sw}} + v_{c1,\mathrm{op}}]$. Since all voltages are uncorrelated, the change in the MS value of the noise charge in C_1 will be the sum of the MS charges due to voltages $v_{c1,1}, v_{c1,\mathrm{sw}}$ and $v_{c1,\mathrm{op}}$, as given by (25). Since C_1 and C_2 become series-connected as Φ_2 rises, C_2 acquires the same additional noise charge as C_1. Hence, the added noise charge for C_2 is $q_{c2} = q_{c1}$, and the MS noise voltage of C_2 is increased by

$$\overline{(\Delta v_{c2})^2} = \frac{kTC_1}{C_2^2}\left(\frac{7/3+2x}{1+x}\right) \quad (26)$$

during each Φ_2 clock phase.

It is often useful to represent the effect of the accumulated noise contribution from a stage by one or more equivalent voltage sources at the input and/or output of an otherwise ideal and noiseless circuit. As discussed above, the effect of thermal noise in the transistors of the switches and the op-amp in a SC integrator is an added noise charge in both C_1 and C_2, with an MS value given in (25). In a noiseless and ideal SC integrator, this charge can be delivered into C_2 by connecting an equivalent noise voltage source $v_{n,\mathrm{in}}$ to the input of the integrator. The MS value of $v_{n,\mathrm{in}}$ is the same as that of v_{c1}, given in (23); $v_{n,\mathrm{in}}$ is a sampled-data signal with a white spectrum.

Frequently, there are several SC input branches in an integrator. Assuming for simplicity that $g_{m1} \gg 1/R_{\mathrm{on}}$, the total noise charge contributed by the switched input capacitors $C_{1a}, C_{1b}, \ldots$ to C_2 is given by

$$\overline{q_{c2}^2} = 2kT(C_{1a} + C_{1b} + \cdots). \quad (27)$$

[7]Expressions (18), (21), and (22) represent the continuous-time dynamics of the voltage $v_{c1}(t)$, and (23) assumes that the corresponding charge distribution is ideally frozen in time at the end of the respective clock phases. In other words, the turn-off transition of the switches is assumed to be ideal. Several nonidealities associated with the turn-off transition of real world MOSFET-based switches, however, may affect the circuit's noise properties.

- Finite transition time of the switches' control signals will cause a gradual transition of their impedance from R_{on} to R_{off}. If this effect becomes pronounced, the effective value of x may be higher than $x = 2R_{\mathrm{on}}g_{m1}$.
- MOSFET-based switches store charge in the conductive channel when they are turned on. This inversion charge is released when the switch is turned off. The distribution of the released charge carriers to the two switch terminals is to some (unknown) extent a stochastic process. Expression (23) does not account for this noise contribution. The error is believed to be negligible in many cases, but the reader is cautioned that (21) may underestimate the sampled noise from the switches for small values of x (the inversion charge is proportional to $1/R_{\mathrm{on}}$). A conservative circuit designer may choose to replace (21) by kT/C_1, which is an upper limit for the switches' (S_2 and S_4) total sampled noise contribution.

Note also that the derivation of (18) is based on the assumption that the settling time constant is given by $\tau_0 = 2R_{\mathrm{on}}C_1$, i.e., it is assumed that the signal source driving C_1 has an arbitrarily high bandwidth. If the bandwidth is effectively limited by the signal source rather than R_{on}, the effective noise contribution from S_1 and S_3 may be less than kT/C_1. In that case, (18) should be replaced by an expression similar to (21). However, considering the uncertainty pertaining to the nonidealities associated with the switches' turn-off transition, the conservative circuit designer may choose to use the upper limit $2kT/C_1$ for the total switch-induced noise power in C_1.

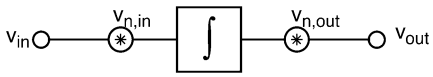

Fig. 8. Equivalent noise sources for the integrator of Fig. 4.

Thus, a large input capacitor contributes more noise than a small one does. In the typical case where $g_{m1} \ll 1/R_{\rm on}$, we may use (25) and (26) by substituting $C_1 = C_{1a} + C_{1b} + \cdots$.

In the input stage of a SC delta-sigma loop, it is possible to use either a single capacitor to enter both input and DAC signals, or to use two separate ones. As (27) demonstrates, the latter solution introduces up to twice as much thermal noise power as the first one, so the SNR is reduced by up to 3 dB. Using only one capacitor, however, may cause signal-dependent disturbances in the DAC reference voltage, which is another important aspect to consider in the design.

The input-referred noise source $v_{n,\rm in}$ models the noise charge entering C_2 in every clock period, and hence the noise voltage v_{c2}. However, the output voltage is the sum of v_{c2} and the voltage v_- at the inverting input terminal of the op-amp [Fig. 5(c)]. During $\Phi_1 = 1$, when the output voltage is sampled, the circuit is in a unity-gain configuration (in small-signal sense), and the MS value of v_- may be obtained from (9). Since v_- is added only to the output voltage, it may be represented by an output-referred sampled-data voltage source $v_{n,\rm out} = v_-$. The MS value of $v_{n,\rm out}$ is given by (9); for the op-amp representation of Fig. 6(a), $C_0 = C_L$ should be used (Fig. 4). The overall model of thermal noise effects is shown in Fig. 8, where the center box represents an ideal noiseless SC integrator.

As will be illustrated in the example given below, the effect of $v_{n,\rm out}$ is usually negligible compared to that of $v_{n,\rm in}$. Hence, the relative contributions of the switches and the op-amp to the integrator noise can be predicted from (23), as functions of $x = 2R_{\rm on}g_{m1}$. The resulting curves are shown in Fig. 7. As the curves illustrate, the noise due to the op-amp is comparable to the noise due to the switches when x is small, but when x is large the switch noise dominates.

Next, the use of the above estimation results in the design of the integrator will be discussed. As (24) shows, the MS value of v_{c1} increases with x, and it is inversely proportional to τ and g_{m1}. Hence, it is expedient to choose $x \ll 1$, and to make τ as large as (12) allows, i.e., to choose

$$\tau = [(2\ln 2)(N+1)f_s]^{-1}. \tag{28}$$

If, for example, $N = 10$ bits, then $\tau \approx 0.0656/f_s$ should be chosen. Then, g_{m1} can be found from (24). For $x \ll 1$, this gives

$$g_{m1} \approx \frac{7}{3}\frac{kT}{\tau\overline{v_{c1}^2}} \tag{29}$$

where the permissible MS value of v_{c1} is again determined by N and by the input signal level of the integrator. Finally, C_1 can be calculated from (29) and from (20), which may be rewritten in the form

$$C_1 = \frac{g_{m1}\tau}{x+1} \approx \frac{7}{3}\frac{kT}{\overline{v_{c1}^2}}. \tag{30}$$

V. Single-Ended Versus Differential Circuits

The described noise calculations assume single-ended circuit configurations. We will now estimate and compare the noise performance of a fully differential circuit based on the same total capacitance $C_1 + C_2$. To preserve the total capacitance, capacitors C_1 and C_2 are each split in two equal parts, and the two halves are assigned respectively to the positive and the negative side of the differential circuit.

To enable a fair comparison of the noise properties of single-ended versus differential circuits, we must first determine the key properties characterizing the opamps driving the respective capacitor configurations. We will use the single-ended transconductance amplifier (opamp) shown in Fig. 1 as a vehicle for this analysis. The opamp's input signal $v_{\rm diff}$ is divided equally between the two input transistors, Q1 and Q2, producing the drain currents $i_d = \pm(v_{\rm diff}/2)\cdot g_{m1}$. The current mirror (Q3 and Q4) will invert the current i_{d1}, and the single-ended opamp will thus produce the output current

$$i_{\rm out,se} = i_{d2} - i_{d1} = 2\cdot\frac{v_{\rm diff}}{2}\cdot g_{m1} = v_{\rm diff}\cdot g_{m1}. \tag{31}$$

In an equivalent fully differential opamp, the gate terminals of Q3 and Q4 will be driven by a common-mode feedback circuit, and the two output currents will simply be the drain currents of Q1 and Q2

$$i_{\rm out,diff} = \pm\frac{v_{\rm diff}}{2}\cdot g_{m1}. \tag{32}$$

To facilitate the noise analysis, we have to determine for each type of circuit the transconductance g_{m1} (of Q1 and Q2) needed to make the respective circuits settle with the appropriate time constant (12): $\tau \simeq [2\ln(2)f_s(N+1)]^{-1}$. The required g_{m1} values differ for the two types of circuit.

For simplicity and without loss of generality, we will assume that the five transistors have predefined aspect ratios, and that they all contain unit devices with the same multiplicity: $M_{\rm se}$ for the single-ended opamp and $M_{\rm diff}$ for the differential opamp. The effective transconductances g_{m1} of the opamps are thus respectively $M_{\rm se}\cdot g_u$ and $M_{\rm diff}\cdot g_u$, where g_u is the transconductance of each unit-sized transistor used to implement Q1 and Q2. The topology and the main features of the circuits are shown in Fig. 9.

The single-ended circuit will settle with the time constant $\tau_{\rm se} = (C_1/M_{\rm se}\cdot g_u)$. Using the concept of half circuits, $v_{\rm in}$ and $v_{\rm diff}$ may each be split into two halves, and we find that the differential circuit will settle with the time constant $\tau_{\rm diff} = (C_1/2/M_{\rm diff}\cdot g_u)$. Notice that, when compared to the single-ended circuit, each half of the differential circuit has the same effective transconductance $M\cdot g_u$, and that it (for $M_{\rm diff} = M_{\rm se}$) will settle twice as fast, because it is subject to only half the capacitive load. In practice, however, the circuits should be designed to settle with the same time constant[8], which implies that $M_{\rm diff} = (M_{\rm se}/2)$.

[8]In reality, the capacitive load is not reduced exactly by a factor of two, because the differential opamp's input capacitance is larger than that of the single-ended opamp. Specifically, if $C_{\rm gs,u}$ denotes the gate-source capacitance of one unit transistor, the differential opamp's input capacitance is $M_{\rm diff}\cdot C_{\rm gs,u}$ (half circuit), and the single-ended opamp's input capacitance is $(M_{\rm se}/2)\cdot C_{\rm gs,u}$. When taking this difference into account, we may calculate the settling time constants as $\tau_{\rm se} = (C_1 + 0.5M_{\rm se}C_{\rm gs,u})/M_{\rm se}\cdot g_u$ and $\tau_{\rm diff} = (0.5C_1 + M_{\rm diff}C_{\rm gs,u})/M_{\rm diff}\cdot g_u = (C_1 + 2M_{\rm diff}C_{\rm gs,u})/2M_{\rm diff}\cdot g_u$. Equivalent settling properties are, therefore, achieved when $M_{\rm diff} = (M_{\rm se}/2)(1-(M_{\rm se}\cdot C_{\rm gs,u}/2C_1))^{-1}$.

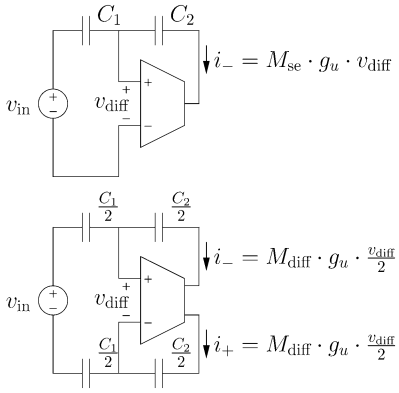

Fig. 9. Topology and main properties of the single-ended and fully-differential circuits.

With the above results in place, we are now ready to compare the noise performances of the two types of circuits assuming the same total capacitance and settling time constant. The total noise of the single-ended circuit is given by (23). The differential circuit has more and larger noise sources. Because the capacitors are each half the size (and twice as many), we find that the noise contribution corresponding to (18) is $2 \cdot (kT/C_1/2) = (4kT/C_1)$. Likewise, we find that the noise contribution corresponding to (21) is $(4kT/C_1/(1+1/x))$. Finally, we may calculate the noise contribution corresponding to (22) by adding the noise contributions from the two half circuits[9]

$$\overline{v_{\rm op,diff}^2} = 2 \cdot \frac{(8/3) \cdot kT/(M_{\rm diff} \cdot g_u)}{4\tau_{\rm diff}} = \frac{8}{3} \cdot \frac{kT/C_1}{(1+x)}. \quad (33)$$

The total input-referred noise [corresponding to (23)] for the differential circuit is thus

$$\begin{aligned} \overline{v_{n,\rm diff}^2} &= \frac{kT}{C_1}\left(4 + \frac{4}{1+1/x} + \frac{8/3}{1+x}\right) \\ &= 4 \cdot \frac{2kT}{C_1}\left(1 - \frac{1/6}{1+x}\right). \end{aligned} \quad (34)$$

We can calculate the ratio of the differential circuit's noise level to that of the single-ended circuit from

$$\frac{\overline{v_{n,\rm diff}^2}}{\overline{v_{n,\rm se}^2}} = 4 \cdot \frac{(1+x) - 1/6}{(1+x) + 1/6} \simeq 2.8 \text{ for } x \ll 1. \quad (35)$$

At first sight it may be disappointing that the differential circuit has a relatively much higher (4.5 dB) noise floor, but the result should be evaluated in the proper context. The full-scale signal swing of the differential circuit is twice that of the single-ended circuit, and hence, the dynamic range of the differential circuit is about 6 dB $-$ 4.5 dB $=$ 1.5 dB higher than that of the single-ended circuit. Furthermore, it is important to remember that the imposed requirement of equivalent settling behavior implied that $M_{\rm diff} = M_{\rm se}/2$, i.e., the fully-differential circuit consumes only half as much power as the single-ended one does.

Now consider a comparison where the power consumption and the time constants are assumed to be equal. The differential circuit will drive twice as much capacitance as the single-ended circuit. This will improve the dynamic range of the differential circuit by an extra 3 dB, which makes the dynamic range advantage a full 4.5 dB.

Typically, a given application will require the circuit to have a specified dynamic range. If we make a comparison where the dynamic ranges and the time constants are equal, we find that the differential circuit will consume only $10^{-4.5/10} \simeq 35\%$ of the power required by the single-ended circuit. Fully differential circuits are thus preferable not only because they suppress even-order harmonic distortion and are more robust to extrinsic noise, but also because they allow a longer battery life and/or smaller chip size.

The above results have been verified by means of simulations. A cascoded version of the considered simple amplifier structure (Fig. 1) was designed and simulated for $M_{\rm se} = 10$ and $M_{\rm diff} = 5$. The corresponding current consumptions were, respectively, 30 μA and 15 μA, and the opamps were driving capacitive loads $C_1 = 10$ pF. The unit-sized input transistors each had a transconductance of $g_u = 22$ μS. The observed/simulated time constants were, respectively, 44.6 and 46.0 ns, which is within a few percent of the values anticipated by our analysis. The input-referred noise from the opamps was, respectively, $(12.2 \text{ nV})^2$/Hz and $(17.4 \text{ nV})^2$/Hz, which is about 51% higher (power) than the anticipated values. This discrepancy is not a cause of concern, since the additional noise can be tracked back to Q3 and Q4 (and the increase is approximately the same for both the single-ended and the differential circuit). Overall, we find that the noise power of the single-ended circuit is (for $x \simeq 0$)

$$\overline{v_{n,\rm se}^2} = \frac{kT}{10 \text{ pF}} + \frac{(12.2 \text{ nV})^2/\text{Hz}}{4 \cdot 44.6 \text{ ns}} = (35.4\ \mu\text{V})^2 \quad (36)$$

and that the total noise of the differential circuit is

$$\overline{v_{n,\rm diff}^2} = \frac{2kT}{5\text{pF}} + \frac{(17.4 \text{ nV})^2/\text{Hz}}{4 \cdot 46.0 \text{ ns}} = (57.5\ \mu\text{V})^2 \quad (37)$$

which implies that the dynamic range of the differential circuit is approximately 1.8 dB better than that of the single-ended circuit. This is remarkable in itself, but more so when taking into account that the differential circuit uses only half the power.

Finally, it should be noted that the noise estimation process discussed here remains a good approximation up to a radian frequency $\omega = \beta g_{m1}/C_L$, even if the op-amp model includes an output capacitance C_L in parallel with R_L (Fig. 6).

VI. Integrator Noise Analysis Example

The following example illustrates how to calculate the output noise for the integrator shown in Fig. 4, given some specific values.

It is assumed that the clock frequency is $f_s = 100$ MHz. The signals must settle to an accuracy of $N = 10$ bits, and an input-referred noise voltage $\overline{v_{c1}} = 100$ μV is desired. The integrator has a gain factor $k = C_1/C_2 = 1$, and must drive the load capacitance $C_L = 0.5$ pF during phase Φ_1. To ensure that the op-amp dominates bandwidth and noise, $x = 0.1$ was selected.

These specifications are used next to calculate the circuit parameters according to (28)–(30). The settling time constant is determined as $\tau = 0.66$ ns, and thus 7.6 times smaller than the

[9]Note that the opamp's contribution for each half circuit, $(4/3) \cdot (kT/C_1/(1+x))$, for $x \simeq 0$ is less than $(kT/C_1/2) = (2kT/C_1)$, which is not surprising considering that the input-referred noise of a MOSFET, $(2/3) \cdot (4kT/g_m)$, is less than the noise of a resistor having the same conductance g_m.

settling period of $0.5/f_s = 5$ ns. The amplifier is an OTA with transconductance $g_{m1} = 1.47$ mA/V. For simplicity, to make the dc gain $A = 1000$, the output impedance is assumed to be $R_L = 680.3$ kΩ. The input capacitance is then calculated as $C_1 = 0.97$ pF, and $C_2 = C_1/k = 0.97$ pF. The switches must have an on-resistance $R_{\rm on} = x/(2g_{m1}) = 34\ \Omega$.

The PSD of the output-referred noise is given by

$$S_{\rm vo} = S_{\rm vin} \cdot |H|^2 + S_{\rm vout}. \tag{38}$$

In this equation, the power of the input-referred noise source $v_{n,\rm in}$ is given by (23), while that of the output noise source $v_{n,\rm out}$ is given by (9). $S_{\rm vin}(S_{\rm vout})$ is obtained by dividing the power of $v_{n,\rm in}(v_{n,\rm out})$ by $f_s/2$.

In (38), $H(z)$ is the integrator transfer function. It can be found using available SC analysis programs, such as SWITCAP, or analytically, as shown below. For the integrator with a finite-gain op-amp, $H(z)$ is given by [6]

$$H(z) = \frac{kz^{-1}}{1 + \mu(1+k) - (1+\mu)z^{-1}}. \tag{39}$$

The parameter k is the integrator gain factor, as defined above. Also, $\mu = 1/A = 10^{-3}$. The parameter x in the input-referred noise source is $x = 2g_m R_{\rm on} = 0.1$.

The output-referred noise power can be calculated by integrating the output PSD $S_{\rm vo}$ [given in (38)] in the signal band, from 0 to $f_B = f_s/(2 \cdot {\rm OSR})$. The resulting equation is very complicated, and tedious to calculate manually. Since both $S_{\rm vin}$ and $S_{\rm vout}$ are frequency-independent, only $|H|^2$ needs to be integrated. This can be done simply numerically, using (39). Alternatively, the integration may be carried out analytically. A symbolic analysis tool, such as Maple [7], can be used for this calculation. The integrated noise power is then found to be

$$N_0^2 = 3.13 \times 10^{-6} \tan^{-1}\left[2003 \tan\left(\frac{\pi}{2{\rm OSR}}\right)\right] + \frac{5.61 \times 10^{-9}}{\rm OSR}. \tag{40}$$

The output noise power can also be simulated by a dedicated CAD tool, such as SpectreRF [8]. This circuit simulator has built-in analysis routines that can handle discrete-time circuits. Fig. 10 shows the calculated and simulated output noise powers, as functions of f_B. It also shows the noise contribution of $v_{n,\rm out}$, which is negligible here for all values of f_B shown, as predicted earlier. The good agreement between the calculated noise and the simulated one confirms the usefulness of the theory discussed earlier.

VII. Thermal Noise Effects in a Delta-Sigma Loop

As an example of the use of the described noise estimation algorithm, we shall next apply it to the design of a second-order low-distortion delta-sigma modulator. Its block diagram is shown in Fig. 11; the $H(z)$ blocks represent SC integrators using the circuit of Fig. 4. The complete circuit is shown in Fig. 12. We shall assume an oversampling ratio ${\rm OSR} = 32$, a maximum input signal power of 0.25 $\rm V^2$ (−6.0 dBV), and a desired 13-bit performance (i.e., an SNR of 80.0 dB). The

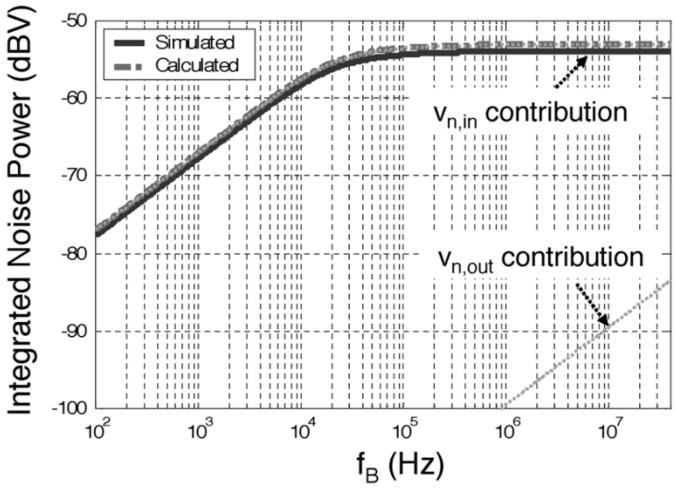

Fig. 10. Calculated and simulated integrated noise powers at the output of an integrator.

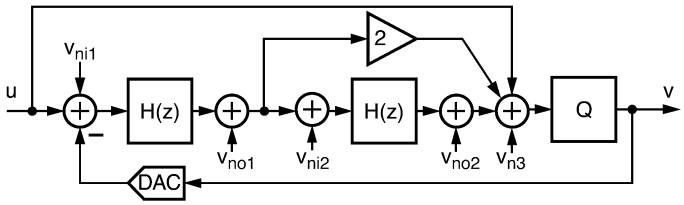

Fig. 11. Noise sources in the feedforward topology.

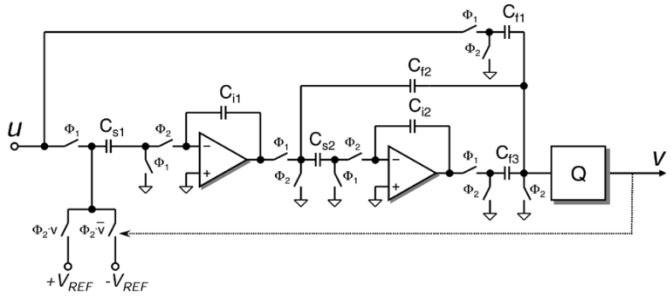

Fig. 12. Schematic of the feedforward topology.

total permissible noise power (including quantization error, extrinsic noise, etc.) is then $10^{(-6.0-80.0)/10}\ {\rm V}^2 = (50.1\ \mu{\rm V})^2$. Assigning 75% of the noise power to thermal noise [4], the total permissible input-referred thermal noise power turns out to be $\overline{v_{\rm th}^2} = (43.4\ \mu{\rm V})^2$.

In addition, the quantizer resolution must be chosen such that the quantization noise power is a negligible portion of the total noise power. Assigning 10% of the total noise power to the shaped in-band quantization noise, we find that a 5-bit quantizer is required for this structure.

Since the signal transfer function for this structure is ideally ${\rm STF} = 1$, the output-referred noise power is the same as the input-referred one[10].

[10]Here, for simplicity, we assume that the quantizer has a gain of 1. Note that this assumption effectively assigns a physical unit, say volts, to the digital output value. Note also that in the circuit diagram of Fig. 12, a capacitive voltage divider attenuates the input signal at the quantizer input by a factor of 4. This can be compensated for by using a quantizer gain with the same factor.

To find the minimum acceptable values of the switched input capacitors C_{s1} and C_{s2} of the two integrators, and of the input capacitors of the quantizer Q, the following steps need to be performed.

1) Identify the thermal noise sources (SC branches, op-amps) in the circuit:

   In this circuit, there are five SC branches (Fig. 12): one at the input of the first integrator (note that C_{s1} is shared between the input and feedback signal paths), one at the input of the second integrator, and three at the input of the quantizer. The latter are ratioed, so only one of them (say, C_{f1} connecting u to the input of Q) may be selected arbitrarily. There are also two op-amps, one in each integrator. The corresponding noise sources are indicated in Fig. 11.

2) Find the PSDs of all noise sources:

   Since all noise sources are sampled, with white PSDs, for the jth source the PSD may be found from the MS noise voltage simply as

$$S_{vj} = \frac{\overline{v_j^2}}{f_s/2}. \tag{41}$$

   The MS value of the input-referred noise voltage of the first integrator is, by (23)

$$\overline{v_{\mathrm{ni}1}^2} = \left(\frac{kT}{C_{s1}}\right)\frac{7/3+2x}{1+x}. \tag{42}$$

   The noise source at the output of the first integrator has the MS value [from (9)]

$$\overline{v_{\mathrm{no}\,1}^2} = \frac{4}{3}\frac{kT}{C_{01}} \tag{43}$$

   where C_{01} is the effective load capacitance of the op-amp during clock phase Φ_1, given by $C_{01} = C_{s2}+C_{f2}(C_{f1}+C_{f3})/(C_{f2}+C_{f1}+C_{f3})$.

   The MS noise voltages at the input and output of the second integrator are given by expressions similar to (42) and (43).

   The noise contributions of the three SC branches at the input of Q can be combined to give a noise power

$$\begin{aligned}\overline{v_{n3}^2} &= \frac{2kT}{C_{f1}}\left(1+\frac{C_{f2}}{C_{f1}}+\frac{C_{f3}}{C_{f1}}\right)\\ &= \frac{2kT}{C_{f1}}(1+2+1) = \frac{8kT}{C_{f1}}.\end{aligned} \tag{44}$$

3) Find the voltage and power transfer functions from each noise source to the output:

   This may be done numerically, using a dedicated SC analysis program, or analytically. We shall illustrate the latter method. Using

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \tag{45}$$

   the noise voltage transfer function from the input of the first integrator to the output of the modulator is found to be

$$\mathrm{NTF}_{i1}(z) = \frac{H^2+2H}{1+2H+H^2} = 2z^{-1}-z^{-2}. \tag{46}$$

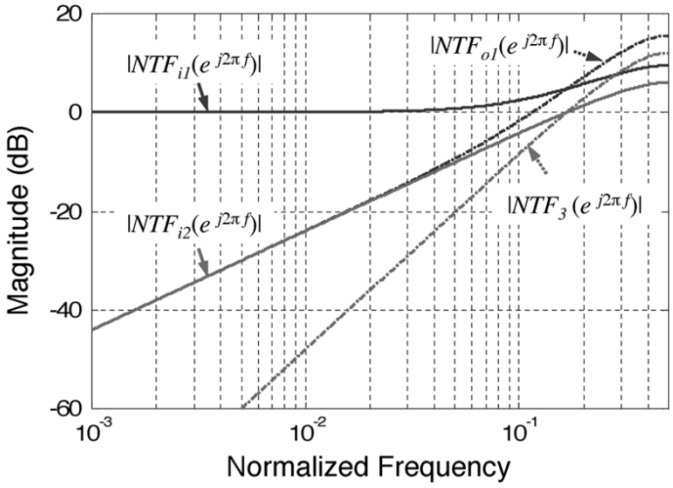

Fig. 13. Frequency responses of the noise power transfer functions.

   The NTF from the output of the first integrator is

$$\mathrm{NTF}_{o1}(z) = \frac{H+2}{1+2H+H^2} = (1-z^{-1})(2-z^{-2}). \tag{47}$$

   The NTF from the input of the second integrator is

$$\mathrm{NTF}_{i2}(z) = \frac{H}{1+2H+H^2} = z^{-1}(1-z^{-1}). \tag{48}$$

   Finally, the NTF from the input of the quantizer (and from the output of the second integrator) to the modulator output is

$$\mathrm{NTF}_3(z) = \mathrm{NTF}_{o2}(z) = \frac{1}{1+2H+H^2} = (1-z^{-1})^2. \tag{49}$$

   The corresponding frequency responses are shown in Fig. 13.

4) Integrate all noise PSDs, multiplied by the corresponding power transfer functions $|\mathrm{NTF}|^2$, from dc to the signal band edge $f_s/(2\mathrm{OSR})$:

   This may be performed numerically or analytically. If the latter procedure is followed, a symbolic analysis tool may be used. The resulting output noise powers turn out to be

$$\begin{aligned}\overline{N_{i1}^2} &= \frac{2\overline{v_{\mathrm{ni}1}^2}}{f_s}\int_0^{f_s/(2\mathrm{OSR})}|\mathrm{NTF}_{i1}|^2 df\\ &= \overline{v_{\mathrm{ni}1}^2}\left[\frac{5}{\mathrm{OSR}}-\frac{4}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\right]\end{aligned} \tag{50}$$

$$\begin{aligned}\overline{N_{o1}^2} = \overline{v_{\mathrm{no}1}^2}\Bigg[&\frac{14}{\mathrm{OSR}}+\frac{4}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\cos\left(\frac{\pi}{\mathrm{OSR}}\right)\\ &-\frac{18}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\Bigg]\end{aligned} \tag{51}$$

$$\overline{N_{i2}^2} = \overline{v_{\mathrm{ni}2}^2}\left[\frac{2}{\mathrm{OSR}}-\frac{2}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\right] \tag{52}$$

$$\begin{aligned}\overline{N_3^2} = \left(\overline{v_{\mathrm{no}2}^2}+\overline{v_{n3}^2}\right)\Bigg[&\frac{6}{\mathrm{OSR}}-\frac{8}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\\ &+\frac{2}{\pi}\sin\left(\frac{\pi}{\mathrm{OSR}}\right)\cos\left(\frac{\pi}{\mathrm{OSR}}\right)\Bigg].\end{aligned} \tag{53}$$

These expressions can be considerably simplified if a high OSR is used. With $\mathrm{OSR} \gg 1$, the output noise powers become

$$\overline{N_{i1}^2} \approx \frac{\overline{v_{\mathrm{ni1}}^2}}{\mathrm{OSR}}, \tag{54}$$

$$\overline{N_{o1}^2} \approx \overline{v_{\mathrm{no1}}^2} \frac{\pi^2}{3\mathrm{OSR}^3} \tag{55}$$

$$\overline{N_{i2}^2} \approx \overline{v_{\mathrm{ni2}}^2} \frac{\pi^2}{3\mathrm{OSR}^3} \tag{56}$$

$$\overline{N_3^2} \approx \left(\overline{v_{\mathrm{no2}}^2} + \overline{v_{n3}^2}\right) \frac{\pi^4}{5\mathrm{OSR}^5}. \tag{57}$$

5) Add the noise powers due the individual noise sources to obtain the total output thermal noise; equate it to the permissible noise, and use this to find the minimum values of the SC.

Substituting $x = 0.1$ into the expressions for $\overline{v_{\mathrm{ni1}}^2}$ and $\overline{v_{\mathrm{ni2}}^2}$, and $\mathrm{OSR} = 32$ into the equations obtained in Step 4, the total output thermal noise power is

$$\begin{aligned}\overline{v_{\mathrm{th}}^2} = {} & 7.24 \times 10^{-2} \frac{kT}{C_{s1}} + 1.35 \times 10^{-4} \frac{kT}{C_{01}} \\ & + 2.31 \times 10^{-4} \frac{kT}{C_{s2}} + 7.73 \times 10^{-7} \frac{kT}{C_{02}} \\ & + 4.64 \times 10^{-6} \frac{kT}{C_{f1}}.\end{aligned} \tag{58}$$

Since the first term dominates, the minimum value of C_{s1} can be obtained directly

$$C_{s1} \approx 7.24 \times 10^{-2} \frac{kT}{\overline{v_{\mathrm{th}}^2}} = 0.16 \text{ pF}. \tag{59}$$

The other SC may be chosen to be much smaller than C_{s1}.

Note that, as indicated in Step 4, it is the high OSR which makes the output noise (almost) independent of all switched capacitances other than C_{s1} for this modulator. In general, a simple optimization can be performed to minimize the total capacitance for a desirable thermal noise level.

VIII. Conclusion

The effects of thermal noise generated by the switches and op-amp devices in an SC circuit were analyzed. The analysis was simplified by assuming that the circuit contains only first-order blocks (SC branches, feedback op-amps), all designed to settle within half a clock period. This very practical assumption allowed a simple noise estimation process, resulting in a noise model consisting of input- and output-referred equivalent noise sources. The model was verified by comparing the estimation results for a typical SC integrator with those given by a state-of-the-art CAD program.

Based on the model, an optimum strategy was also suggested for the design of SC integrators incorporating thermal noise considerations.

Finally, an example illustrated the use of the proposed estimation process in the design of a second-order delta-sigma modulator.

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