Design Report: Design of Analog Integrated Circuits

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1 Hand calculations

1.1 Settling error

For the analysis of the settling error, the circuit digram as shown in the figure 1 has been used.

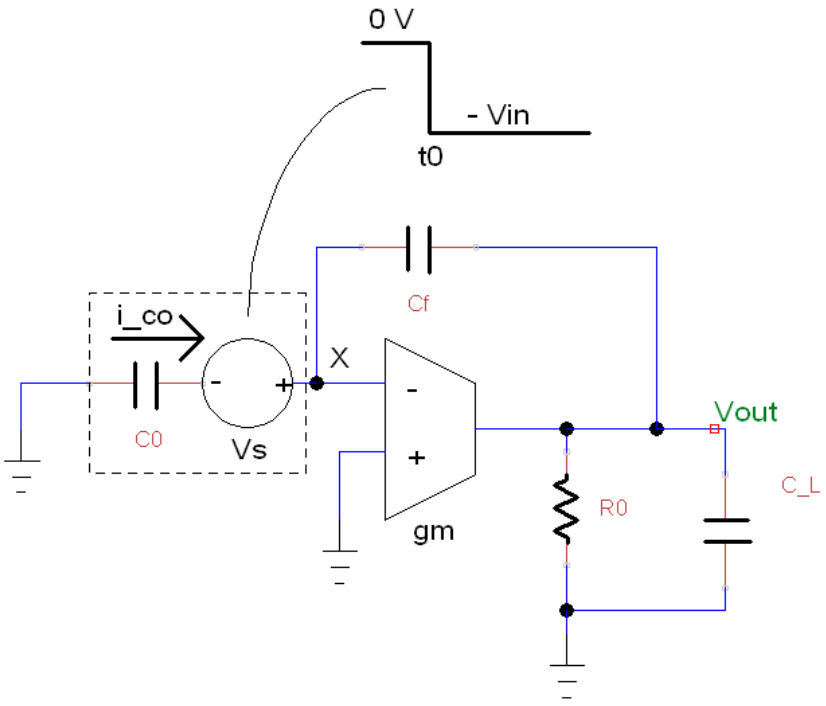

Figure 1: During amplification phase

During the sampling phase, capacitor C0 is charged to V_{in}. At the beginning of the amplification phase, because he voltage across a capacitor cannot change simultaneously, there will be a negative step on node X. This can be represented as an ideal capacitor with a voltage source in series whose output in a negative going step as shown. The transfer fucntion $\frac{V_{out}}{V_s}(s)$ needs to be determined. The current through the capacitor C_o can be written as $i_{c0} = -\frac{V_x - V_s}{sC_0}$
Also,

$$(V_x - V_{out})sC_f = g_m V_x + V_{out}(\frac{1}{R_0} + sC_L) \tag{1}$$

$$V_{out} = V_x - \frac{i_{c0}}{sC_f} = V_x + \frac{(V_x - V_s)C_0}{C_f}$$

The last equation can be re-written as

$$V_x = \frac{V_{out} + V_s \frac{C_0}{C_f}}{1 + \frac{C_0}{C_f}} \tag{2}$$

Combining equations (1) and (2), the transfer function is derived as:

$$\frac{V_{out}}{V_s}(s) = \frac{\frac{-g_m C_0 R_0}{g_m R_0 C_f + C_0 + c_f}}{1 + \frac{s(C_L C_0 + C_L C_f + C_0 C_f) R_0}{g_m R_0 C_f + C_0 + C_f}} \tag{3}$$

The time constant of the settiling behavior, is thus given by

$$\tau = \frac{(C_L C_0 + C_L C_f + C_0 C_f) R_0}{g_m R_0 C_f + C_0 + C_f} \tag{4}$$

Assuming that the duty cycle of the clock is 50%, then there will be just half the period left for settling. Because it is a single pole system, the exprsssion for settling time can be derived simply as: Settling error $=e^{-\frac{1}{2 f_{clk} \tau}}$

$$Error = e^{-\frac{g_m R_0 C_f + C_0 + C_f}{[(C_L C_0 + C_L C_f + C_0 C_f) R_0] 2 f_{clk}}} \tag{5}$$

An interesting observation (not so if you think about it) is that the pole in the expression is approximated by: $\frac{\beta gm}{C_L + C_0 // C_f}$ The look in impedance (with the feedback network) is $\frac{1}{\beta g_m}$ and the total capacitance is indeed C_L in parallel with the series combination of C_0 and C_f. However this expression is only valid for a single stage OTA. The settling of the internal node comes into picture. Because the pole at the output of the first stage is typically the lowest frequency, it may be a safe approximation to say that the internal node's GBW will limit the setling behavior. A detailed analysis of it can be found in [1]. .

However, for the simplicity of the design we approximated the settling time constant for settling as the inverse of GBW.

2 Common Mode feedback

In a fully differntial amplifer, where a current source is used as the load, there are two current sources in series. [encirled in figure 2]. Because of the high impedance of the current sources, the output common mode is not well defined. To define the output common mode, a CMFB circuit is used. A CMFB circuit senses the output common mode variation and changes the bias voltage of one of the current sources so that the output common mode is set to a fixed value. A CMFB circuit works in unity gain;

An ideal CMFB circuit is shown in figure 3. The two resistors forms a voltage divider to cancel out the differential mode signals. The resistor along with the capacitance at the output of the CMFB circuit will define the GBW of the

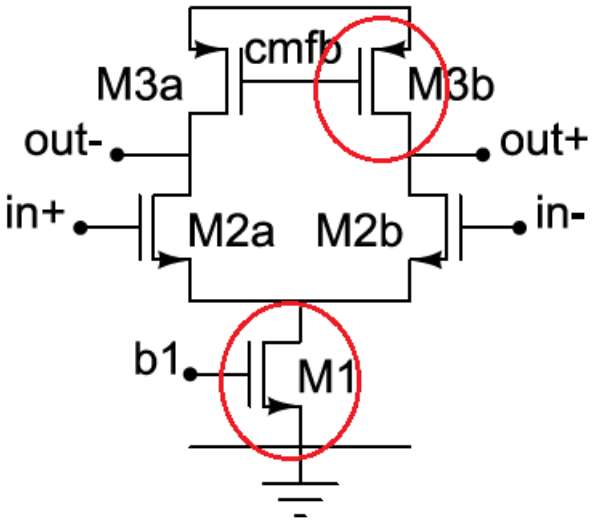

Figure 2: During amplification phase

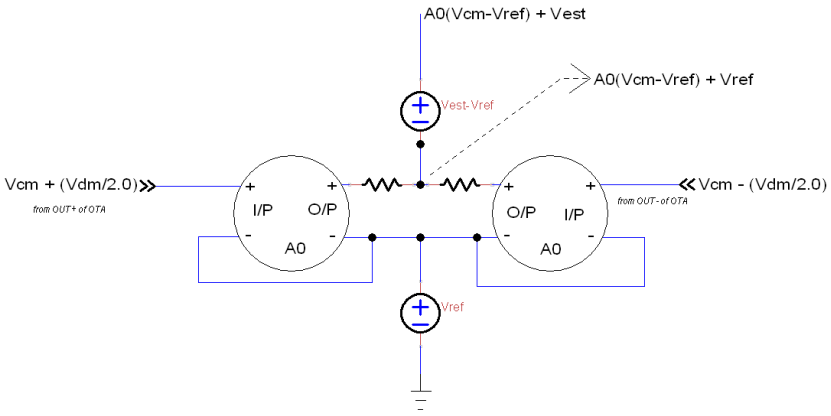

Figure 3: During amplification phase

CMFB circuit. A CMFB circuit needs to be faster than the differential circuit. If it is slower, then it may be possible that the bias voltages are not stable.
The A0 in the circuit is (part) of open loop gain of the CMFB circuit. The other part of the gain comes from the transfer function from the output of the CMFB circuit to the node where the CMFB circuit is connected. In this case,

larger the value of A0 is, smaller is the requirement on the accuracy of Vest. Vest is the estimated bias voltage of the current source that the CMFB will be driving. Vest does not need to be very accurate if A0 is large enough.
One of the problems seen during simulation if the simulator finds the solution as a large gate voltage which causes a large drain to gate current [basically a gate breakdown] but no drain to source current. In a real situation the voltage will be limited by the supply rails. The cmfb.cir netlist has been modified to reflect clamping of the output voltage to supply rails.

References

[1] J. Ruiz-Amaya, M. Delgado-Restituto, and . Rodriguez-Vazquez. Accurate settling-time modeling and design procedures for two-stage miller-compensated amplifiers for switched-capacitor circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(6):1077–1087, June 2009.