Design of the folded cascode OTA

1. Design of the nMOS input pair.

An over-drive of 70mV was selected. Lower overdrive requires larger device sizes, but lesser current. Higher over-drive will require much more current, but will result in much lesser capacitance. Also minimum channel length was selected. The following netlist was used:

\*\*\*\*\*\*\*\*\*\*\*\*\*\*

\* Model file \*

.lib "../../models/45nm.lib" tt

\*\*\*\*\*\*\*\*\*\*\*\*\*\*

.param W\_MOS=1u

\* ----- Circuit

\* Because this script will be used to design for the transistor of the input pair,

\* they can be of the minimum length

X\_nmos2 vds\_200m vgs vss vss nmos w=W\_MOS l=45n

vgs vgs vss 530m

vds2 vds\_200m vss 200m

vgnd vss 0 0

\* ------ Ends

.op

.dc sweep W\_MOS 1u 100u 1u

.defwave gm\_nmos2 = gm(X\_nmos2.M1)

.defwave w\_width= W\_MOS

.meas dc current\_required find id(X\_nmos2.M1) when gm(X\_nmos2.M1)=34.22m

.meas dc width\_required find w(w\_width) when gm(X\_nmos2.M1)=34.22m

.meas drain\_capacitance find cdd(X\_nmos2.M1) when gm(X\_nmos2.M1)=34.22m

.probe V I

.plot dc gm(X\_nmos2.M1)

.plot dc w(w\_width)

.option captab

.end

The results from the netlist are as shown below:

CURRENT\_REQUIRED = 2.5873E-03

WIDTH\_REQUIRED = 4.3014E-05

DRAIN\_CAPACITANCE = 4.0893E-14

(To be noted at this point is the fact that VDSAT> VGS-VTH = 97mV)

1. Design of the tail current source

The tail current source needs to carry twice the current. Choosing a length of ~4xLmin, and choosing an over-drive of 100mV, the tail current source was designed using the following netlist.